



Dual 1:5 Differential LVPECL/LVECL/HSTL Clock and Data Drivers

General Description

The MAX9312/MAX9314 are low skew, dual 1-to-5 differential drivers designed for clock and data distribution. These devices accept two inputs. Each input is reproduced at five differential outputs. The differential inputs can be adapted to accept single-ended inputs by connecting the on-chip V_{BB} supply to one input as a reference voltage.

The MAX9312/MAX9314 feature low part-to-part skew (30ps) and output-to-output skew (12ps), making them ideal for clock and data distribution across a backplane or a board. For interfacing to differential HSTL and LVPECL signals, these devices operate over a +2.25V to +3.8V supply range, allowing high-performance clock or data distribution in systems with a nominal +2.5V or +3.3V supply. For differential LVECL operation, these devices operate from a -2.25V to -3.8V supply.

The MAX9312 features an on-chip V_{BB} reference output of 1.425V below the positive supply voltage. The MAX9314 offers an on-chip V_{BB} reference output of 1.32V below the positive supply voltage.

Both devices are offered in an industry-standard 32-pin 7mm x 7mm LQFP package. In addition, the MAX9312 is offered in a space-saving 32-pin 5mm x 5mm TQFN package.

Applications

Precision Clock Distribution
Low-Jitter Data Repeater

Features

- ◆ +2.25V to +3.8V Differential HSTL/LVPECL Operation
- ◆ -2.25V to -3.8V Differential LVECL Operation
- ◆ 30ps (typ) Part-to-Part Skew
- ◆ 12ps (typ) Output-to-Output Skew
- ◆ 312ps (typ) Propagation Delay
- ◆ $\geq 300\text{mV}$ Differential Output at 3GHz
- ◆ On-Chip Reference for Single-Ended Inputs
- ◆ Output Low with Open Input
- ◆ Pin Compatible with MC100LVEP210 (MAX9312) and MC100EP210 (MAX9314)
- ◆ Offered in Tiny QFN* Package (70% Smaller Footprint than LQFP)

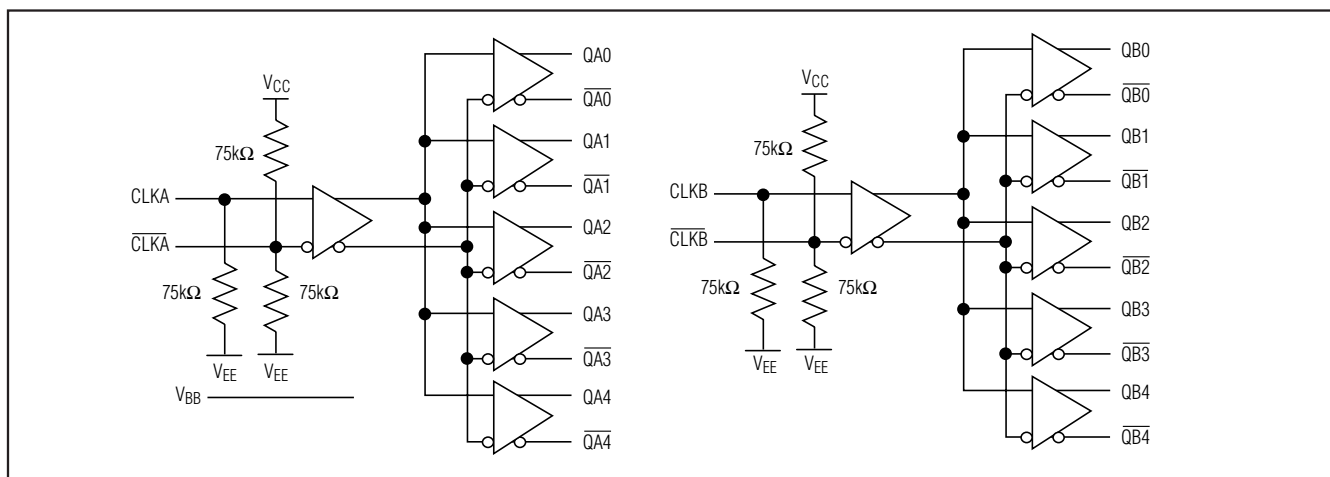
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9312ECJ+	-40°C to +85°C	32 LQFP
MAX9312ETJ+	-40°C to +85°C	32 TQFN-EP*
MAX9314ECJ	-40°C to +85°C	32 LQFP

*Exposed pad.

+Denotes a lead(Pb)-free/RoHS-compliant package.

Functional Diagram



Pin Configuration appears at end of data sheet.



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For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

MAX9312/MAX9314

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ABSOLUTE MAXIMUM RATINGS

V _{CC} - V _{EE}	4.1V
Inputs (CLK ₋ , $\overline{\text{CLK}}_{-}$).....	V _{EE} - 0.3V to V _{CC} + 0.3V
CLK ₋ to $\overline{\text{CLK}}_{-}$	±3.0V
Continuous Output Current.....	50mA
Surge Output Current.....	100mA
V _{BB} Sink/Source Current.....	±0.65mA
Continuous Power Dissipation (T _A = +70°C)	
32-Pin LQFP (derate 20.7mW/°C above +70°C).....	1652.9mW
32-Pin TQFN (derate 34.5mW/°C above +70°C).....	2758.6mW
Junction-to-Case Thermal Resistance (T _{JC}) (Note A)	
32-Pin LQFP.....	12°C/W
32-Pin TQFN.....	2°C/W

Junction-to-Ambient Thermal Resistance (T _{JA}) (Note 1)	
32-Pin LQFP.....	48.4°C/W
32-Pin TQFN.....	29°C/W
Operating Temperature Range.....	-40°C to +85°C
Junction Temperature.....	+150°C
Storage Temperature Range.....	-65°C to +150°C
ESD Protection	
Human Body Model (CLK ₋ , $\overline{\text{CLK}}_{-}$, Q ₋ , $\overline{\text{Q}}_{-}$).....	2kV
Soldering Temperature (10s).....	+300°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maxim-ic.com/thermal-tutorial.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} - V_{EE} = +2.25V to +3.8V, outputs loaded with 50Ω ±1% to V_{CC} - 2V.) (Notes 2–5)

PARAMETER	SYMBOL	CONDITIONS		-40°C		+25°C		+85°C		UNITS
				MIN	MAX	MIN	MAX	MIN	MAX	
INPUTS (CLK_, CLK_)										
Single-Ended Input High Voltage	V _{IH}	V _{BB} connected to CLK_ (V _{IL} for V _{BB} connected to CLK_)	MAX9312	V _{CC} - 1.23	V _{CC}	V _{CC} - 1.23	V _{CC}	V _{CC} - 1.23	V _{CC}	V
			MAX9314	V _{CC} - 1.165	V _{CC}	V _{CC} - 1.165	V _{CC}	V _{CC} - 1.165	V _{CC}	
Single-Ended Input Low Voltage	V _{IL}	V _{BB} connected to CLK_ (V _{IL} for V _{BB} connected to CLK_)	MAX9312	V _{EE}	V _{CC} - 1.62	V _{EE}	V _{CC} - 1.62	V _{EE}	V _{CC} - 1.62	V
			MAX9314	V _{EE}	V _{CC} - 1.475	V _{EE}	V _{CC} - 1.475	V _{EE}	V _{CC} - 1.475	
High Voltage of Differential Input	V _{IHD}			V _{EE} + 1.2	V _{CC}	V _{EE} + 1.2	V _{CC}	V _{EE} + 1.2	V _{CC}	V
Low Voltage of Differential Input	V _{ILD}			V _{EE}	V _{CC} - 0.095	V _{EE}	V _{CC} - 0.095	V _{EE}	V _{CC} - 0.095	V
Differential Input Voltage	V _{IHD} - V _{ILD}	For V _{CC} - V _{EE} < 3.0V		0.095	V _{CC} - V _{EE}	0.095	V _{CC} - V _{EE}	0.095	V _{CC} - V _{EE}	V
		For V _{CC} - V _{EE} ≥ 3.0V		0.095	3.0	0.095	3.0	0.095	3.0	
Input High Current	I _{IH}			150		150		150		μA
CLK_ Input Low Current	I _{ILCLK}			-10	+10	-10	+10	-10	+10	μA

Dual 1:5 Differential LVPECL/LVECL/HSTL Clock and Data Drivers

DC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} - V_{EE} = +2.25V$ to $+3.8V$, outputs loaded with $50\Omega \pm 1\%$ to $V_{CC} - 2V$.) (Notes 2–5)

PARAMETER	SYMBOL	CONDITIONS	-40°C		+25°C		+85°C		UNITS	
			MIN	MAX	MIN	MAX	MIN	MAX		
CLK_ Input Low Current	I_{ILCLK}		-150		-150		-150		μA	
OUTPUTS (Q__, Q__)										
Single-Ended Output High Voltage	V _{OH}	Figure 1	V _{CC} - 1.025	V _{CC} - 0.900	V _{CC} - 1.025	V _{CC} - 0.900	V _{CC} - 1.025	V _{CC} - 0.900	V	
Single-Ended Output Low Voltage	V _{OL}	Figure 1	V _{CC} - -1.930	V _{CC} - 1.695	V _{CC} - -1.930	V _{CC} - 1.695	V _{CC} - -1.930	V _{CC} - 1.695	V	
Differential Output Voltage	V _{OH} - V _{OL}	Figure 1	670	950	670	950	670	950	mV	
REFERENCE (V _{BB})										
Reference Voltage Output (Note 6)	V _{BB}	I _{BB} = ±0.5mA	MAX9312	V _{CC} - 1.525	V _{CC} - 1.325	V _{CC} - 1.525	V _{CC} - 1.325	V _{CC} - 1.525	V _{CC} - 1.325	V
			MAX9314	V _{CC} - 1.38	V _{CC} - 1.26	V _{CC} - 1.38	V _{CC} - 1.26	V _{CC} - 1.38	V _{CC} - 1.26	
POWER SUPPLY										
Supply Current (Note 7)	I _{EE}		75		82		95		mA	

Dual 1:5 Differential LVPECL/LVECL/HSTL Clock and Data Drivers

AC ELECTRICAL CHARACTERISTICS

($V_{CC} - V_{EE} = +2.25V$ to $+3.8V$, outputs loaded with $50\Omega \pm 1\%$ to $V_{CC} - 2V$, input frequency = $1.5GHz$, input transition time = $125ps$ (20% to 80%), $V_{IHD} = V_{EE} + 1.2V$ to V_{CC} , $V_{ILD} = V_{EE}$ to $V_{CC} - 0.15V$, $V_{IHD} - V_{ILD} = 0.15V$ to the smaller of $3V$ or $V_{CC} - V_{EE}$, unless otherwise noted. Typical values are at $V_{CC} - V_{EE} = 3.3V$, $V_{IHD} = V_{CC} - 1V$, $V_{ILD} = V_{CC} - 1.5V$.) (Note 8)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Differential Input-to-Output Delay	t_{PLHD} , t_{PHLD}	Figure 2	220	321	380	220	312	410	260	322	400	ps
Output-to-Output Skew (Note 9)	t_{SKOO}			12	46		12	46		10	35	ps
Part-to-Part Skew (Note 10)	t_{SKPP}			30	160		30	190		30	140	ps
Added Random Jitter (Note 11)	t_{RJ}	$f_{IN} = 1.5GHz$ clock pattern		1.2	2.5		1.2	2.5		1.2	2.5	ps (RMS)
		$f_{IN} = 3.0GHz$ clock pattern		1.2	2.6		1.2	2.6		1.2	2.6	
Added Deterministic Jitter (Note 11)	t_{DJ}	3Gbps, 2 ²³ -1 PRBS pattern		80	95		80	95		80	95	ps (pk-pk)
Switching Frequency	f_{MAX}	$V_{OH} - V_{OL} \geq 300mV$, clock pattern, Figure 2		3.0			3.0			3.0		GHz
		$V_{OH} - V_{OL} \geq 500mV$, clock pattern, Figure 2		1.5			1.5			1.5		
Output Rise/Fall Time (20% to 80%)	t_R , t_F	Figure 2	100	112	140	100	116	140	100	121	140	ps

Note 2: Measurements are made with the device in thermal equilibrium.

Note 3: Current into a pin is defined as positive. Current out of a pin is defined as negative.

Note 4: Single-ended input operation using V_{BB} is limited to $V_{CC} - V_{EE} = 3.0V$ to $3.8V$ for the MAX9312 and $V_{CC} - V_{EE} = 2.7V$ to $3.8V$ for the MAX9314.

Note 5: DC parameters production tested at $T_A = +25^\circ C$. Guaranteed by design and characterization over the full operating temperature range.

Note 6: Use V_{BB} only for inputs that are on the same device as the V_{BB} reference.

Note 7: All pins open except V_{CC} and V_{EE} .

Note 8: Guaranteed by design and characterization limits are set at ± 6 sigma.

Note 9: Measured between outputs on the same part at the signal crossing points for a same-edge transition.

Note 10: Measured between outputs of different parts at the signal crossing points under identical conditions for a same-edge transition.

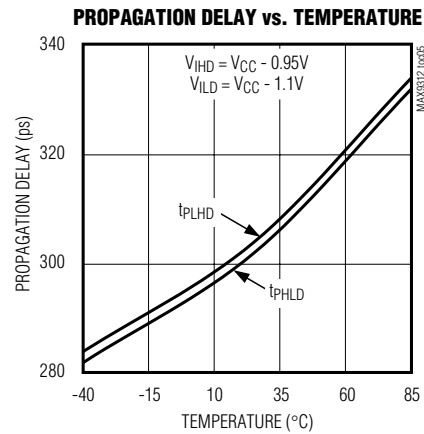
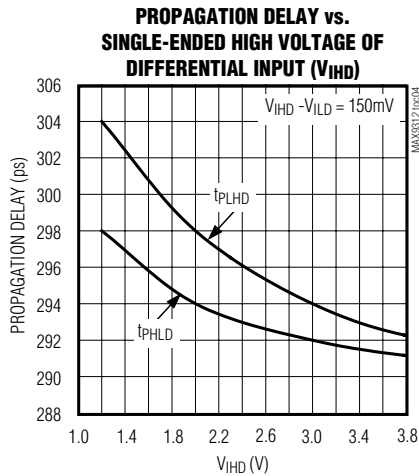
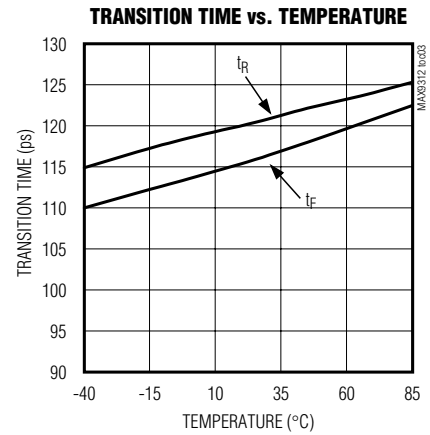
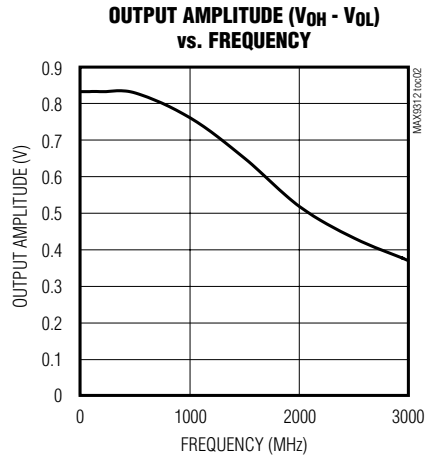
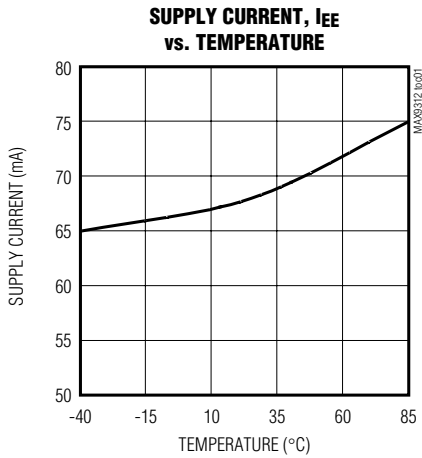
Note 11: Device jitter added to the input signal.

Dual 1:5 Differential LVPECL/LVECL/HSTL Clock and Data Drivers

Typical Operating Characteristics

($V_{CC} = +3.3V$, $V_{EE} = 0$, $V_{IHD} = V_{CC} - 0.95V$, $V_{ILD} = V_{CL} - 1.25V$, input transition time = 125ps (20% to 80%), $f_{IN} = 1.5GHz$, outputs loaded with 50Ω to $V_{CC} - 2V$, $T_A = +25^\circ C$, unless otherwise noted.)

MAX9312/MAX9314



Dual 1:5 Differential LVPECL/LVECL/HSTL Clock and Data Drivers

Pin Description

PIN	NAME	FUNCTION
1, 9, 16, 25, 32	V _{CC}	Positive Supply Voltage. Bypass from V _{CC} to V _{EE} with 0.1μF and 0.01μF ceramic capacitors. Place the capacitors as close to the device as possible with the smaller value capacitor closest to the device.
2	N.C.	No Connection. Internally not connected.
3	CLKA	Noninverting Differential Clock Input A
4	CLKA	Inverting Differential Clock Input A
5	V _{BB}	Reference Output Voltage. Connect to the inverting or noninverting clock input to provide a reference for single-ended operation. When used, bypass to V _{CC} with a 0.01μF ceramic capacitor.
6	CLKB	Noninverting Differential Clock Input B
7	CLKB	Inverting Differential Clock Input B
8	V _{EE}	Negative Supply Voltage
10	QB4	Inverting QB4 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V.
11	QB4	Noninverting QB4 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V.
12	QB3	Inverting QB3 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V.
13	QB3	Noninverting QB3 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V.
14	QB2	Inverting QB2 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V.
15	QB2	Noninverting QB2 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V.
17	QB1	Inverting QB1 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V.
18	QB1	Noninverting QB1 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V.
19	QB0	Inverting QB0 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V.
20	QB0	Noninverting QB0 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V.
21	QA4	Inverting QA4 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V.
22	QA4	Noninverting QA4 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V.
23	QA3	Inverting QA3 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V.
24	QA3	Noninverting QA3 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V.
26	QA2	Inverting QA2 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V.
27	QA2	Noninverting QA2 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V.
28	QA1	Inverting QA1 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V.
29	QA1	Noninverting QA1 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V.
30	QA0	Inverting QA0 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V.
31	QA0	Noninverting QA0 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V.
—	EP	Exposed Pad (TQFN package only). Internally connected to V _{EE} . Connect EP to the V _{EE} pad on the PCB.

Dual 1:5 Differential LVPECL/LVECL/HSTL Clock and Data Drivers

Detailed Description

The MAX9312/MAX9314 are low-skew, dual 1-to-5 differential drivers designed for clock and data distribution.

For interfacing to differential HSTL and LVPECL signals, these devices operate over a +2.25V to +3.8V supply range, allowing high-performance clock or data distribution in systems with a nominal +2.5V or +3.3V supply. For differential LVECL operation, these devices operate from a -2.25V to -3.8V supply.

The differential inputs can be configured to accept single-ended inputs when operating at approximately $V_{CC} - V_{EE} = 3.0V$ to 3.8V for the MAX9312 or $V_{CC} - V_{EE} = 2.7V$ to 3.8V for the MAX9314. This is accomplished by connecting the on-chip reference voltage, V_{BB} , to an input as a reference. For example, the differential $\overline{CLKA}$, $\overline{CLKA}$ input is converted to a noninverting, single-ended input by connecting V_{BB} to $\overline{CLKA}$ and connecting the single-ended input to $CLKA$. Similarly, an inverting input is obtained by connecting V_{BB} to $CLKA$ and connecting the single-ended input to $\overline{CLKA}$. With a differential input configured as single ended (using V_{BB}), the single-ended input can be driven to V_{CC} and V_{EE} or with a single-ended LVPECL/LVECL signal.

When a differential input is configured as a single-ended input (using V_{BB}), the approximate supply range is $V_{CC} - V_{EE} = 3.0V$ to 3.8V for the MAX9312 and $V_{CC} - V_{EE} = 2.7V$ to 3.8V for the MAX9314. This is because one of the inputs must be $V_{EE} + 1.2V$ or higher for proper operation of the input stage. V_{BB} must be at least $V_{EE} + 1.2V$ because it becomes the high-level input when the other (single-ended) input swings below it. Therefore, minimum $V_{BB} = V_{EE} + 1.2V$.

The minimum V_{BB} output for the MAX9312 is $V_{CC} - 1.525V$ and the minimum V_{BB} output for the MAX9314 is $V_{CC} - 1.38V$. Substituting the minimum V_{BB} output for each device into $V_{BB} = V_{EE} + 1.2V$ results in a minimum supply of 2.725V for the MAX9312 and 2.58V for the MAX9314. Rounding up to standard supplies gives the single-ended operating supply ranges of $V_{CC} - V_{EE} = 3.0V$ to 3.8V for the MAX9312 and $V_{CC} - V_{EE} = 2.7V$ to 3.8V for the MAX9314.

When using the V_{BB} reference output, bypass it with a 0.01 μF ceramic capacitor to V_{CC} . If the V_{BB} reference is not used, it can be left open. The V_{BB} reference can source or sink 0.5mA, which is sufficient to drive two inputs. Use V_{BB} only for inputs that are on the same device as the V_{BB} reference.

The maximum magnitude of the differential input from CLK_{-} to $\overline{CLK}_{-}$ is 3.0V or $V_{CC} - V_{EE}$, whichever is less.

This limit also applies to the difference between any reference voltage input and a single-ended input.

The differential inputs have bias resistors that drive the outputs to a differential low when the inputs are open. The inverting inputs ($\overline{CLKA}$ and $\overline{CLKB}$) are biased with a 75k Ω pullup to V_{CC} and a 75k Ω pulldown to V_{EE} . The noninverting inputs ($CLKA$ and $CLKB$) are biased with a 75k Ω pulldown to V_{EE} .

Specifications for the high and low voltages of a differential input (V_{IHD} and V_{ILD}) and the differential input voltage ($V_{IHD} - V_{ILD}$) apply simultaneously (V_{ILD} cannot be higher than V_{IHD}).

Output levels are referenced to V_{CC} and are considered LVPECL or LVECL, depending on the level of the V_{CC} supply. With V_{CC} connected to a positive supply and V_{EE} connected to GND, the outputs are LVPECL. The outputs are LVECL when V_{CC} is connected to GND and V_{EE} is connected to a negative supply.

A single-ended input of at least $V_{BB} \pm 95mV$ or a differential input of at least 95mV switches the outputs to the V_{OH} and V_{OL} levels specified in the *DC Electrical Characteristics* table.

Applications Information

Supply Bypassing

Bypass V_{CC} to V_{EE} with high-frequency surface-mount ceramic 0.1 μF and 0.01 μF capacitors in parallel as close to the device as possible, with the 0.01 μF value capacitor closest to the device. Use multiple parallel vias for low inductance. When using the V_{BB} reference output, bypass it with a 0.01 μF ceramic capacitor to V_{CC} (if the V_{BB} reference is not used, it can be left open).

Traces

Input and output trace characteristics affect the performance of the MAX9312/MAX9314.

Connect each signal of a differential input or output to a 50 Ω characteristic impedance trace. Minimize the number of vias to prevent impedance discontinuities. Reduce reflections by maintaining the 50 Ω characteristic impedance through connectors and across cables. Reduce skew within a differential pair by matching the electrical length of the traces.

Output Termination

Terminate outputs through 50 Ω to $V_{CC} - 2V$ or use an equivalent Thevenin termination. When a single-ended signal is taken from a differential output, terminate both outputs. For example, if QA0 is used as a single-ended output, terminate both QA0 and $\overline{QA0}$.

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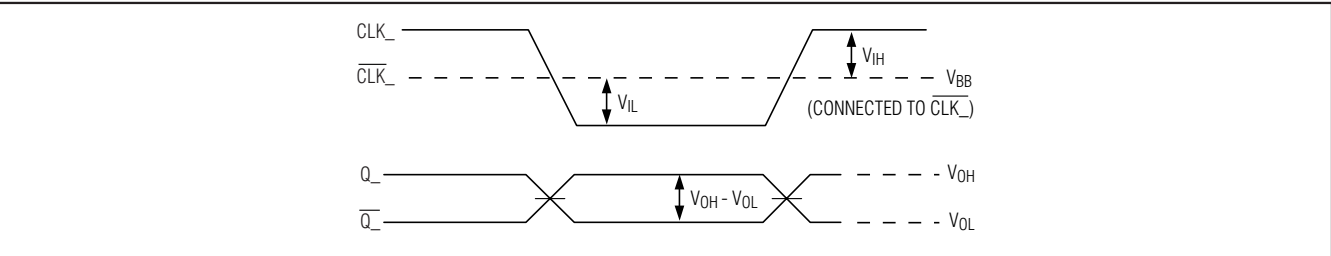


Figure 1. Switching with Single-Ended Input

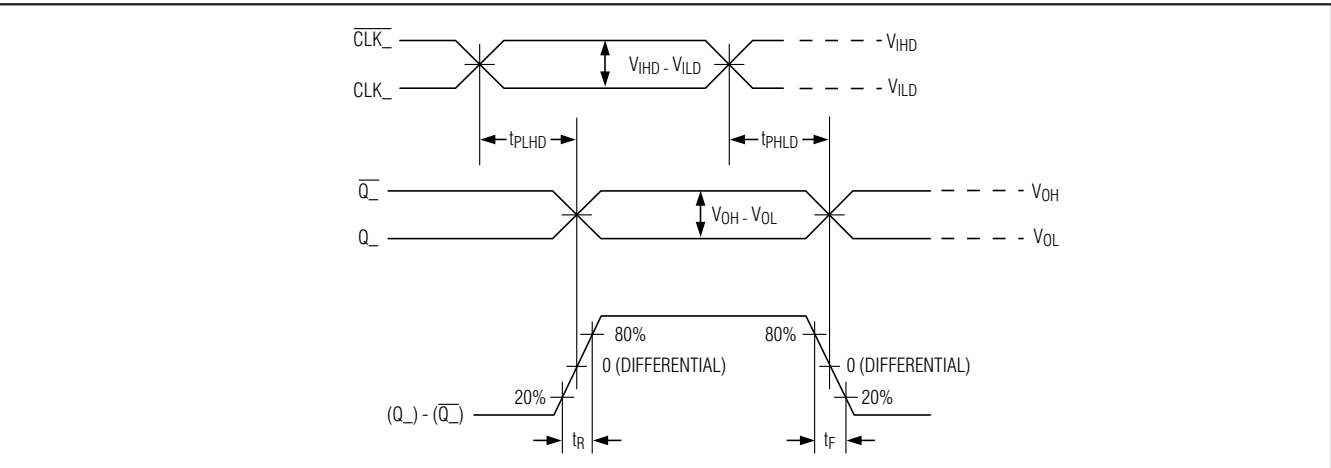
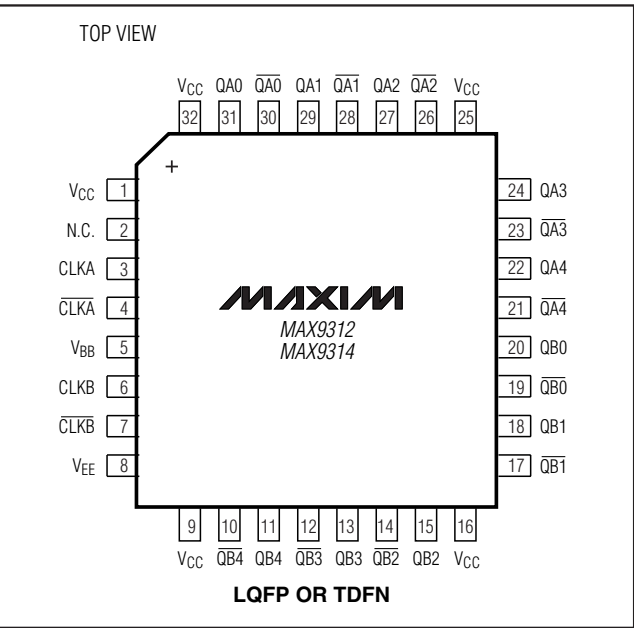


Figure 2. Differential Transition Time and Propagation Delay Timing Diagram

Pin Configuration



Chip Information

PROCESS: BIPOLAR

Package Information

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
32 LQFP	C32-1	21-0054
12 TQFN-EP	T3255+4	21-0140

Dual 1:5 Differential LVPECL/LVECL/HSTL Clock and Data Drivers

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
2	4/09	Added lead-free TQFN package for MAX9312, deleted future product packages for MAX9314, and updated <i>Pin Description</i>	1, 6

MAX9312/MAX9314

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