

### FEATURES

- Micropower at high voltage (18 V): 22  $\mu$ A maximum
- Low offset voltage: 350  $\mu$ V maximum
- Low input bias current: 20 pA maximum
- Gain bandwidth product: 230 kHz at  $A_v = 100$  typical
- Unity-gain crossover: 230 kHz
- 3 dB closed-loop bandwidth: 305 kHz
- Single-supply operation: 2.7 V to 18 V
- Dual-supply operation:  $\pm 1.35$  V to  $\pm 9$  V
- Unity-gain stable
- Excellent electromagnetic interference immunity

### APPLICATIONS

- Portable operating systems
- Current monitors
- 4 mA to 20 mA loop drivers
- Buffer/level shifting
- Multipole filters
- Remote/wireless sensors
- Low power transimpedance amplifiers

### GENERAL DESCRIPTION

The AD8657/AD8659 are dual and quad micropower, precision, rail-to-rail input/output amplifiers optimized for low power and wide operating supply voltage range applications.

The AD8657/AD8659 operate from 2.7 V to 18 V with a typical quiescent supply current of 18  $\mu$ A. The devices use the Analog Devices, Inc., patented DigiTrim<sup>®</sup> trimming technique, which achieves low offset voltage. The AD8657/AD8659 also have high immunity to electromagnetic interference.

The combination of low supply current, low offset voltage, very low input bias current, wide supply range, and rail-to-rail input and output make the AD8657/AD8659 ideal for current monitoring in process and motor control applications. The combination of precision specifications makes these devices ideal for dc gain and buffering of sensor front ends or high impedance input sources in wireless or remote sensors or transmitters.

The AD8657/AD8659 are specified over the extended industrial temperature range ( $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ). The AD8657 is available in an 8-lead MSOP package and an 8-lead LFCSP package; the AD8659 is available in a 14-lead SOIC package and 16-lead LFCSP package.

### PIN CONNECTION DIAGRAMS



Figure 1. AD8657 Pin Configuration, 8-Lead MSOP



- NOTES  
1. CONNECT THE EXPOSED PAD TO V- OR LEAVE IT UNCONNECTED.

Figure 2. AD8657 Pin Configuration, 8-Lead LFCSP

Note: For AD8659 pin connections and for more information about the pin connections for these products, see the Pin Configurations and Function Descriptions section.

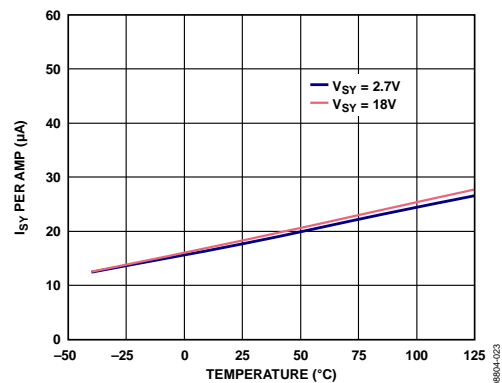


Figure 3. AD8657, Supply Current vs. Temperature

Table 1. Precision Micropower Op Amps (<250  $\mu$ A)

Supply Voltage	5 V	12 V to 16 V	36 V
Single	AD8538 AD8603 ADA4051-1	OP196	
Dual	AD8539 AD8607 ADA4051-2	AD8657	AD8622 ADA4091-2 ADA4096-2
Quad	AD8609	AD8659	AD8624 ADA4091-4 ADA4096-4

### Rev. C

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### 8/2012—Rev. A to Rev. B

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### 3/2011—Rev. 0 to Rev. A

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### 1/2011—Revision 0: Initial Version

## SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS—18 V OPERATION

$V_{SY} = 18\text{ V}$ ,  $V_{CM} = V_{SY}/2\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise specified.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage	$V_{OS}$	$V_{CM} = 0\text{ V to }18\text{ V}$ $V_{CM} = 0.3\text{ V to }17.7\text{ V}$ , $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ $V_{CM} = 0.3\text{ V to }17.7\text{ V}$ , $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ $V_{CM} = 0\text{ V to }18\text{ V}$ , $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			350 1.8 2 16	$\mu\text{V}$ mV mV mV
Input Bias Current	$I_B$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		5	20	$\mu\text{A}$ nA
Input Offset Current	$I_{OS}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			40 5.8	$\mu\text{A}$ nA
Input Voltage Range			0		18	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V to }18\text{ V}$ $V_{CM} = 0.3\text{ V to }17.7\text{ V}$ , $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ $V_{CM} = 0.3\text{ V to }17.7\text{ V}$ , $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ $V_{CM} = 0\text{ V to }18\text{ V}$ , $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	94	110		dB dB dB dB
Large Signal Voltage Gain	$A_{VO}$	$R_L = 100\text{ k}\Omega$ , $V_O = 0.5\text{ V to }17.5\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	115	120		dB dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			2		$\mu\text{V}/^\circ\text{C}$
Input Resistance	$R_{IN}$			10		G $\Omega$
Input Capacitance, Differential Mode	$C_{INDM}$			11		pF
Input Capacitance, Common Mode	$C_{INCM}$			3.5		pF
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage High	$V_{OH}$	$R_L = 100\text{ k}\Omega$ to $V_{CM}$ , $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	17.97			V
Output Voltage Low	$V_{OL}$	$R_L = 100\text{ k}\Omega$ to $V_{CM}$ , $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			30	mV
Short-Circuit Current	$I_{SC}$			$\pm 12$		mA
Closed-Loop Output Impedance	$Z_{OUT}$	$f = 1\text{ kHz}$ , $A_V = 1$		15		$\Omega$
<b>POWER SUPPLY</b>						
Power Supply Rejection Ratio	PSRR	$V_{SY} = 2.7\text{ V to }18\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	100 90	115		dB dB
Supply Current per Amplifier	$I_{SY}$	$I_O = 0\text{ mA}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		18	22 34	$\mu\text{A}$ $\mu\text{A}$
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate	SR	$R_L = 1\text{ M}\Omega$ , $C_L = 10\text{ pF}$ , $A_V = 1$		80		V/ms
Settling Time to 0.1%	$t_s$	$V_{IN} = 1\text{ V step}$ , $R_L = 100\text{ k}\Omega$ , $C_L = 10\text{ pF}$		15		$\mu\text{s}$
Unity-Gain Crossover	UGC	$V_{IN} = 10\text{ mV p-p}$ , $R_L = 1\text{ M}\Omega$ , $C_L = 10\text{ pF}$ , $A_V = 1$		230		kHz
Phase Margin	$\Phi_M$	$V_{IN} = 10\text{ mV p-p}$ , $R_L = 1\text{ M}\Omega$ , $C_L = 10\text{ pF}$ , $A_V = 1$		60		Degrees
Gain Bandwidth Product	GBP	$V_{IN} = 10\text{ mV p-p}$ , $R_L = 1\text{ M}\Omega$ , $C_L = 10\text{ pF}$ , $A_V = 100$		230		kHz
-3 dB Closed-Loop Bandwidth	$f_{-3\text{ dB}}$	$V_{IN} = 10\text{ mV p-p}$ , $R_L = 1\text{ M}\Omega$ , $C_L = 10\text{ pF}$ , $A_V = 1$		305		kHz
Channel Separation	CS	$f = 10\text{ kHz}$ , $R_L = 1\text{ M}\Omega$		95		dB
EMI Rejection Ratio of +IN x	EMIRR	$V_{IN} = 100\text{ mV}_{PEAK}$ ; $f = 400\text{ MHz}$ , $900\text{ MHz}$ , $1800\text{ MHz}$ , $2400\text{ MHz}$		90		dB
<b>NOISE PERFORMANCE</b>						
Voltage Noise	$e_n$ p-p	$f = 0.1\text{ Hz to }10\text{ Hz}$		5		$\mu\text{V p-p}$
Voltage Noise Density	$e_n$	$f = 1\text{ kHz}$ $f = 10\text{ kHz}$		50 45		nV/ $\sqrt{\text{Hz}}$ nV/ $\sqrt{\text{Hz}}$
Current Noise Density	$i_n$	$f = 1\text{ kHz}$		0.1		pA/ $\sqrt{\text{Hz}}$

**ELECTRICAL CHARACTERISTICS—10 V OPERATION**

$V_{SY} = 10\text{ V}$ ,  $V_{CM} = V_{SY}/2\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise specified.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage	$V_{OS}$	$V_{CM} = 0\text{ V to }10\text{ V}$ $V_{CM} = 0.3\text{ V to }9.7\text{ V}$ , $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ $V_{CM} = 0.3\text{ V to }9.7\text{ V}$ , $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ $V_{CM} = 0\text{ V to }10\text{ V}$ , $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			350	$\mu\text{V}$
					1.6	mV
					2	mV
					16	mV
Input Bias Current	$I_B$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		2	15	$\mu\text{A}$
Input Offset Current	$I_{OS}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			2.6	nA
Input Voltage Range			0		10	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V to }10\text{ V}$ $V_{CM} = 0.3\text{ V to }9.7\text{ V}$ , $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ $V_{CM} = 0.3\text{ V to }9.7\text{ V}$ , $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ $V_{CM} = 0\text{ V to }10\text{ V}$ , $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	88	105		dB
			76			dB
			75			dB
			59			dB
Large Signal Voltage Gain	$A_{VO}$	$R_L = 100\text{ k}\Omega$ , $V_O = 0.5\text{ V to }9.5\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	108	120		dB
			100			dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			2		$\mu\text{V}/^\circ\text{C}$
Input Resistance	$R_{IN}$			10		$\text{G}\Omega$
Input Capacitance, Differential Mode	$C_{INDM}$			11		pF
Input Capacitance, Common Mode	$C_{INCM}$			3.5		pF
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage High	$V_{OH}$	$R_L = 100\text{ k}\Omega$ to $V_{CM}$ , $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	9.98			V
Output Voltage Low	$V_{OL}$	$R_L = 100\text{ k}\Omega$ to $V_{CM}$ , $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			20	mV
Short-Circuit Current	$I_{SC}$			$\pm 11$		mA
Closed-Loop Output Impedance	$Z_{OUT}$	$f = 1\text{ kHz}$ , $A_V = 1$		15		$\Omega$
<b>POWER SUPPLY</b>						
Power Supply Rejection Ratio	PSRR	$V_{SY} = 2.7\text{ V to }18\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	100	115		dB
			90			dB
Supply Current per Amplifier	$I_{SY}$	$I_O = 0\text{ mA}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		18	22	$\mu\text{A}$
					34	$\mu\text{A}$
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate	SR	$R_L = 1\text{ M}\Omega$ , $C_L = 10\text{ pF}$ , $A_V = 1$		75		V/ms
Settling Time to 0.1%	$t_s$	$V_{IN} = 1\text{ V step}$ , $R_L = 100\text{ k}\Omega$ , $C_L = 10\text{ pF}$		15		$\mu\text{s}$
Unity-Gain Crossover	UGC	$V_{IN} = 10\text{ mV p-p}$ , $R_L = 1\text{ M}\Omega$ , $C_L = 10\text{ pF}$ , $A_V = 1$		225		kHz
Phase Margin	$\Phi_M$	$V_{IN} = 10\text{ mV p-p}$ , $R_L = 1\text{ M}\Omega$ , $C_L = 10\text{ pF}$ , $A_V = 1$		60		Degrees
Gain Bandwidth Product	GBP	$V_{IN} = 10\text{ mV p-p}$ , $R_L = 1\text{ M}\Omega$ , $C_L = 10\text{ pF}$ , $A_V = 100$		230		kHz
-3 dB Closed-Loop Bandwidth	$f_{-3\text{ dB}}$	$V_{IN} = 10\text{ mV p-p}$ , $R_L = 1\text{ M}\Omega$ , $C_L = 10\text{ pF}$ , $A_V = 1$		300		kHz
Channel Separation	CS	$f = 10\text{ kHz}$ , $R_L = 1\text{ M}\Omega$		95		dB
EMI Rejection Ratio of +IN x	EMIRR	$V_{IN} = 100\text{ mV}_{PEAK}$ ; $f = 400\text{ MHz}$ , $900\text{ MHz}$ , $1800\text{ MHz}$ , $2400\text{ MHz}$		90		dB
<b>NOISE PERFORMANCE</b>						
Voltage Noise	$e_n\text{ p-p}$	$f = 0.1\text{ Hz to }10\text{ Hz}$		5		$\mu\text{V p-p}$
Voltage Noise Density	$e_n$	$f = 1\text{ kHz}$		50		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 10\text{ kHz}$		45		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	$i_n$	$f = 1\text{ kHz}$		0.1		$\text{pA}/\sqrt{\text{Hz}}$

**ELECTRICAL CHARACTERISTICS—2.7 V OPERATION**

$V_{SY} = 2.7\text{ V}$ ,  $V_{CM} = V_{SY}/2\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise specified.

**Table 4.**

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage	$V_{OS}$	$V_{CM} = 0\text{ V to } 2.7\text{ V}$ $V_{CM} = 0.3\text{ V to } 2.4\text{ V}$ , $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ $V_{CM} = 0.3\text{ V to } 2.4\text{ V}$ , $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ $V_{CM} = 0\text{ V to } 2.7\text{ V}$ , $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			350	$\mu\text{V}$
Input Bias Current	$I_B$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		1	10	pA
Input Offset Current	$I_{OS}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			20	pA
Input Voltage Range			0		2.7	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V to } 2.7\text{ V}$ $V_{CM} = 0.3\text{ V to } 2.4\text{ V}$ , $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ $V_{CM} = 0.3\text{ V to } 2.4\text{ V}$ , $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ $V_{CM} = 0\text{ V to } 2.7\text{ V}$ , $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	77	95		dB
Large Signal Voltage Gain	$A_{VO}$	$R_L = 100\text{ k}\Omega$ , $V_O = 0.5\text{ V to } 2.2\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	95	105		dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			2		$\mu\text{V}/^\circ\text{C}$
Input Resistance	$R_{IN}$			10		G $\Omega$
Input Capacitance, Differential Mode	$C_{INDM}$			11		pF
Input Capacitance, Common Mode	$C_{INCM}$			3.5		pF
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage High	$V_{OH}$	$R_L = 100\text{ k}\Omega$ to $V_{CM}$ , $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	2.69			V
Output Voltage Low	$V_{OL}$	$R_L = 100\text{ k}\Omega$ to $V_{CM}$ , $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			10	mV
Short-Circuit Current	$I_{SC}$			$\pm 4$		mA
Closed-Loop Output Impedance	$Z_{OUT}$	$f = 1\text{ kHz}$ , $A_V = 1$		20		$\Omega$
<b>POWER SUPPLY</b>						
Power Supply Rejection Ratio	PSRR	$V_{SY} = 2.7\text{ V to } 18\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	100	115		dB
Supply Current per Amplifier	$I_{SY}$	$I_O = 0\text{ mA}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	90	18	22	$\mu\text{A}$
					34	$\mu\text{A}$
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate	SR	$R_L = 1\text{ M}\Omega$ , $C_L = 10\text{ pF}$ , $A_V = 1$		50		V/ms
Settling Time to 0.1%	$t_s$	$V_{IN} = 1\text{ V step}$ , $R_L = 100\text{ k}\Omega$ , $C_L = 10\text{ pF}$		20		$\mu\text{s}$
Unity-Gain Crossover	UGC	$V_{IN} = 10\text{ mV p-p}$ , $R_L = 1\text{ M}\Omega$ , $C_L = 10\text{ pF}$ , $A_V = 1$		190		kHz
Phase Margin	$\Phi_M$	$V_{IN} = 10\text{ mV p-p}$ , $R_L = 1\text{ M}\Omega$ , $C_L = 10\text{ pF}$ , $A_V = 1$		55		Degrees
Gain Bandwidth Product	GBP	$V_{IN} = 10\text{ mV p-p}$ , $R_L = 1\text{ M}\Omega$ , $C_L = 10\text{ pF}$ , $A_V = 100$		200		kHz
–3 dB Closed-Loop Bandwidth	$f_{-3\text{ dB}}$	$V_{IN} = 10\text{ mV p-p}$ , $R_L = 1\text{ M}\Omega$ , $C_L = 10\text{ pF}$ , $A_V = 1$		245		kHz
Channel Separation	CS	$f = 10\text{ kHz}$ , $R_L = 1\text{ M}\Omega$		95		dB
EMI Rejection Ratio of +IN x	EMIRR	$V_{IN} = 100\text{ mV}_{PEAK}$ ; $f = 400\text{ MHz}$ , $900\text{ MHz}$ , $1800\text{ MHz}$ , $2400\text{ MHz}$		90		dB
<b>NOISE PERFORMANCE</b>						
Voltage Noise	$e_n$ p-p	$f = 0.1\text{ Hz to } 10\text{ Hz}$		6		$\mu\text{V p-p}$
Voltage Noise Density	$e_n$	$f = 1\text{ kHz}$		60		nV/ $\sqrt{\text{Hz}}$
		$f = 10\text{ kHz}$		56		nV/ $\sqrt{\text{Hz}}$
Current Noise Density	$i_n$	$f = 1\text{ kHz}$		0.1		pA/ $\sqrt{\text{Hz}}$

## ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Supply Voltage	20.5 V
Input Voltage	(V <sub>-</sub> ) – 300 mV to (V <sub>+</sub> ) + 300 mV
Input Current <sup>1</sup>	±10 mA
Differential Input Voltage	±V <sub>SY</sub>
Output Short-Circuit Duration to GND	Indefinite
Temperature Ranges	
Storage	–65°C to +150°C
Operating	–40°C to +125°C
Junction	–65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

<sup>1</sup> The input pins have clamp diodes to the power supply pins. Limit the input current to 10 mA or less whenever input signals exceed the power supply rail by 0.3 V.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

$\theta_{JA}$  is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages using a standard 4-layer JEDEC board. The exposed pad (LFCSP packages only) is soldered to the board.

Table 6. Thermal Resistance

Package Type	$\theta_{JA}$	$\theta_{JC}$	Unit
8-Lead MSOP (RM-8)	142	45	°C/W
8-Lead LFCSP (CP-8-11)	75	12	°C/W
14-Lead SOIC (R-14)	115	36	°C/W
16-Lead LFCSP (CP-16-20)	52	13	°C/W

## ESD CAUTION

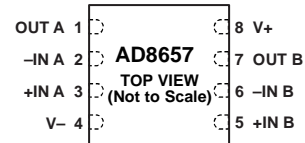


**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



Figure 4. AD8657 Pin Configuration, 8-Lead MSOP



NOTES  
1. CONNECT THE EXPOSED PAD TO V- OR LEAVE IT UNCONNECTED.

Figure 5. AD8657 Pin Configuration, 8-Lead LFCSP

Table 7. Pin Function Descriptions, AD8657

Pin No. <sup>1</sup>		Mnemonic	Description
8-Lead MSOP	8-Lead LFCSP		
1	1	OUT A	Output Channel A.
2	2	-IN A	Negative Input Channel A.
3	3	+IN A	Positive Input Channel A.
4	4	V-	Negative Supply Voltage.
5	5	+IN B	Positive Input Channel B.
6	6	-IN B	Negative Input Channel B.
7	7	OUT B	Output Channel B.
8	8	V+	Positive Supply Voltage.
N/A	EPAD <sup>2</sup>	EPAD	Exposed Pad. For the AD8657 (8-lead LFCSP only), connect the exposed pad to V- or leave it unconnected.

<sup>1</sup> N/A means not applicable.

<sup>2</sup> The exposed pad is not shown in the pin configuration diagram.



Figure 6. AD8659 Pin Configuration, 14-Lead SOIC\_N



NOTES  
 1. NIC = NO INTERNAL CONNECTION.  
 2. CONNECT THE EXPOSED PAD TO V- OR LEAVE IT UNCONNECTED.

Figure 7. AD8659 Pin Configuration, 16-Lead LFCSP

Table 8. Pin Function Descriptions, AD8659

Pin No. <sup>1</sup>		Mnemonic	Description
14-Lead SOIC	16-Lead LFCSP		
1	15	OUT A	Output Channel A.
2	1	-IN A	Negative Input Channel A.
3	2	+IN A	Positive Input Channel A.
11	10	V-	Negative Supply Voltage.
5	4	+IN B	Positive Input Channel B.
6	5	-IN B	Negative Input Channel B.
7	6	OUT B	Output Channel B.
4	3	V+	Positive Supply Voltage.
8	7	OUT C	Output Channel C.
9	8	-IN C	Negative Input Channel C.
10	9	+IN C	Positive Input Channel C.
12	11	+IN D	Positive Input Channel D.
13	12	-IN D	Negative Input Channel D.
14	14	OUT D	Output Channel D.
N/A	13	NIC	No Internal Connection.
N/A	16	NIC	No Internal Connection.
N/A	EP <sup>2</sup>	EPAD <sup>2</sup>	Exposed Pad. For the AD8659 (16-lead LFCSP only), connect the exposed pad to V- or leave it unconnected.

<sup>1</sup> N/A means not applicable.

<sup>2</sup> The exposed pad is not shown in the pin configuration diagram.



# TYPICAL PERFORMANCE CHARACTERISTICS

T<sub>A</sub> = 25°C, unless otherwise noted.



Figure 8. Input Offset Voltage Distribution



Figure 11. Input Offset Voltage Distribution



Figure 9. Input Offset Voltage Drift Distribution



Figure 12. Input Offset Voltage Drift Distribution

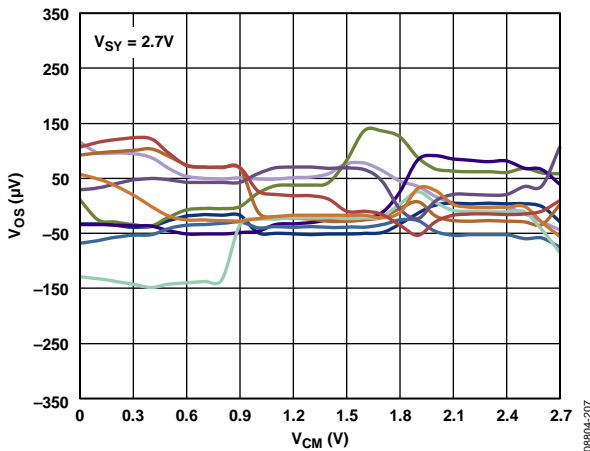


Figure 10. Input Offset Voltage vs. Common-Mode Voltage



Figure 13. Input Offset Voltage vs. Common-Mode Voltage



Figure 14. Input Offset Voltage vs. Common-Mode Voltage

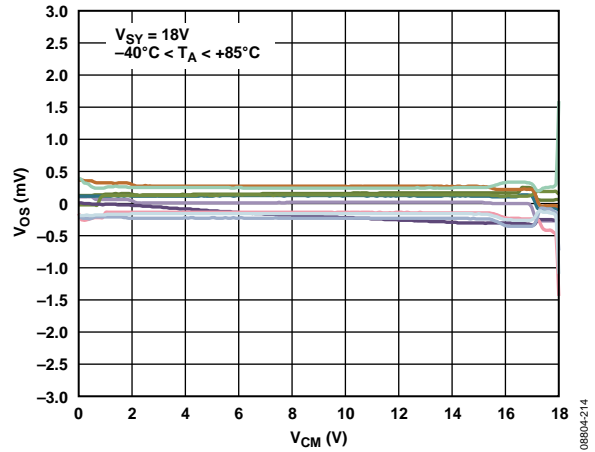


Figure 17. Input Offset Voltage vs. Common-Mode Voltage

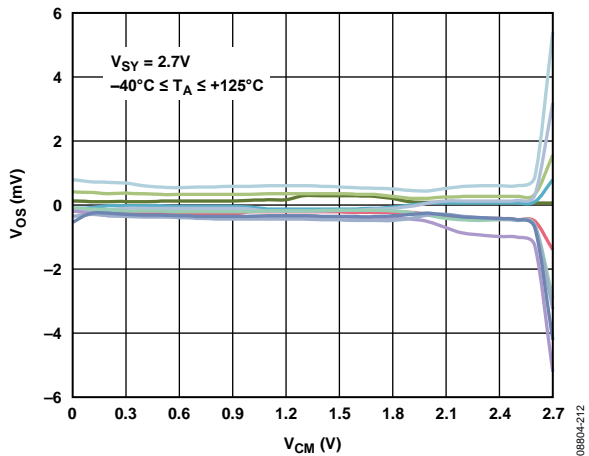


Figure 15. Input Offset Voltage vs. Common-Mode Voltage

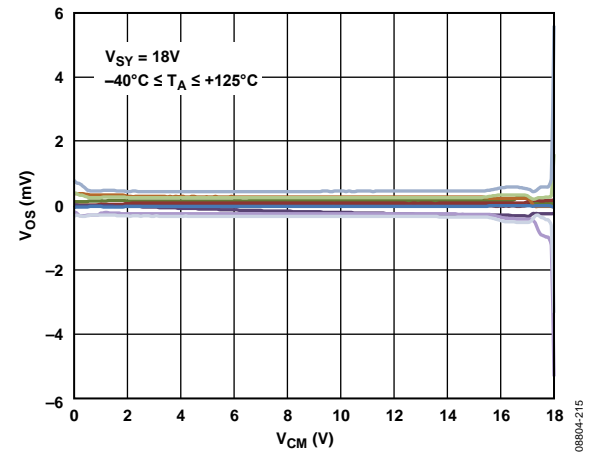


Figure 18. Input Offset Voltage vs. Common-Mode Voltage

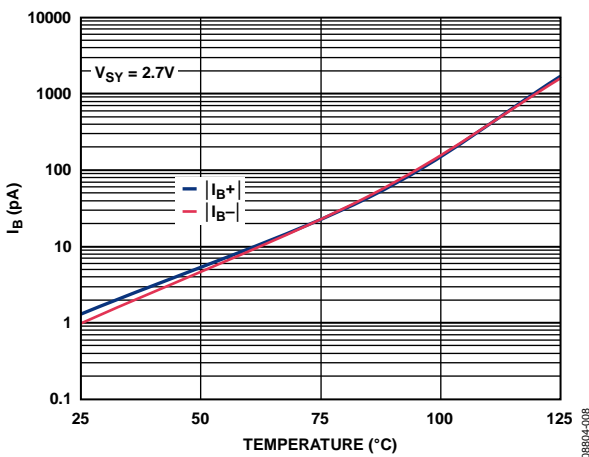


Figure 16. Input Bias Current vs. Temperature

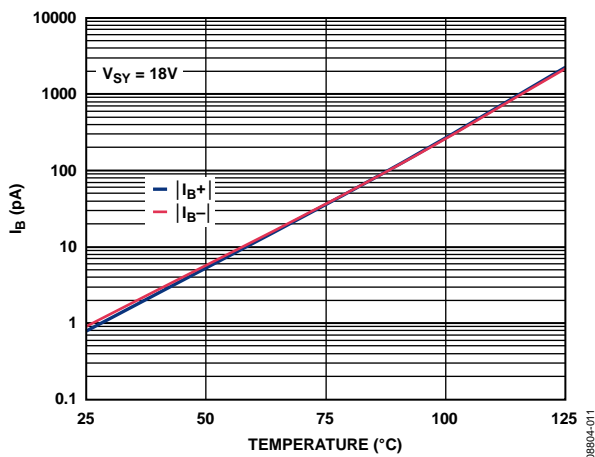


Figure 19. Input Bias Current vs. Temperature

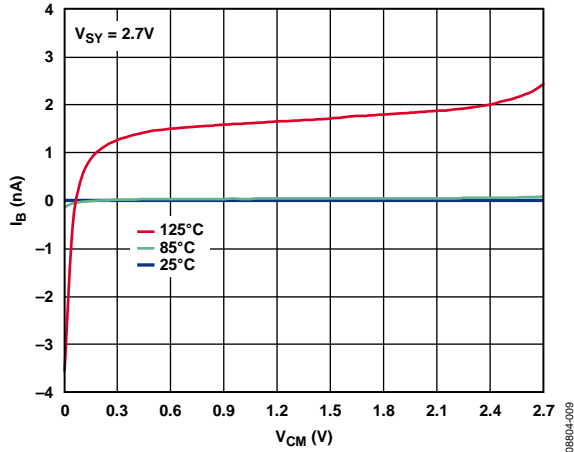


Figure 20. Input Bias Current vs. Common-Mode Voltage



Figure 23. Input Bias Current vs. Common-Mode Voltage

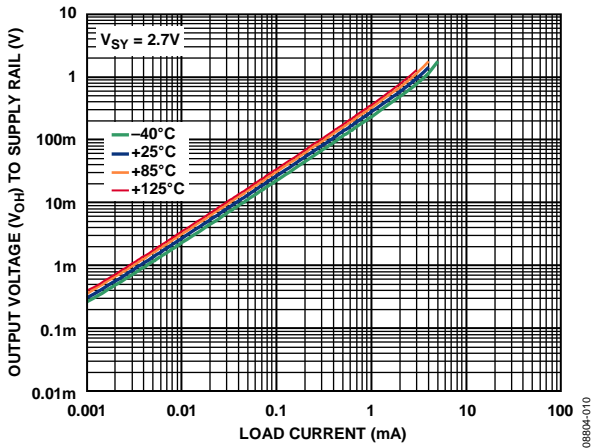


Figure 21. Output Voltage ( $V_{OH}$ ) to Supply Rail vs. Load Current

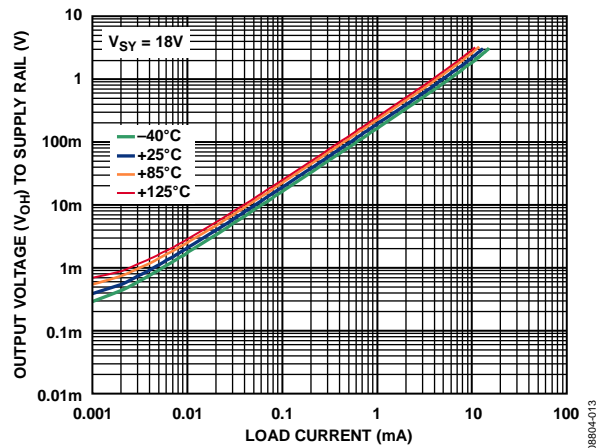


Figure 24. Output Voltage ( $V_{OH}$ ) to Supply Rail vs. Load Current

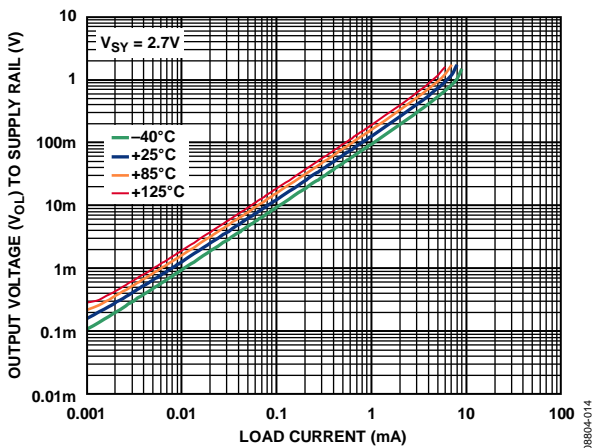


Figure 22. Output Voltage ( $V_{OL}$ ) to Supply Rail vs. Load Current

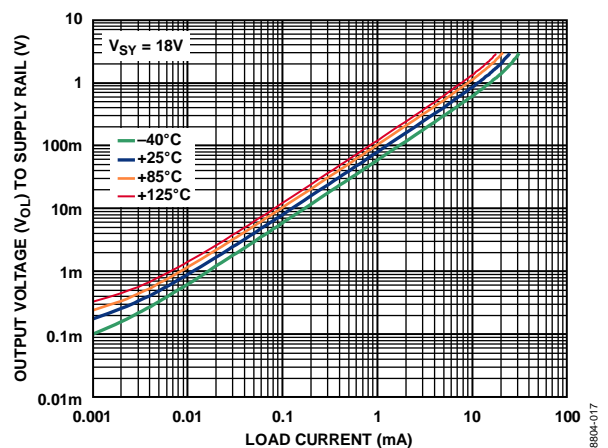


Figure 25. Output Voltage ( $V_{OL}$ ) to Supply Rail vs. Load Current



Figure 26. Output Voltage ( $V_{OH}$ ) vs. Temperature



Figure 29. Output Voltage ( $V_{OH}$ ) vs. Temperature

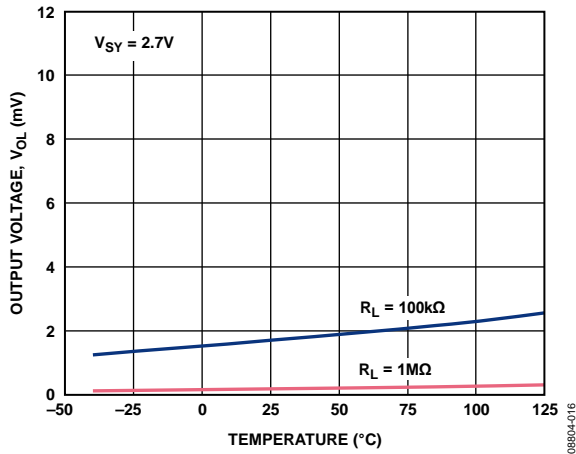


Figure 27. Output Voltage ( $V_{OL}$ ) vs. Temperature

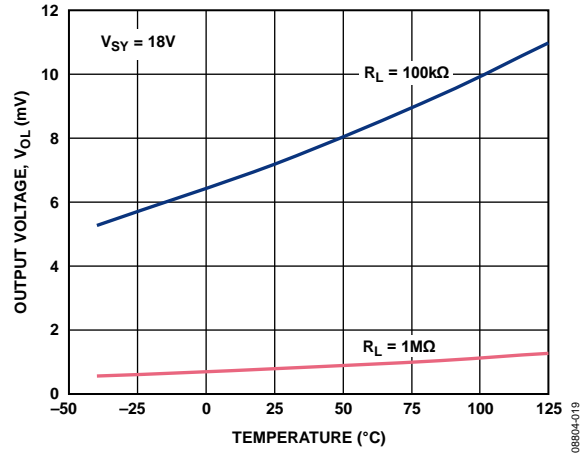


Figure 30. Output Voltage ( $V_{OL}$ ) vs. Temperature

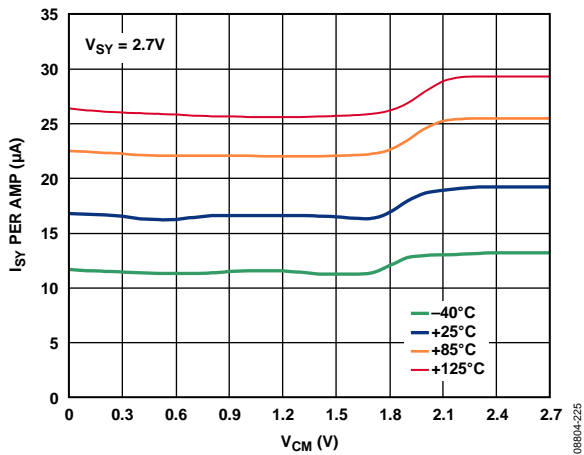


Figure 28. Supply Current vs. Common-Mode Voltage

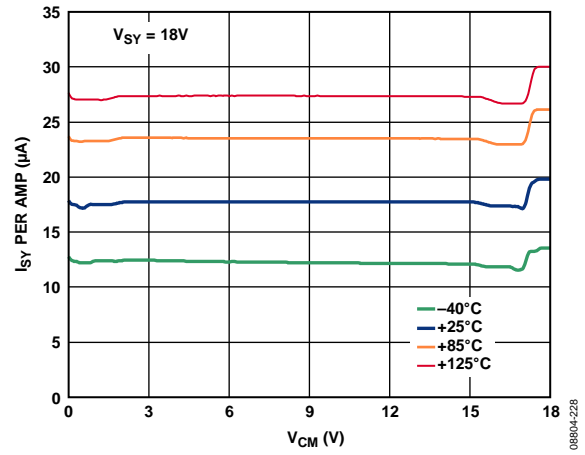


Figure 31. Supply Current vs. Common-Mode Voltage



Figure 32. Supply Current vs. Supply Voltage



Figure 35. Supply Current vs. Temperature



Figure 33. Open-Loop Gain and Phase vs. Frequency

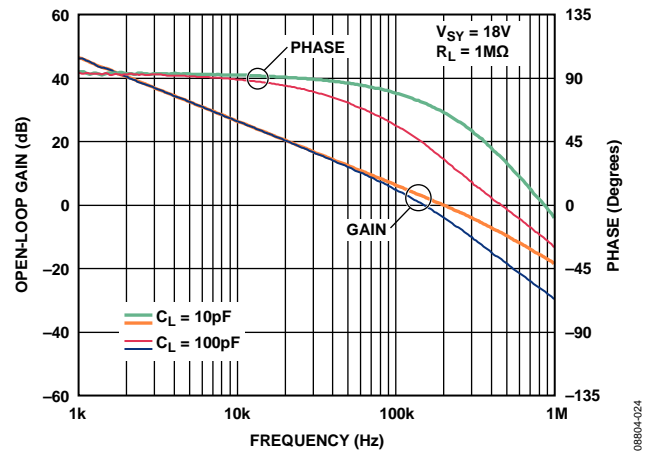


Figure 36. Open-Loop Gain and Phase vs. Frequency

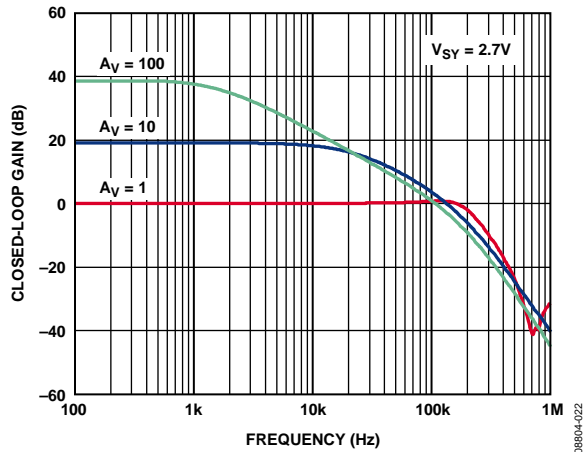


Figure 34. Closed-Loop Gain vs. Frequency

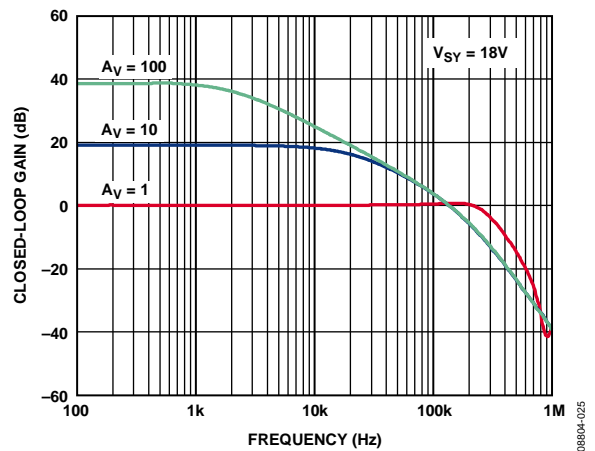


Figure 37. Closed-Loop Gain vs. Frequency



Figure 38. Output Impedance vs. Frequency



Figure 41. Output Impedance vs. Frequency



Figure 39. CMRR vs. Frequency



Figure 42. CMRR vs. Frequency



Figure 40. PSRR vs. Frequency



Figure 43. PSRR vs. Frequency



Figure 44. Small Signal Overshoot vs. Load Capacitance



Figure 47. Small Signal Overshoot vs. Load Capacitance



Figure 45. Large Signal Transient Response

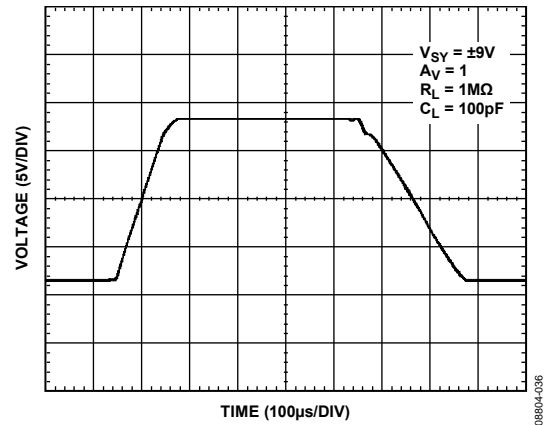


Figure 48. Large Signal Transient Response

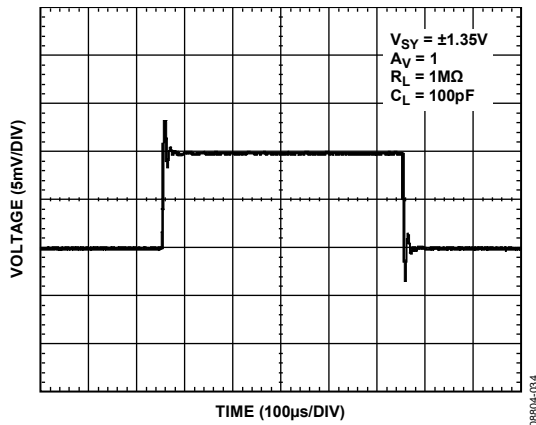


Figure 46. Small Signal Transient Response

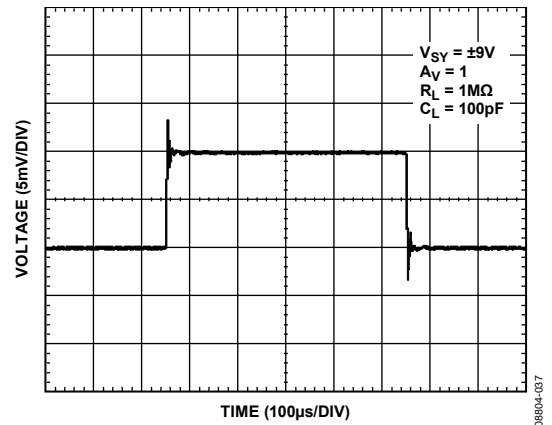


Figure 49. Small Signal Transient Response



Figure 50. Positive Overload Recovery

08804-039



Figure 53. Positive Overload Recovery

08804-042



Figure 51. Negative Overload Recovery

08804-038



Figure 54. Negative Overload Recovery

08804-041



Figure 52. Positive Settling Time to 0.1%

08804-040



Figure 55. Positive Settling Time to 0.1%

08804-043



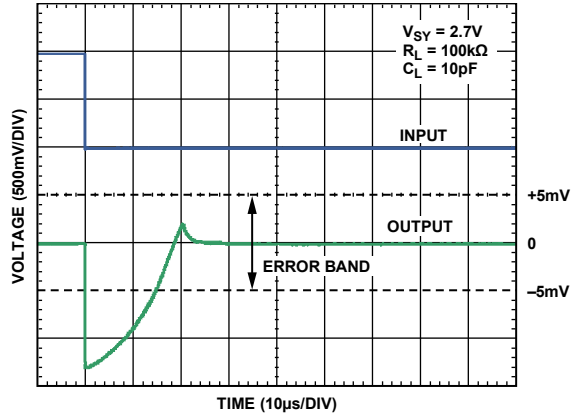


Figure 56. Negative Settling Time to 0.1%

08804-044

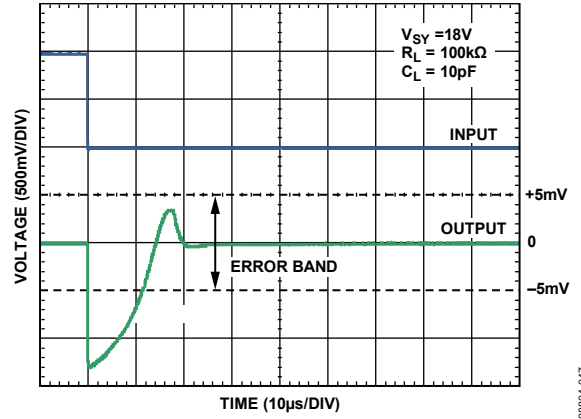


Figure 59. Negative Settling Time to 0.1%

08804-047

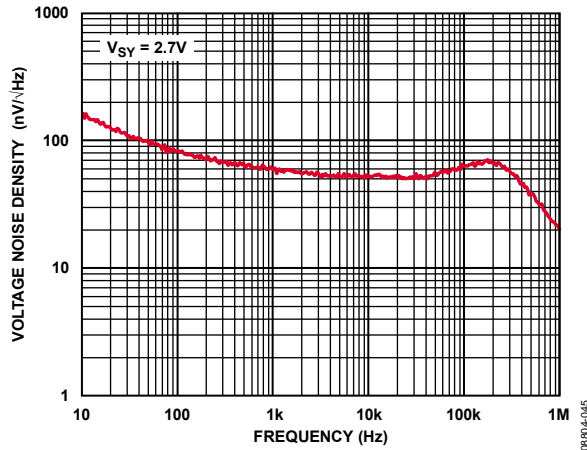


Figure 57. Voltage Noise Density vs. Frequency

08804-045

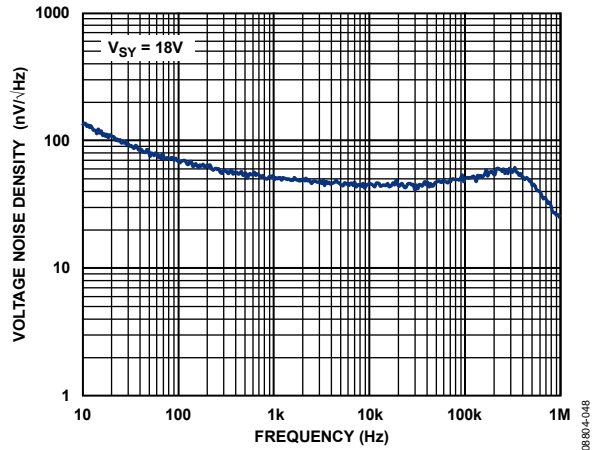


Figure 60. Voltage Noise Density vs. Frequency

08804-048



Figure 58. 0.1 Hz to 10 Hz Noise

08804-046

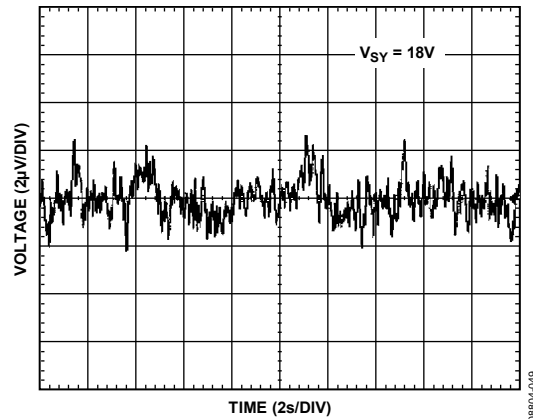


Figure 61. 0.1 Hz to 10 Hz Noise

08804-049



Figure 62. Output Swing vs. Frequency



Figure 65. Output Swing vs. Frequency

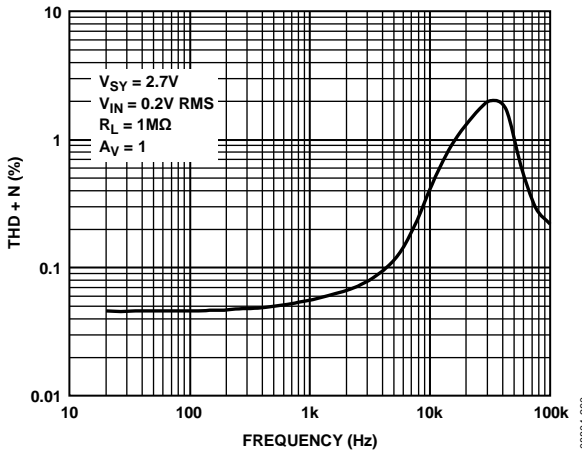


Figure 63. THD + N vs. Frequency



Figure 66. THD + N vs. Frequency

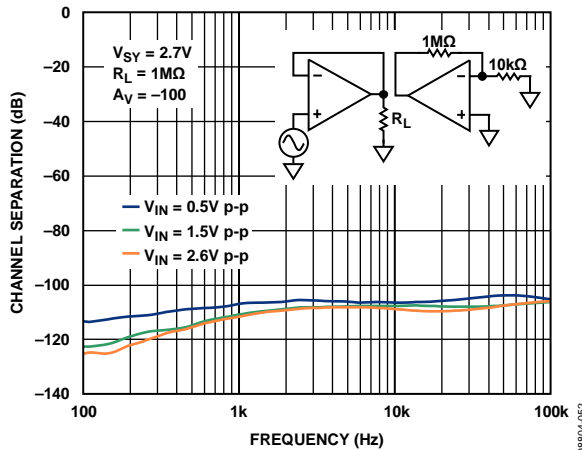


Figure 64. Channel Separation vs. Frequency



Figure 67. Channel Separation vs. Frequency

## APPLICATIONS INFORMATION



Figure 68. Simplified Schematic

The [AD8657/AD8659](#) are low power, rail-to-rail input and output precision CMOS amplifiers that operate over a wide supply voltage range of 2.7 V to 18 V. The [AD8657/AD8659](#) use the Analog Devices DigiTrim technique to achieve a higher degree of precision than is available from other CMOS amplifiers. The DigiTrim technique is a method of trimming the offset voltage of an amplifier after assembly. The advantage of post-package trimming is that it corrects any shifts in offset voltage caused by mechanical stresses of assembly.

The [AD8657/AD8659](#) also employ unique input and output stages to achieve a rail-to-rail input and output range with a very low supply current.

## INPUT STAGE

Figure 68 shows the simplified schematic of the [AD8657/AD8659](#). The input stage comprises two differential transistor pairs, an NMOS pair (M1, M2) and a PMOS pair (M3, M4). The input common-mode voltage determines which differential pair turns on and is more active than the other.

The PMOS differential pair is active when the input voltage approaches and reaches the lower supply rail. The NMOS pair is needed for input voltages up to and including the upper supply rail. This topology allows the amplifier to maintain a wide dynamic input voltage range and to maximize signal swing to both supply rails.

For the majority of the input common-mode voltage range, the PMOS differential pair is active. Differential pairs commonly exhibit different offset voltages. The handoff from one pair to the other creates a step-like characteristic that is visible in the  $V_{OS}$  vs.  $V_{CM}$  graphs (see Figure 10 and Figure 13). This characteristic is inherent in all rail-to-rail amplifiers that use the dual differential pair topology. Therefore, always choose a common-mode voltage that does not include the region of handoff from one input differential pair to the other.

Additional steps in the  $V_{OS}$  vs.  $V_{CM}$  curves are also visible as the input common-mode voltage approaches the power supply rails.

These changes are a result of the load transistors (M8, M9, M14, and M15) running out of headroom. As the load transistors are forced into the triode region of operation, the mismatch of their drain impedances contributes to the offset voltage of the amplifier. This problem is exacerbated at high temperatures due to the decrease in the threshold voltage of the input transistors (see Figure 14, Figure 15, Figure 17, and Figure 18 for typical performance data).

Current Source I1 drives the PMOS transistor pair. As the input common-mode voltage approaches the upper rail, I1 is steered away from the PMOS differential pair through the M5 transistor. The bias voltage, VB1 (see Figure 68), controls the point where this transfer occurs. M5 diverts the tail current into a current mirror consisting of the M6 and M7 transistors. The output of the current mirror then drives the NMOS pair. Note that the activation of this current mirror causes a slight increase in supply current at high common-mode voltages (see Figure 28 and Figure 31 for more details).

The [AD8657/AD8659](#) achieve their high performance by using low voltage MOS devices for their differential inputs. These low voltage MOS devices offer excellent noise and bandwidth per unit of current. Each differential input pair is protected by proprietary regulation circuitry (not shown in the simplified schematic). The regulation circuitry consists of a combination of active devices that maintain the proper voltages across the input pairs during normal operation and passive clamping devices that protect the amplifier during fast transients. However, these passive clamping devices begin to forward bias as the common-mode voltage approaches either power supply rail, thereby causing an increase in the input bias current (see Figure 20 and Figure 23).

The input devices are also protected from large differential input voltages by clamp diodes (D1 and D2). These diodes are buffered from the inputs with two 10 k $\Omega$  resistors (R1 and R2). The differential diodes turn on whenever the differential voltage exceeds approximately 600 mV; in this condition, the differential input resistance drops to 20 k $\Omega$ .

## OUTPUT STAGE

The AD8657/AD8659 feature a complementary output stage consisting of the M16 and M17 transistors. These transistors are configured in Class AB topology and are biased by the voltage source, VB2. This topology allows the output voltage to go within millivolts of the supply rails, achieving a rail-to-rail output swing. The output voltage is limited by the output impedance of the transistors, which are low  $R_{ON}$  MOS devices. The output voltage swing is a function of the load current and can be estimated using the output voltage to the supply rail vs. load current diagrams (see Figure 21, Figure 22, Figure 24, and Figure 25).

## RAIL TO RAIL

The AD8657/AD8659 feature rail-to-rail input and output with a supply voltage from 2.7 V to 18 V. Figure 69 shows the input and output waveforms of the AD8657/AD8659 configured as a unity-gain buffer with a supply voltage of  $\pm 9$  V and a resistive load of 1 M $\Omega$ . With an input voltage of  $\pm 9$  V, the AD8657/AD8659 allow the output to swing very close to both rails. Additionally, they do not exhibit phase reversal.



Figure 69. Rail-to-Rail Input and Output

## RESISTIVE LOAD

The feedback resistor alters the load resistance that an amplifier sees. It is, therefore, important to be aware of the value of feedback resistors chosen for use with the AD8657/AD8659. The amplifiers are capable of driving resistive loads down to 100 k $\Omega$ . The following two examples, inverting and noninverting configurations, show how the feedback resistor changes the actual load resistance seen at the output of the amplifier.

## Inverting Op Amp Configuration

Figure 70 shows the AD8657/AD8659 in an inverting configuration with a resistive load,  $R_L$ , at the output. The actual load seen by the amplifier is the parallel combination of the feedback resistor,  $R_2$ , and load,  $R_L$ . For example, the combination of a feedback resistor of 1 k $\Omega$  and a load of 1 M $\Omega$  results in an equivalent load resistance of 999  $\Omega$  at the output. Because the AD8657/AD8659 are incapable of driving such a heavy load, performance degrades greatly.

To avoid loading the output, use a larger feedback resistor, but consider the resistor thermal noise effect on the overall circuit.



Figure 70. Inverting Op Amp Configuration

## Noninverting Op Amp Configuration

Figure 71 shows the AD8657/AD8659 in a noninverting configuration with a resistive load,  $R_L$ , at the output. The actual load seen by the amplifier is the parallel combination of  $R_1 + R_2$  and  $R_L$ .

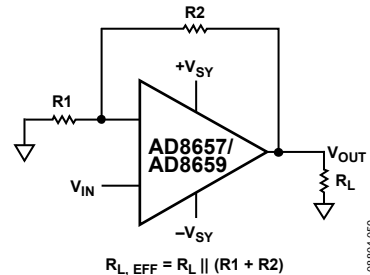


Figure 71. Noninverting Op Amp Configuration

**COMPARATOR OPERATION—AD8657**

An op amp is designed to operate in a closed-loop configuration with feedback from its output to its inverting input. Figure 72 shows the AD8657 configured as a voltage follower with an input voltage that is always kept at midpoint of the power supplies. The same configuration is applied to the unused channel. A1 and A2 indicate the placement of ammeters to measure supply current.  $I_{SY+}$  refers to the current flowing from the upper supply rail to the op amp, and  $I_{SY-}$  refers to the current flowing from the op amp to the lower supply rail. As shown in Figure 73, as expected in normal operating condition, the total current flowing into the op amp is equivalent to the total current flowing out of the op amp, where,  $I_{SY+} = I_{SY-} = 36 \mu\text{A}$  for the dual AD8657 at  $V_{SY} = 18 \text{ V}$ .



Figure 72. Voltage Follower



Figure 73. Supply Current vs. Supply Voltage (Voltage Follower)

In contrast to op amps, comparators are designed to work in an open-loop configuration and to drive logic circuits. Although op amps are different from comparators, occasionally an unused section of a dual op amp is used as a comparator to save board space and cost; however, this is not recommended.

Figure 74 and Figure 75 show the AD8657 configured as a comparator, with 100 kΩ resistors in series with the input pins. Any unused channels are configured as buffers with the input voltage kept at the midpoint of the power supplies. The AD8657/AD8659 have input devices that are protected from large differential input voltages by Diode D1 and Diode D2 (refer to Figure 68).

These diodes consist of substrate PNP bipolar transistors, and conduct whenever the differential input voltage exceeds approximately 600 mV; however, these diodes also allow a current path from the input to the lower supply rail, thus resulting in an increase in the total supply current of the system. As shown in Figure 76, both configurations yield the same result. At 18 V of power supply,  $I_{SY+}$  remains at 36  $\mu\text{A}$  per dual amplifier, but  $I_{SY-}$  increases to 140  $\mu\text{A}$  in magnitude per dual amplifier.

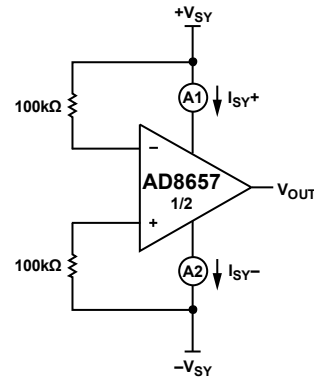


Figure 74. Comparator A

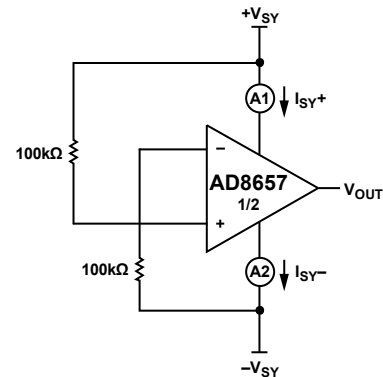


Figure 75. Comparator B

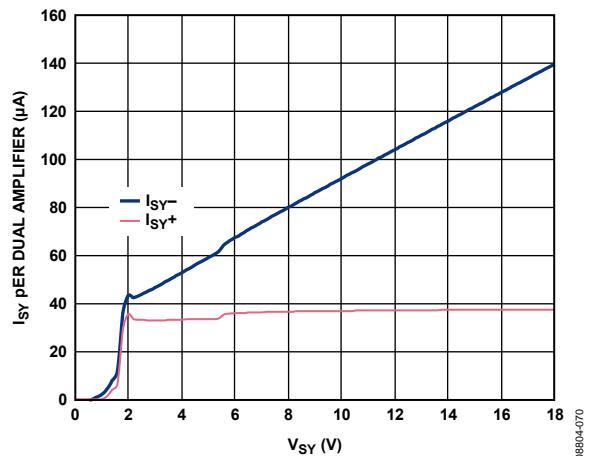


Figure 76. Supply Current vs. Supply Voltage (AD8657 as a Comparator)

Note that 100 kΩ resistors are used in series with the input of the op amp. If smaller resistor values are used, the supply current of the system increases much more. For more details on op amps as comparators, refer to the [AN-849 Application Note Using Op Amps as Comparators](#).

**EMI REJECTION RATIO**

Circuit performance is often adversely affected by high frequency electromagnetic interference (EMI). In the event where signal strength is low and transmission lines are long, an op amp must accurately amplify the input signals. However, all op amp pins—the noninverting input, inverting input, positive supply, negative supply, and output pins—are susceptible to EMI signals. These high frequency signals are coupled into an op amp by various means such as conduction, near field radiation, or far field radiation. For example, wires and PCB traces can act as antennas and pick up high frequency EMI signals.

Precision op amps, such as the [AD8657](#) and [AD8659](#), do not amplify EMI or RF signals because of their relatively low bandwidth. However, due to the nonlinearities of the input devices, op amps can rectify these out-of-band signals. When these high frequency signals are rectified, they appear as a dc offset at the output.

To describe the ability of the [AD8657/AD8659](#) to perform as intended in the presence of an electromagnetic energy, the electromagnetic interference rejection ratio (EMIRR) of the noninverting pin is specified in Table 2, Table 3, and Table 4 of the Specifications section. A mathematical method of measuring EMIRR is defined as follows:

$$EMIRR = 20 \log (V_{IN\_PEAK} / \Delta V_{OS})$$



Figure 77. EMIRR vs. Frequency

**4 mA TO 20 mA PROCESS CONTROL CURRENT LOOP TRANSMITTER—AD8657**

The 2-wire current transmitters are often used in distributed control systems and process control applications to transmit analog signals between sensors and process controllers. Figure 78 shows a 4 mA to 20 mA current loop transmitter.

The transmitter powers directly from the control loop power supply, and the current in the loop carries signal from 4 mA to 20 mA. Thus, 4 mA establishes the baseline current budget within which the circuit must operate. Using the [AD8657](#) is an excellent choice due to its low supply current of 34 μA per amplifier over temperature and supply voltage. The current transmitter controls the current flowing in the loop, where a zero-scale input signal is represented by 4 mA of current and a full-scale input signal is represented by 20 mA. The transmitter also floats from the control loop power supply, V<sub>DD</sub>, while signal ground is in the receiver. The loop current is measured at the load resistor, R<sub>L</sub>, at the receiver side.

At a zero-scale input, a current of V<sub>REF</sub>/R<sub>NULL</sub> flows through R'. This creates a current flowing through the sense resistor, I<sub>SENSE</sub>, determined by the following equation (see Figure 78 for details):

$$I_{SENSE, MIN} = (V_{REF} \times R') / (R_{NULL} \times R_{SENSE})$$

With a full-scale input voltage, current flowing through R' is increased by the full-scale change in V<sub>IN</sub>/R<sub>SPAN</sub>. This creates an increase in the current flowing through the sense resistor.

$$I_{SENSE, DELTA} = (Full\text{-Scale Change in } V_{IN} \times R') / (R_{SPAN} \times R_{SENSE})$$

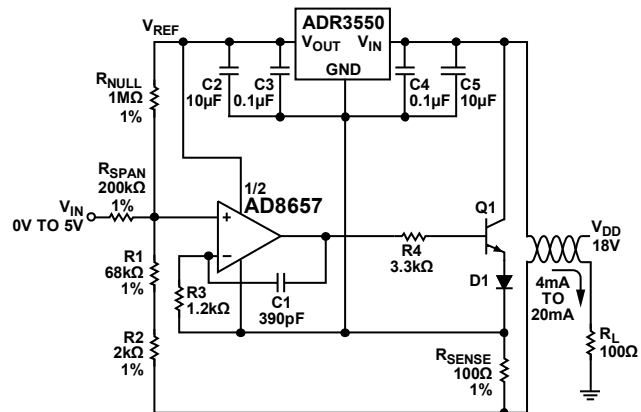
Therefore

$$I_{SENSE, MAX} = I_{SENSE, MIN} + I_{SENSE, DELTA}$$

When R' >> R<sub>SENSE</sub>, the current through the load resistor at the receiver side is almost equivalent to I<sub>SENSE</sub>.

Figure 78 is designed for a full-scale input voltage of 5 V. At 0 V of input, loop current is 3.5 mA; and at a full scale of 5 V, the loop current is 21 mA. This allows software calibration to fine tune the current loop to the 4 mA to 20 mA range.

The [AD8657](#) and [ADR3550](#) both consume only 160 μA quiescent current, making 3.34 mA current available to power additional signal conditioning circuitry or to power a bridge circuit.



NOTES  
1. R1 + R2 = R'

Figure 78. 4 mA to 20 mA Current Loop Transmitter





COMPLIANT TO JEDEC STANDARDS MS-012-AB  
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

060606-A

Figure 81. 14-Lead Standard Small Outline Package [SOIC\_N]  
 Narrow Body  
 (R-14)  
 Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-220-WGGC.

Figure 82. 16-Lead Lead Frame Chip Scale Package [LFCSP]  
 4 mm x 4 mm Body and 0.75 mm Package Height  
 (CP-16-17)  
 Dimensions shown in millimeters

ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Package Option	Branding
AD8657ARMZ	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2N
AD8657ARMZ-R7	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2N
AD8657ARMZ-RL	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2N
AD8657ACPZ-R7	-40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSP]	CP-8-11	A2N
AD8657ACPZ-RL	-40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSP]	CP-8-11	A2N
AD8659ARZ	-40°C to +125°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14	
AD8659ARZ-R7	-40°C to +125°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14	
AD8659ARZ-RL	-40°C to +125°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14	
AD8659ACPZ-R7	-40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-17	
AD8659ACPZ-RL	-40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-17	

<sup>1</sup> Z = RoHS Compliant Part.