D2-4P Family Audio SOC

Intelligent Digital Amplifier PWM Controller and Audio Processor

FN6766
Rev 2.00
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The D2-4P (D2-8001) and (D2-8002) devices are complete System-on-Chip (SoC) Class-D digital audio amplifiers. These devices combine high performance integrated Power Stages, Digital Signal Processor (DSP) and Audio Processor (AP) core controller to offer a complete, powerful, and very cost-effective audio solution for high volume and cost-critical products.

This 4th generation Digital Audio Processor D2-4P device combines extensive integrated Digital Signal Processor (DSP) audio processing with amplifier control for a complete audio solution. Its ease of integration into the existing system architecture provides complete support for all system product and amplifier functions.

The four configurable Power Stages operate as four separate Half-Bridge outputs, as two Full-Bridge outputs, or in combinations of Half-Bridge plus Full-Bridge, which provides flexible loudspeaker drive solutions. Separate PWM outputs provide additional combinations to drive headphone outputs or line-level stereo audio outputs.

Related Literature

For a full list of related documents, visit our website:

- D2-8001 and D2-8002 device pages

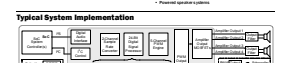
Features

- All digital Class-D amplifier and controller with integrated Digital Signal Processing (DSP)
- Four Integrated Power Stages supporting:
  - 2 Channels, Bridged
  - 4 Channels, Half-Bridge
  - 2 Channels, Half-Bridge, plus 1 Channel, Bridged
- Output power (bridged)
  - 20W (8Ω), 32V (THD), 30W (8Ω), 32V (THD)
- Fully programmable Digital Signal Processing (DSP)
  - Up to 8 programmable biquad peak parameters
  - Programmable equalizer, crossover, and limiter
- Sabre™ 32-bit DSP Sound Enhancement Algorithm and DTS®/SRS/WOW/MBT Audio Enhancement Algorithms
- I²S and Sony PDM™ digital audio inputs
- Asynchronous sample rate converters, sample rates from 8kHz to 192kHz
- Wide 10V to 26V Power Stage HV supply range, plus internally-generated gate drive supply
- Temperature and overload voltage monitoring and individual channel protection

Applications

- PC multimedia speakers
- Digital TV audio systems
- Portable device docking stations
- Powered speaker systems

Typical System Implementation


Boot Control
Boot Memory
Power Supplies
Clock Generation
Serial Control Interface
Digital Audio Interface
Sample Rate Converters
Sabre™ 32-bit DSP Sound Enhancement Algorithm
Digital Audio Processor
Power Stage Control
Power Stage Control
Power Stage Control

Ordering Information

PART NUMBER (Note 1, 2)	PART MARKING	SOME PROCESSING ALGORITHMS SUPPORT (Note 3)	TAPE AND REEL (Note 4)	TAPE WIDTH (Note 4)	PACKAGE (RoHS-Compliant)	PKG. DWG. #
D2-4P-007-QFI	D2-4P-007-QFI	D2 Audio DSP Sound Enhancement Algorithm	2Ku +8K	3k	68-Ld QFN	4B.3x3.0C
D2-4P-007-QFI-T	D2-4P-007-QFI	D2 Audio DSP Sound Enhancement Algorithm	2Ku +8K	3k	68-Ld QFN	4B.3x3.0C
D2-4P-007-QIB	D2-4P-007-QIB	D2 Audio DSP Sound Enhancement Algorithm (DTS®, SRS® WOW HD™	2Ku +8K	-	68-Ld QFN	4B.3x3.0C
D2-4P-007-QIB-T	D2-4P-007-QIB	D2 Audio DSP Sound Enhancement Algorithm (DTS®, SRS® WOW HD™	2Ku +8K	3k	68-Ld QFN	4B.3x3.0C

NOTES:

1. The D2-4P chipsets support and/or processing algorithms for the D2 Audio DSP Sound Enhancement Algorithm and DTS®, SRS® WOW HD™ audio enhancement features. Algorithm support for these enhancements is device dependent. See the device part number for feature support.
2. See TN1047 for details about reel specifications.
3. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials and NiPdAu plate - all terminations finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. The Pb-free product meet IEEE J-Std-020d.1 Pb-free peak reflow temperatures. Add more to round the Pb-free requirements of IPC/JEDEC J-STD-020.
4. For Moisture Sensitivity Level (MSL), see the D2-4P-007 and D2-4P-007-QIB device pages. For more information, see also TB363.

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Absolute Maximum Ratings (Note.1)

Supply Voltage	
Core Supply Voltage	-0.3V to +2.0V
PVDD, PVDDD	-0.3V to 4.2V
CVDD, CVDDD	-0.3V to +4.2V
Input Voltage	
Digital Input (5V)	-0.3V to PVDD +0.3V
5Vtol	-0.3V to PLLVDD +0.3V
Input Current, Any Pin but Supplies	±10mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA}(°C/W) θ_{JC}(°C/W)
80 Ld EPS Package (Note.2, 3)	24 1.5
Maximum Junction Temperature	+150°C to +150°C
Pb-Free Reflow Profile	see TB493

Recommended Operating Conditions

Temperature Range	-20°C to +85°C
Supply Voltage	
Digital I/O Supply Voltage, PVDD	3.3V to 3.6V
Core Supply Voltage, CVDD	1.8V
Digital Core Supply Voltage, CVDDD	1.8V
Minimum Load Impedance (RDDD,RDD,CDDD,DD)	Ω

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See TB379.
2. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
3. Absolute Maximum parameters are not tested in production.

Electrical Specifications T_A = -20°C, AVDD,DVDD,VDDH = 3.3V, CVDD = PLLVDD = 1.8V ±5%, RDDD = PVDDD = 3.3V ±5%

All grounds at 0.0V. All voltages referenced to ground. PLL at 25.6/12.8MHz, DDC at 25.6MHz, over operating or ±47.5/50/50/+5% typical audio data rates

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT
Digital Input High Level Voltage (Note.4)		V_{IH}	2	-	-	V
Digital Input Low Level Voltage (Note.4)		V_{IL}	-	-	0.8	V
High Level Output Drive Voltage (Pins 2,3,4,5,6,7,8,9,10,11,12,13,14,15,16,17,18,19,20,21,22,23,24,25,26,27,28,29,30,31,32,33,34,35,36,37,38,39,40,41,42,43,44,45,46,47,48,49,50,51,52,53,54,55,56,57,58,59,60,61,62,63,64,65,66,67,68,69,70,71,72,73,74,75,76,77,78,79,80)		V_{OH}	RDDD - 0.4	-	-	V
Low Level Output Drive Voltage (Pins 2,3,4,5,6,7,8,9,10,11,12,13,14,15,16,17,18,19,20,21,22,23,24,25,26,27,28,29,30,31,32,33,34,35,36,37,38,39,40,41,42,43,44,45,46,47,48,49,50,51,52,53,54,55,56,57,58,59,60,61,62,63,64,65,66,67,68,69,70,71,72,73,74,75,76,77,78,79,80)		V_{OL}	-	-	0.4	V
Input Low Level Drive Voltage (Pin 75)		V_{IDL}	0.7	-	PLLVDD	V
Low Level Input Drive Voltage (Pin 75)		V_{IL}	-	-	0.3	V
Input Leakage Current (Note.5)		I_{IN}	-	-	±10	µA
Input Capacitance		C_{IN}	-	-	10	pF
Output Capacitance	All Digital Output Pins (Pins 2,3,4,5,6,7,8,9,10,11,12,13,14,15,16,17,18,19,20,21,22,23,24,25,26,27,28,29,30,31,32,33,34,35,36,37,38,39,40,41,42,43,44,45,46,47,48,49,50,51,52,53,54,55,56,57,58,59,60,61,62,63,64,65,66,67,68,69,70,71,72,73,74,75,76,77,78,79,80)	C_{OUT}	-	6	-	pF
	DATA (0)		-	200	-	pF
µRESET Pulse Width		T_{RST}	-	300	-	ns
Internal Pull-Up Resistance on PWRGOOD (for µRESET, CLKTL, CLKTL, µRXD)			-	300	-	kΩ
Digital I/O Supply Pin Voltage, Current		RDDD and PVDDD Pins	3.3	3.3	3.6	V
	Active Current		-	0.1	-	mA
	Power-Down Current		-	0.01	-	mA
Core Supply Pins		CVDD, CVDDD	1.7	1.8	1.9	V
	Active Current		-	100	-	mA
	Power-Down Current (Note.6)		-	4	-	mA

Electrical Specifications T_A = -10°C, $V_{DD(D,A,C)}$ = 3.0V, $V_{DD(P)}$ = 2.4V, C_{DD} = $V_{DD(D)}$ - 1.8V, V_{SS} = $V_{SS(D,A,C,P)}$ = 0.0V, $V_{DD(D,A)}$ = 3.3V, $V_{DD(C)}$ = 2.5V, all voltages referenced to ground. PLL at 24.576 MHz, CKO 12.288 MHz, core running at 147.456MHz with typical audio data traffic.

Standard

	MIN	TYP	MAX	UNIT
Analog Supply Pins (Pin)	$V_{DD(D)}$ -0.3	3.3	3.6	V
Active Current		30		mA
Power Down Current (Note 2)		6		mA

GENERAL SPECIFICATIONS

Crystal Frequency (Fundamental Mode Crystal)	f_{XT}	20	24.576	25	MHz
Crystal Load Capacitance	C_L	40		60	%
Start-Up Time (Start-Up Time to Oscillator Enable at Power Down Supply to Sector Decoder)	t_{STUP}		5	20	ms

PLL

VCO Frequency	F_{VCO}	260	294.912	300	MHz
PLL Lock Time from any input change				5	ms

I/O VOLTAGE CHECKS

Power Down Voltage Level	V_{PD}	-0.05		0.4	V
Pull Minimum Power Pulse Width	T_{PW}		5		µs

I/O VOLTAGE CHECKS

Reset Level		0.4	3.3	3.7	V
Pulse Width Rejection	T_{RPW}		200		ns
Minimum Reset Pulse Width	T_{RS}		20		ms

I/O (PARALLEL/SERIAL) CHECKS

Reset Level		2.3	2.7	2.9	V
Pulse Width Rejection	T_{RPW}		200		ns
Minimum Reset Pulse Width	T_{RS}		20		ms

I/O CHECKS (SERIAL, PIO CHECKS OTHERS)

Gate Drive Supply (Interface Transistor)			4.5	V
Gate Drive Supply (Interface Transistor) Hysteresis			200	mV
Gate Drive Supply (Interface Transistor) Glitch Rejection			50	ns

PARALLEL I/O

High Voltage (+5.0Vtol) (Interface Protection)			7	V
Overcurrent Trip Threshold			2	A
Overcurrent Deglitch			20	ns
Short Circuit Current Limit (Peak)			8	A
Overcurrent Response Time			25	ns
Thermal Shutdown (Power Stages)			200	°C
Thermal Shutdown Hysteresis (Power Stages)			5	°C

NOTES:

1. All input pins except XTAL1.
2. Input leakage applies to all pins except XTAL1.
3. Power-down is with device in reset and clocks stopped.

Performance Specifications

T_A = -20° C, $AVDD_{LO}$/$DVDD_{LO}$/$VDDH$ = 24V, $DVDD$ = $PLLVDD$ = 1.8V ±5%, $RVDD$ = $PWRVDD$ = 3.3V ±5%.
All grounds at 0V. All voltages referenced to ground. R_L of 24Ω, SQ24Ω, 20Ω at 24/12/6Ω, over sampling at 128 SCKI/Bit with typical audio data traffic.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
I_{VDDH} (Electronic MOSFETs at 12Ω)	I_{VDDH}	-	200	-	mA
I_{RVDD} (Normal)	I_{RVDD}	-	4	-	mA
PWM Switching Rate		-	384	-	kHz
ePDR Input 3V Delay	$t_{DelayEP}$	-	3.4	-	ms
ePDR Input 0v Delay	$t_{DelayEN}$	-	3.4	-	ms
PERFORMANCE					
12Ω THD, Bridged, Load = 8Ω, VOUT(p2-p) = 24V	P_{OUT}	-	26	-	W
12Ω THD, Bridged, Load = 8Ω, VOUT(p2-p) = 23V	P_{OUT}	-	23	-	W
12Ω THD, Half-Bridge, Load = 8Ω, VOUT(p2-p) = 24V	P_{OUT}	-	7	-	W
12Ω THD, Half-Bridge, Load = 8Ω, VOUT(p2-p) = 23V	P_{OUT}	-	9	-	W
TRIMS					
Level = 8Ω, Power = 23W, Bridged, 3dBw	THD+N	-	0.3	-	%
Level = 8Ω, Power = 23W, Bridged, 0dBw		-	0.05	-	%
SNR	SNR	-	110	-	dB
Efficiency (Power-Stage, Load = 8Ω)		-	90	-	%

Serial Audio Interface Port Timing

T_A = -20° C, $AVDD_{LO}$/$DVDD_{LO}$/$VDDH$ = 24V, $DVDD$ = $PLLVDD$ = 1.8V ±5%, $RVDD$ = $PWRVDD$ = 3.3V ±5%.
All grounds at 0V. All voltages referenced to ground. R_L of 24Ω, SQ24Ω, 20Ω at 24/12/6Ω, over sampling at 128 SCKI/Bit with typical audio data traffic.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
f_{SCKI}	SCKI Frequency (MCLK)	-	-	13.5	MHz
t_{SCKI}	SCKI Pulse Width high and low (MCLK)	40	-	-	ns
t_{LRCSU}	LRCKR Setup to SCLK Rising (LRCK)	20	-	-	ns
t_{LRCHD}	LRCKR Hold from SCLK Rising (LRCK)	20	-	-	ns
t_{SDS}	SDIN Data to SCLK Rising (SDIN)	20	-	-	ns
t_{SDH}	SDIN Hold from SCLK Rising (SDIN)	20	-	-	ns

FIGURE 3. SERIAL AUDIO INTERFACE PORT TIMING

Two-Wire (I^2C) Interface Port Timing

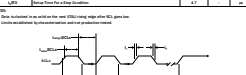
T_A = -20° C, CVDD = PLLVDD = 1.8V (±5%), RVDD = PWRVDD = 3.3V (±5%). All grounds at 0.0V. All voltages referenced to ground.

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
f_{SCL}	SCL Frequency	-	400	kHz
t_{rise}	Rise Time Between Transmissions	4.7	-	µs
$t_{hold(STA)}$	SCL Clock Low	4.7	-	µs
$t_{high(STA)}$	SCL Clock High	4.0	-	µs
t_{SUTA}	Setup Time for a (Repeated) Start	4.7	-	µs
t_{HDTA}	Start Condition Hold Time	4.0	-	µs
t_{LOWSCL}	SDA Hold Time SCL Falling (Note 1)	0 (typical)		ns/cycle
t_{SUSDA}	SDA Set Up Time to SCL Rising	250	-	ns
t_{HDSDA}	SDA Output Delay Time Per SCL Falling	-	3.5	µs
T_r	Rise Time of Both SDA and SCL (Note 2)	-	1	µs
T_f	Fall Time of Both SDA and SCL (Note 2)	-	300	ns
t_{SUTO}	Setup Time For a Stop Condition	4.7	-	µs

NOTES:

1). Data is clocked in as soid on the next SCLL rising edge after SCL goes low.

2). Limits established by characterization and not production tested.


tSUTA
tSUTO
SCL
tLOW
tHDSDA
tSUSDA
tHDTA
SDA
(INPUT)
SDA
(OUTPUT)
tSUTA
tHDTA
tSUSDA
tHDSDA
tLOW
tSUTO
tHDTA
tSUTA
tHDTA
tSUSDA
tHDSDA
tSUTO

SPI™ Master Mode Interface Port Timing T_A = -10 °C, DVDD = PLLVDD = 1.8V ±5%, RVDD = PWRVDD = 3.3V ±10%. All grounds at 0V. All voltages referenced to ground.

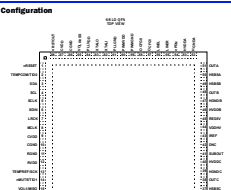
SYMBOL	DESCRIPTION	MIN	MAX	UNIT
t_{sc}	MISO Valid Prior Clock Edge	8		ns
t_{hc}	MISO Data up to Clock Edge	1.0		ns
t_{lc}	MISO Valid Prior Clock Edge	1 system clock + 2ns		
t_{dd}	MISO Minimum Width	3 system clocks + 2ns		

SPI™ Slave Mode Interface Port Timing T_A = +-20 °C, DVDD = PLLVDD = 1.8V ±5%, RVDD = PWRVDD = 3.3V ±10%. All grounds at 0V. All voltages referenced to ground.

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
t_{sc}	MISO Valid Prior Clock Edge	3 system clocks + 2ns		
t_{hc}	MISO Data up to Clock Edge	1.0		ns
t_{lc}	MISO Valid Prior Clock Edge	3 system clock + 2ns		
t_{dd}	MISO Minimum Width	3 system clocks + 2ns		

FIGURE 6. SPI TIMING

Pin Configuration



Pin Descriptions

PIN	PIN NAME	TYPE	DRIVE STRENGTH (mA)	DESCRIPTION
1	nRESET	I	3.3	Active low reset input with hysteresis. A low level activates a system level reset, which initializes all internal logic and program operations. The system latches the boot mode selection on the [RX] input pins on the rising edge of nRESET.
2	TEMPCONTROL	O	3.3	Board temperature monitor on mono I2S pin. Provides 50mA drive strength when operating as an output.
3	SDA	O/B	3.3	Receive serial data port, open drain driver with 8mA drive strength. Bidirectional signal used by both the master and slave controllers for data transport. Pin floats on reset.

Pin Descriptions (continued)

PIN NAME	PIN NO.	VOLTAGE (VDD=3.3V)	DESCRIPTION
SCL	128	3.3_O	Serial port clock pin. open drain driver with Schmitt-trigger receiver. Bidirectional signal used by both the serial port and the internal boot EEPROM. Pull-up required.
SDA	1	3.3_O	PC serial data bi-directional (SDA) input. Open drain output.
SDIN	1	3.3_I	PC serial audio data (SDIN) input. Input/output pin.
LRCK	1	3.3_I	PC serial audio left/right (LRCK) input. Input/output pin.
MCLK	0	3.3	PC serial audio master clock output for external ADC/DAC components, directly or via smart. Output is an 8mA driver.
CVDD	P	3.3	Core power, +1.8VDC. Used in the chip internal DSP logic, and interfaces.
CGND	GND	3.3	Core ground.
RSND	GND	3.3	Digital analog ground. Internally connected to PSNDD.
RVDD	P	3.3	Digital analog power. Nominally 3.3V. This 3.3V supply is used to all the digital I/O pad drivers and receivers, except for the analog pads. Both of these pins must be connected. Internally connected to PRVDD.
TEMPREF/ SDR	1	3.3_O	Reference output for the temperature sensor (TEMPREF). Also, the serial port data output (SDR) pin, operates as a SPI slave with Bi-directional strength. Upon internal 32kP Reference resistor, this pin becomes a temperature sensor output.
nRESET/ D	0	3.3_I	Reset signal input. When active low, a reset sequence initializes pin. See The output is a 16mA driver. Upon internal 32kP Reset resistor, this pin becomes a digital output (D) for monitoring boot.
VOLL/ VSL	1/0	3.3_O	Volume control pulse input and PWM output. Upon internal 32kP Reset resistor, this pin becomes a digital output (D) for monitoring boot. Also, the serial port left/right (VSL) pin, operates as a SPI slave with Bi-directional strength. Upon internal 32kP Reset resistor, this pin becomes an input for monitoring boot. Also, the serial port left/right (VSL) pin, operates as a SPI slave with Bi-directional strength.
TEMPIN/ MISO	1/0	3.3_O	Reset temperature sensor input. Also, the serial port data input (MISO) pin. Upon internal 32kP Reset resistor, this pin operates as a SPI master output or slave input (when operating as an output, pin drives low). Upon internal 32kP Reset resistor, this pin becomes an input for monitoring boot. Also, the serial port data input (MISO) pin.
SPIGPIO0	1	3.3	SPI GPIO pin. Open drain output.
SPIGPIO1	0	3.3	SPI GPIO pin. Open drain output. To pull up, Upon internal 32kP Reset resistor, this pin becomes an input for monitoring boot.
TEST	1	3.3	Reserved. Pull-down. Connect to GND. Do Factory use only. Must be tied low.
IRQ0	1	3.3	Interrupt request pin 0. One of four IRQ pins, tied to logic 0, IRQ high or to ground. High/low logic values established on the last rising edge of the reset signal. Also, operates as the nIRQ0 input.
IRQ1	1	3.3	Interrupt request pin 1. One of four IRQ pins, tied to logic 0, IRQ high or to ground. High/low logic values established on the last rising edge of the reset signal. Also, operates as the nIRQ1 input.
RSND	GND	3.3	Digital analog ground. Internally connected to PSNDD.
SPIMOSI/ GPIO3	1/0	3.3_O	Output configurable serial port and general purpose output. Bi-direction mode, this pin operates as an input and uses an application installed pull-up or pull-down connection to the pin to specify one of four amplifier configurations. Upon internal 32kP Reference resistor, this pin becomes an output and provides a 16mA open drain output driver when amplifier protection monitoring detects an error condition. When operating as an output this pin provides 8mA drive strength. This pin may also be called "PSCLEAR" a consumer reference designs. Functions internal registers or memory.
PSVMON/ GPIO4	1/0	3.3_O	Output configurable reference input and power supply input output. Bi-direction mode, this pin operates as an input and uses an application installed pull-up or pull-down connection to the pin to specify one of four amplifier configurations. Upon internal 32kP Reference resistor, this pin becomes an output and provides a synchronizing signal to an based power supply circuits. When operating as an output, this pin provides 8mA drive strength. This pin may also be called "PSCLEAR" a consumer reference designs. Functions internal registers or memory.
PRDNETS	1/0	3.3_O	PWM pull-down. Input bias bias. Bi-direction. This pin is protection monitoring functionality is enabled by the amplifier configuration. Upon internal 32kP Reference resistor, this pin becomes an output and provides a 16mA open drain output driver when amplifier protection monitoring detects an error condition. When operating as an output, this pin provides 8mA drive strength.

Pin Descriptions (Continued)

PIN NUMBER		VOLTAGE (VDD_2)		DESCRIPTION
24	PRESET[0]	3.3	3.3	PWM pulse-width input. Input has hysteresis. This pin's pulse-width measurement functionality is activated by setting the PRESET_EN bit in the PWM_CONFIG register. Otherwise, this pin is a general-purpose input.
25	PRESET[1]	3.3	3.3	PWM pulse-width input. Input has hysteresis. This pin's pulse-width measurement functionality is activated by setting the PRESET_EN bit in the PWM_CONFIG register. Otherwise, this pin is a general-purpose input.
26	AERROR0	3.3	3.3	Overcurrent protection output, channel 0 (active-low). Open-drain 3.3V-tolerant with internal 100kΩ pull-up (approximate). Pulls low when active. Non-overcurrent detection of this output stage.
27	AERROR1	3.3	3.3	Overcurrent protection output, channel 1 (active-low). Open-drain 3.3V-tolerant with internal 100kΩ pull-up (approximate). Pulls low when active. Non-overcurrent detection of this output stage.
28	AERROR2	3.3	3.3	Overcurrent protection output, channel 2 (active-low). Open-drain 3.3V-tolerant with internal 100kΩ pull-up (approximate). Pulls low when active. Non-overcurrent detection of this output stage.
29	AERROR3	3.3	3.3	Overcurrent protection output, channel 3 (active-low). Open-drain 3.3V-tolerant with internal 100kΩ pull-up (approximate). Pulls low when active. Non-overcurrent detection of this output stage.
30	VDDIO	P	P	Output stage 3.3Vdd voltage (nominally power. A separate power pin connection is provided for each of the output stages. All of the VDDIO(3.3)[n] pins connect to system "4V" power ground (see Note 3.0).
31	NON_OD	GND	P	Output stage 3.3Vdd voltage (nominally ground. Every output ground pin connection is provided for each of the output stages. All of the NON_OD[n] pins connect to system "4V" power ground (see Note 3.0).
32	GND	0	P	PWM power amplifier, channel 0.
33	HSRC0	3.3	P	High-side boot strap input, channel 0. Capacitor coupled to OUT0 amplifier output.
34	HSRC1	3.3	P	High-side boot strap input, channel 1. Capacitor coupled to OUT1 amplifier output.
35	GND	0	P	PWM power amplifier, channel 1.
36	NON_OD	GND	P	Output stage 3.3Vdd voltage (nominally ground. A separate ground pin connection is provided for each of the output stages. All of the NON_OD[n] pins connect to system "4V" power ground (see Note 3.0).
37	VDDIO	P	P	Output stage 3.3Vdd voltage (nominally power. A separate power pin connection is provided for each of the output stages. All of the VDDIO(3.3)[n] pins connect to system "4V" power ground (see Note 3.0).
38	SUBOUT	3.3	3.3	Subwoofer channel PWM output with 3.3Vdd drive strength. Connects to Wire network for supplying subwoofer channel.
42	SNC			Do not connect to this pin.
43	SUBIN			Subwoofer reference analog input. Used for setting the overcurrent error detect internally set threshold. This pin needs to be connected to a 3.3VDD resistor to ground to set the overcurrent threshold according to the application.
44	VDD1V	P	P	Output stage 1.0Vdd voltage (nominally power. A separate power pin connection is provided for each of the output stages. All of the VDD(1.0)[n] pins connect to system "4V" power ground (see Note 3.0).
45	RESET	P	3.3	3V interrupt-tolerant Reset control. A VDD supply brownout, power from the voltage source provided at the VDD pin, RESET is used for external connection of decoupling capacitors.
46	VDDIO	P	P	Output stage 3.3Vdd voltage (nominally power. A separate power pin connection is provided for each of the output stages. All of the VDDIO(3.3)[n] pins connect to system "4V" power source.
47	NON_OD	GND	P	Output stage 3.3Vdd voltage (nominally ground. A separate ground pin connection is provided for each of the output stages. All of the NON_OD[n] pins connect to system "4V" power ground (see Note 3.0).
48	GND	0	P	PWM power amplifier, channel 2.
49	HSRC2	3.3	P	High-side boot strap input, channel 2. Capacitor coupled to OUT2 amplifier output.
50	HSRC3	3.3	P	High-side boot strap input, channel 3. Capacitor coupled to OUT3 amplifier output.
51	GND	0	P	PWM power amplifier, channel 3.
52	NON_OD	GND	P	Output stage 3.3Vdd voltage (nominally ground. A separate ground pin connection is provided for each of the output stages. All of the NON_OD[n] pins connect to system "4V" power ground (see Note 3.0).

Pin Descriptions (Continued)

PIN	PIN NAME (Note 1)	TYPE (Note 2)	VOLTAGE (Note 3)	DESCRIPTION
69	MIDOUT	P	3.3	Output stage 3.3V-tolerant open-drain. Enabled in power-on reset mode to pass the output of the output stage to the pin. Disabled in power-on reset mode to tri-state the output stage.
70	uRDY	I	3.3	Active-low input and pull-up. Active-low. When the input stage, after the output stage has reset (reset and then output stage Reset, and then output stage is reset), internal logic and other other resets remain active during the power-down state.
71	USBP	O	3.3	Digital 12 mend PWM output, with 10mA drive strength. Connects to the filter network to supply the line level analog output.
72	USBN	O	3.3	Sub1 channel PWM output, with 10mA drive strength. Connects to the filter network to supply the line level analog output.
73	SDTO0	I	3.3	Serial configuration control select. SDTO0 and SDTO1 are logic inputs to select the output configuration mode of the output stages. Connects to either the PWM0/M2 ground or PWM0/M2=3.3V. (Keep a reserved SDTO0 mode for select output configuration)
74	SDTO1	I	3.3	Serial configuration control select. SDTO0 and SDTO1 are logic inputs to select the output configuration mode of the output stages. Connects to either the PWM0/M2 ground or PWM0/M2=3.3V. (Keep a reserved SDTO0 mode for select output configuration)
75	PWM0/M2	P	3.3	PWM output pin ground. Internally connected to PGND.
76	PWM0/M2	P	3.3	Sub2 channel PWM output, with 10mA drive strength. To use the PWM pad drivers, internally connected to PGND.
77	PLLGND	P	1.8	PLL analog ground. This is a low voltage ground. (GND). PGND is through a single point connection to isolate ground noise on the board and minimize effects on the PLL.
78	ETM2	P	1.8	Digital oscillator analog frequency
79	ETM1	P	1.8	Digital oscillator analog frequency (this output drives the crystal and ETM2 does not have a drive strength is not floating)
80	PLLVDD	P	1.8	PLL analog power, 1.8V.
81	VDD1 (1V)	I/O	3.3	Volume control pulse input and OP drive select. When drive mode is demanded, this pin operates as a SPI serial data output pin. Internal 32 OP Transmit enable. this pin becomes an input for monitoring up-down phase pulses from volume control (one of two volume input pins).
82	CGND	P	1.8	Core ground
83	CVDD	P	1.8	Core power, 1.8SDC. Used in the chip internal DSP logic, and oscillator.
84	uVREADY	O	3.3	Active-low open-drain output with 10mA drive strength. This pin drives low when the PWM0/M2 3.3V is nominal detector. PWM0/M2 3.3V is nominal detector, or USB transceiver detector gets active (Use this output to control a system reset to the uRESET pin in power-down mode).

NOTES:

12. Unused pin names are active high unless otherwise specified. Active low signals have an "n" prefix, such as nRESET.
13. All pins and ground pins should be left open (floating) or tied to ground in all other modes of their same name (that is, for CODS pins together, CGND pins together, PGND pins together, and PGND pin on signal Ref). The CGND and PGND signals can be tied ground and the PGND and PWM0/M2 pins are internally connected and tied together on the board.
14. The thermal pad is internally connected to all four GND ground pins (AGNDA, AGNDB, AGNDC, and AGNDD). Any connection to the thermal pad must be made to the common ground on the ear four ground pins.

Typical Performance Characteristics

Test Considerations

- Typical performance measurements are made using an Audio Precision® 2700 Series audio analyzer.
- Precision power resistors are used for the BD loadpseudo loads.
- Measurements are done using a +5V supply of +25.0VDC.

Full-Bridge Typical Performance Curves

FIGURE 5. THD+N POWER, FULL-BRIDGE

FIGURE 6. THD+N FREQUENCY, FULL-BRIDGE

FIGURE 7. FREQUENCY RESPONSE, FULL-BRIDGE

FIGURE 8. NOISE FLOOR, FULL-BRIDGE

Half-Bridge Typical Performance Curves

FIGURE 9. THD vs POWER, HALF-BRIDGE

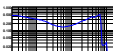


FIGURE 10. THD vs FREQUENCY, HALF-BRIDGE

FIGURE 11. FREQUENCY RESPONSE, HALF-BRIDGE

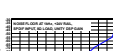
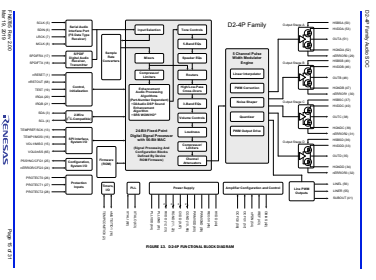


FIGURE 12. NOISE FLOOR, HALF-BRIDGE


D2-4P Family
SCLK (C)
SDIN (B)
LRCK (F)
MCLK (E)
SPDIFTX (J7)
SPDIFTX (J8)
VRINT (T)
VRINTOUT (R)
TEST (H)
RSLA (G)
RSB (G)
RSN (G)
SCL (E)
TEMPTMSR (G)
TEMPTMSR (H)
VRLIMMS (H)
VOLMAX (H)
PWRINGOFF (H)
VRRINGOFF (H)
PROTECTS (H)
PROTECTS (H)
PROTECTS (H)
Serial Audio Interface (Tri-State Type Receiver)
Serial Audio Interface (Tri-State Type Transmitter)
Control, Initialization
GPIO Port Control
MI Interface Control Unit
Configuration Control
Protection Inputs
Sample Rate Converter
Input Selector
Mixer
Equalizer
Equalizer Coefficient Calculation Unit
Delay Memory
Input Selector
Mixer
Mixer Memory
Limiter
Limiter Memory
Volume Control
Volume Control Memory
Protection Control
Protection Control Memory
Output Selector
Output Selector Memory
Sample Rate Converter
Sample Rate Converter Memory
Serial Port Control
Serial Port Control Memory
Clock Generator
Clock Generator Memory
Interrupt Control
Interrupt Control Memory
Interrupt Output
Interrupt Output Memory
Interrupt Input
Interrupt Input Memory
Interrupt Input Control
Interrupt Input Control Memory
Interrupt Input Control Memory
Interrupt Input Control Memory

Functional Description

Overview

The D2-4P devices, shown in Table 12 on page 120, are integrated system-on-Chip (SoC) audio processors and Class D digital audio amplifiers. The processor includes signal selection, signal routing, complete audio processing, PWM generation, and digital audio interfaces supporting multi-channel I2S, TDM, S/PDIF and S/PDIF Digital input signals. pin I^2C and 2-wire SPI control interfaces, provide integration, compatibility with existing system architectures and solutions.

The four configurable power-stages can operate as four separate half-bridge outputs, two full-bridge outputs, or in combinations of half-bridge plus Full-Bridge outputs. Separate power-stage outputs can be configured for driving headphone outputs, or stereo line-level analog outputs. These application dependent configurations provide for driving 3ohm (2Ω Speaker, 2.5Speaker, and 3ohm (2.2Ω) long Speaker solutions, as well as providing Stereo Line outputs, Headphone outputs, or Subwoofer outputs.

Audio output implementations are defined by the configuration of the power-stage outputs. Four independent power-stages can be four amplifier outputs as shown in Table 2. The four independent audio processing paths feed a PWM engine, where the four PWM channels are mapped to the configuration-selected power-stages and line-outputs.

The audio path includes a stereo Sample Rate Converter (SRC), four independent audio processing paths, and four independently audio enhancement algorithms.

Programmable processing capability for audio processing include volume control, path routing and mixing, high/low pass filtering, dynamic range compression, expansion, and loudness. These parameters can be adjusted using the D2 Audio Customization Suite. The audio path includes a tone/EQ/Bass/Treble/Loudness through the D2-4P's control interface.

Audio Enhancement Features

The D2-4P Family devices include the D2 Audio DSP Sound Enhancement Algorithms. Multiple Sound Enhancement Algorithms are integrated within the firmware as part of the standard audio processing signal flow and are supported by the D2 Audio Suite.

D2 Audio sound enhancement algorithm (included in the D2-4P/D2-4 devices)

- 2-channel stereo spatialization
- Bass enhancement
- Content/configuration EQ presets
- Improved vocal clarity
- Automatic room audio setup/ equalization/optimization
- Automatic loudspeaker/setup/equalization/correction

DTS/SRS/DOLBY/WOW/MP3

- Included in the D2-4/D2-4P devices

Each of these enhancements provide a unique algorithms, where choice of enhancement is specifically device part number. The D2-4 devices include the DTS/SRS/DOLBY/WOW/MP3 algorithms, while the D2-4P devices include only DTS/SRS/WOW/MP3 support. These enhancements also have their own unique set of programmable parameters to control operation.

Serial Audio Digital Input

The D2-4P devices include one Serial Audio Interface (SAI) port supporting multi-channel I2S, TDM, and S/PDIF formats. The SAI port operates in slave mode only, supports four Rx/Digital inputs, includes an indirect clock, and can carry up to 24bit Linear PCM audio words.

The digital audio input from the SAI input port routes directly through the Sample Rate Converters (SRC) then to the DSP. Digital input on the S/PDIF Digital input can be selected as the audio path source.

S/PDIF Digital Audio I/O

The D2-4P devices include one IEC60958 compliant S/PDIF Digital receiver input and one IEC60958 compatible S/PDIF Digital transmitter.

The S/PDIF Digital receiver input includes an input transition detector, a PLL clock recovery, and a data recovery to support the digital audio. The receiver meets the jitter tolerance specified in IEC60958-4.

Table 2. Audio Output Configurations

PWM Channel Configuration	Output Configuration	Description
0	2.0 L/R (Speaker)	Powerstage1 and Powerstage2 with 2 speakers (2.5 or 3 ohm)
1	2.0 L/R Line Out	Powerstage1 and Powerstage2 with 2 speakers (2.5 or 3 ohm)
2	2.1 L/R/Sub Line Out	Powerstage1 and Powerstage2 with 2 speakers (2.5 or 3 ohm)
		Subwoofer line-level output
3	2.1 L/R/Sub (Speaker)	Two half bridge drivers for powered left and right speakers
		Powerstage4, full bridge driver for powered subwoofer output
		Two (stereo left + right) line-level outputs
		Crossover filtering included with audio path signal flow
4	2.0 Headphone	Four half bridge drivers for headphone amp left + right channels
		Crossover filtering included with audio path signal flow

The 8-POP Digital Transceiver complies with the consumer specifications defined in IEC60958-3. The transceiver supports 24bit audio data, but does not support user data and channel status.

Compressed digital formats are not decoded with the 8-POP(S)/D2 and D2-4P(S) Transceiver. A bitstream pass through mode is supported from the SPDIFRX1 input to the SPDIFX output. The 8-POP(S)/D2 and D2-4P(S) Transceiver supports IEC61937 compliant compressed audio input bitstream be made available at the product's SPDIF Digital output.

Sample Rate Converter

The D2-4P Sample Rate Converter is a dual-port asynchronous Sample Rate Converter. Each port supports the audio input signal/bus pair. The SRC converts audio data input sampled at one input sample-rate into a fixed 48kHz output sample-rate, which is independent of input audio streams to a single rate for system processing.

Audio data generated from the SDIF-1 bus can be routed to the 8-POP Digital input sources with an input sample rate from 32kHz to 96kHz. The 8-POP Digital output is fixed at 48kHz regardless of the output sample rate. The 8-POP Digital output sample rate is determined by the SRC to further enhance audio quality.

DSP

A 24-bit fixed-point Digital Signal Processor (DSP) controls the capacity of audio processing and system control functions on the chip.

Audio path signal routing, programmable parameter processing blocks, and control logic are defined within the device's firmware. Audio signals from the input pins are routed to the DSP and processed through hardware-specific function blocks such as the Sample Rate Converter, Digital Volume Control, and Mixer, along with the internal DSP firmware, as well as routing for external control of audio processing parameters.

Clock and PLL

Clock generation and ownership are a fundamental/mode crystal connected across the XTAL1and XTAL2 pins. XTAL2 is an output, and XTAL1 is an input. The crystal can be replaced with a clock source only when XTAL1 is an input that connects to the other side of the crystal.

The chip generation contains a few (five PLL to ensure low noise PWM output and a precise master clock source for sample rate converters and other functions. The PLL's include a low noise 12.288 MHz VCO clock operated at 32x the crystal frequency (3.2 x 24.576MHz) and provides complete device and system timing elements. It is used throughout the device, including clock generation for Internal detection, system and power-on reset, DSP, 8-POP Digital transceiver, and PWM engine timing.

Clock and PLL hardware functions are controlled by internal device firmware. They are not programmable and are optimized for device and system operation.

Timers

Two independent timers are used for device and system control. Timer 0 is used for the internal DSP firmware and system operations. The other is used for the PWM engine and system sensing/control algorithm. Two 16 ports (TBD and TBD) are dedicated to timer 0 for general purpose function accessibility to device firmware. Only TBD is actually used in relationship to its PWM. The PWM engine's timer is used for the PWM's Dead-time or Dim/pulse-modulation algorithm. Timer 0 is used for internal functions of the device. Bo pin (TBD) is not used for this timing/operation and is defined by device firmware as the GPIO3 input pin.

Pulse Width Outputs

Audio outputs are provided through four output power stages that are configurable for driving loudspeakers. Three additional PWM outputs are also available for driving low-level audio outputs. Combinations of outputs and their output processing channel assignment are defined by the device's configuration system settings.

Output Power Stages

The devices include four independent output stages (Figure 24) that are each implemented using a highside-to-positive MOSFET and a lowside-to-negative MOSFET. The output stages are each independent and can be installed in each of these four output stages. Depending on the selected configuration mode, these four stages can be used independently as single half-bridge outputs or as pairs for full-bridge outputs.

Audio processing PWM Internal outputs are routed to the inputs of the four output stages, based on the DCFG2 and DCFG3, configuration settings. The PWM output signals are routed from output stage modules. Its can highside and lowside control, sensing that feeds to internal monitor logic and provides the UVP/OVP output protection. Temperature and overcurrent monitoring also provide status and input to device protection control.

FIGURE 24. OUTPUT STAGE

Output Options

The D2-4P devices provide four configuration options for the output channels. Each of the four output channels is configured by assigning the channel to the DAC, PWM, or Pulse Train. These defined configurations include:

- Two channels of full bridge, Bypassed outputs
- Two channels of full bridge, Bypassed outputs
- Four channels of half-bridge outputs
- Two channels of half bridge and one channel of full bridge

Audio processing routing and control supporting the output stage configurations listed above are described in the section titled "UNIVERSAL DIGITAL OUTPUT PROCESS". Audio path definition, audio path output routing, and output stage configurations are automatically set for each of the four available matrixes based on these configuration settings.

PWM Audio Outputs

Three PWM outputs provide audio for up to three bridged outputs. Audio processing and output assignment is required for these PWM outputs based on the device's available configuration options.

Using only a single power bias, the PWM outputs drive bridged-mode power stages. Two PWM outputs are configurable to add, the PWM outputs can also drive headphone outputs or D_{MIC} at higher bias voltages. Alternately, these PWM outputs can be used to drive power-control outputs (using additional power stages, on the system design).

Control and Operation

Control Interfaces Summary

The control interface provides access to the registers used for audio processing blocks and other flash parameters. Audio input selection ("S input or S PDM" reserve input) and all configuration options are controlled by the control interface. Flash parameters include configuration register parameters, and audio parameter is defined with its specific register address. Programming details, register identification, and parameter calculations are provided in the D2-Family, D2-4P Register API Specification document.

I²C-2-Wire Control Interface

The I²C-2-Wire control interface allows communication with an external controller. This interface is usable through either an external microcontroller bus, or the communication to SEPROM, or other compatible flash devices.

The I²C interface supports normal and fast mode operation and is multimaster capable. In D2-4P system application, it operates as an I²C slave device where the system controller operates as the I²C master.

Reading and Writing Control Registers

All reads or writes to registers (shown in Table 2-1 and Table 2-2) are made through the control interface. Reads and writes are made using the Device Address, Register Address, and Data Condition.

Register entries through the I²C interface are initiated by setting the read/write bit that is within the device address byte. The Write sequence shown in Table 2-3 or Table 2-4 is described in Table 2.

TABLE. PROGRAMMING

BYTE	FORMAT	DESCRIPTION
1	Device Address	Device address with W bit set
1	Register Address [23:16]	Upper eight bits of address
1	Register Address [15:8]	Middle eight bits of address
1	Register Address [7:0]	Lower eight bits of address
4	Data[31:24]	Upper eight bits of write data
4	Data[23:16]	Middle eight bits of write data
4	Data[7:0]	Lower eight bits of write data

All reads/writes, shown in Table 2-1 or Table 2-2, require two bytes to initiate the read/write. The first byte is the device address of sending a Write, followed by the device address with the write bit set, and three register address bytes. Next, the master must send a repeated START, send the device address with the read/write bit set to Read, and read the next three data bytes. The master must send a NACK after the last byte read, and send a Not Acknowledge (NACK) on the third data byte read, and send a Stop condition to complete the transaction. The device's control interface acknowledges each byte by pulling SDA low on the third incremental falling clock edge for each byte. The read sequence shown in Table 2-5 is described in Table 2.

TABLE. PROGRAMMING

BYTE	FORMAT	DESCRIPTION
0	Device Address	Device address with Write bit
1	Register Address [23:16]	Upper eight bits of address
1	Register Address [15:8]	Middle eight bits of address
1	Register Address [7:0]	Lower eight bits of address
4	Data[31:24]	Upper eight bits of read data
4	Data[23:16]	Middle eight bits of read data
4	Data[7:0]	Lower eight bits of read data

FIGURE 23. I²C WRITE SEQUENCE OPERATION

FIGURE 24. I²C READ SEQUENCE OPERATION

Control Interface Address Spaces

Registers are accessed through the I^2C control interface using the I^2C channel address of 0x82. This establishes the device as a slave under control through I^2C communication as the D2-4P.

Registers and memory spaces are defined within the D2-4P by the I^2C Control Interface Address Space. The Control Interface Address Space register address (Bits [23:16]) determines the internal address space used for control read or write access. The remaining 16 bits (Bits [15:0]) determine the internal address within that space.

Programmable settings for the audio processing blocks are internally mapped to the address space defined with the highest order bits (all zero. For example, 0x000xxxx, where xxxx is the address bits as defined in the Address Space.

Storing Parameters to EEPROM

The D2-4P provides two parameters to address, one for an EEPROM is installed on the application, the programmable settings can be stored in the EEPROM for boot-up. This source also can then be created upon reset or power-up.

Serial Peripheral Interface (SPI)

The Serial Peripheral Interface (SPI) is an alternate serial input port that provides an interface for loading parameter data from an optional EEPROM or Flash device during boot-up operation.

The four SPI interface pins are all shared functions:

- Following a reset condition and while the device is initializing the boot-up process, these four SPI pins (TEMPREF, SCK, TERR, MISO, VOL1, MISO, VOL0, VAR) function as a SPI input port for external boot loading operation.
- As soon as the boot-up process is completed and the device initialization is completed, these pins are then no longer used for SPI functions and are dedicated to the functions for volume control, error indication, I/O for amplifier operation.
- See the application pin description section for more information about these pin functions.

Reset and Device Initialization

The D2-4P must be reset to initialize and begin proper operation. A system reset is defined by applying a low level to the nRESET input pin. External hardware circuitry or a controller within the amplifier system design provide the reset signal that connect to the nRESET input to initiate the reset process. Device initialization begins after the nRESET pin is released from its low state.

The chip contains power-on sensors and brownout detectors on the 3.3V VCCD and PWRVCCD power supplies and the 1.8V CCD2 power supply. A loss or drop of power from these supplies causes the nRESET input to be asserted. Brownout detection output pin, driving it low. The nRESET pin should connect to the nRESET input through hardware on the amplifier design to ensure a proper reset occurs if the power supply voltage drop below their design specifications.

In the absence of nRESET, the chip mode the status of the boot mode selection pins (PRQA and PRQB) and begins the boot process according to the boot mode selected. The boot mode pins are logic inputs. These three pins are sampled either high or low on the system's design (PCB). The state of these pins that is latched into defines the boot mode operation.

Boot Modes

The D2-4P devices contain embedded firmware to operate the chip. This firmware is stored in internal ROM memory and upon reset, by the programmable settings can be written to the device after it's operational and running. However, parameter data can also be read at boot time, which gives several parameter settings to be used, or allows another function to be set through a system controller. Parameters can be read from a serial EEPROM or from four parallel boot modes, allowing control and data to be provided through these boot sources:

- I²C (slave to external microcontroller)
- I²C EEPROM
- Internal device ROM only
- SPI slave

The specific boot mode is selected based on the state of the GPIO[3:0] pins at power-up. The pin settings for the boot modes and boot functions are shown in Table 4. Setting the "Boot mode" describes the mode of device initialization with respect to the source of parameter settings or program control. Do not confuse Boot Mode with "Output Mode" or audio processing "Configuration Mode" settings that define amplifier-specific functions.

TABLE 4. BOOT SELECTIONS

BOOT MODE	GPIO3 PIN	GPIO2 PIN	GPIO1 PIN	GPIO0 PIN	DESCRIPTION
1	0	0	0	0	Operates as an I²C slave boot, or operates in a standalone mode using the I²C master pins for the boot source
2	0	0	0	1	Reserved. Device reverts to Mode 1 boot from internal ROM and EEPROM
3	0	0	1	0	Reserved
4	0	0	1	1	SPI Slave	SPI slave. An external MCU can write to the boot ram

The device initializes as defined by its boot mode, but gets its configuration and parameter data from the boot device. This boot device is typically a serial EEPROM connected to the I²C port of the system, also, both an external controller and an EEPROM, the EEPROM loads first. During this time, the controller must remain off-bus I²C bus until after the reading sequence from the EEPROM is complete.

Power Supply Requirements

The device requires operating power for these voltages:

- PVDD[1:0] and PGND
  - 3.3V DC supply voltage
  - PWM output driver stage and I/O logic
- PWRVDD is the same voltage and is used for the PWM outputs and output stage drive
- CVDD and PLLVDD
  - 1.8V DC supply voltage
  - CVDD operates the internal processor and DSP core
  - PLLVDD also operates at the internal processor voltage levels, but is provided through a separate connection to minimize noise coupling from the core and digital circuitry
- "High Voltage" (HVDD[3:0], and VDDHV)
  - Operates at 3.3V DC. HVDD[3:0] provides the "High Voltage" supplies used for operating each of the four output power stages.
  - VDDHV is used as the source for the on-chip +9V regulator that is used for output stage drivers.
  - Individual power HVDD[3:0] and their corresponding power ground connections are provided for each of the four power stage outputs, providing maximum isolation and low impedance source connections to each of the outputs. All the HVDD[3:0]/VDDHV pins are connected to the same voltage source

Single-Ended Gate Drive Voltage

An on-chip boostrap circuit provides the gate drive voltage used for each output stage. A pin is included for each output stage (HVBS[3:0]) for connection of a capacitor (nominal, 22uF) 50V ceramic pin to that output's PWM output.

Driver's for higher-side FETs on the output stages require a voltage higher than the 3.3V supply voltage. The HVBS[3:0] pins provide a charge pump of the driving HVBS to drive pin-outs, the "bootstrap" voltage, and uses this capacitor to filter and hold this charge for a little longer. Allows amplifier operation without needing a converter to an additional power supply voltage.

Power Supply Sequencing

The the PWRVDD, CVDD pin provides a power supply sequencer/monitor signal for switching power supplies. If firmware configures this pin to the frequency and duty cycle needed by the switching power supply, the sequencer/monitor signal can enable supplies used with the device to operate without generating in-band audio interference signals. But could use or if the switching power supply is not bonded to the amplifier switching.

This PWRVDD CVDD pin is a shared pin, (see the multi-purpose pin-out section in Table 3 on page 10). Depending on the pin-out and initialization, the pin operates as one of two configuration input/output pins. Upon reset, the pin is a GPIO input, and the boot mode configuration reads. After completing reset and before the device firmware begins operating, this pin becomes the PWRVDD output.

Power Sequence Requirements

Voltage sensors and brownout detectors monitor supply voltages to ensure the chip is in a valid operating condition. The monitoring prevents disconnect of supply voltages from other than specified limits. However, during application of power, the CVDD and DVDD (including DVDDIO) voltages should be brought up together to avoid high current transients that could fall back power-supply regulator.

During application of power to the system and while the CVDD and DVDD voltages are ramping, the voltage difference between the VDD and VDDIO supplies (nominal +3.3V) must not exceed the voltage that is present at CVDD. If $V_{CVDD} < 1.0$V when the VDD-VDDIO difference is nominal 3V, V_{CVDD} differ CVDD exceeds its minimum limit.

Similarly, during application of power, the difference to remain within the specified limits must be brought up separately.

The best practice is for all supplies to freed from regulation using a common power source. Simplicity this can be achieved by using a single-low voltage supply power source and regulating the 3.3V and 1.8V supplies from the single source. Alternatively, Semiconductor recommends all voltages of the same sources must be kept together in order.

REGSV

The output stage internal drivers require their own +5VDC supply voltage. An on-chip regulator operates from the 5VDDIO voltage to generate the REGSV voltage. The REGSV voltage is used to operate converters. The regulated voltage of 5.0V and 0.3µF capacitor must be connected to this pin, and the connection should be made as close as possible to the. This internal +5V is used only by the output stage drivers. Do not isolate other analog circuits this pin.

Pin and Control Block Functions

I/O Control Pins

Several dozen pins are used as specific function inputs and outputs to control amplifier and detector operation. These pins are powered by the 5VDDIO supply and are compatible with 5V logic levels. Reserved. Reserved pins are not pin-compatible and their specific function is totally defined by the 02-2P-Reserved Pin Mapping. Reserved pins are not pin-compatible and their specific function is totally defined by the 02-2P-Reserved Pin Mapping. Descriptions of the functional blocks where these pins are used follow pins, sub-multiple groups, and their functions are defined accordingly by the operational state (for example, resetting, initializing, running) operating of the 02-2P. These multiple-purpose pins and their descriptions and uses are described in more detail in Table 8 on page 22.

nPDN Input Pin

This nPDN pin is a control input that is used to powerdown the outputs. When this input is pulled low, all audio outputs turn off and the internal oscillator and PLL are stopped. Internal logic stages is turned off, and all output stages float. Internal logic and other references remain active during this power-down state. Asserting nPDN also causes all four nRERROR(X) outputs to pull active. Each of the four output stages incorporates its own latching overcurrent detection circuitry. This circuitry is addition to the separate protection events that cause through firmware control from an overcurrent condition. Remaining in power-down mode allows other status to clear this hardware latched shutdown, although issuing nPDN resets the hardware latch immediately.

The nPDN pin is active low and is inactive when at logic high. In normal operation, it is held high with pullup to the 5VDD supply.

nERROR(0-3) Output Pins

Each of the four output stages includes a two-level overload and overcurrent monitor. An overcurrent or overload condition asserts the nERROR output for that channel.

An undervoltage condition for the voltages sent by the output stage also asserts the nERROR output. Any fault condition on any channel causes the nERROR outputs to assert.

The nERROR pins are open drain, active-low, and can be wire-or connected together. Strapping pins provide a configuration where more than one output stage can be used for the audio channel. nERROR pin configuration with multi-channel are connected together to provide the monitoring status. Alternative configurations with multi-channel, can be defined for an audio channel, the nERROR pins for that a power stage. Refer to the Pin Mapping for the 02-2P-Reserved Pin Mapping for information on the pin assignments. See Table 8 on page 22 for the connections for the different configuration modes.

nREF Pin

This pin sets the overcurrent and overload monitoring threshold. The design requires a 200kΩ resistor to connect from this pin to ground.

Configuration Assignment Pin Differences

The pins of pins are used for configuration assignment. Multi-pin pins are used for the assignment, and their settings must be set to the appropriate requirements for the configuration mode. Two pin pairs are:

- CFG0, CFG1: Defines the output stage topology and operation of the output configuration.
- nERROR/CFG2, PRSTCFG: CFG2: Defines the audio processing and amplifier control supporting the output configuration.

CFG0, CFG1 Input Pins

These two pins define the configuration of the four output stages, and the pins are sampled at the rising edge of nPDN. The pins are CFG0 (pin 6) and CFG1 (pin 7) PWRDNS to establish which of the four output configurations is used in the design. See Pin Descriptions, starting on page 5, for additional information.

nERROR/CF00 and PSENC/CF01 Pins

These pins define the amplifier configuration mode that the firmware uses to initialize the amplifier. Both nERROR/CF00 and SCFG pins, that at operation of the output stages, the nERROR/CF00 and PSENC/CF01 pins, also establish audio signal processing path assignments and up monitoring and protection for the configuration mode. The configuration pin logic levels are defined by pull-up or pull-down resistors installed on that application.

The configuration defined by these pins is assigned when the CS8416CF00 ASSIGN bit, is reset state. At that time, the high states of the PSENC/CF01 and nERROR/CF00 pins are latched into internal shadow registers. These an shared function pins, and after firmware begins executing, their functions are redefined as PSENC and nERROR. See Section 3.2 for more information about these pins and their alternate functions.

Temperature Monitoring

The TEMPREF_SCA, TEMPC_REDC, and TEMPCREDC TEO pins are used to monitor temperature for the firmware thermal protection. These pins share other functions, see the multiple-purpose pin descriptions in Table 5 on page 25. During firmware execution, they operate as inputs and outputs for the measurement algorithm. Figure 21 shows the circuit for this temperature measurement implementation.

FIGURE 17. TEMPERATURE MONITOR CIRCUIT

A Negative Temperature Coefficient (NTC) 100kΩ resistor connects to the TEMPC_REDC pin, and using the resistor's temperature/resistance correlation, the firmware monitors temperature of the NTC resistor. The internal device trimg functions associated with the TEO pin provide calibration that allows the firmware to use the 100kΩ resistor connects to the TEMPREF_SCK pin as the a standard non-temperature-dependent reference for this algorithm.

The firmware algorithm is internal to the DSP. The status from this temperature monitor is used for the temperature protection functions of the device and its application. There are no adjustments or parameters for changing settings.

TABLE 6. DEL-PIN-FUNCTIONS ON CONTROL-PIN-ASSIGNMENT-AND-OPTIONS

PIN DEL-PIN-FUNCTIONS		FOR DEVICE SIGNAL-DISTRIBUTION		FOR DEVICE SIGNAL-DISPATCHER	
PIN NAME	**I/O**	**FUNCTIONS**	**I/O**	**FUNCTIONS**	**COMMENTS/REMARKS**
TEMP-C/ SDO	Input or Output	SPI-clock output	Input	Temperature monitor or temperature-sensor-connection input, or reserved for manufacturing-use	Typical connection is to 4K-bit EEPROM or temperature-sensor-connection input. Also, SPI-clock output if SPI is used in this application.
CCLK/ MISO	Input or Output	SPI-master input or slave output. Function (master or slave) is determined by the nSS input pin.	Input	Volume control Phase-B input. Used to monitor volume-control-knob rotation.	Typical connection is to 10-bit DAC or pull-up resistors and to a 2-bit volume control encoder. Also, SPI-master input if SPI is used in this application.
TEMP-L/ MOSI	Input or Output	SPI-master output or slave input. Function (master or slave) is determined by the nSS input pin.	I/O	Temperature monitor or temperature-sensor-connection I/O, or reserved for manufacturing-use	Typical connection is to a 4K-bit EEPROM or temperature-sensor-connection. Also, SPI-slave-input if SPI is used in this application.
nSPDIF/ CPO	Output	CPO-S1 Configuration Mode Input Select. Using pull-up or pull-down resistor, this input can be defined as one of four amplifier-configurations.	Output	Active-low output amplifier protection and monitoring status indication.	Connects to 10-bit or to ground with a 20kΩ resistor to select high-left or low-left setting for the output-pin-pair. Also, connects to the mute or indicator circuit to provide status (either 'PRESENT' or some or between design-1).
PSDIN-L/ CPO1	Input	CPO-L1 Configuration Mode Input Select. Using pull-up or pull-down resistor, this input can be defined as one of 4 amplifier-configurations.	Output	Sync Output for Synchronizing the Serial Power Supply analog-PWM.	Connects to 10-bit or to ground with a 20kΩ resistor to select high-left or low-left setting for the output-pin-pair. Also, connects to the sync-input of the on-board switching-power-supply. 'PRESENT' or some between design-1.
CCLK/ nSS	Input	SPI-Slave Select.	Input	Volume Control Phase-A input. Used to monitor volume-control-knob rotation.	Typical connection is to 10-bit DAC or pull-up resistors and to a 2-bit volume control encoder.

Configuration Setting

The configuration mode is assigned through two pairs of pin settings. When the D2-4P ends its reset state, the logic states of the PWRTRIG pin and the nCONFIG pin are latched into internal sense registers. During this initialization time, these two pins are treated as inputs with internal pull-up resistors and the internal Schmitt-trigger input buffers enabled. These pins are re-assigned as outputs for their shared functions, and the internal isolated-logic state that defines the pin-function-sense-resistor and the device is powered-down or reset again. The DCRDO and nCONFIG pins are latched. Once a pin-mode reverts to their pull-up or pull-down state.

Selection of one of the four configuration-modes is defined by stopping the configuration pins high or low:

- DCRDO and DCFUSE define the output power-stage configuration
- nERROR (CFG) and PWRTRIG (CFG) define the amplifier and internal configuration

These four pins are connected to either a high level (+3.3V) or low level (ground). Pull-resistors should be through 2.2kΩ resistor and not directly to the supply or ground.

See Bias-power-pin-table, the code-pin-assigned channel assignment, sub-control, and output-assignments for each of the four configuration-modes.

Both pairs of configuration-setting pins (DCRDO, DCFUSE) and (nERROR, PWRTRIG) can be shared for used and both must be set to the same configuration-mode.

In modes 2 and 3, the filtering for high and low pass processors is applied to the audio-signal flow path, enabling the appropriate high or low pass content to be properly filtered for the PWM output channels.

TABLE. SUPPORTED PROTECTION AND CHANNEL ASSIGNMENTS

| Mode | Output Configuration | Output Type | Protection Mode | Protection Type | Protection Type | Protection Type

Protection

The 02-4P devices include multiple protection mechanisms. Output overload and overcurrent states for each output stage provide two levels of monitoring. Temperature monitoring provides two levels of warning and a shutdown. Overvoltage detection is included for all supply pins.

The 02-4P devices use several strategies to prevent damage from high voltages, currents, and temperatures present in class-D amplifiers. This protection is also effective against user-induced faults such as shorting output terminals or output shorts, including both short-to-ground outputs or short-to-ground faults. Protection includes faults such as:

- Output overcurrent
- Output short-circuit
- Over-temperature
- Power-supply brown out
- Short-through overcurrent

Certain levels of protection are managed using on-chip hardware. Other protection is integrated into device firmware, and involves actions to:

- Shut down the outputs for a short-circuit, over-temperature, or undervoltage event.
- Shut down the device if power-supply sensors detect voltages dropping below their trip thresholds.
- Provide initialization and device lockdown (if needed) for power-on reset, brown-out, and overvoltage conditions, and restart automatically when conditions are in high-current conditions.
- Chip temperature monitoring provides dual thresholds status of high temperature conditions, providing both indication and device shutdown if needed.

Error Reporting

The system and internal internal monitoring uses an I²C pin (MERROR/CPE2), as an output to signal a channel shutdown event or a critical power-supply or temperature condition. This output can be used to turn on a simple indicator.

The error output is also used to signal an external microcontroller that the I²C bus is busy. When the error output is low during system initialization, the I²C bus is busy as a master device.

This error output is latched in one and only two events and an error reporting output after the device firmware initialization, and begins running. The error pin is shared as an input line (see Table 4) and output, for more information about shared function pins.

The error output is a single-ended output, and the pull-up resistor of the error input pins used to define the configuration mode. A resistor pull-up or pulldown on this pin establishes the mode input configuration. After completing the initialization sequence, these resistors do not affect the error output operation.

Short-Circuit and Overcurrent Sensing

Each PWM output INT includes a dual threshold overcurrent sensing. The output stage provides two separate levels of overcurrent protection:

- The lower threshold monitors fault conditions such as shorts and overloads at the loudspeaker output.
- The higher threshold monitors fault conditions of the PWM output pin
- The ±80MOR output asserts for the channel detecting the fault
- For the lower level threshold, ±80MOR remains asserted as through the duration of the overcurrent event
- For the higher threshold event, the output is latch down and the ±80MOR output is asserted. These conditions remain latched until the controller acknowledges the error condition by turning off the channel's PWM drive (for PWM pin fault, when shut down)

The intent is both into the second threshold detection to suppress PWM switching transient events.

Protection Monitoring and Control

The overcurrent detection generates either a pulse or latched high signal depending on the mode, and the output stage provides dual of high current. The detector status is presented to the PROTECTION 2 pin.

The PROTECTION2 pins are used as protection inputs to the output stage. The output stage uses the PROTECTION2 inputs to the selected output stage to shut down the output. For the output pins and the PROTECT2 input pins are connected together on the output and output mode configuration shown in Table 4 on page 20.

Thermal Protection and Monitors

Temperature sensing provides two thresholds of temperature monitoring.

If the device reaches the lower threshold, a warning indication is provided and some level of thermal protection (gain compensation) is triggered.

Only hardware thermal protection shuts down the device upon a high-threshold temperature condition. If the device reaches the lower threshold, the device firmware reads the status and reports the condition to the error output. The error output is active low (active), providing this dual-level status to the firmware through the connected PROTECTION 2 inputs.

Graceful Overcurrent and Short-Circuit

Hard faults from overcurrent or short-circuit conditions shutdown the output stage and provide a latched error condition and shutdown. For lower-threshold event detections, graceful protection is provided for each output. Specific operation depends on the output and mode. For a lower-level event, but action takes it to reduce conditions that contribute to the event, the output stage of a complete shutdown is not required.

Overcurrent monitoring status is presented to the PROTECT2 inputs from peripheral shutdown status that drives the

WARNING: Overload, Overcurrent detection algorithms in firmware monitor these peak level detections, and upon detection of an overload condition, automatically reduce PWM gain. The Automatic Gain Control (AGC) action helps prevent audio output clipping and helps avoid related excessive heat conditions. Overcurrent detection also helps avoid excessive heat conditions and PWM pulse-reduction corresponding to Overloads and low-most detection of overloads. At the lower (non-clipped) high-frequency threshold, the AGC function also acts to attenuate the outputs to attempt to reduce temperature.

Output level gain and thermal algorithm effects from the AGC function are similar to operation from a compressor. However, unlike a compressor, the AGC function does not attenuate low-level signals, but PWM AGC operation is controlled through detection of near-overload output levels, or from high temperature detections.

Power Supply Voltage Monitoring

Undervoltage sensors and brownout detectors monitor all supply voltages to the device. This logic and buffer protection of this voltage monitoring prevents operation until all supply voltages are within their specifications. If any of these monitored voltages drop below their threshold, the device shuts down its outputs and asserts Reset, or the nMUTE outputs.

Audio Processing

The audio processing, signal flow, and system definition is defined by the D2-4F-Universal ROM firmware and is executed by the DSP. This firmware defines the audio flow architecture, including the audio processing blocks. Each block is parameterized, and the firmware provides parameter processors. The signal flow and audio processing blocks are shown in Figure 26. This architecture includes audio processing functions for:

- Input selection
- Mixers
- Input compressors and output limiters
- Tone controls
- 3-band and 5-band parametric equalizers
- Router
- High/low pass crossover filters
- Volume and output level controls
- Loudness contour

Enhancement Audio Processing

The D2-4EXMT supports the D2 Audio DSP Sound Enhancement Algorithm. The D2-4EXMT supports the DTS®/SRS/ WOW HD™ algorithm.

Audio Processing Signal Flow Blocks

INPUT SELECTION

The input Select register specifies the audio inputs that are assigned to the audio processing input path. Either the I^2S or S/PDIF digital inputs are available.

MIXERS

An input mixer provides a two-input, two-output mixing and routing path. Either input can be mixed at adjustable gain into either or both of the two outputs. The default setting is 0dB through each channel, with full cut-off for non-through channels. Attenuation is continuously variable with the programmable parameters.

Actives mixer provides a path from the two input channels. Stereo mixers are typically used to provide a mix of both stereo input channels for crossover processing and become the source for the subwoofer channel. Gains for both input channels are adjustable in fixed five-single stereo mixer output.

TONE CONTROLS

Both input channels contain a tone control block. Each of the tone blocks has a bass and treble control. Bass control shelf-filtered cut-off, using programmable corner frequency and a boost or attenuating gain. The signal flow processing automatically provides a smooth transition between tone control changes.

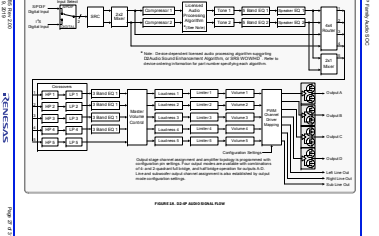


FIGURE 18. 32-BIT AUDIO SIGNAL FLOW

COMPRESSORS AND LIMITERS

Two individual input compressors can be included in the input audio path. Each can be set to Compressor or Limiter operation. Four outputs are also included in the output path channels. The Compressor and Limiter blocks operate identically, and their parameters are identical except for default parameter settings. Typically, the input path limiters are programmed to provide a compression function and the output path blocks are programmed to limit output signal levels. However, each path can be programmed as needed. Each Compressor/Limiter has independently adjustable Attack, Threshold, Knee and Release Time, as well as Makeup Gain.

MULTI-BAND EQUALIZERS

Three sets of Multi-Band Parametric Equalizers are included in the audio signal processing path. Each have all three equalizers programmable with gain, frequency, and Q factor adjustments.

A Bass Enhancer and a Speaker Equalizer (EQ) are included in both of the two input channels. Four 3-Band Equalizers are also included in the output channels.

STEREO ROUTES

A 6-Channel mixer assigns any one of the four input channel paths to each of the four output paths. The router performs path assignment only. It does not provide gain or signal level adjustment.

HIGH/ LOW-PASS CROSSOVER FILTERS

High-Pass and Low-Pass filter blocks are provided for each of the four output channels downstream of the Route and Stereo Mixer. These filter blocks provide a flexible Crossover function for the output channels. Each filter block implements the selected channel's frequency response.

The High and Low Pass blocks operate together and are implemented as a total of four cascaded biquads. Four of each of the elements are allocated for High-Pass functionality and the other four elements are allocated for Low-Pass functionality. Complete flexibility allows each element to be optionally defined as a 1st-order, 2nd-order, 3rd-order, or 4th-order filter with a choice of Butt, LR24, LR36, or 24dB, or can be bypassed. Butterworth, Bessel, or Linkwitz-Riley filter implementations are available.

MASTER VOLUME CONTROL

Use the software-controlled Master Volume control to adjust the global volume for all four output channels. Master Volume operates simultaneously adjustable attenuation, from unity gain down to -120dB and cutoff.

Each of the four output channels has its own dedicated output level adjustments that provides individual channel gain or attenuation. Each channel's output level range provides output level adjustment from +12dB to -120dB.

LOUDNESS CONTOUR

An individual software-controlled Loudness Contour is included in the output path of each output channel. The Loudness Contour curve is automatically adjusted for psychoacoustically and automatically enhancing the frequency response of the audio signal according to the volume level. The Loudness Contour uses the Loudness Contour module that implements the equal-loudness as defined by the Fletcher/Munson audio response curve. It provides amplitude or volume changes in signals to which the ear does not respond equally at very low listening levels.

SIGNAL ENHANCEMENT ALGORITHM PROCESSING

The D2 Audio DSP Sound Enhancement Algorithm suite provides a full set of enhancements to audio that greatly add to the quality and listening experience of sound in consumer products. The D2 Audio DSP Sound Enhancement Algorithm suite also provides sound processing enhancements creates a noticeably enhanced sound from small speakers and synthesizes the sound and quality equivalent to more complex systems. It is especially suited for consumer products that include televisions, desktop stereos, and mini-hi-fi stereo products.

Sound enhancement algorithm processing includes:

- 2-channel stereo spatialization
- Bass enhancement
- Custom/ configurable EQ presets
- Improved vocal clarity
- Automatic room audio setup/ equalization/ optimization
- Automatic loudspeaker setup/ equalization/ optimization

The D2 Audio DSP Sound Enhancement Algorithm is completely included within the D2-4F Family devices.

Revision History

The revision history provided is for informational purposes only, and is believed to be accurate, but not warranted. Contact our website to make sure you have the latest datasheet revision.

Date	Revision	Details
Mar.19, 2020	FN6785.2	Changed datasheet base part number to "D2-4iP" Family Audio SOC. Changed the following terms throughout the datasheet: "DSAudio" to "3D Audio DSP" "DSP" to "3D Audio DSP" "SSP-DP" to "3D-Processor" "Digital Audio Engine" to "Digital Audio Processor" "Advanced Audio Processing Unit Advancement Algorithm" Updated Related Literature. Updated audio sub-accessories features on page 25. Updated Figure 10 on page 14, Figure 13 on page 16, and Figure 18 on page 21. Removed General Information. Updated disclaimer.
May.8, 2020	FN6785.3	Updated section statement applying Intersil's new standards. Updated the Ordering Information table on page 2. Updated the package to Green/Intersil verbiage. Added DTS disclaimer.
Jul.29, 2020	FN6785.0	Initial Release

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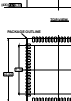
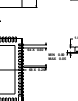
Package Outline Drawing

For the most recent package outline drawing, see L68.10x10C.

L68.10x10C

68 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 0, 06/09





NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension is applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The marking area of the pin #1 identifier is optional, but must be located within the zone indicated. The pin#1 identifier may be either a mold or mark feature.

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