D2-4P Family Audio SOC

Intelligent Digital Amplifier PWM Controller and Audio Processor

FN6785
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The D2-4P (D2-45057 and D2-45157) devices are complete System-on-Chip (SoC) Class-D digital audio amplifiers. These devices combine high performance integrated Power Stages, an optimized Audio Processor feature set, and a PWM controller to offer a complete, powerful, and very cost effective audio solution for high volume and cost-critical products.

This 4th generation Digital Audio Processor (D2-4P) device combines extensive integrated Digital Signal Processor (DSP) audio processing with amplifier control for a complete audio solution. Its ease of integration into the existing system processor provides complete support for all system product and amplifier functions.

The four configurable Power Stages operate as four separate Half-Bridge outputs, as two Full-Bridge outputs, or in combinations of Half-Bridge plus Full-Bridge, which provides flexible loudspeaker drive solutions. Separate PWM outputs provide additional combinations to drive headphone outputs or line level stereo and subwoofer outputs.

Related Literature

For a full list of related documents, visit our website:

- D2-45057 and D2-45157 device pages

Features

- All digital Class-D amplifier and controller with integrated Digital Signal Processing (DSP)
- Four integrated Power Stages supporting:
  - 2 Channels, Bridged
  - 4 Channels, Half-Bridge
  - 2 Channels, Half-Bridge, plus 1 Channel, Bridged
- Output power (bridged)
  - 25W (8Ω, <1% THD); 30W (8Ω, <10% THD)
- Fully programmable Digital Signal Processing (DSP)
  - Up to 5 programmable audio signal path channels
  - Programmable equalizers, filters, mixers, and limiters
- Includes D2 Audio DSP Sound Enhancement Algorithm and DTS®(SRS) WOW/HD™ Audio Enhancement Algorithms
- I^2S and S/PDIF™ digital audio inputs
- Asynchronous sample rate converters; sample rates from 32kHz up to 192kHz
- Wide 9V to 26V Power Stage HV supply range, plus internally-generated gate drive supply
- Temperature and undervoltage monitoring and individual channel protection

Applications

- PC/multimedia speakers
- Digital TV audio systems
- Portable device docking stations
- Powered speaker systems

Typical System Implementation

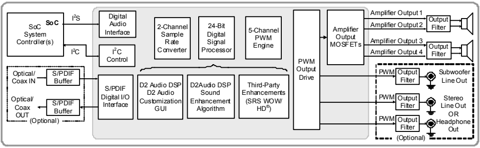

FIGURE 1. SYSTEM APPLICATION IMPLEMENTING 2X FULL-BRIDGE LOUDSPEAKER OUTPUTS PLUS 3 LINE-LEVEL OUTPUTS

Ordering Information

PART NUMBER (Notes 3, 4)	PART MARKING	AUDIO PROCESSING FEATURE SET SUPPORT (Note 1)	TEMP. RANGE (°C)	TAPE AND REEL (UNITS) (Note 2)	PACKAGE (RoHS Compliant)	PKG. DWG. #
D2-45057-QR	D2-45057-QR	D2 Audio DSP Sound Enhancement Algorithm	-10 to +85	-	68 Ld QFN	L68.10x10C
D2-45057-QR-T	D2-45057-QR	D2 Audio DSP Sound Enhancement Algorithm	-10 to +85	3k	68 Ld QFN	L68.10x10C
D2-45157-QR	D2-45157-QR	D2 Audio DSP Sound Enhancement Algorithm DTS®(SRS) WOW/HD™	-10 to +85	-	68 Ld QFN	L68.10x10C
D2-45157-QR-T	D2-45157-QR	D2 Audio DSP Sound Enhancement Algorithm DTS®(SRS) WOW/HD™	-10 to +85	3k	68 Ld QFN	L68.10x10C

NOTES:

1. The D2-4P devices support audio processing algorithms for the D2 Audio DSP Sound Enhancement Algorithm and DTS®(SRS) WOW/HD™ audio enhancement features. Algorithm support for these enhancements is device-dependent. See the device part number for feature support.
2. See TB347 for details about reel specifications.
3. These Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. The Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. For Moisture Sensitivity Level (MSL), see the D2-45057 and D2-45157 device pages. For more information about MSL, see TB363.

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Absolute Maximum Ratings (Note 7)

Supply Voltage	
HVDD[A:D], VDDHV	-0.3V to +28.0V
RVDD, PWMVDD	-0.3V to 4.0V
CVDD, PLLVDD	-0.3V to 2.4V
Input Voltage	
Any Input but XTALI	-0.3V to RVDD +0.3V
XTALI	-0.3V to PLLVDD +0.3V
Input Current, Any Pin but Supplies	±10mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
68 Ld QFN Package (Notes 5, 6)	25	1

Maximum Storage Temperature	-55°C to +150°C
Pb-Free Reflow Profile	see TB493

Recommended Operating Conditions

Temperature Range	-10°C to +85°C
High Voltage Supply Voltage,	
HVDD[A:D], VDDHV	9.0V to 26.5V
Digital I/O Supply Voltage, PWMVDD	3.3V
Core Supply Voltage, CVDD	1.8V
Analog Supply Voltage, PLLVDD	1.8V
Minimum Load Impedance (HVDD[A:D] ≤24.0V), Z_L	4Ω

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

NOTES:

5. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with "direct attach" features. See TB379.
6. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
7. Absolute Maximum parameters are not tested in production.

Electrical Specifications

T_A = +25°C, HVDD[A:D]/VDDHV = 24V, CVDD = PLLVDD = 1.8V ±5%, RVDD = PWMVDD = 3.3V±10%. All grounds at 0.0V. All voltages referenced to ground. PLL at 294.912MHz, OSC at 24.576MHz, core running at 147.456MHz with typical audio data traffic.

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Digital Input High Logic Level (Note 8)		V_{IH}	2	-	-	V
Digital Input Low Logic Level (Note 8)		V_{IL}	-	-	0.8	V
High Level Output Drive Voltage (I_{OUT} at -Pin Drive Strength Current)		V_{OH}	RVDD - 0.4	-	-	V
Low Level Output Drive Voltage (I_{OUT} at +Pin Drive Strength Current)		V_{OL}	-	-	0.4	V
High Level Input Drive Voltage XTALI Pin		V_{IHX}	0.7	-	PLLVDD	V
Low Level Input Drive Voltage XTALI Pin		V_{ILX}	-	-	0.3	V
Input Leakage Current (Note 9)		I_{IN}	-	-	±10	µA
Input Capacitance		Cin	-	9	-	pF
Output Capacitance	All Outputs Except OUT[A:D]	C_{OUT}	-	9	-	pF
	OUT[A:D]		-	190	-	pF
nRESET Pulse-Width		t_{RST}	-	10	-	ns
Internal Pull-Up Resistance to PWMVDD (for nERROR0-3, OCFG, nPDN)		-	-	100	-	kΩ
Digital I/O Supply Pin Voltage, Current		RVDD and PWMVDD	3	3.3	3.6	V
	Active Current		-	10	-	mA
	Power-Down Current		-	0.01	-	mA
Core Supply Pins		CVDD	1.7	1.8	1.9	V
	Active Current		-	300	-	mA
	Power-Down Current (Note 10)		-	6	-	mA

Electrical Specifications

T_A = +25° C, HVDD[A:D]/VDDHV = 24V, CVDD = PLLVDD = 1.8V ±5%, RVDD = PWMVDD = 3.3V±10%. All grounds at 0.0V. All voltages referenced to ground. PLL at 294.912MHz, OSC at 24.576MHz, core running at 147.456MHz with typical audio data traffic. **(Continued)**

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Analog Supply Pins (PLL)		PLLVDD	1.7	1.8	1.9	V
	Active Current		-	10	-	mA
	Power-Down Current (Note 10)		-	5	-	mA
CRYSTAL OSCILLATOR						
Crystal Frequency (Fundamental Mode Crystal)		Xo	20	24.576	25	MHz
Duty Cycle		Dt	40	-	60	%
Start-Up Time (Start-Up Time is Oscillator Enabled (with Valid Supply) to Stable Oscillation)		t_{START}	-	5	20	ms
PLL						
VCO Frequency		F_{VCO}	240	294.912	300	MHz
PLL Lock Time from any Input Change			-	3	-	ms
1.8V POWER-ON RESET						
Reset Enabled Voltage Level		V_{EN}	0.95	1.1	1.3	V
POR Minimum Output Pulse Width		t_{DIS}	-	5	-	µs
1.8V BROWNOUT DETECTION						
Detect Level			1.4	1.5	1.7	V
Pulse-Width Rejection		t_{BOD1}	-	100	-	ns
Minimum Output Pulse-Width		t_{O1}	-	20	-	ns
3.3V (PWMVDD) BROWNOUT DETECTION						
Detect Level			2.5	2.7	2.9	V
Pulse-Width Rejection		t_{BOD3}	-	100	-	ns
Minimum Output Pulse-Width		t_{O3}	-	20	-	ns
GATE DRIVE INTERNAL +5V BROWNOUT DETECTION						
Gate Drive Supply Undervoltage Threshold			-	4.5	-	V
Gate Drive Supply Undervoltage Threshold Hysteresis			-	200	-	mV
Gate Drive Supply Undervoltage Threshold Glitch Rejection			-	50	-	ns
PROTECTION DETECT						
High Voltage (+VDDHV) Undervoltage Protection			-	7	9	V
Overcurrent Trip Threshold			-	4	-	A
Overcurrent De-Glitch			-	2.5	-	ns
Short-Circuit Current Limit (Peak)			-	8	-	A
Overcurrent Response Time			-	20	-	ns
Thermal Shutdown (Power Stages)			-	140	-	°C
Thermal Shutdown Hysteresis (Power Stages)			-	30	-	°C

NOTES:

8. All input pins except XTALI.
9. Input leakage applies to all pins except XTALO.
10. Power-down is with device in reset and clocks stopped.

Performance Specifications

T_A = +25° C, HVDD[A:D]/VDDHV = 24V, CVDD = PLLVDD = 1.8V ±5%, RVDD = PWMVDD = 3.3V ±10%. All grounds at 0.0V. All voltages referenced to ground. PLL at 294.912MHz, OSC at 24.576MHz, core running at 147.456MHz with typical audio data traffic.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
$r_{DS(ON)}$ (Maximum, MOSFETs at +25° C)	$r_{DS(ON)}$	-	200	-	mΩ
$r_{DS(ON)}$ Mismatch		-	1	-	%
PWM Switching Rate		-	384	-	kHz
nPDN Input Off Delay	t_{PDNOFF}	-	1.4	-	ms
nPDN Input On Delay	t_{PDNON}	-	1.4	-	ms
POWER OUTPUT					
<1% THD, Bridged, Load = 8Ω, HVDD[A:D] = 24V	P_{OUT}	-	25	-	W
<10% THD, Bridged, Load = 8Ω, HVDD[A:D] = 24V	P_{OUT}	-	30	-	W
<1% THD, Half-Bridge, Load = 8Ω, HVDD[A:D] = 24V	P_{OUT}	-	7	-	W
<10% THD, Half-Bridge, Load = 8Ω, HVDD[A:D] = 24V	P_{OUT}	-	9	-	W
THD+N					
Load = 8Ω, Power = 25W, Bridged, 1kHz	THD+N	-	0.3	-	%
Load = 8Ω, Power = 1W, Bridged, 1kHz		-	0.05	-	%
SNR	SNR	-	110	-	dB
Efficiency (Power Stage, Load = 8Ω)		-	90	-	%

Serial Audio Interface Port Timing

T_A = +25° C, HVDD[A:D]/VDDHV = 24V, CVDD = PLLVDD = 1.8V ±5%, RVDD = PWMVDD = 3.3V ±10%. All grounds at 0.0V. All voltages referenced to ground. PLL at 294.912MHz, OSC at 24.576MHz, core running at 147.456MHz with typical audio data traffic.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_cSCLK	SCLK Frequency - (SCLK)	-	-	12.5	MHz
t_wSCLK	SCLK Pulse-Width (high and low) - (SCLK)	40	-	-	ns
t_sLRCLK	LRCKR Setup to SCLK Rising - (LRCK)	20	-	-	ns
t_hLRCLK	LRCKR Hold from SCLK Rising - (LRCK)	20	-	-	ns
t_sSDI	SDIN Setup to SCLK Rising - (SDIN)	20	-	-	ns
t_hSDI	SDIN Hold from SCLK Rising - (SDIN)	20	-	-	ns

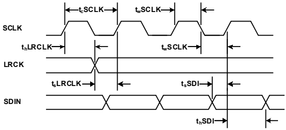


FIGURE 2. SERIAL AUDIO INTERFACE PORT TIMING

Two-Wire (I^{2}C) Interface Port Timing

T_A = +25° C, CVDD = PLLVDD = 1.8V ±5%, RVDD = PWMVDD = 3.3V ±10%. All grounds at 0.0V. All voltages referenced to ground.

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
f_{SCL}	SCL Frequency	-	100	kHz
t_{buf}	Bus Free Time Between Transmissions	4.7	-	µs
t_{wlow}SCLx	SCL Clock Low	4.7	-	µs
t_{whigh}SCLx	SCL Clock High	4.0	-	µs
t_sSTA	Setup Time For a (Repeated) Start	4.7	-	µs
t_hSTA	Start Condition Hold Time	4.0	-	µs
t_hSDAx	SDA Hold From SCL Falling (Note 11)	1 (typical)		sysclk
t_sSDAx	SDA Set-Up Time to SCL Rising	250	-	ns
t_dSDAx	SDA Output Delay Time From SCL Falling	-	3.5	µs
t_r	Rise Time of Both SDA and SCL (Note 12)	-	1	µs
t_f	Fall Time of Both SDA and SCL (Note 12)	-	300	ns
t_sSTO	Setup Time For a Stop Condition	4.7	-	µs

NOTES:

11. Data is clocked in as valid on the next XTALI rising edge after SCL goes low.
12. Limits established by characterization and not production tested.

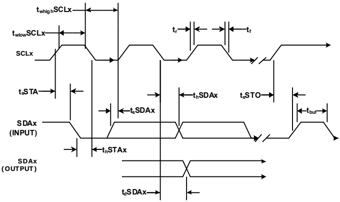


FIGURE 3. I^{2}C INTERFACE TIMING

SPI™ Master Mode Interface Port Timing

T_A = +25°C, CVDD = PLLVDD = 1.8V ±5%, RVDD = PWMVDD = 3.3V ±10%. All grounds at 0.0V. All voltages referenced to ground.

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
t_V	MOSI Valid From Clock Edge	-	8	ns
t_S	MISO Setup to Clock Edge	10	-	ns
t_H	MISO Hold From Clock Edge	1 system clock + 2ns		
t_{WI}	nSS Minimum Width	3 system clocks + 2ns		

SPI™ Slave Mode Interface Port Timing

T_A = +25°C, CVDD = PLLVDD = 1.8V ±5%, RVDD = PWMVDD = 3.3V ±10%. All grounds at 0.0V. All voltages referenced to ground.

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
t_V	MISO Valid From Clock Edge	3 system clocks + 2ns		
t_S	MOSI Setup to Clock Edge	10	-	ns
t_H	MOSI Hold From Clock Edge	1 system clock + 2ns		
t_{WI}	nSS Minimum Width	3 system clocks + 2ns		

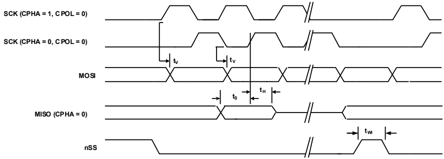
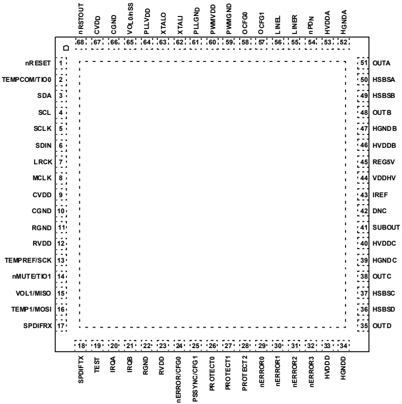


FIGURE 4. SPI TIMING

Pin Configuration

68 LD QFN
TOP VIEW



Pin Descriptions

PIN	PIN NAME (Note 13)	TYPE	VOLTAGE LEVEL (V)	DESCRIPTION
1	nRESET	I	3.3	Active low reset input with hysteresis. A low level activates a system level reset, which initializes all internal logic and program operations. The system latches the boot mode selection on the IRQ input pins on the rising edge.
2	TEMPCOM/TIO0	I/O	3.3	Board temperature monitor common I/O pin. Provides 16mA drive strength when operating as an output.
3	SDA	I/O	3.3	Two-wire serial data port, open drain driver with 8mA drive strength. Bidirectional signal used by both the master and slave controllers for data transport. Pin floats on reset.

Pin Descriptions (Continued)

PIN	PIN NAME (Note 13)	TYPE	VOLTAGE LEVEL (V)	DESCRIPTION
4	SCL	I/O	3.3	Two-wire serial clock port, open drain driver with 8mA drive strength. Bidirectional signal used by both the master and slave controllers for clock signaling. Pin floats on reset.
5	SCLK	I	3.3	I^{2}S serial audio bit clock (SCLK) Input. Input has hysteresis.
6	SDIN	I	3.3	I^{2}S serial audio data (SDIN) Input. Input has hysteresis.
7	LRCK	I	3.3	I^{2}S serial audio left/right (LRCK) Input. Input has hysteresis.
8	MCLK	O	3.3	I^{2}S serial audio master clock output for external ADC/DAC components, drives low on reset. Output is an 8mA driver.
9	CVDD	P	3.3	Core power, +1.8VDC. Used in the chip internal DSP, logic, and interfaces.
10	CGND	GND	3.3	Core ground.
11	RGND	GND	3.3	Digital pad ring ground. Internally connected to PWMGND.
12, 23	RVDD	P	3.3	Digital pad ring power, 3.3V. This 3.3V supply is used for all the digital I/O pad drivers and receivers, except for the analog pads. Both of these pins must be connected. Internally connected to PWMVDD.
13	TEMPREF/ SCK	I/O	3.3	Reference pin for the temperature monitor and SPI clock. At deassertion of device reset, this pin operates as a SPI clock with 8mA drive strength. Upon internal D2-4P firmware execution, this pin becomes a temperature monitor reference.
14	nMUTE/ TIO1	O	3.3	Mute signal output. When active low, a mute condition drives this pin low. The output is a 16mA driver. Initializes as an input at reset, then becomes an output upon internal firmware execution.
15	VOL1/ MISO	I/O	3.3	Volume control pulse input and SPI master-input/slave-output data signal. At deassertion of device reset, this pin operates as a SPI master input or slave output (when operating as an output, provides 4mA drive strength). At internal D2-4P firmware execution, this pin becomes an input for monitoring up/down phase pulses from volume control (one of two volume input pins).
16	TEMP1/ MOSI	I/O	3.3	Board temperature monitor pin and SPI master-output/slave-input data signal. At deassertion of device reset, this pin operates as a SPI master output or slave input (when operating as an output, provides 4mA drive strength). At internal D2-4P firmware execution, this pin becomes an input for monitoring board temperature.
17	SPDIFRX	I	3.3	S/PDIF digital audio data input.
18	SPDIFTX	O	3.3	S/PDIF digital audio data output. This pin is the S/PDIF audio output and drives an 8mA, 3.3V stereo output up to 192kHz. Pin floats on reset.
19	TEST	I	3.3	Hardware test mode control. For factory use only. Must be tied low.
20	IRQA	I	3.3	Interrupt request port A. One of two IRQ pins, tied to logic (3.3V) high or to ground. High/low logic status establishes the boot mode selection upon deassertion of the reset (nRESET) cycle.
21	IRQB	I	3.3	Interrupt request port B. One of two IRQ pins, tied to logic (3.3V) high or to ground. High/low logic status establishes the boot mode selection upon deassertion of the reset (nRESET) cycle.
22	RGND	GND	3.3	Digital pad ring ground. Internally connected to PWMGND.
24	nERROR/ CFG0	I/O	3.3	Output configuration selection input and nERROR output. At device reset, this pin operates as an input and uses an application-installed pull-up or pull-down connection to the pin to specify one of four amplifier configurations. At internal D2-4P firmware execution, this pin becomes an output and provides an active-low output drive when amplifier protection monitoring detects an error condition. When operating as an output, this pin provides 4mA drive strength. **Note:** This pin may also be called “PSCURR” on some reference designs. Function is identical regardless of name.
25	PSSYNC/ CFG1	I/O	3.3	Output configuration selection input and power supply sync output. At device reset, this pin operates as an input and uses an application-installed pull-up or pull-down connection to the pin to specify one of four amplifier configurations. At internal D2-4P firmware execution, this pin becomes an output and provides a synchronizing signal to on-board power supply circuits. When operating as an output, this pin provides 4mA drive strength. **Note:** This pin may also be called “PSTEMP” on some reference designs. Function is identical regardless of name.
26	PROTECT0	I/O	3.3	PWM protection input. Input has hysteresis. This pin’s protection monitoring functionality is controlled by internal D2-4P firmware and is dependent on which of the four amplifier configurations is enabled.

Pin Descriptions (Continued)

PIN	PIN NAME (Note 13)	TYPE	VOLTAGE LEVEL (V)	DESCRIPTION
27	PROTECT1	I/O	3.3	PWM protection input. Input has hysteresis. This pin's protection monitoring functionality is controlled by internal D2-4P firmware and is dependent on which of the four amplifier configurations is enabled.
28	PROTECT2	I/O	3.3	PWM protection input. Input has hysteresis. This pin's protection monitoring functionality is controlled by internal D2-4P firmware and is dependent on which of the four amplifier configurations is enabled.
29	nERROR0	O	3.3	Overcurrent protection output, channel A output stage. Open drain 16mA driver with internal 100kΩ pull-up (approximate). Pulls low when active from overcurrent detection of the output stage.
30	nERROR1	O	3.3	Overcurrent protection output, channel B output stage. Open drain 16mA driver with internal 100kΩ pull-up (approximate). Pulls low when active from overcurrent detection of the output stage.
31	nERROR2	O	3.3	Overcurrent protection output, channel C output stage. Open drain 16mA driver with internal 100kΩ pull-up (approximate). Pulls low when active from overcurrent detection of the output stage.
32	nERROR3	O	3.3	Overcurrent protection output, channel D output stage. Open drain 16mA driver with internal 100kΩ pull-up (approximate). Pulls low when active from overcurrent detection of the output stage.
33	HVDDD	P	HV	Output stage D high voltage supply power. A separate power pin connection is provided for each of the output stages. All of the HVDD[A:D] pins and the VDDHV pin connect to the system "HV" power source.
34	HGNDD	GND	HV	Output stage D high voltage supply ground. A separate ground pin connection is provided for each of the output stages. All of the HGND[A:D] pins connect to system "HV" power ground (see Note 15).
35	OUTD	O	HV	PWM power amplifier output, channel D.
36	HSBSD	I	HV	High-side boot strap input, output channel D. Capacitor couples to OUTD amplifier output.
37	HSBSC	I	HV	High-side boot strap input, output channel C. Capacitor couples to OUTC amplifier output.
38	OUTC	O	HV	PWM power amplifier output, channel C.
39	HGNDC	GND	HV	Output stage C high voltage supply ground. A separate ground pin connection is provided for each of the output stages. All of the HGND[A:D] pins connect to system "HV" power ground (see Note 15).
40	HVDDC	P	HV	Output stage C high voltage supply power. A separate power pin connection is provided for each of the output stages. All of the HVDD[A:D] pins and the VDDHV pin connect to the system "HV" power source.
41	SUBOUT	O	3.3	"Subwoofer" channel PWM output with 16mA drive strength. Connects to filter network for supplying line-level analog output to subwoofer.
42	DNC	-	-	Do not connect to this pin.
43	IREF	I	-	Overcurrent reference analog input. Used in setting the overcurrent error detect externally-set threshold. The pin needs to be connected to a 100kΩ resistor to ground to set the overcurrent threshold according to the specified limits.
44	VDDHV	P	+HV	High voltage internal driver supply power. All of the HVDD[A:D] pins and the VDDHV pin connect to the system "HV" power source. The internal +5V supply regulators also operate from this VDDHV input.
45	REG5V	P	5	5V internal regulator filter connect. A +5V supply is internally generated from the voltage source provided at the VDD pin. REG5V is used for external connection of decoupling capacitors.
46	HVDDB	P	HV	Output stage B high voltage supply power. A separate power pin connection is provided for each of the output stages. All of the HVDD[A:D] pins and the VDDHV pin connect to the system "HV" power source.
47	HGNDB	GND	HV	Output stage B high voltage supply ground. A separate ground pin connection is provided for each of the output stages. All of the HGND[A:D] pins connect to system "HV" power ground (see Note 15).
48	OUTB	O	HV	PWM power amplifier output, channel B.
49	HSBSB	I	HV	High-side boot strap input, output channel B. The capacitor couples to the OUTB amplifier output.
50	HSBSA	I	HV	High-side boot strap input, output channel A. The capacitor couples to the OUTA amplifier output.
51	OUTA	O	HV	PWM power amplifier output, channel A.
52	HGNDA	GND	HV	Output stage A high voltage supply ground. A separate ground pin connection is provided for each of the output stages. All of the HGND[A:D] pins connect to system "HV" power ground (see Note 15).

Pin Descriptions (Continued)

PIN	PIN NAME (Note 13)	TYPE	VOLTAGE LEVEL (V)	DESCRIPTION
53	HVDDA	P	HV	Output stage A high voltage supply power. A separate power pin connection is provided for each of the output stages. All of the HVDD[A:D] pins and the VDDHV pin connect to the system "HV" power source.
54	nPDN	I	3.3	Power-down and mute input. Active low. When this input is low, all four outputs become inactive and their output stages float, and their output is muted. Internal logic and other references remain active during this power-down state.
55	LINER	O	3.3	"Right" channel PWM output, with 16mA drive strength. Connects to the filter network to supply the line-level analog output.
56	LINEL	O	3.3	"Left" channel PWM output, with 16mA drive strength. Connects to the filter network to supply the line-level analog output.
57	OCFG1	I	3.3	Output configuration control select. OCFG0 and OCFG1 are logic inputs to select the output configuration mode of the output stages. Connects to either the PWMGND ground or PWMVDD (+3.3V) through a nominal 10kΩ resistor to select output configuration.
58	OCFG0	I	3.3	Output configuration control select. OCFG0 and OCFG1 are logic inputs to select the output configuration mode of the output stages. Connects to either the PWMGND ground or PWMVDD (+3.3V) through a nominal 10kΩ resistor to select output configuration.
59	PWMGND	P	3.3	PWM output pin ground. Internally connected to RGND.
60	PWMVDD	P	3.3	PWM output pin power. This 3.3V supply is used for the PWM pad drivers. Internally connected to RVDD.
61	PLLGND	P	1.8	PLL analog ground. Tie to a low voltage ground (CGND, RGND) through a single point connection to isolate ground noise on the board and minimize effects on the PLL.
62	XTALI	P	1.8	Crystal oscillator analog input port.
63	XTALO	P	1.8	Crystal oscillator analog output port (this output drives the crystal and XTALO does not have a drive strength specification).
64	PLLVDD	P	1.8	PLL analog power, 1.8V.
65	VOL0/ nSS	I/O	3.3	Volume control pulse input and SPI slave select. When device reset is deasserted, this pin operates as a SPI slave select input. At internal D2-4P firmware execution, this pin becomes an input for monitoring up/down phase pulses from volume control (one of two volume input pins.)
66	CGND	P	1.8	Core ground
67	CVDD	P	1.8	Core power, +1.8VDC. Used in the chip internal DSP, logic, and interfaces.
68	nRSTOUT	O	3.3	Active low open-drain output with 16mA drive strength. This pin drives low when either the RVDD 3.3V brownout detector, PWMVDD 3.3V brownout detector, or 1.8V brownout detector goes active. Use this output to initiate a system reset to the nRESET pin upon brownout event detection.

NOTES:

13. All pin names are active high unless otherwise specified. Active low pins have an "n" prefix, such as nRESET.
14. All power and ground pins with the same names must be tied together to all other pins of their same name (that is, tie CVDD pins together, CGND pins together, RVDD pins together, and RGND pins together). Tie CGND and RGND together on the board and ensure the RGND and PWMGND pins are internally connected and tied together on the board.
15. The thermal pad is internally connected to all four HGND ground pins (HGNDA, HGNDB, HGNDC, and HGNDD). Any connection to the thermal pad must be made to the common ground for these four ground pins.

Typical Performance Characteristics

Test Considerations

- Typical performance measurements are made using an Audio Precision™ 2700 Series audio analyzer.
- Precision power resistors are used for the 8Ω loudspeaker loads
- Measurements are done using a +HV supply of +24.0VDC.

Full-Bridge Typical Performance Curves

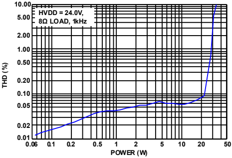


FIGURE 5. THD vs POWER, FULL-BRIDGE

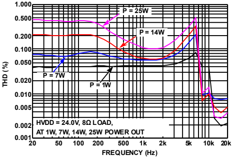


FIGURE 6. THD vs FREQUENCY, FULL-BRIDGE

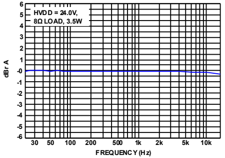


FIGURE 7. FREQUENCY RESPONSE, FULL-BRIDGE

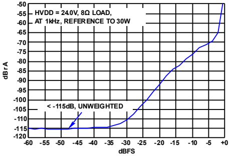


FIGURE 8. NOISE FLOOR, FULL-BRIDGE

Half-Bridge Typical Performance Curves

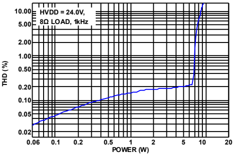


FIGURE 9. THD vs POWER, HALF-BRIDGE

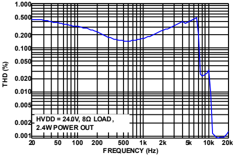


FIGURE 10. THD vs FREQUENCY, HALF-BRIDGE

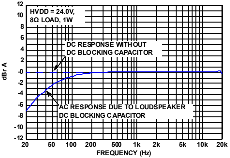


FIGURE 11. FREQUENCY RESPONSE, HALF-BRIDGE

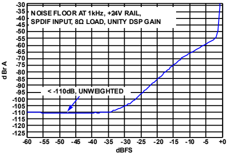


FIGURE 12. NOISE FLOOR, HALF-BRIDGE

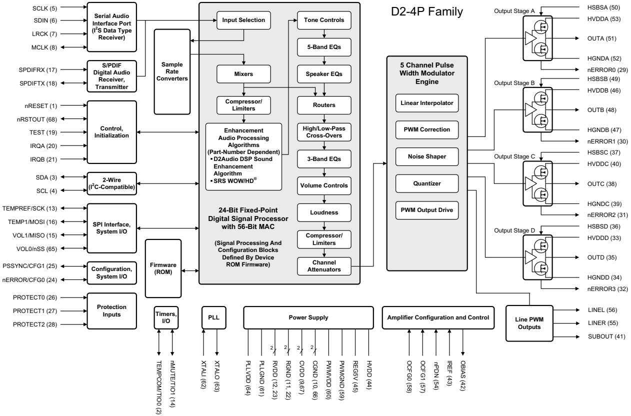


FIGURE 13. D2-4P FUNCTIONAL BLOCK DIAGRAM

Functional Description

Overview

The D2-4P devices, shown in Figure 13 on page 15, are integrated System-on-Chip (SoC) audio processors and Class D digital audio amplifiers. They include digital audio input selection, signal routing, complete audio processing, PWM controllers, amplifier and protection control, and integrated power stages. Stereo I^2S and S/PDIF Digital input support, plus I^2C and 2-wire SPI control interfaces, provide integration compatibility with existing system architectures and solutions.

The four configurable power stages can operate as four separate Half-Bridge outputs, as two Full-Bridge outputs, or in combinations of Half-Bridge plus Full-Bridge outputs. Separate PWM outputs provide additional combinations to drive headphone outputs or line-level stereo and subwoofer outputs. These application-dependent configurations provide for driving Stereo (2.0) Speaker, 2.1 Speaker, and Stereo (2.2) Bi-Amp Speaker solutions, as well as providing Stereo Line outputs, Headphone outputs, or Subwoofer line outputs.

Audio output implementations are defined by the configuration mode select pins and provide four combinations of powered and line amplifier outputs as shown in Table 1. The five independent audio processing paths feed a PWM engine, where the five PWM channels are mapped to the configuration-selected power stages and line outputs.

TABLE 1. OUTPUT CONFIGURATION MODES

CONFIGURATION MODE	NAME	FUNCTION
0	2.0 L/R 4-Quadrant	• Powered left and right outputs with 4-quadrant, full bridge drivers • No line-level outputs
1	2.0 L/R + L/R/Sub Line	• Powered left and right outputs with 2-quadrant, full bridge drivers • Stereo left + right line-level outputs • Subwoofer line-level output
2	2.1 L/R/Sub + L/R Line	• Two half bridge drivers for powered left and right outputs • 2-quadrant, full bridge driver for powered subwoofer output • Two (stereo left + right) line-level outputs • Crossover filtering included within audio path signal flow
3	2.2 Bi-Amp	• Four half bridge drivers for powered bi-amp left + right outputs • Crossover filtering included within audio path signal flow

The audio path includes a stereo Sample Rate Converter (SRC), five independent audio processing channels, and device-specific audio enhancement algorithms.

Programmable parameter settings for audio processing include volume control, path routing and mixing, high/low pass filtering, multi-band equalizers, compressors, and loudness. These parameters can be adjusted using the D2 Audio Customization GUI, or can be set by a system/amplifier microcontroller through the D2-4P's control interface.

Audio Enhancement Features

The D2-4P family devices include the D2 Audio DSP Sound Enhancement Algorithm or DTS®(SRS) WOW/HD™ audio enhancement algorithms. These device-specific functions are integrated within the firmware as part of the standard audio processing signal flow and are supported per device as:

D2 Audio sound enhancement algorithm (Included in the D2-45057 device)

- 2-channel stereo spatialization
- Bass enhancement
- Content/configuration EQ presets
- Improved vocal clarity
- Automatic room audio setup/equalization/optimization
- Automatic loudspeaker setup/equalization/correction
- DTS®(SRS) WOW/HD™
  - Included in the D2-45157 device

Each of these enhancements uses its own algorithms, where choice of enhancement is specified by device part number. The D2-45057 includes only D2 Audio DSP Sound Enhancement Algorithm support, and the D2-45157 includes only DTS®(SRS) WOW/HD™ support. These enhancements also have their own unique set of programmable parameters to control operation.

Serial Audio Digital Input

The D2-4P devices include one Serial Audio Interface (SAI) port that accommodates two digital audio input channels. The SAI port operates in slave mode only, supports the I^2S digital audio industry standard, and can carry up to 24-bit Linear PCM audio words.

The digital audio input from the SAI input port routes directly through the Sample Rate Converters (SRC). Either the I^2S digital input or the S/PDIF Digital input can be selected as the audio path source.

S/PDIF Digital Audio I/O

The D2-4P devices contain one IEC60958 compliant S/PDIF Digital receiver input and one IEC60958 compatible S/PDIF Digital transmitter.

The S/PDIF Digital receiver input includes an input transition detector, digital PLL clock recovery, and a decoder to separate the audio data. The receiver meets the jitter tolerance specified in IEC60958-4.

The S/PDIF Digital transmitter complies with the consumer applications defined in IEC60958-3. The transmitter supports 24-bit audio data, but does not support user data and channel status.

Compressed digital formats are not decoded within the D2-45057 and D2-45157. However, a bit-exact pass-through mode is supported from the SPDIFRX input to the SPDIFTX output, which allows for designs that require IEC61937-compliant original compressed audio input bitstream be made available at the product's S/PDIF Digital output.

Sample Rate Converter

The D2-4P devices contain a 2-channel asynchronous Sample Rate Converter (SRC) within the audio input signal flow path. The SRC converts audio data input sampled at one input sample rate to a fixed 48kHz output sample rate, which aligns asynchronous input audio streams to a single rate for system processing.

Audio data presented to the SRC can be from either the SAI or S/PDIF Digital input sources with an input sample rate from 16kHz to 192kHz. In addition to converting the input sample rate to the output sample rate, input clock jitter and sampling jitter is attenuated by the SRC to further enhance audio quality.

DSP

A 24-bit fixed-point Digital Signal Processor (DSP) controls the majority of audio processing and system control functions on the D2-4P.

Audio path signal routing, programmable-parameter processing blocks, and control logic are defined within the device's internal firmware. Signal flows through the device are buffered and processed through hardware specific-function blocks such as the SRC. Internal device registers allow full integration of DSP control with the internal ROM-based firmware, as well as providing for external control of audio processing parameters.

Clock and PLL

Clocks are generated on-chip using a fundamental-mode crystal connected across the XTALI and XTALO pins. XTALO is an output, but it is designed only to drive the crystal and does not connect to any other circuit. XTALI is an input that connects to the other side of the crystal.

The clock generation contains a low jitter PLL to ensure low noise PWM output and a precise master clock source for sample rate conversion and the audio processing data paths. The internal PLL's VCO clock operates at 12x the crystal frequency (12 x 24.576MHz) and provides complete device and system timing reference. It is used throughout the device, including clock generators for brownout detection, system and power-on reset, DSP, S/PDIF Digital transmitter, and PWM engine timing.

Clock and PLL hardware functions are controlled by internal device firmware. They are not programmable and are optimized for device and system operation.

Timers

Two independent timers are used for device and system control. One timer is used for internal references for chip-specific operations. The other is used for the system/board temperature sensing control algorithm. Two I/O pins (TIO0 and TIO1) are associated with the timers. Their pin functions are defined by the device firmware. Only TIO0 is actually used in relationship to its timer, Timer 0, and operates the timing-related I/O functions of the temperature monitoring algorithm. Timer 1 is used for internal functions of the device. Its pin (TIO1) is not used for this timing operation and is defined by device firmware as the nMUTE input pin.

Audio Outputs

Audio outputs are provided through four output power stages that are configurable for driving loudspeakers. Three additional PWM outputs are also available for driving line-level audio outputs. Combinations of outputs and their audio processing channel assignment are defined by the device's configuration mode settings.

Output Power Stages

The devices include four independent output stages (Figure 14) that are each implemented using a high-side (to positive HVDD supply) and a low-side (to HV supply ground) FET pair. Drivers and overcurrent monitoring are included in each of these four output stages. Depending on the selected configuration mode, these four stages can be used independently as single half-bridge outputs or as pairs for full-bridge outputs.

Audio processing PWM channel outputs are routed to the inputs of the four output stages based on the OCFG0 and OCFG1, nERROR/CFG0, and PSSYNC/CFG1 configuration settings. Each output stage includes its own high-side and low-side current sensing that feeds to internal monitor logic and provides its nERROR output connection. Temperature and undervoltage monitoring also provide status and input to device protection control.

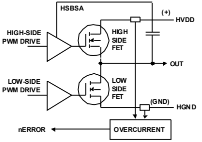


FIGURE 14. OUTPUT STAGE

Output Options

The D2-4P devices provide four configuration options for the power stage outputs. The power stage configuration is selected by strapping the OCFG0 and OCFG1 pins high or low. These defined configurations include:

- Two channels of full bridge, 4-quadrant outputs
- Two channels of full bridge, 2-quadrant outputs
- Four channels of half-bridge outputs
- Two channels of half-bridge and one channel of full bridge

Audio processing routing and control supporting the output stage configurations is defined by the logical high or low strapping of the nERROR/CFG0 and PSSYNC/CFG1 pins. Audio path definition, audio path output routing, and output stage configurations are automatically set to one of the four available modes based on these configuration settings.

PWM Audio Outputs

Three PWM outputs provide audio for up to three line-level outputs. Audio processing channel assignment is mapped to these PWM outputs based on the device's available configuration settings.

Using only a simple passive filter, the PWM outputs drive line-level outputs at a nominal $1V_{RMS}$. If active filter configurations are added, the PWM outputs can also drive headphone outputs or $2V_{rms}$ or higher line outputs. (alternately, these PWM outputs can also be used to drive powered outputs using additional power stages on the system design).

Control and Operation

Control Register Summary

The control interface provides access to the registers used for audio processing blocks and signal flow parameters. Audio input selection (I^{2}S input or S/PDIF receiver input) and all programmable data elements used in the audio processing paths are controlled through these register parameters, and each parameter is defined with its specific register address. Programming details, register identification, and parameter calculations are provided in the D2-4 Family/*D2-4P Register API Specification* document.

I^{2}C 2-Wire Control Interface

The 2-Wire I^{2}C compatible interface allows communication with an external controller. This interface is usable through either an external microcontroller bus, or for communication to EEPROMs, or other compatible peripheral chips.

The I^{2}C interface supports normal and fast mode operation and is multi-master capable. In a D2-4P system application, it operates as an I^{2}C slave device where the system controller operates as the I^{2}C master.

Reading and Writing Control Registers

All reads or writes to registers (shown in Figures 15 and 16) begin with a Start Condition, followed by the Device Address byte, three Register Address bytes, three Data bytes, and a Stop Condition.

Register writes through the I^{2}C interface are initiated by setting the read/write bit that is within the device address byte. The Write sequence shown in Figure 15 on page 19 is described in Table 2.

TABLE 2. I^{2}C WRITE SEQUENCE

BYTE	NAME	DESCRIPTION
0	Device Address	Device address with R/W bit set
1	Register Address [23:16]	Upper eight bits of address
2	Register Address [15:8]	Middle eight bits of address
3	Register Address [7:0]	Lower eight bits of address
4	Data[23:16]	Upper eight bits of write data
5	Data[15:8]	Middle eight bits of write data
6	Data[7:0]	Lower eight bits of write data

All reads to registers, shown in Figure 16 on page 19, require two steps. First, the master must send a dummy write, which consists of sending a Start, followed by the device address with the write bit set, and three register address bytes. Next, the master must send a repeated Start, send the device address with the read/write bit set to Read, and read the next three data bytes. The master must Acknowledge (ACK) the first two read bytes, send a Not Acknowledge (NACK) on the third byte received, and send a Stop condition to complete the transaction. The device's control interface acknowledges each byte by pulling SDA low on the bit immediately following each write byte. The read sequence shown in Figure 16 is described in Table 3.

TABLE 3. I^{2}C READ SEQUENCE

BYTE	NAME	DESCRIPTION
0	Device Address	Device address with Write bit set
1	Register Address [23:16]	Upper eight bits of address
2	Register Address [15:8]	Middle eight bits of address
3	Register Address [7:0]	Lower eight bits of address
4	Device Address	Device address with Read bit set
5	Data[23:16]	Upper eight bits of write data
6	Data[15:8]	Middle eight bits of write data
7	Data[7:0]	Lower eight bits of write data

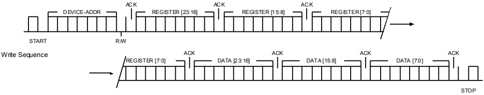


FIGURE 15. I^{2}C WRITE SEQUENCE OPERATION

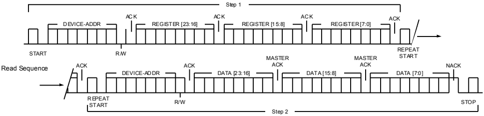


FIGURE 16. I^{2}C READ SEQUENCE OPERATION

Control Interface Address Spaces

Registers are accessed through the I^{2}C control interface using the I^{2}C channel address of 0xB2. This establishes the device or product under control through I^{2}C communication as the D2-4P.

Registers and memory spaces are defined within the D2-4P for specific internal operation and control. The highest-order byte of the register address (Bits 23:16) determines the internal address space used for control read or write access. The remaining 16 bits (Bits 15:0) describe the actual address within that space.

Programmable settings for the audio processing blocks are internally mapped to the address space defined with the highest order bits all zero. For example, 0x00nnnn, where nnnn is the address location within this address space.

Storing Parameters to EEPROM

The D2-4P can store parameters data to an EEPROM. If an EEPROM is installed in the application, the programmable parameter data can be saved in this EEPROM. This stored data can then be recalled upon reset or power-up.

Serial Peripheral Interface (SPI)

The Serial Peripheral Interface (SPI) is an alternate serial input port that provides an interface for loading parameter data from an optional EEPROM or Flash device during boot-up operation.

The four SPI interface pins are all shared functions:

- Following a reset condition and while the device is initiating the boot-up process, these four SPI pins (TEMPREF/SCK, TEMP1/MOSI, VOL1/MISO, VOL0/nSS) function as a SPI input port for external boot loading operation
- As soon as the boot-up process is completed and the device begins executing its firmware program, these pins are no longer used for SPI functions and are reassigned by the firmware for use as dedicated-function I/O for amplifier operation

See the multiple-purpose pin descriptions in Table 5 for more information about these pin functions.

Reset and Device Initialization

The D2-4P must be reset to initialize and begin proper operation. A system reset is initiated by applying a low level to the nRESET input pin. External hardware circuitry or a controller within the amplifier system design must provide this reset signal and connect to the nRESET input to initiate the reset process. Device initialization begins after the nRESET pin is released from its low-active state.

The chip contains power rail sensors and brownout detectors on the 3.3V RVDD and PWMVDD power supplies and the 1.8V CVDD power supply. A loss or droop of power from these supplies triggers their brownout detectors, which asserts the nRSTOUT output pin, driving it low. The nRSTOUT pin should connect to the nRESET input through hardware on the amplifier design to ensure a proper reset occurs if the power supply voltages drop below their design specifications.

At the deassertion of nRESET, the chip reads the status of the boot mode selection pins (IRQA and IRQB) and begins the boot process, determined by the boot mode that is defined by these pins' logic state. These device pins are strapped either high or low on the system's design (PCB). The state of these pins that is latched into defines the boot mode operation.

Boot Modes

The D2-4P devices contain embedded firmware to operate the part and run the amplifier system. Parameter information used by the programmable settings can be written to the device after it is operational and running. However, parameter data can also be read at boot time, which allows saved parameter settings to be used, or allows amplifier function to be set through a system microcontroller interface. The device is designed to boot in one of four possible boot modes, allowing control and data to be provided through these boot sources:

- I^2C slave (to external microcontroller)
- I^2C EEPROM
- Internal device ROM only
- SPI slave

The specific boot mode is selected based on the state of the IRQB and IRQA input pins at the time of reset de-assertion. Boot modes and their functions are shown in Table 4. **Note:** "Boot mode" describes the mode of device initialization with respect to the source of parameter data or start-up control settings. Do not confuse Boot Mode with "Output Mode" or audio processing "Configuration Mode" settings that define amplifier-specific functions.

TABLE 4. BOOT MODE SETTINGS

BOOT MODE	IRQB PIN	IRQA PIN	MASTER/ SLAVE	DESCRIPTION
0	0	0	I^2C Slave	Operates as an I^2C slave, boot at address 0x88. An external 2-wire I^2C master provides the boot code
1	0	1	I^2C Master	Operates as a 2-wire master; loads the bootcode from ROM on the I^2C port
2	1	0	-	Internal ROM boot/operation
3	1	1	SPI Slave	SPI slave. An external SPI master provides the boot code

The device initializes as defined by its boot mode, but gets its configuration and parameter data from the host device. This host device can be either an external controller, or from an EEPROM. If a system uses both an external controller and an EEPROM, the EEPROM loads first. During this time, the controller must remain off the I^2C bus until after the reading sequence from the EEPROM is complete.

Power Supply Requirements

The device requires operating power for these voltages:

- PWMVDD and RVDD:
  - 3.3V DC supply voltage
  - RVDD operates interface and I/O logic
  - PWMVDD is the same voltage and is used for the PWM outputs and output stage drive
- CVDD and PLLVDD
  - 1.8V DC supply voltage
  - CVDD operates the internal processor and DSP core
  - PLLVDD also operates at the internal processor voltage levels, but is provided through a separate connection to allow isolation and bypassing for noise and performance improvements
- "High Voltage" (HVDD[A:D], and VDDHV)
  - HVDDA, HVDDB, HVDDC, and HVDDD are the "High Voltage" supplies used for operating each of the four output power stages
  - VDDHV is used as the source for the on-chip +5V regulator that is used for the output stage drivers
  - Individual power (HVDD[A:D]) and their corresponding ground (HGND[A:D]) pins are included for each of the four power stage outputs, providing channel isolation and low impedance source connections to each of the outputs. All the HVDD[A:D]/VDDHV pins connect to the same voltage source

High-Side Gate Drive Voltage

An on-chip bootstrap circuit provides the gate drive voltage used by each output stage. A pin is included for each output channel (HSBS[A:D]) for connection of a capacitor (nominal, 0.22µF/50V) from this pin to that channel's PWM output.

Drivers for high-side FETs on the output stages require a voltage above the supply used for powering that FET. The charge pumping action of the driving PWM to this driver produces this "bootstrap" voltage, and uses this capacitor to filter and hold this gate drive voltage. This enables amplifier operation without needing a connection to an additional power supply voltage.

Power Supply Synchronization

The the PSSYNC/CFG1 pin provides a power supply synchronization signal for switching power supplies. Firmware configures this pin to the frequency and duty cycle needed by the system switching regulator. This synchronization allows switching supplies used with the device to operate without generating in-band audio interference signals that could occur if the switching power supply is not locked to the amplifier switching.

This PSSYNC/CFG1 pin is a shared pin (see the multiple-purpose pin descriptions in Table 5 on page 23). During device reset and initialization, the pin operates as one of two configuration input pins, where its high or low logic state is used to set the amplifier configuration mode. After completing reset and when the device firmware begins operating, this pin becomes the PSSYNC output.

Power Sequence Requirements

Voltage sensors and brownout detectors monitor supply voltages to the device. The logic and built-in protection of this voltage monitoring prevents operation until all supply voltages are within their specified limits. However, during application of power, the CVDD and RVDD (including PWMVDD) voltages should be brought up together to avoid high current transients that could fold back a power supply regulator.

During application of power to the system and while the CVDD voltage (nominal +1.8V) is below its minimum specified limit, the RVDD and PWMVDD supplies (nominal +3.3V) must not exceed the voltage that is present at CVDD. (if V_{CVDD} < minimum-specified, then $V_{RVDD/PWMVDD}$ must be < V_{CVDD}.) After CVDD reaches its minimum limit, RVDD/PWMVDD can then continue to increase to its nomal design (3.3V) value (PLLVDD can be brought up separately).

The best practice is for all supplies to feed from regulators using a common power source. Typically this can be achieved by using a single low-voltage supply power source and regulating the 3.3V and 1.8V supplies from that source. Also, as noted in "Electrical Specifications" on page 4, all voltages of the same names must be tied together at the board level.

REG5V

The output stage internal drivers require their own +5VDC supply voltage. An on-chip regulator operates from the VDDHV voltage to produce this +5V voltage. The REG5V pin is used for external capacitor connection to filter this regulated voltage. A 1.0µF and 0.1µF capacitor should be connected to this pin, and the connection should be made as close as practical to the pin. This internal +5V is used only by the output stage drivers. Do not makes other connections to this pin.

Pin and Control Block Functions

I/O Control Pins

Several device pins are used as specific-function inputs and outputs to control amplifier and device operation. These pins are implemented within the device hardware as general purpose inputs/outputs. However, their operation is not programmable, and their specific function is totally defined by the D2-4P internal firmware. These pins' functions are defined in "Pin Descriptions" on page 9, and additional detail is included within the descriptions of the functional blocks where these pins are used.

Some pins are multiple-purpose, and their functions are defined accordingly by the operational state (for example, resetting, initializing, booting, running) of the D2-4P. These multiple-purpose pins and their descriptions and uses are described in more detail in Table 5 on page 23.

nPDN Input Pin

The nPDN pin is a control input that is used to power-down the outputs. When this input is pulled low, all audio outputs turn off and become inactive, the internal PWM drive to the output stages is turned off, and all output stages float. Internal logic and other references remain active during this power-down state. Asserting nPDN also causes all four nERROR[0:3] outputs to pull (active) low.

Each of the four output stages incorporates its own latching overcurrent hardware shutdown logic, in addition to the separate protection events that occur through firmware control from an overcurrent condition. Firmware protection control performs other steps to clear this hardware latched shutdown, although asserting nPDN also resets the hardware-latched state.

The nPDN pin is active low and is inactive when at logic high. In normal operation, it is held high with pull-up to the RVDD supply.

nERROR[0-3] Output Pins

Each of the four output stages includes a two-level overload and overcurrent monitor. An overcurrent or overload condition asserts the nERROR output for that channel.

An undervoltage condition for the voltages used by the output stages (HVDD[A:D]/VDDHV, REG5V, PWMVDD), or assertion of nPDN causes all four nERROR outputs to assert.

The nERROR pins are open drain, active-low, and can be wire-or connected together. Depending on the output mode configuration where more than one output stage can be used for an audio channel, nERROR pins associated with that audio channel are connected together to provide the monitoring status.

In applications where multiple power stage outputs are defined for an audio channel, the nERROR pins for these power stages should be tied together, and tied to the PROTECT input pin associated with that audio channel. See Table 6 on page 24 for the connections for the different configuration modes.

IREF Pin

The IREF pin sets the overcurrent and overload monitoring threshold. The design requires a 100kΩ resistor to connect from this pin to ground.

Configuration Assignment Pin Differences

Two pairs of pins are used for configuration assignments. Both pin pairs are used for the assignment, and their settings must both match their requirements for the configuration mode. The pin pairs are:

- OCFG0, OCFG1: Defines the output stage topology and operation of the output configuration
- nERROR/CFG0, PSSYNC/CFG1: Defines the audio processing and amplifier control supporting the output configuration

OCFG0, OCFG1 Input Pins

These two pins define the configuration of the four output stages. They are logic level input pins and are connected to logic high (PWMVDD) or logic ground (PWMGND) to establish which of the four output configurations is used in the design. See "Pin Descriptions" starting on page 9 for additional information.

nERROR/CFG0 and PSSYNC/CFG1 Pins

These pins define the amplifier configuration mode that the firmware uses to operate the amplifier. In addition to the OCFG0 and OCFG1 pins that set operation of the output stages, the nERROR/CFG0 and PSSYNC/CFG1 pins also establish audio signal processing path assignments and set up monitoring and protection for the configuration mode. The configuration pin logic levels are assigned by pull-up or pull-down resistors installed on that application.

The configuration defined by these pins is assigned when the D2-45057/D2-45157 exits its reset state. At that time, the logic statuses of the PSSYNC/CFG1 and nERROR/CFG0 pins are latched into internal device registers. These are shared-function pins, and after firmware begins executing, their functions are reassigned as outputs. See Table 5 on page 23 for more information about these pins and their shared functions.

Temperature Monitoring

The TEMPREF/SCK, TEMP1/MOSI, and TEMPCOM/TIO0 pins are used in a firmware-controlled algorithm to monitor temperature. These pins share other functions (see the multiple-purpose pin descriptions in Table 5 on page 23). During firmware execution, they operate as inputs and outputs for the measurement algorithm. Figure 17 shows the circuit for this temperature measurement implementation.

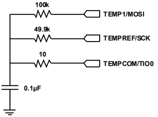


FIGURE 17. TEMPERATURE MONITOR CIRCUIT

A Negative Temperature Coefficient (NTC) 100kΩ resistor connects to the TEMP1/MOSI pin, and using the resistor's temperature/resistance correlation, the firmware monitors temperature of the NTC resistor. The internal device timing functions associated with the TIO0 pin provide calibration that correlates to system clock. A 49.9kΩ resistor connects to the TEMPREF/SCK pin and is used as a constant non-temperature-dependent reference for this algorithm.

The firmware algorithm is internal to the D2-4P. The status from this temperature monitor is used for the temperature protection functions of the device and its application. There are no adjustments or parameters for changing settings.

TABLE 5. MULTI-FUNCTION I/O CONTROL PIN ASSIGNMENT AND OPERATION

	PIN STATE DURING INITIALIZATION		PIN STATE DURING OPERATION		
PIN NAME	**I/O**	**FUNCTION**	**I/O**	**FUNCTION**	**CONNECTION REFERENCE**
TEMPREF/ SCK	Output	SPI clock output	Input	Temperature monitor reference. Used for the temperature monitoring algorithm.	Typical connection is to a 49.9kΩ resistor as a temperature monitor reference. Available for SPI connect if SPI is used in the application.
VOL1/ MISO	Input or Output	SPI master input or slave output. Function (master or slave) is determined by the nSS input state.	Input	Volume control Phase-B input. Used for monitoring rotary-encoder volume control.	Typical connection to +3.3V with 10kΩ pull-up resistors and to a 2-bit volume control encoder.
TEMP1/ MOSI	Output or Input	SPI master output or slave input. Function (master or slave) is determined by the nSS input state.	I/O	Temperature monitor reference I/O pin. Used for the temperature monitoring algorithm.	Typical connection is to a 100kΩ NTC resistor as the temperature monitor reference. Available for SPI connect if SPI is used in application.
nERROR/ CFG0	Input	(CFG0) Configuration Mode Input Select. Uses pull-up or pull-down to set the logic input level to define one of four amplifier configurations.	Output	Active low output amplifier protection and monitoring status indication.	Connects to +3.3V or to ground with a 10kΩ resistor to select logic high or low for setting configurations. Also connects to the input of the monitor or indicator circuit to provide status (called "PSTEMP" on some reference designs).
PSSYNC/ CFG1	Input	(CFG1) Configuration Mode Input Select. Uses pull-up or pull-down to set logic input level, to define one of 4 amplifier configurations.	Output	Sync Output for Synchronizing On-Board Power Supply regulator.	Connects to +3.3V or to ground with a 10kΩ resistor to select logic high or low for setting configurations. Also connects to the clock sync input of the on-board switching regulator (called "PSCURR" on some reference designs).
VOL0/ nSS	Input	SPI Slave Select.	Input	Volume Control Phase-A input. Used for monitoring rotary-encoder volume control.	Typical connection to +3.3V with 10kΩ pull-up resistors and to a 2-bit volume control encoder.

Configuration Setting

The configuration mode is assigned through two pairs of pin settings. When the D2-4P exits its reset state, the logic status of the PSSYNC/CFG1 and nERROR/CFG0 pins is latched into internal device registers. During this initialization time, these pins operate as logic inputs. After initialization completes and the internal firmware begins executing, these pins are re-assigned as outputs for their shared functions, and the internal latched logic state that defines the configuration mode remains until the device is powered down or reset again. The OCFG0 and OCFG1 pin status is not latched; those pins must remain in their pull-up or pull-down state.

Selection of one of the four configuration modes is defined by strapping the configuration pins high or low:

- OCFG0 and OCFG1 define the output power stage configuration
- nERROR/CFG0 and PSSYNC/CFG1 define the amplifier and channel configuration

These four pins are connected to either a high level (+3.3V) or low level (ground = 0). Connections should be through a 10kΩ resistor and not directly to the supply or ground.

Table 6 on page 24 shows the audio processing channel assignment, audio content, and output assignments for each of the four configuration modes.

Both pairs of configuration setting pins (OCFG0, OCFG1) and (PSSYNC/CFG1, nERROR/CFG0) must be used and both must be set to the same configuration mode.

In modes 2 and 3, the filtering for high and low pass crossovers is applied to the audio signal flow path, enabling the appropriate high or low pass content to be properly filtered for the PWM output channels.

TABLE 6. CONFIGURATION MODE AND CHANNEL ASSIGNMENTS

MODE	CONFIGURATION DESCRIPTION	OUTPUT CFG PINS		CONFIG MODE PINS		AUDIO PROC CHANNEL	AUDIO CONTENT	POWER STAGE OUTPUTS					PWM LINE OUTPUTS		
		OCFG1	OCFG0	PSSYNC /CFG1	nERROR /CFG0			OUTA	OUTB	OUTC	OUTD	nERROR[0:3] to PROTECT[0:2]	LINEL	LINER	SUB LINE
"00"	2-Channel 4-Quad Full Bridge (3-Level)	0	0	0	0	1	L SPKR	Left Full Bridge				nERROR0 +nERROR1 to PROT0			
						2	R SPKR			Right Full Bridge		nERROR2 +nERROR3 to PROT1			
						3						PROTECT2 Unused (tie high)			
						4									
						5									
"01"	2-Channel 2-Quad Full Bridge + L Line + R Line + Sub Line	0	1	0	1	1	L SPKR	Left Full Bridge				nERROR0 +nERROR1 to PROT0			
						2	R SPKR			Right Full Bridge		nERROR2 +nERROR3 to PROT1			
						3	L Line					PROTECT2 Unused (tie high)	Left		
						4	R Line							Right	
						5	Sub								Sub
"10"	2-Channel Half Bridge + 1-Channel Full Bridge for Sub,+ L Line, + R Line	1	0	1	0	1	L SPKR	Left HB				nERROR0 to PROT0			
						2	R SPKR		Right HB			- nERROR1 to PROT1			
						3	L Line						Left		
						4	R Line							Right	
						5	Sub			Ch 5 Sub Full Bridge		nERROR2 +nERROR3 to PROT2			
"11"	4-Channel Half Bridge 2.2 Bi-Amp	1	1	1	1	1	L HF SPKR	Left HF (HB)				nERROR0 to PROT0			
						2	L LF SPKR		Left LF (HB)			nERROR1 to PROT1			
						3	R HF SPKR			Right HF (HB)		nERROR2 to PROT2			
						4	R LF SPKR				Right LF (HB)	nERROR3 to PROT2			
						5									

NOTE: LF = Low Frequency, HF = High Frequency for Bi-Amp Config; HB = Half-Bridge

Protection

The D2-4P devices include multiple protection mechanisms. Output overload and overcurrent status for each output power stage provides two levels of monitoring. Temperature monitoring provides two levels of temperature status. On-chip undervoltage detection is included for all supply voltages.

The D2-4P devices use several strategies to prevent damage from the high voltages, currents, and temperatures present in class-D amplifiers. This protection is also effective against user-induced faults such as clipping, output overload, or output shorts, including both shorted outputs or short-to-ground faults. Protection includes events such as:

- Output overcurrent
- Output short-circuit
- Over-temperature
- Power supply brown-out
- Shoot-through overcurrent

Certain levels of protection are managed using on-chip hardware. Other protection is integrated into device firmware, and involves actions to:

- Shut down the outputs for a short-circuit, over-temperature, or undervoltage event.
- Shut down the device if power supply sensors detect voltages dropping below their design thresholds
- Provide indication and device shutdown (if needed) for overload and overcurrent monitor detection. Dual threshold monitors provide two levels of high current conditions
- Chip temperature monitoring provides dual threshold status of high temperature conditions, providing both indication and device shutdown if needed

Error Reporting

The system and device internal monitoring uses an I/O pin (nERROR/CFG1) as an output to signal a channel shutdown error condition to an external system controller. This output can be used to turn on a simple indicator.

The error output is also used to signal an external microcontroller that the I^2C bus may be busy. When the error output is low during system initialization, the I^2C bus is busy as a master device.

This error output is active low and only becomes used as an error reporting output after the device firmware initializes and begins running. The same pin is shared as an input (see Table 5 on page 23 for more information about shared-function pins). During a reset condition, this pin operates as an input and is one of two input pins used to define the configuration mode. A resistor pull-up or pull-down on this pin establishes the mode input configuration state. After completing the initialization sequence, these resistors do not affect the error output operation.

Short-Circuit and Overcurrent Sensing

Each PWM output FET includes a dual-threshold overcurrent sensor. Multiple functions occur depending on detection of overcurrent conditions:

- The lower threshold monitors fault conditions such as shorts and overloads on the loudspeaker outputs
- The higher threshold monitors fault conditions of the PWM output pin
- The nERROR output asserts for the channel detecting the fault
- For the lower level threshold, nERROR remains asserted only through the duration of the overcurrent event
- For the higher level threshold, the output is shut down and its nERROR output is asserted. These conditions remain latched until the controller acknowledges the fault event by turning off the channel's PWM drive (the PWM pin floats when shut down)

Hysteresis is built into the overcurrent detectors to suppress PWM switching transient events.

Protection Monitoring and Control

The overcurrent detectors generate either a pulse or latched logic level (depending on the low or high threshold) upon detection of high current. The detector status is presented to the nERROR[0:3] pins.

The PROTECT[0:2] pins are used as protection inputs to the firmware. Firmware action based on these pins' status depends on the selected output mode configuration. The nERROR[0:3] output pins and the PROTECT[0:2] input pins are connected together based on the system and output mode configuration shown in Table 6 on page 24.

Thermal Protection and Monitors

Temperature sensing provides two thresholds of temperature monitoring.

If the device reaches the lower threshold, a warning indication is generated and one level of thermal protection management is triggered.

On-chip hardware thermal protection shuts down the device upon a high-threshold temperature condition. If the device reaches the higher threshold, on-chip hardware latches and shuts down all four output stages. It also drives all four nERROR0-3 outputs low (active), providing this shut-down status to the firmware through the connected PROTECT0-2 inputs.

Graceful Overcurrent and Short-Circuit

Hard faults from overcurrent or short-circuit conditions shut down the outputs. High-threshold over-temperature also causes a shutdown. For lower-threshold event detections, graceful protection is provided for each output. Specific operation depends on the type and severity of the detected event, but action taken is to reduce conditions that contribute to the event, without the severity of a complete shutdown as in a high-limit fault condition.

Overcurrent monitoring status is presented to the PROTECT0-2 inputs from per-output detector status that drives the nERROR0-3 outputs. Overcurrent detection algorithms in firmware monitor these peak level detections, and upon detection of an overload condition, automatically reduce PWM gain. This Automatic Gain Control (AGC) action helps prevent audio output clipping and helps avoid related excessive-level conditions. The AGC algorithm operation functions through a stepped-changing of PWM gain reduction corresponding to characteristics and time-event detection of overloads. At the lower (non shut-down) high-temperature threshold, the AGC function also acts to attenuate the outputs to attempt to reduce temperature.

Output level gain and level change effects from the AGC function are similar to operation from a compressor. However, unlike a compressor where characteristics are determined by input levels, the PWM AGC operation is controlled through detection of near-overload output levels or from high temperature detection.

Power Supply Voltage Monitoring

Undervoltage sensors and brownout detectors monitor all supply voltages to the device. The logic and built-in protection of this voltage monitoring prevents operation until all supply voltages are within their specified limits. If any of these monitored voltages drop below their threshold, the device shuts down its outputs and asserts all four of the nERROR outputs.

Audio Processing

The audio processing, signal flow, and system definition is defined by the D2-4P internal ROM firmware and is executed by the DSP. The firmware defines the audio flow architecture, including the audio processing blocks. Each block is programmable and has adjustable audio-controlling parameters. The signal flow and audio processing blocks are shown in Figure 18. This architecture includes audio processing functions for:

- Input selection
- Mixers
- Input compressors and output limiters
- Tone controls
- 5-band and 3-band parametric equalizers
- Router
- High/low-pass crossover filters
- Volume and output level controls
- Loudness contour

Enhancement Audio Processing

The D2-45057 supports the D2 Audio DSP Sound Enhancement Algorithm. The D2-45157 supports the DTS®(SRS) WOW/HD™ algorithm.

Audio Processing Signal Flow Blocks

INPUT SELECTION

The Input Select register specifies the audio inputs that are assigned to the audio processing input path. Either the I^2S or S/PDIF Digital inputs are available.

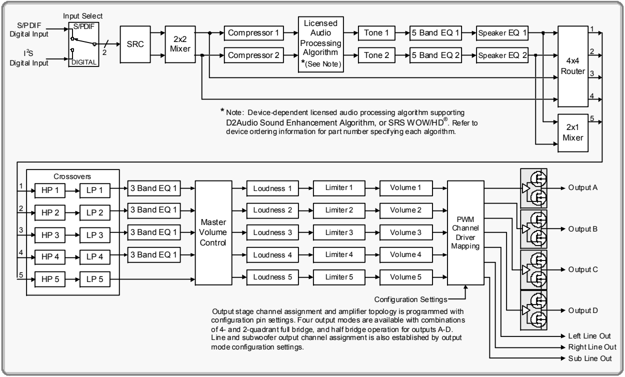
MIXERS

An input mixer provides a two-input, two-output mixing and routing path. Either input can be mixed at adjustable gain into either or both of the two outputs. The default setting is 0dB through each channel, with full cut-off for non-through channels. Attenuation is continuously variable with the programmable parameters.

A stereo mixer provides a path from the two input channels. Stereo mixers are typically used to provide a mix of both stereo input channels for crossover processing and become the source for the subwoofer channel. Gains for both input channels are adjustable to feed the single stereo mixer output.

TONE CONTROLS

Both input channels contain a tone control block. Each of the filters (bass or treble) is implemented with a first-order (6dB/octave) roll-off, using programmable corner frequency and a boost or attenuating gain. The signal flow processing automatically provides a smooth transition between tone control changes.



* Note: Device-dependent licensed audio processing algorithm supporting D2Audio Sound Enhancement Algorithm, or SRS WOW/HD®. Refer to device ordering information for part number specifying each algorithm.

Output stage channel assignment and amplifier topology is programmed with configuration pin settings. Four output modes are available with combinations of 4- and 2-quadrant full bridge, and half bridge operation for outputs A-D. Line and subwoofer output channel assignment is also established by output mode configuration settings.

FIGURE 18. D2-4P AUDIO SIGNAL FLOW

COMPRESSORS AND LIMITERS

Two individual input compressors are included in the input audio path, one for each of the two input channels. Five output limiters are also included in the five output path channels. The Compressor and Limiter blocks operate identically, and their parameter settings allow independent control of the audio signals. Typically, the input path blocks are programmed to provide a compression function and the output path blocks are programmed to limit output signal levels. However, each path can be programmed as needed. Each Compressor/Limiter has configurable Compression Ratio, Threshold, Attack and Release Time, as well as Makeup Gain.

MULTI-BAND EQUALIZERS

Three sets of Multi-Band Parametric Equalizers are included in the audio signal processing path. Each band of the equalizers provides independent gain, frequency, and Q-factor programming.

A 5-Band Equalizer and a Speaker Equalizer (SEQ) are included in both of the two input channels. Four 3-Band Equalizers are also located in the four output channels.

STEREO ROUTER

A 4x4 stereo router assigns any one of the four input channel paths to each of the four output paths. The router performs path assignment only. It does not provide gain or signal level adjustment.

HIGH/LOW-PASS CROSSOVER FILTERS

High-Pass and Low-Pass filter blocks are provided for each of the five output channels downstream of the Router and Stereo Mixer. These filter blocks provide a flexible Crossover function for all the output channels, including defining the subwoofer channel's frequency response.

The High and Low Pass blocks operate together and are implemented as a total of four cascaded elements. Two of each of the elements are allocated for High Pass functionality and the other two elements are allocated for Low Pass functionality. Complete flexibility allows each element to be optionally defined for either High Pass or Low Pass. Each element is selectable for a slope of 6dB, 12dB, 18dB, or 24dB, or can be bypassed. Butterworth, Bessel, or Linkwitz-Riley filter implementations are available.

MASTER VOLUME CONTROL

Use the software-controlled Master Volume control to adjust the global volume for all five output channels. Master Volume operates a continuously adjustable attenuator, from unity gain down to -100dB and cutoff.

Each of the five output channels has its own dedicated output level adjustments that provides individual channel gain or attenuation after the output limiter stages. Settings provide output level adjustment from +12dB to -100dB.

LOUDNESS CONTOUR

An individual software-controlled Loudness Contour is included for each of the five amplifier output channels. The Loudness Contour curve is customized to allow for dynamically and automatically enhancing the frequency response of the audio program material relative to the Master Volume Level setting. The Loudness Contour models the frequency response correction as defined by the Fletcher/Munson audio response curve. It provides amplitude or volume changes to signals to which the ear does not respond equally at very low listening levels.

SOUND ENHANCEMENT ALGORITHM PROCESSING

The D2 Audio DSP Sound Enhancement Algorithm audio processing provides a full set of enhancements to audio that greatly add to the quality and listening experience of sound in wide scopes of consumer devices. The D2 Audio DSP Sound Enhancement Algorithm uses psycho-acoustic processing that creates a rich-sounding environment from small speakers and synthesizes the sound and quality equivalent to more complex systems. It is especially suited to consumer products that include televisions, docking stations, and mini hi-fi stereo products.

Sound enhancement algorithm processing includes:

- 2-channel stereo spatialization
- Bass enhancement
- Content/configuration EQ presets
- Improved vocal clarity
- Automatic room audio setup/equalization/optimization
- Automatic loudspeaker setup/equalization/correction

The D2 Audio DSP Sound Enhancement Algorithm is completely included within the D2-4P Family devices.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Visit our website to make sure you have the latest datasheet revision.

DATE	REVISION	CHANGE
Mar 19, 2019	FN6785.2	Changed datasheet base part number to "D2-4P" Family Audio SOC". Changed the following terms throughout the datasheet: -"D2Audio" to "D2 Audio DSP" -"DAE-4" to "D2-4P family" -"DAE-4P" to "D2-4P family" -"Digital Audio Engine" to "Digital Audio Processor" -"SoundSuite" to "Sound Enhancement Algorithm" Updated Related Literature Updated audio enhancement features on page 16. Updated Figure 1 on page 1, Figure 13 on page 15, and Figure 18 on page 27. Removed About Intersil section. Updated disclaimer.
May 5, 2016	FN6785.1	Updated entire datasheet applying Intersil's new standards. Updated the Ordering Information table on page 2. Replaced Products verbiage to About Intersil verbiage. Added DTS disclaimer.
Jul 29, 2010	FN6785.0	Initial Release

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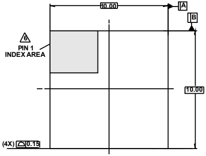
Package Outline Drawing

For the most recent package outline drawing, see L68.10x10C.

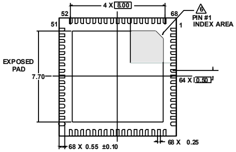
L68.10x10C

68 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE

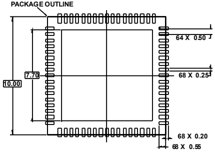
Rev 0, 04/09



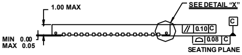
TOP VIEW



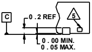
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.23mm and 0.28mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.

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(Rev.4.0-1 November 2017)

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