Future Technology Devices International Ltd

UM232H Single Channel USB Hi-Speed FT232H Development Module

Datasheet

1 Introduction

The UM232H is a USB-to-serial/FIFO development module in the FTDI product range which utilizes the FT232H USB Hi-Speed (480Mb/s) single-port bridge chip to handle the USB signaling and protocols. The UM232H is ideal for development purposes to quickly prove functionality of adding USB to a target design. The UM232H is a module designed to plug into a standard 0.6" wide 28 pin DIP socket. The USB connection to a host system is via a mini-B USB connector. All components used, including the FT232H, are Pb-free (RoHS compliant).

Figure 1 – UM232H USB to Serial/FIFO Development Module

1.1 FT232H

The FT232H is a single channel USB 2.0 Hi-Speed (480Mb/s) to Serial/FIFO IC. It can be configured in a variety of serial or parallel interfaces, such as UART, FIFO or FTDI's MPSSE mode which can configure either of the following interfaces: JTAG, SPI and I^2C. For MPSSE mode, there is also 14 bit-banging lines available along with the four interface lines. In addition to these, the FT232H supports a CPU-Style FIFO mode and a fast serial interface mode. It also introduces a half-duplex FT1248 interface that provides a flexible data communication and high performance interface between the FT232H device and external logic. For further details on the FT232H and the FT1248 mode, please refer to the FT232H datasheet and application note AN_167 for more details.

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2 Typical Applications

The UM232H module is used for prototyping and evaluation in an application using the FT232H.

- Rapid USB integration into existing and new electronic systems
- USB to multi-port JTAG, SPI and I^2C interfaces
- USB to FT1248 interfaces
- USB to RS232 / RS422 / RS485 Converters
- USB Instrumentation
- USB Industrial Control
- USB Electronic Point Of Sale Control
- Upgrading Legacy Peripherals to USB
- Cellular and Cordless Phone USB data transfer cables and interfaces
- Interfacing MCU / PLD / FPGA based designs to USB
- USB Audio and Low Bandwidth Video data transfer
- PDA to USB data transfer
- USB Smart Card Readers
- USB MP3 Player Interface
- USB FLASH Card Reader / Writers
- Set Top Box PC - USB interface
- USB Digital Camera Interface
- USB Hardware Modems
- USB Wireless Modems
- USB Bar Code Readers
- USB Software / Hardware Encryption Dongles
- USB Medical applications

2.1 Driver Support

The UM232H development module requires USB device drivers, available free from FTDI website. There is the Virtual Com Port driver which allows the UM232H to appear as a serial port allowing legacy applications for serial ports to function over USB (for example TTY). Another FTDI USB driver, the D2XX driver, can also be used with application software to directly access the FT232H on the UM232H through a DLL.

Supported platforms include: current Microsoft® Windows® operating systems, Linux®version 2.6.39 or later (VCP drivers), Linux®version 2.6.32 or later (D2XX drivers), Mac OS® and Microsoft Windows CE® version 4.2 onwards.

2.2 Part Numbers

Part Number	Description
UM232H	Development module for FT232H

Table 1 - Part Numbers

2.3 Features

The UM232H has the following features:

- Based on the Single chip USB Hi-Speed FT232H device.
- USB 2.0 Hi-Speed (480Mbits/Second) and Full Speed (12Mbits/Second) compatible
- Entire USB protocol handled on the chip – No USB-specific firmware programming required.
- Small USB Type B connector common on many commercial devices
- USB bus or self-powered options.
- Asynchronous UART transfer data rate up to 12Mbaud.
- UART interface support for 7 or 8 data bits, 1 or 2 stop bits and odd / even / mark / space / no parity.
- Fully assisted hardware or X-On / X-Off software handshaking.
- Auto-transmit buffer control for RS485 applications.
- Supports a half-duplex FT1248 interface with a bi-directional data bus (1, 2, 4 or 8 bits wide).
- Synchronous Serial (MPSSE) data rates of up to 30Mbps on JTAG, SPI and I2C
- Support for USB suspend and resume
- UHCI / OHCI / EHCI host controller compatible
- FTDI's royalty-free VCP and D2XX drivers eliminate the requirement for USB driver development in most cases.
- 1kByte receive and transmit buffers for high data throughput.
- Transmit and receive LED drive signals.
- Adjustable receive buffer timeout.
- Synchronous and asynchronous bit bang mode interface options with RD# and WR# strobes.
- Support for USB suspend and resume.
- Integrated 3.3V level converter for USB I/O.
- USB bulk transfer mode.
- +2.97V to +5.25V Single Supply Operation.
- Low operating and USB suspend current.
- Low USB bandwidth consumption.
- -40°C to +85°C operating temperature range
- Reduce development time
- Rapid integration into existing systems

3 FT232H Features and Enhancements

3.1 Key Features

USB Hi-Speed to UART/FIFO Interface. The FT232H provides a USB 2.0 Hi-Speed (480Mbits/s) to flexible and configurable UART/FIFO Interfaces.

Functional Integration. The FT232H integrates a USB protocol engine, which controls the physical Universal Transceiver Macrocell Interface (UTMI) and handles all aspects of the USB 2.0 Hi-Speed interface. The FT232H includes an integrated +1.8V/3.3V Low Drop-Out (LDO) regulator. It also includes 1Kbytes Tx and Rx data buffers. The FT232H integrates the entire USB protocol on a chip with no firmware required.

MPSSE. Multi-Protocol Synchronous Serial Engines (MPSSE), capable of speeds up to 30 Mbits/s, provides flexible synchronous interface configurations.

FT1248 interface. The FT232H supports a half-duplex FT1248 interface with a bi-directional data bus interface that can be configured as 1, 2, 4 or 8-bits wide and this enables the flexibility to expand the size of the data bus to 8 pins. The FT1248 interface provides flexible data communication between an FT232H FT1248 slave and an external FT1248 master. The FT1248 interface consists of four signals called –

- **MIOSIO,** the bi-directional data lines between the FT232H and an external master controller,
- **SCLK**, which is the external clock, input for latching data in or out the device at frequency up to 30MHz,
- **SS_N** Slave select input
- **MISO,** which is the Master In Slave Out is an output from the FT232H in FT1248 mode.
  An external FT1248 master selects one of the FT1248 slave devices or enables the interface by pulling the Slave select input (**SS_N**) to logic 0. The FT1248 mode can be configured via the EEPROM settings with the free utility called FT_Prog , which can be downloaded from the FTDI utilities page. For further details about FT1248 mode, refer to FT232H datasheet and AN_167 application note.

Data Transfer rate. The FT232H supports a data transfer rate up to 12 Mbaud when configured as an RS232/RS422/RS485 UART interface or up to 40 Mbytes/second over a synchronous 245 parallel FIFO interface or up to 8 Mbyte/Sec over an asynchronous 245 FIFO interface.

Latency Timer. A feature of the driver used as a timeout to transmit short packets of data back to the PC. The default is 16ms, but it can be altered between 0ms and 255ms.

Bus (ACBUS) functionality, signal inversion and drive strength selection. There are 11 configurable ACBUS I/O pins. These configurable options are:

1. **TXDEN** - transmit enable for RS485 designs.
2. **PWREN#** - Power control for high power, bus powered designs.
3. **TXLED#** - for pulsing an LED upon transmission of data.
4. **RXLED#** - for pulsing an LED upon receiving data.
5. **TX&RXLED#** - which will pulse an LED upon transmission OR reception of data**.**
6. **SLEEP#** - indicates that the device going into USB suspend mode.
7. **CLK30 / CLK15 / CLK7.5 -** 30MHz, 15MHz and 7.5MHz clock output signal options.
8. **TriSt-PU** – Input pulled up, not used
9. **DRIVE 1** – Output driving high
10. **DRIVE 0** - Output driving low
11. **I/O mode** – ACBUS Bit Bang

The ACBUS pins can also be individually configured as GPIO pins, similar to asynchronous bit bang mode. It is possible to use this mode while the UART interface is being used, thus providing up to 4 general purpose I/O pins which are available during normal operation.
The ACBUS lines can be configured with any one of these input/output options by setting bits in the external EEPROM.

Multi-Purpose UART/FIFO Controllers. The FT232H has one independent Serial/FIFO Controller. This controls the UART data, 245 FIFO data, Fast Serial (opto isolation) or Bit-Bang mode that can be selected by SETUP (SetBitMode) command. Each Multi-Purpose UART/FIFO Controller also contains an MPSSE (Multi-Protocol Synchronous Serial Engine). Using this MPSSE, the Multi-Purpose Serial/FIFO Controller can be configured under software command, to have one of the MPSSE interfaces (SPI, I^2C, and JTAG).

USB Protocol Engine and FIFO control. The USB Protocol Engine controls and manages the interface between the UTMI PHY and the FIFOs of the chip. It also handles power management and the USB protocol specification.

Port FIFO TX Buffer (1Kbytes). Data from the Host PC is stored in these buffers to be used by the Multi-purpose UART/FIFO controllers. This is controlled by the USB Protocol Engine and FIFO control block.

Port FIFO RX Buffer (1Kbytes). Data from the Multi-purpose Serial/FIFO controllers is stored in these blocks to be sent back to the Host PC when requested. This is controlled by the USB Protocol Engine and FIFO control block.

RESET Generator – The integrated Reset Generator Cell provides a reliable power-on reset to the device internal circuitry at power up. The RESET# input pin allows an external device to reset the FT232H. RESET# should be tied to VCCIO (+3.3V) if not being used.

Baud Rate Generators – The Baud Rate Generators provides an x16 or an x10 clock input to the UART's from a 120MHz reference clock and consists of 14-bit pre-scaler and 4 register bits, which provide fine-tuning of the baud rate (used to divide by a number plus a fraction). This determines the Baud Rate of the UART, which is programmable from 183 baud to 12 Mbaud. See FTDI application note AN_120 for more details.

EEPROM Interface. If the external EEPROM is fitted, the FT232H can be configured as an asynchronous serial UART (default mode), parallel FIFO (245) mode, FT1248, fast serial (opto isolation) or CPU-Style FIFO. The EEPROM should be a 16 bit wide configuration such as a 93LC56B or equivalent capable of a 1Mbit/s clock rate at VCCIO = +2.97V to 3.63V. The EEPROM is programmable in-circuit over USB using a utility program called FT_Prog available from FTDI web site.

+1.8/3.3V LDO Regulator. The +3.3/+1.8V LDO regulator generates +1.8 volts for the core and the USB transceiver cell and +3.3V for the IO and the internal PLL and USB PHY power supply.

UTMI PHY. The Universal Transceiver Macrocell Interface (UTMI) physical interface cell. This block handles the Full speed / Hi-Speed SERDES (serialise – deserialise) function for the USB TX/RX data. It also provides the clocks for the rest of the chip. A 12 MHz crystal must be connected to the OSCI and OSCO pins or 12 MHz Oscillator must be connected to the OSCI, and the OSCO is left unconnected. A 12K Ohm resistor should be connected between REF and GND on the PCB.

The UTMI PHY functions include:

- Supports 480 Mbit/s "Hi-Speed" (HS)/ 12 Mbit/s "Full Speed" (FS).
- SYNC/EOP generation and checking
- Data and clock recovery from serial stream on the USB.
- Bit-stuffing/unstuffing; bit stuff error detection.
- Manages USB Resume, Wake Up and Suspend functions.
- Single parallel data clock output with on-chip PLL to generate higher speed serial data clocks.

4 UM232H Pin Out and Signal Descriptions

4.1 UM232H Pin Out

The signal labels and pin designators for each pin of the UM232H is illustrated in Figure 2.

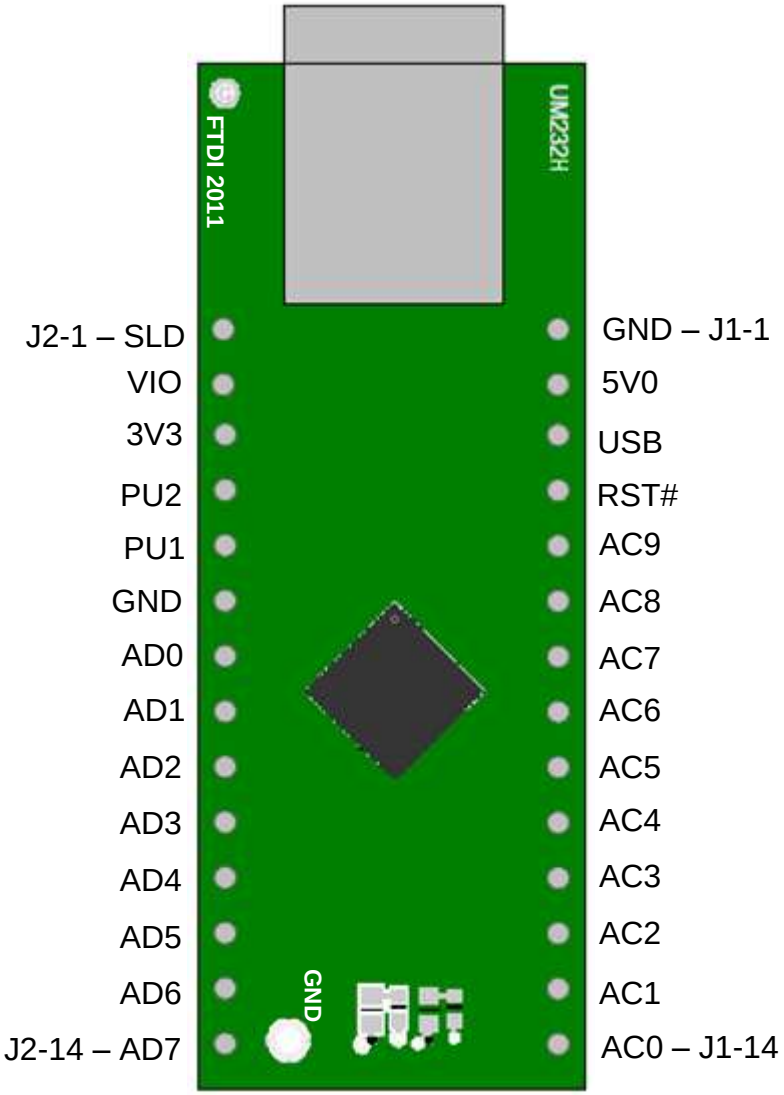

Figure 2 – UM232H USB to Serial/FIFO Development Module

4.2 Signal Descriptions

Pins marked * are EEPROM selectable

FT232H										
Pin		Pin functions (depends on configuration)								
Pin #	Pin Name	ASYNC Serial (RS232)	SYNC 245 FIFO	STYLE ASYNC 245 FIFO	ASYNC Bit-bang	SYNC Bit-bang	MPSSE	Fast Serial interface	CPU Style FIFO	FT1248
13	ADBUS 0	TXD	D0	D0	D0	D0	TCK/SK	FSDI	D0	MIOSI0
14	ADBUS 1	RXD	D1	D1	D1	D1	TDI/DO	FSCLK	D1	MIOSI1
15	ADBUS 2	RTS#	D2	D2	D2	D2	TDO/DI	FSDO	D2	MIOSI2
16	ADBUS 3	CTS#	D3	D3	D3	D3	TMS/CS	FSCTS	D3	MIOSI3
17	ADBUS 4	DTR#	D4	D4	D4	D4	GPIOL0	** TriSt-UP	D4	MIOSI4
18	ADBUS 5	DSR#	D5	D5	D5	D5	GPIOL1	** TriSt-UP	D5	MIOSI5
19	ADBUS 6	DCD#	D6	D6	D6	D6	GPIOL2	** TriSt-UP	D6	MIOSI6
20	ADBUS 7	RI#	D7	D7	D7	D7	GPIOL3	** TriSt-UP	D7	MIOSI7
21	ACBUS 0	* TXDEN	RXF#	RXF#	ACBUS0	ACBUS0	GPIOH0	** ACBUS0	CS#	SCLK
25	ACBUS 1	** ACBUS1	TXE#	TXE#	WRSTB#	WRSTB#	GPIOH1	** ACBUS1	A0	SS_N
26	ACBUS 2	** ACBUS2	RD#	RD#	RDSTB#	RDSTB#	GPIOH2	** ACBUS2	RD#	MISO
27	ACBUS 3	* RXLED#	WR#	WR#	ACBUS3	ACBUS3	GPIOH3	** ACBUS3	WR#	ACBUS3
28	ACBUS 4	* TXLED#	SIWU#	SIWU#	SIWU#	SIWU#	GPIOH4	SIWU#	SIWU#	ACBUS4
29	ACBUS 5	** ACBUS5	CLKOUT	ACBUS5	** ACBUS5	** ACBUS5	GPIOH5	** ACBUS5	** ACBUS5	ACBUS5
30	ACBUS 6	** ACBUS6	OE#	ACBUS6	ACBUS6	ACBUS6	GPIOH6	** ACBUS6	** ACBUS6	ACBUS6
31	ACBUS 7	PWRSAV #	PWRSAV #	PWRSAV #	PWRSAV #	PWRSAV #	*** GPIOH7	PWRSAV #	PWRSAV #	PWRSAV #
32	ACBUS 8	** ACBUS8	** ACBUS8	** ACBUS8	** ACBUS8	** ACBUS8	** ACBUS 8	** ACBUS8	** ACBUS8	ACBUS8
33	ACBUS 9	** ACBUS9	** ACBUS9	** ACBUS9	** ACBUS9	** ACBUS9	** ACBUS 9	** ACBUS9	** ACBUS9	ACBUS9

Table 2 – UM232H Signals

Pins marked ** default to tri-stated inputs with an internal 75KΩ (approx.) pull up resistor to VCCIO.

Pin marked *** default to GPIO line with an internal 75KΩ pull down resistor to GND. Using the EEPROM this pin can be enabled USBVCC mode instead of GPIO mode.

Table 3 and 4 provides a description of the signals available on each pin of the UM232H module

Pin No.	Name	Type	Description
J1-1	GND	PWR	Module Ground Supply Pins
J1-2	5V0	Input	+5.0V or +3.3V power supply input.
J1-3	USB	Output	5V Power output USB port. For a low power USB bus powered design, up to 100mA can be sourced from the 5V supply on the USB bus. A maximum of 500mA can be sourced from the USB bus in a high power USB bus powered design.
J1-4	RST#	Input	Can be used by an external device to reset the FT232H. If not required can be left unconnected, or pulled up to VCCIO
J1-5	AC9	I/O	Configurable ACBUS I/O Pin. Function of this pin is configured by EEPROM. The default configuration is TriSt-PU. See ACBUS Signal Options, Table 4.3
J1-6	AC8	I/O	Configurable ACBUS I/O Pin. Function of this pin is configured by EEPROM. The default configuration is TriSt-PU. See ACBUS Signal Options, Table 4.3
J1-7	AC7	I/O	Configurable ACBUS I/O Pin. Function of this pin is configured by EEPROM. The default configuration is TriSt-PD. See ACBUS Signal Options, Table 4.3
J1-8	AC6	I/O	Configurable ACBUS I/O Pin. Function of this pin is configured by EEPROM. The default configuration is TriSt-PU. See ACBUS Signal Options, Table 4.3
J1-9	AC5	I/O	Configurable ACBUS I/O Pin. Function of this pin is configured by EEPROM. The default configuration is TriSt-PU. See ACBUS Signal Options, Table 4.3
J1-10	AC4	I/O	Configurable ACBUS I/O Pin. Function of this pin is configured by EEPROM. The default configuration is TriSt-PU. See ACBUS Signal Options, Table 4.3
J1-11	AC3	I/O	Configurable ACBUS I/O Pin. Function of this pin is configured by EEPROM. The default configuration is TriSt-PU. See ACBUS Signal Options, Table 4.3
J1-12	AC2	I/O	Configurable ACBUS I/O Pin. Function of this pin is configured by EEPROM. The default configuration is TriSt-PU. See ACBUS Signal Options, Table 4.3
J1-13	AC1	I/O	Configurable ACBUS I/O Pin. Function of this pin is configured by EEPROM. The default configuration is TriSt-PU. See ACBUS Signal Options, Table 4.3
J1-14	AC0	I/O	Configurable ACBUS I/O Pin. Function of this pin is configured by EEPROM. The default configuration is TriSt-PU. See ACBUS Signal Options, Table 4.3

Table 3 – UM232H Connector J1 Signal Description

Pin No.	Name	Type	Description
J2-1	SLD	Shield to GND	USB Cable Shield shorted to GND via a 0Ω resistor.
J2-2	VIO	PWR	1.8 to +3.3V supply to the UART Interface and ACBUS I/O pins
J2-3	3V3	Output/Input	+3.3V output from the integrated L.D.O. regulator if the UM232H is running on 5V self or bus powered designs. Therefore, this pin can be used to supply the FT232HL's VCCIO pin by connecting this pin to J2-2 (VIO). This pin can also be an input if the UM232H is running on 3.3V self-powered designs.
J2-4	PU2	Control	Pull up resistor pin connection 1. Connect to J1-3 (USB) in a self-powered configuration.
J2-5	PU1	Control	Pull up resistor pin connection 2. Connect to J1-4 (RST#) in a self-powered configuration.
J2-6	GND	PWR	Module Ground Supply Pins
J2-7	AD0	Output	Configurable Output Pin, the default configuration is Transmit Asynchronous Data Output / Handshake Signal..
J2-8	AD1	Input	Configurable Input Pin, the default configuration is Receiving Asynchronous Data Input / Handshake Signal..
J2-9	AD2	Output	Configurable Output Pin, the default configuration is Request to Send Control Output / Handshake Signal.
J2-10	AD3	Input	Configurable Input Pin, the default configuration is Clear To Send Control Input / Handshake Signal.
J2-11	AD4	Output	Configurable Output Pin, the default configuration is Data Terminal Ready Control Output / Handshake Signal.
J2-12	AD5	Input	Configurable Input Pin, the default configuration is Data Set Ready Control Input / Handshake Signal.
J2-13	AD6	Input	Configurable Input Pin, the default configuration is Data Carrier Detect Control Input / Handshake Signal..
J2-14	AD7	Input	Configurable Input Pin, the default configuration is RI#, Ring Indicator Control Input/ Handshake Signal. When remote wake up is enabled in the EEPROM taking RI# low >20ms can be used to resume the PC USB host controller from suspend.

Table 4 – UM232H Connector J2 Signal Description

Note: When used in Input Mode, the input pins are pulled to VCCIO via internal 75kΩ (approx.) resistors. These pins can be programmed to gently pull low during USB suspend (PWREN# = "1") by setting an option in the EEPROM.

4.3 ACBUS Signal Options

The table below describes the EEPROM options which can be configured on the ACBUS I/O pins using the software utility FT_PROG (which can be downloaded from the FTDI utilities page) The default EEPROM configuration is described in section 9.

ACBUS Signal Option	Available On ACBUS Pin	Description
TXDEN	ACBUS0, ACBUS1, ACBUS2, ACBUS3, ACBUS4, ACBUS5, ACBUS6, ACBUS8, ACBUS9	TXDEN = (TTL level). Used with RS485 level converters to enable the line driver during data transmit. TXDEN is active from one-bit time before the start bit is transmitted on TXD until one-bit time after the last stop bit.
*PWREN#	ACBUS0, ACBUS1, ACBUS2, ACBUS3, ACBUS4, ACBUS5, ACBUS6, ACBUS8, ACBUS9	Output is low after the device has been configured by USB, then high during USB suspend mode. This output can be used to control power to external logic P-Channel logic level MOSFET switch. Enable the interface pull-down option when using the PWREN# in this way.*
TXLED#	ACBUS0, ACBUS1, ACBUS2, ACBUS3, ACBUS4, ACBUS5, ACBUS6, ACBUS8, ACBUS9	TXLED = Transmit signalling output. Pulses low when transmitting data (TXD) to the external device. This can be connected to an LED.
RXLED#	ACBUS0, ACBUS1, ACBUS2, ACBUS3, ACBUS4, ACBUS5, ACBUS6, ACBUS8, ACBUS9	RXLED = Receive signalling output. Pulses low when receiving data (RXD) from the external device. This can be connected to an LED.
TX&RXLED#	ACBUS0, ACBUS1, ACBUS2, ACBUS3, ACBUS4, ACBUS5, ACBUS6, ACBUS8, ACBUS9	LED drive – pulses low when transmitting or receiving data from or to the external device. For more details, refer to the FT232H datasheet.
SLEEP#	ACBUS0, ACBUS1, ACBUS2, ACBUS3, ACBUS4, ACBUS5, ACBUS6, ACBUS8, ACBUS9	Goes low during USB suspend mode. Typically used to power down an external TTL to RS232 level converter IC in USB to RS232 converter designs.
**CLK30	ACBUS0, ACBUS5, ACBUS6,ACBUS8, ACBUS9	30MHz Clock output.
**CLK15	ACBUS0, ACBUS5, ACBUS6,ACBUS8, ACBUS9	15MHz Clock output.
**CLK7.5	ACBUS0, ACBUS5, ACBUS6,ACBUS8, ACBUS9	7.5MHz Clock output.
TriSt-PU	ACBUS0, ACBUS1, ACBUS2, ACBUS3, ACBUS4, ACBUS5, ACBUS6, ACBUS8, ACBUS9	Input Pull Up
DRIVE 1	ACBUS0, ACBUS5, ACBUS6,ACBUS8, ACBUS9	Output High
DRIVE 0	ACBUS0, ACBUS1, ACBUS2, ACBUS3, ACBUS4, ACBUS5, ACBUS6, ACBUS8, ACBUS9	Output Low
I/O mode	ACBUS5, ACBUS6,ACBUS8, ACBUS9	ACBUS Bit Bang

Table 5 – ACBUS Signal Option

* A 10kΩ resistor pull up is also recommended.
**When in USB suspend mode, the output clocks are also suspended.

5 Module Dimensions

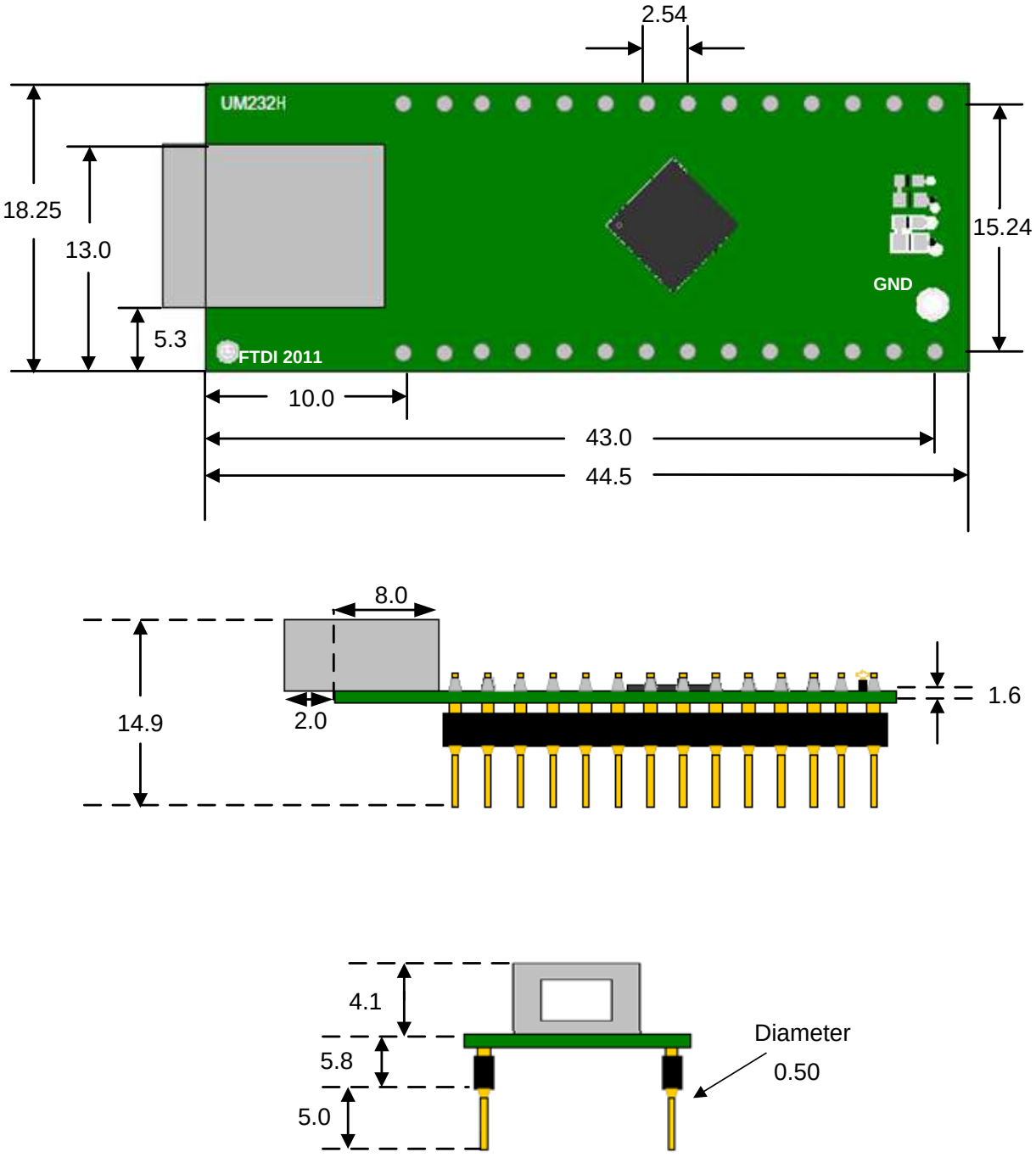

Figure 3 – UM232H Module Dimensions

All dimensions are in millimetres.

The UM232H module uses exclusively lead free components, and are fully compliant with European Union directive 2002/95/EC.

6 FT232H Device Characteristics and Ratings

6.1 DC Characteristics

The I/O signal levels are +3.3V, and all IO pins are +5V tolerant (except the USB PHY pins).

DC Characteristics (Ambient Temperature = -40°C to +85°C)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
VCCIO*	VCCIO Operating Supply Voltage	2.97		3.63	V	Cells are 5V tolerant
VREGIN	VREGIN Voltage regulator Input	3.6	5	5.5	V	+5V Supply
Ireg	Regulator Output Current			100	mA	+3V3 Output
Icc_{5v0}	UM232H current drawn	2	62		mA	+5V Supply
Icc_{3v3}	UM232H current drawn	1.2	59		mA	+3.3V Supply

Table 6 – Operating Voltage & Current (except PHY)

Note: Failure to connect all VCCIO pins the device will have unpredictable behaviour.

For the electrical characteristics of the FT232H device, please refer to the FT232H datasheet.

7 Module Configurations

The UM232H Module can be configured as USB Bus-Powered or USB Self-Powered. This section describes how to configure the UM232H for a number of different power supply arrangements.

7.1 BUS Powered Configuration

Bus powered configuration, where the +5V supply that powers the module is sourced from the USB bus, and the 3V3 regulator output powers the core of the FT232H.

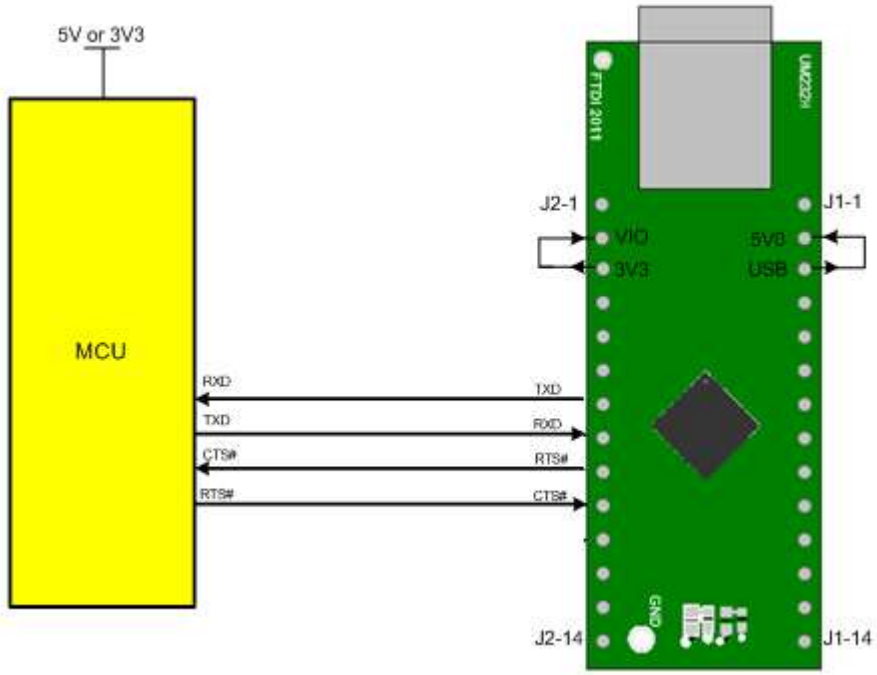

Figure 4 – Bus Powered Configuration

Figure 4 illustrates the UM232H in a typical USB bus powered design configuration, which consists of two connections, a J1-2 to J1-3 connection and a J2-2 to J2-3 connection.

Connecting J1-2 (5V0) to J1-3 (USB) takes the power from the VBUS pin (J1-3) and supplies it to the on chip voltage regulator input of the FT232H via pin 5V0 (J1-2).

Connecting J2-2 (VIO) (power input for core of the FT232H) and J2-3 (3V3) (power output from the FT232H) powers the VCCIO, VPLL and VPHY pins of the FT232H chip.

A USB Bus Powered device gets its power from the USB bus. Basic rules for USB Bus power devices are as follows –

I. On plug-in to USB, the device must draw no more than 100mA.
II. On USB Suspend the device must draw no more than 500µA.
III. A Bus Powered High Power USB Device (one that draws more than 100mA) should use PWREN# to keep the current below 100mA on plug-in and 500µA on USB suspend.
IV. A device that consumes more than 100mA cannot be plugged into a USB Bus Powered Hub.
V. No device can draw more that 500mA from the USB Bus.

Interfacing the UM232H module to a microcontroller (MCU), or other logic for a bus powered design would be done in exactly the same way as for Self-Powered designs (see Section 7.3), except that the MCU or external logic would take its power supply from the USB bus (either the 5V on the USB pin, or 3.3V on the 3V3 pin).

7.2 USB Bus Powered with Power Switching Configuration

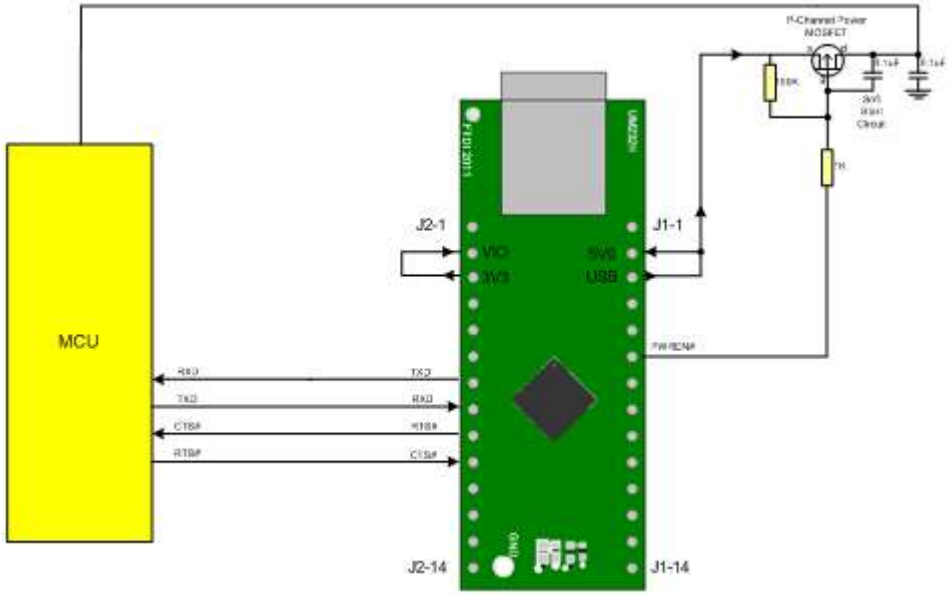

Figure 5 – Bus Powered with Power Switching Configuration

USB Bus Powered circuits need to be able to power down in USB suspend mode in order to meet the <=500µA total USB suspend current requirement (including external logic). Some external hardware can power itself down into a low current state by monitoring the PWREN# signal. For external logic that cannot power itself down in this way the FT232H provides a simple but effective way of turning off power to external circuitry during USB suspend.

Figure 5 shows how to use a discrete P-Channel Logic Level MOSFET to control the power to external logic circuits. A suitable device would be an International Rectifier (www.irf.com) IRLML6402, or equivalent. It is recommended that a "soft start" circuit consisting of a 1kΩ series resistor and a 0.1µF capacitor be used to limit the current surge when the MOSFET turns on. Without the soft start circuit there is a danger that the transient power surge of the MOSFET turning on will reset the FT232H, or the USB host / hub controller. The values used here allow attached circuitry to power up with a slew rate of ~12.5V per millisecond, in other words the output voltage will transition from GND to 5V in approximately 400 microseconds.

A 100kΩ resistor to VBUS creates a week pull up on the gate, this can prevent current from flowing through the transistor during a power up or power down of the FT232H. Alternatively, a dedicated power switch I.C. with inbuilt "soft-start" can be used instead of a MOSFET. A suitable power switch I.C. for such an application would be a Micrel (www.micrel.com) MIC2025-2BM or equivalent.

Please note the following points in connection with power controlled designs:

i) The logic to be controlled must have its own reset circuitry so that it will automatically reset itself when power is applied on coming out of suspend.

ii) Set the Pull-down on Suspend option in the internal EEPROM.

iii) One of the ACBUS pins should be configured as PWREN# in the internal EEPROM, and should be used to switch the power supply to the external circuitry.

iv) For USB high-power bus powered device (one that consumes greater than 100mA, and up to 500mA of current from the USB bus), the power consumption of the device should be set in the max power field in the internal EEPROM. A high-power bus powered device must use this descriptor in the internal EEPROM to inform the system of its power requirements.

v) For 3.3V power controlled circuits, the FT232H's VIO pin must not be powered down with the external circuitry (the PWREN# signal gets its VCC supply from VIO). Either connect the power switch between the output of the 3.3V regulator and the external 3.3V logic or power VIO from the 3V3 pin of the FT232H.

7.3 Self Powered Configuration

7.3.1 Self-Powered Configuration with 3V3 I/O & running on +5V external supply

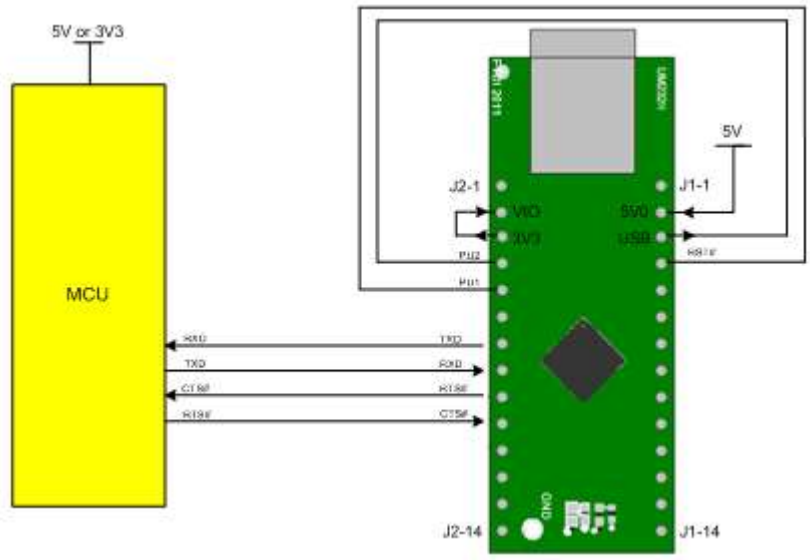

Figure 6 – Self-Powered Configuration – 5V0 External Supply

Figure 6 illustrates the UM232H in a typical USB Self-Powered configuration. An external supply +5.0V is connected to the module's 5V0 pin. J2-2 (VIO) is also connected to J2-3 (3V3) to supply the VCCIO supply from the on board regulator but a separate supply could have been used.

A USB Self Powered device gets its power from its own power supply and does not draw current from the USB bus. The basic rules for USB Self powered devices are as follows:

i) A Self Powered device should not force current down the USB bus when the USB Host or Hub Controller use powered down.

ii) A Self Powered Device can use as much current as it likes during normal operation and USB suspend as it has its own power supply.

iii) A Self Powered Device can be used with any USB Host and both Bus and Self Powered USB Hub. In this case, the power descriptor in the internal EEPROM should be programmed to a value of zero (Self-Powered).

In order to meet requirement (i) the USB Power is used to control the RESET# Pin of the FT232H device. When the USB Host or Hub is powered up the internal 1.5kΩ resistor on USBDP is pulled up to 3.3V, thus identifying the devices as a full speed device to USB. When the USB Host or Hub Power is off, RESET# will go low and the device will be held in reset. As RESET# is low, the internal 1.5kΩ resistor will not be pulled up to 3.3V, so no current will be forced down USBDP via the 1.5kΩ pull-up resistor when the host or hub is powered down.

To do this J1-3 (USB) is connected to PU2 and PU1 is connected to J2-4 (RST#). Failure to do this may cause some USB host or hub controllers to power up erratically.

Note: When the FT232H is in reset, the UART interface pins all go tristate. These pins have internal 200kΩ pull-up resistors to VCCIO, so they will gently pull high unless driven by some external logic.

Figure 7 is also an example of interfacing the FT232H to a Microcontroller (MCU) UART interface. This example uses TXD and RXD for transmission and reception of data and RTS# / CTS# hardware handshaking.

Optionally, RI# can be connected to another I/O pin on the MCU and could be used to wake up the USB host controller from suspend mode. If the MCU is handling power management functions, then an ACBUS pin can be configured as PWREN# and should be connected to an I/O pin of the MCU.

An alternative to connecting the pull-up network to the Reset pin, to prevent current from flowing back the USB power bus line, is to connect the network ACBUS7 pin to achieve the same results but with additional benefits. A function called PWRSAV# is used to prevent current from flowing the USB line in the same way as connecting the reset to the a pull-up network. However, the PWRSAV# function has the additional feature of being able to put FT232H into sleep mode when the USB host is powered down. There is one trade of o using reset instead of PWRSAV#, in MPSSE mode the ACBUS7 pin can be selected as a GPIO pin, using this pin from both PWRSAV# and GPIO mode can cause a conflict. PWRSAV# is enabled and disabled using the EEPROM, this function is disabled by default. Figure 7 illustrates an alternative USB Self-Power configuration.

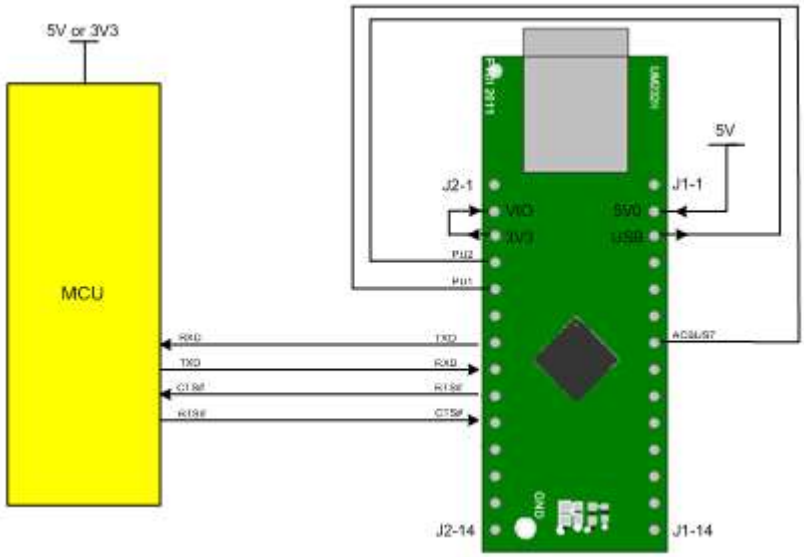

Figure 7 – Alternative Self-Powered Configuration – 5V0 External Supply

7.3.2 Self-Powered Configuration with 3V3 I/O & running on +3.3V external supply

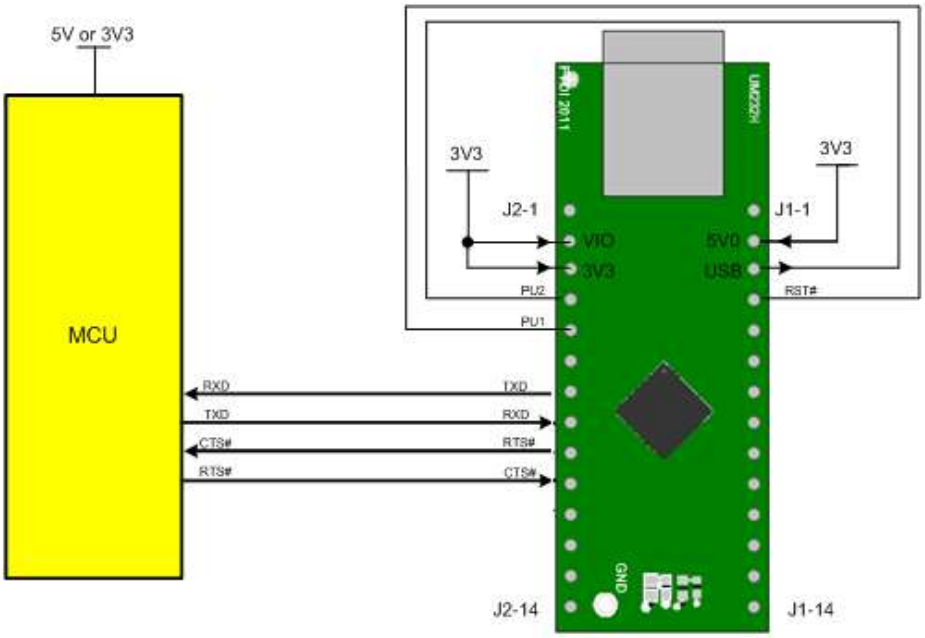

Figure 8 – Self-Powered Configuration – 3V3 External Supply

Figure 8 illustrates the UM232H in a typical USB Self-Powered configuration similar to Figure 7. The difference here is that the UM232H module is powered from an external 3.3V supply which is connected to the 5V0 (+3V3 power supply input can also be supplied to 5V0 pin), VIO and 3V3 pins of the modules. Please note that when the UM232H running from +3V3, the 3V3 pin becomes an input. The VIO and 3V3 pins connection provides 3V3 to the VCCIOs, VPLL and VPHY on the FT232H chip.

Similarly to the USB-Powered configuration an alternative configuration which utilized PWRSAV# can be implemented. Figure 8 illustrates this configuration.

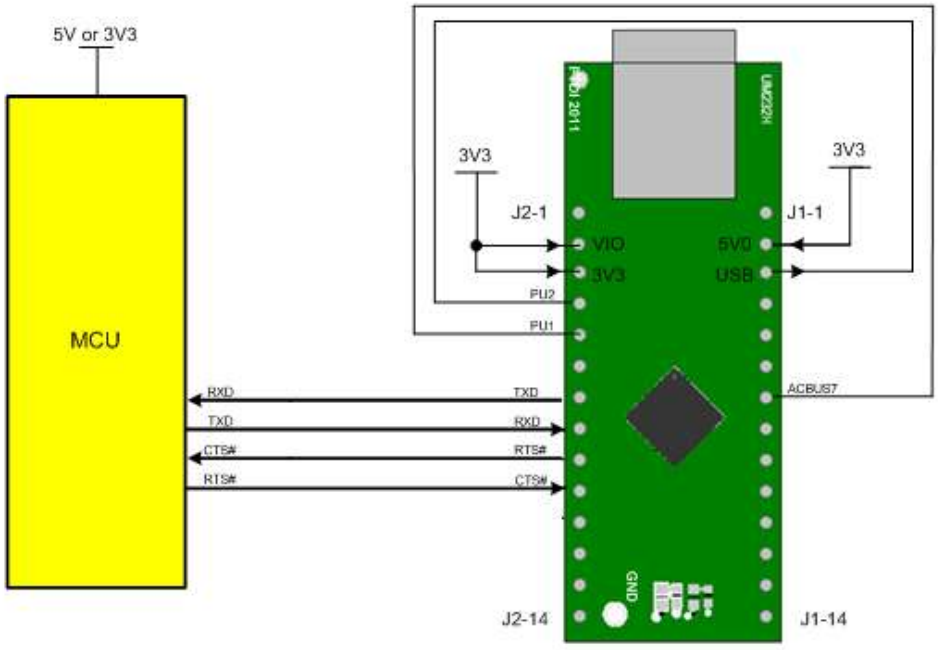

Figure 9 – Alternative Self-Powered Configuration – 3V3 External Supply

8 M232H Module Circuit Schematic

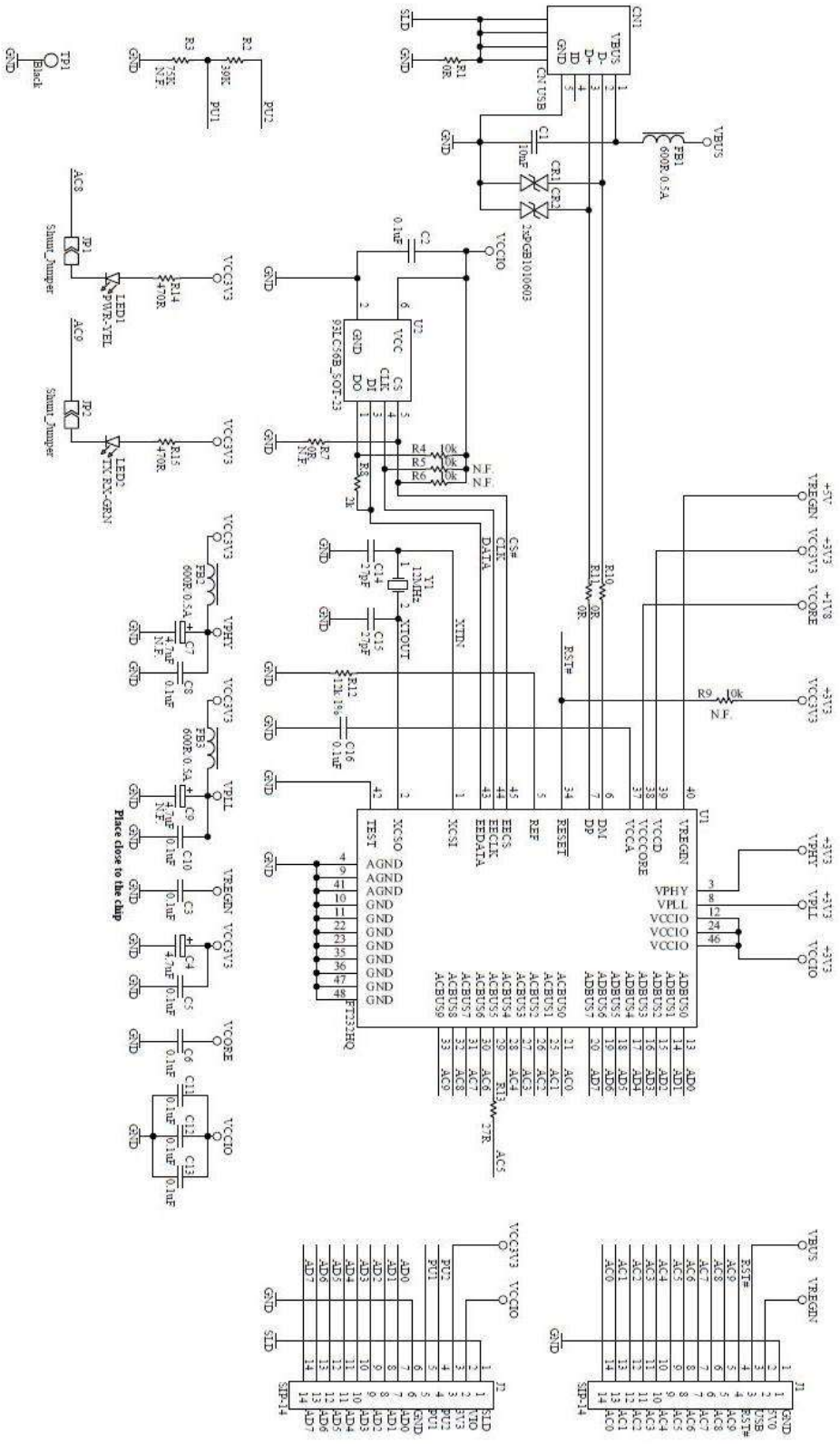

Figure 10 – Module Circuit Schematic

9 EEPROM Configuration

The FT232H uses an external EEPROM (on the UM232H module). This EEPROM can be programmed over USB using FT_Prog. The default settings of the EEPROM are shown in the following table:

Parameter	Value	Notes
USB Vendor ID (VID)	0403h	FTDI default VID (hex)
USB Product UD (PID)	6014h	FTDI default PID (hex)
bcd Device	009h	
Serial Number Enabled	Yes	
Serial Number	See Note	A unique serial number is generated and programmed into the EEPROM during device final test.
Pull down I/O Pins in USB Suspend	Disabled	Enabling this option will make the device pull down on the UART interface lines when in USB suspend mode (PWREN# is high).
Manufacturer Name	FTDI	
Product Description	UM232H	
Max Bus Power Current	90mA	
Power Source	Bus Powered	
Device Type	FT232H	
USB Version	0200	Returns USB 2.0 device description to the host.
Remote Wake Up	Enabled	Taking RI# low will wake up the USB host controller from suspend in approximately 20 ms.
High Current I/Os	Disabled	Enables the high drive level on the UART and ACBUS I/O pins.
Load VCP Driver	Enabled	Makes the device load the VCP driver interface for the device.
ACBUS0	TriSt-PU	Default configuration of ACBUS0 – Input pulled up
ACBUS1	TriSt-PU	Default configuration of ACBUS1 – Input pulled up
ACBUS2	TriSt-PU	Default configuration of ACBUS2 Input pulled up
ACBUS3	TriSt-PU	Default configuration of ACBUS3 – Input pulled up
ACBUS4	TriSt-PU	Default configuration of ACBUS4 – Input pulled up
ACBUS5	TriSt-PU	Default configuration of ACBUS5 – Input pulled up
ACBUS6	TriSt-PU	Default configuration of ACBUS6 – Input pulled up
ACBUS7	TriSt-PU	Default configuration of ACBUS7 – Input pulled down
ACBUS8	PWRENn	Default configuration of ACBUS8 – PWR LED
ACBUS9	TX&RXLED	Default configuration of ACBUS9 – Tx/Rx LED

Table 7 – Default Internal EEPROM Configuration

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Distributor and Sales Representatives

Please visit the Sales Network page of the FTDI Web site for the contact details of our distributor(s) and sales representative(s) in your country.

Appendix A – References

Document References

- FT232H Datasheet
- AN_167 – FT1248 Dynamic Parallel/Serial Interface Basics
- AN_120 – Aliasing VCP Baud Rates
- FT_Prog
- FTDI utilities
- www.irf.com
- www.micrel.com

Acronyms and Abbreviations

Terms	Description
CPU	Central Processing Unit
DLL	Dynamic Link Libraries
EHCI	Enhanced Host Controller Interface
EEPROM	Electrically Erasable Programmable Read Only Memory
FIFO	First In First Out
FPGA	Field Programmable Gate Array
IC	Integrated Circuit
I2C	Inter-Integrated Circuit
JTAG	Joint Test Action Group
LDO	Low Drop Out regulator
LED	Light Emitting Diode
MCU	Micro Controller
MPSSE	Multi-Protocol Synchronous Serial Engines
OHCI	Open Host Controller Interface
PLD	Programmable Logic Device
RoHS	Restriction of Hazardous Substances Directive
SPI	Serial Peripheral Interface
USB	Universal Serial Bus
UART	Universal Asynchronous Receiver Transmitter

UHCI	Universal Host Controller Interface
UTMI	Universal Transceiver Macrocell Interface
VCP	Virtual COM Port

Appendix B – List of Tables & Figures

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Appendix C – Revision History

Document Title: UM232H Single Channel USB Hi-Speed FT232H Development Module Datasheet

Document Reference No.: FT_000367

Clearance No.: FTDI# 198

Product Page: http://www.ftdichip.com/FTProducts.htm

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Revision	Changes	Date
Version 1.0	Initial Release	2011-02-14
Version 1.1	Added additional dimensions; Updated EEPROM default current limit	2011-03-21
Version 1.2	Modified details about ACBUS7; Updated Schematics	2011-04-18
Version 1.21	Updated Section 2.1 Linux Version	2012-01-09
Version 1.3	Updated the pin define position of ADBUS in Figure 4, 5, 6, 7. 8 & 9	2012-07-09
Version 1.4	Updated Table 7; Updated Schematics	2017-11-08