

N-channel clamped 12.5 mΩ, 62 A, TO-220
fully protected MESH OVERLAY™ Power MOSFET

Features

Type	V_{DSS}	$R_{DS(on)}$ max	I_D
STP62NS04Z	Clamped	< 0.015 Ω	62 A

- 100% avalanche tested
- Low capacitance and gate charge
- 175 °C maximum junction temperature

Application

- Switching applications

Description

Fully clamped MOSFET is produced by using ST's most advanced MESH OVERLAY™ process based on strip layout. The inherent benefits of this new technology coupled with the extra clamping capabilities make this product particularly suitable for the harshest operating conditions such as those encountered in the automotive environment. It is also recommended for any other application requiring extra ruggedness.

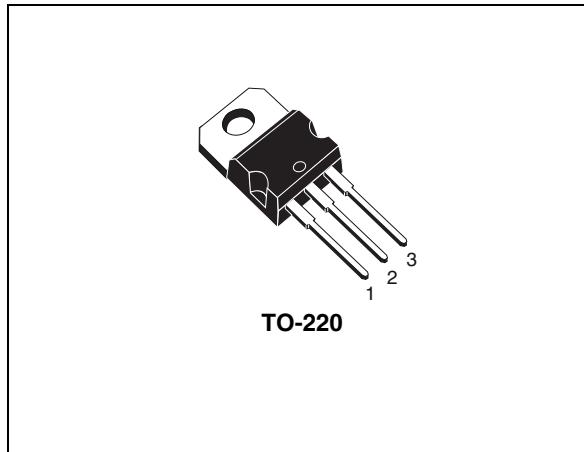
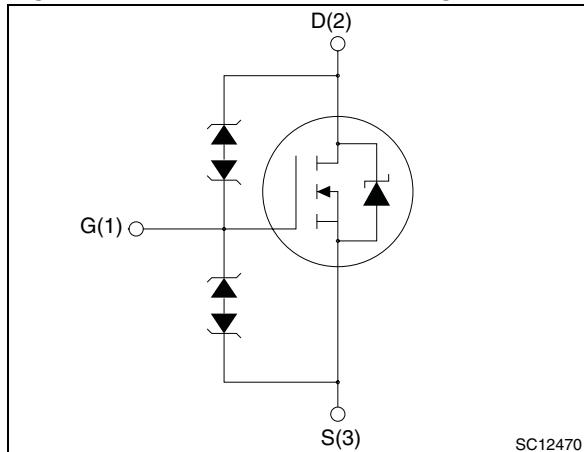


Figure 1. Internal schematic diagram



SC12470

Table 1. Device summary

Order code	Marking	Package	Packaging
STP62NS04Z	P62NS04Z	TO-220	Tube

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
2.1	Electrical characteristics (curves)	6
3	Test circuits	8
4	Package mechanical data	9
5	Revision history	11

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	Clamped	V
V_{GS}	Gate-source voltage	Clamped	V
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	62	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	37.5	A
I_{DG}	Drain gate current (continuous)	± 50	mA
I_{GS}	Gate source current (continuous)	± 50	mA
$I_{DM}^{(1)}$	Drain current (pulsed)	248	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	110	W
	Derating factor	0.74	W/ $^\circ\text{C}$
$dv/dt^{(2)}$	Peak diode recovery voltage slope	8	V/ns
$E_{AS}^{(3)}$	Single pulse avalanche energy	500	mJ
V_{ESD}	ESD (HBM - $C = 100 \text{ pF}$, $R = 1.5 \text{ k}\Omega$)	8	V
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 175	$^\circ\text{C}$

1. Pulse width limited by safe operating area
2. $I_{SD} \leq 40 \text{ A}$, $di/dt \leq 100 \text{ A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$
3. Starting $T_J = 25^\circ\text{C}$, $I_D = 20 \text{ A}$, $V_{DD} = 20 \text{ V}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thj-c}	Thermal resistance junction-casemax	1.36	$^\circ\text{C}/\text{W}$
R_{thj-a}	Thermal resistance junction-ambient max	62.5	$^\circ\text{C}/\text{W}$
T_I	Maximum lead temperature for soldering purpose	300	$^\circ\text{C}$

2 Electrical characteristics

($T_{CASE}=25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}, V_{GS} = 0$	33			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 16\text{ V}$			10	μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 10\text{ V}$			10	μA
V_{GSS}	Gate-source breakdown voltage	$I_{GS} = 100\text{ }\mu\text{A}$	18			V
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2		4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}, I_D = 30\text{ A}$		12.5	15	$\text{m}\Omega$

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15\text{ V}, I_D = 30\text{ A}$	-	20		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25\text{ V}, f = 1\text{ MHz}, V_{GS} = 0$	-	1330 420 135		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 20\text{ V}, I_D = 40\text{ A}$ $V_{GS} = 10\text{ V}$	-	34 10 11.5	47	nC nC nC

1. Pulsed: pulse duration=300 μs , duty cycle 1.5%

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	$V_{DD} = 20\text{ V}, I_D = 20\text{ A}, R_G = 4.7\text{ }\Omega, V_{GS} = 10\text{ V}$ <i>Figure 14 on page 8</i>	-	13 104 41 42	-	ns ns ns ns
$t_{r(V_{off})}$ t_f t_c	Off-voltage rise time Fall time Cross-over time	$V_{clamp} = 30\text{ V}, I_D = 40\text{ A}$ $R_G = 4.7\text{ }\Omega, V_{GS} = 10\text{ V}$ <i>Figure 14 on page 8</i>	-	30 54 90	-	ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current		-		62	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		248	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 62 \text{ A}, V_{GS} = 0$	-		1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 40 \text{ A},$ $di/dt = 100 \text{ A}/\mu\text{s},$ $V_{DD} = 20 \text{ V}, T_J = 150 \text{ }^\circ\text{C}$ <i>Figure 16 on page 8</i>	-	45 65 2.9		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 μ s, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

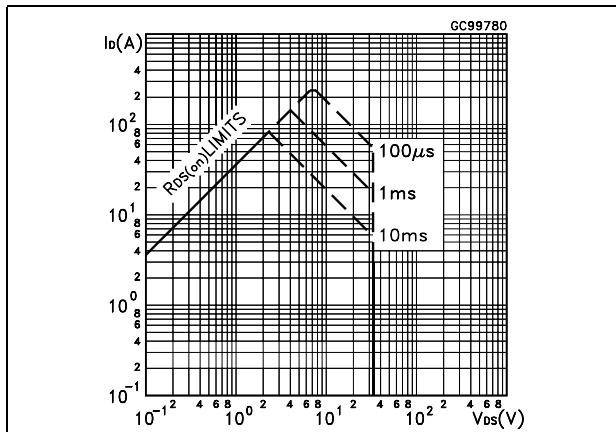


Figure 3. Thermal impedance

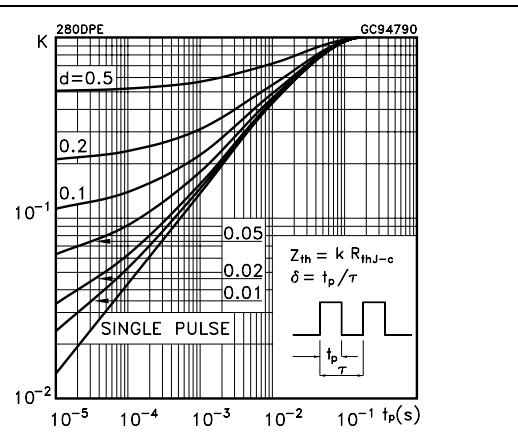


Figure 4. Output characteristics

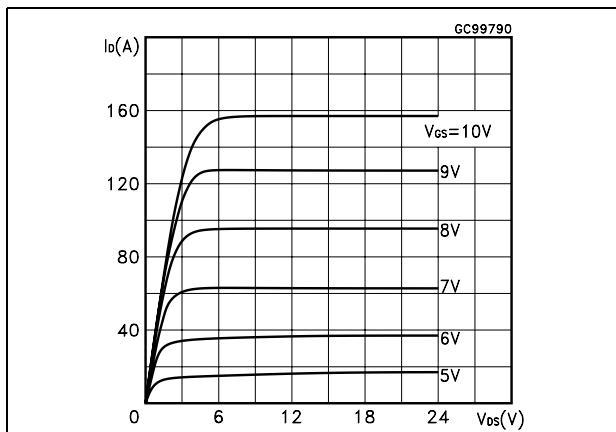


Figure 5. Transfer characteristics

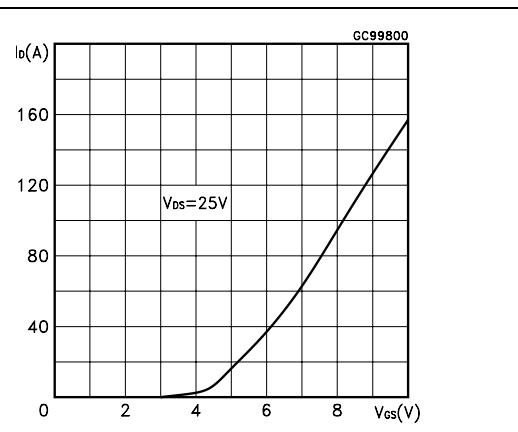


Figure 6. Transconductance

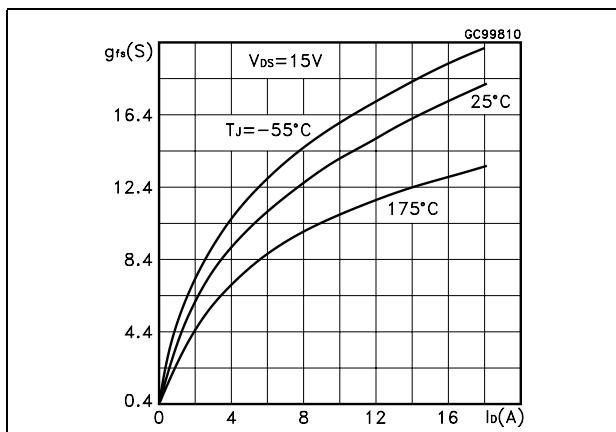


Figure 7. Static drain-source on resistance

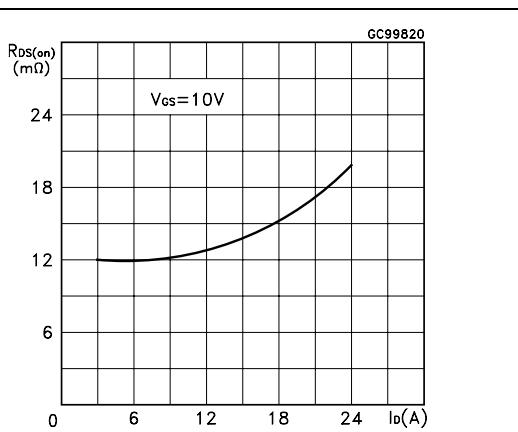


Figure 8. Gate charge vs gate-source voltage

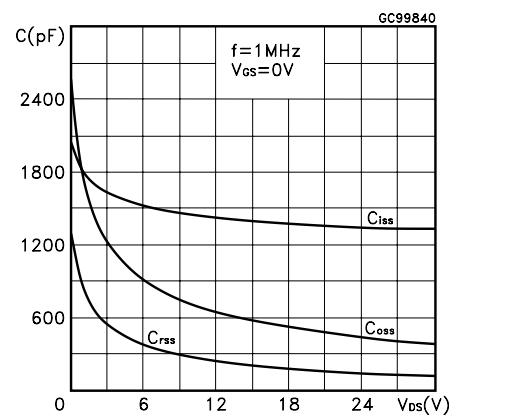
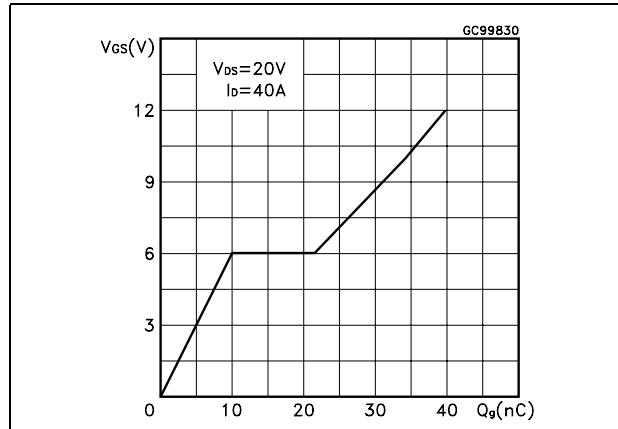


Figure 10. Normalized gate threshold voltage vs temperature

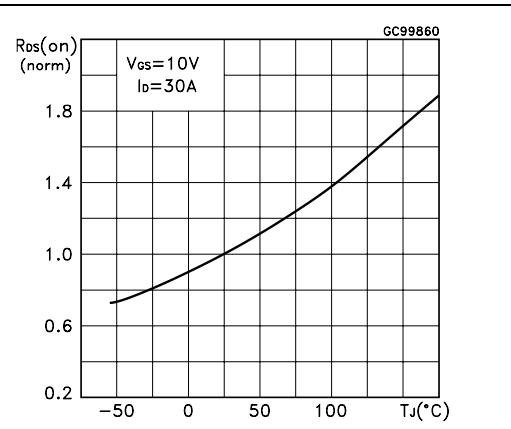
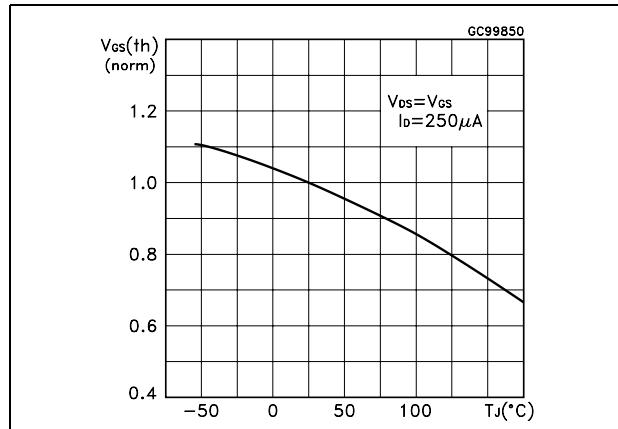
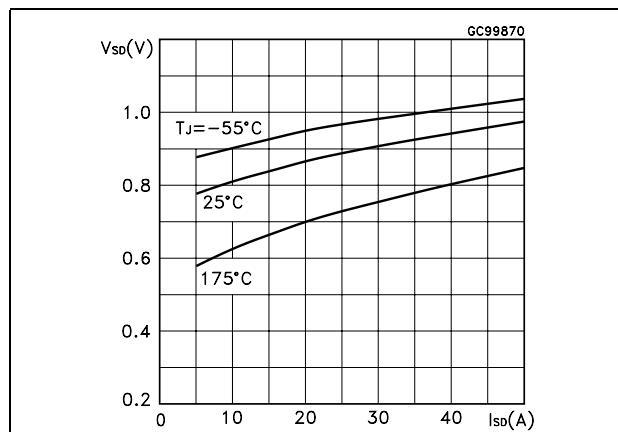
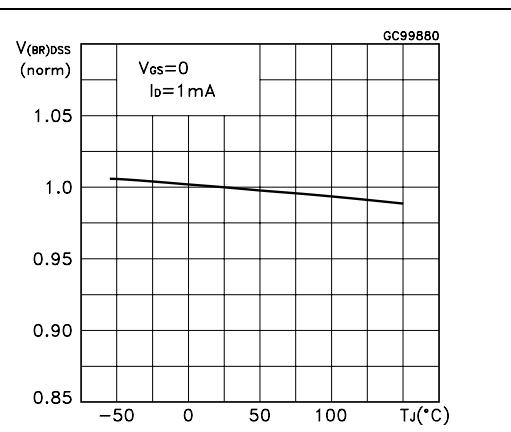


Figure 12. Source-drain diode forward characteristics

Figure 13. Normalized B_{VDSS} vs temperature

3 Test circuits

Figure 14. Switching times test circuit for resistive load

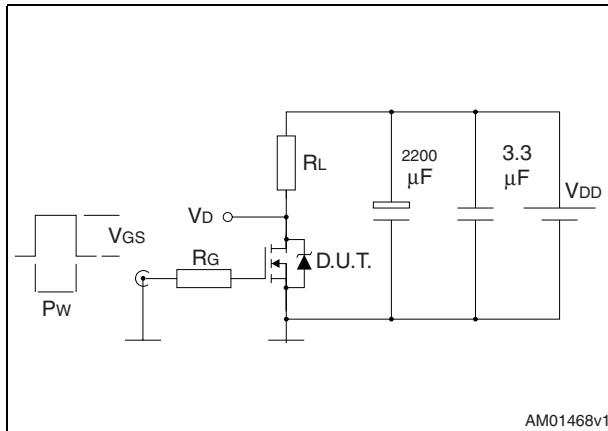


Figure 15. Gate charge test circuit

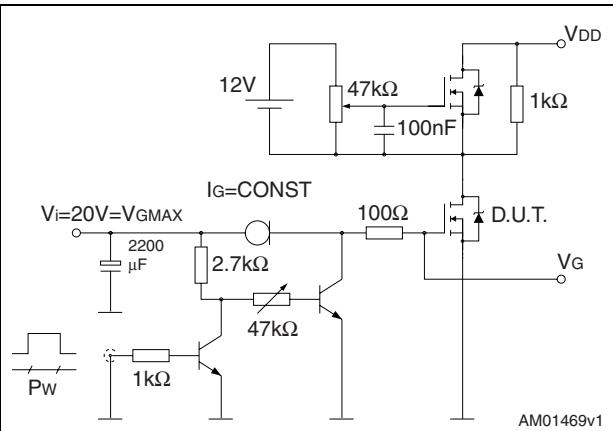


Figure 16. Test circuit for inductive load switching and diode recovery times

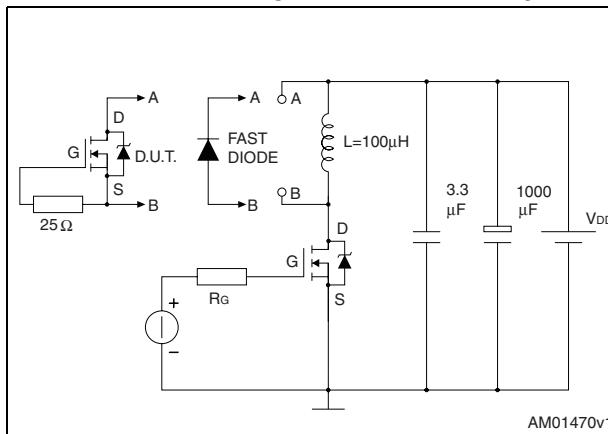


Figure 17. Unclamped inductive load test circuit

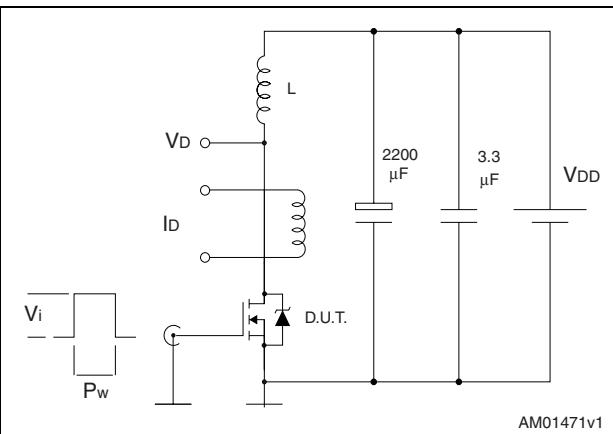
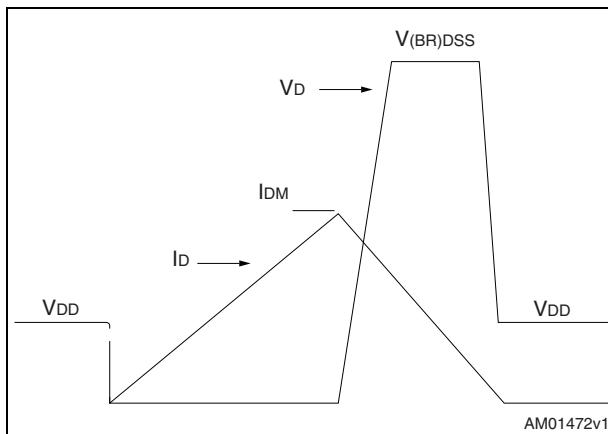


Figure 18. Unclamped inductive waveform

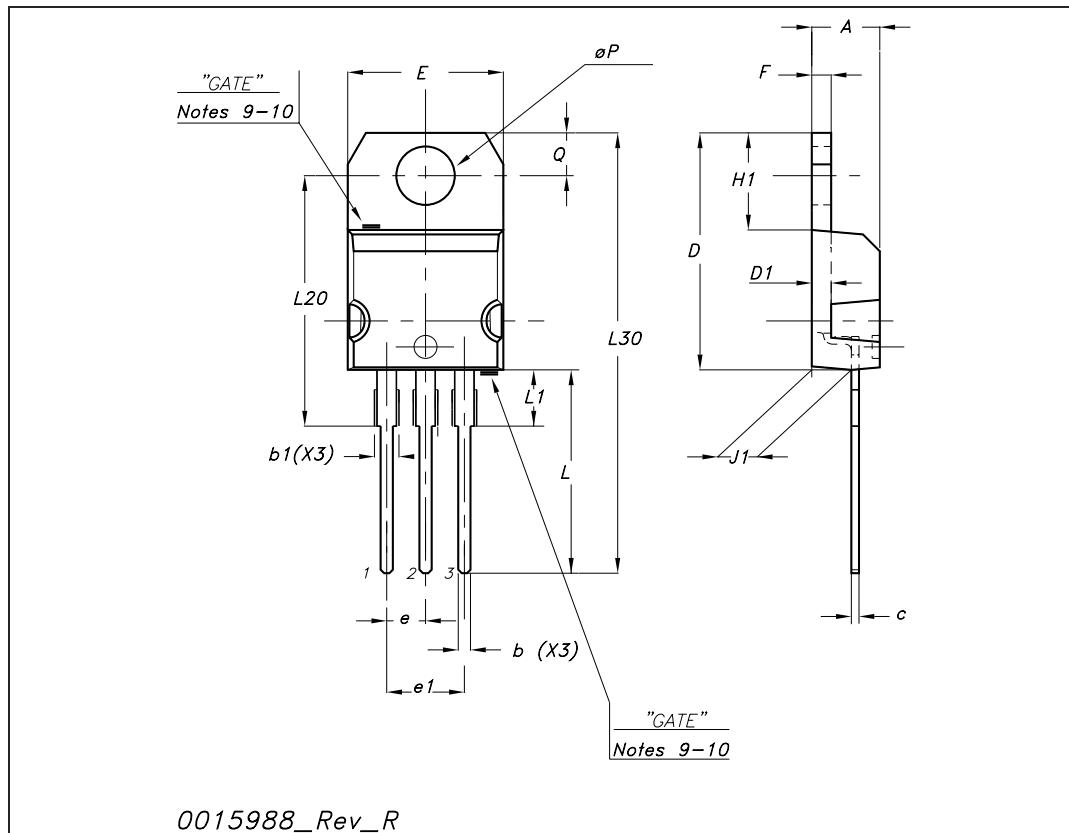


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

TO-220 mechanical data

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.48		0.70	0.019		0.027
D	15.25		15.75	0.6		0.62
D1		1.27			0.050	
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.051
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
$\emptyset P$	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



5 Revision history

Table 8. Document revision history

Date	Revision	Changes
21-Jun-2004	2	Preliminary datasheet
22-Aug-2005	3	Complete document with curves
21-Jan-2006	4	New ECOPAK label
02-Oct-2006	5	New template, no content change
14-May-2009	6	Updated scheme in Figure 1

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