QPC1006

0.15 – 2.8 GHz High Power GaN SP3T Switch

Product Overview

Qorvo's QPC1006 is a Single-Pole, Triple–Throw (SP3T) switch fabricated on Qorvo's QGaN25 0.25um GaN on SiC production process.

Operating from 0.15 to 2.8 GHz, the QPC1006 typically supports 50 W input power handling at control voltages of 0/−40 V for both CW and pulsed RF operations. This switch maintains low insertion loss less than 1.0 dB and greater than 30 dB isolation, making it ideal for high power switching applications across both defense and commercial platforms.

QPC1006 is offered in a 4 x 4 mm plastic overmolded QFN package.

Lead-free and RoHS compliant

Evaluation Boards are available upon request.

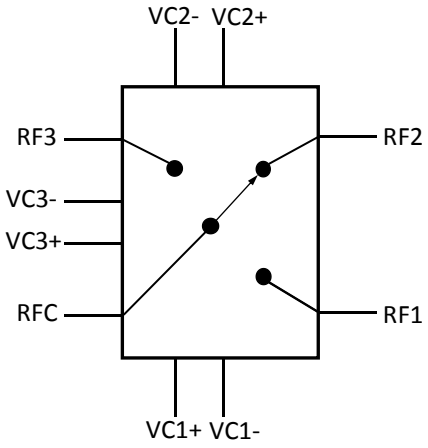
4mm x 4mm 24 Lead OVM QFN

Key Features

- SP3T
- Frequency Range: 0.15 to 2.8 GHz
- Input Power: 50 W
- Insertion Loss: < 1.0 dB
- Isolation: >30 dB Typical
- Switching Speed: 50 ns
- Control Voltages: 0 V/−40 V
- Package Dimensions: 4 x 4 x 0.85 mm

Performance is typical across frequency. Please reference electrical specification table and data plots for more details.

Functional Block Diagram



Applications

- Commercial and Military Radar
- Communications
- Electronic Warfare
- Test Instrumentation
- General Purpose

Ordering Information

Part No.	ECCN	Description
QPC1006	EAR99	0.15–2.8 GHz High Power GaN SP3T Switch
QPC1006EVB		Evaluation Board

Absolute Maximum Ratings

Parameter	Rating
Control Voltage (V_C)	−50 V
Control Current (I_C)	3 mA
Power Dissipation [1]	14 W
RF Input Power, CW, 50 Ω, T = 25 °C	60 W
Channel Temperature, T_{CH}	275 °C
Mounting Temperature (30 sec)	260 °C
Storage Temperature	−40 to 150 °C

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Notes:

1) This is a total loss of which 4 W is mismatched loss and 3 W is dissipated in the passive structures.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V_{C1+}/V_{C1-}		0/-40		V
V_{C2+}/V_{C2-}		-40/0		V
V_{C3+}/V_{C3-}		-40/0		V
Channel Temp., T_{CH}		≤ 225		°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

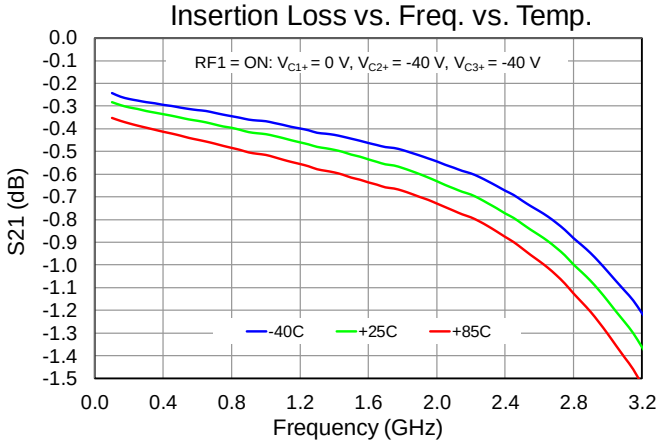
Test conditions unless otherwise noted: 25 °C, V_{C1+}+/V_{C1-} = 0 V/-40V, V_{C2+}+/V_{C2-} = -40 V/0V, V_{C3+}+/V_{C3-} = -40 V/0V.
See Logic table on page 13.

Parameter		Min	Typ	Max	Units
Operational Frequency Range		0.15	–	2.8	GHz
Insertion Loss (On-State)	Frequency = 0.15 GHz		0.30	–	dB
	Frequency = 1.0 GHz		0.43	–	
	Frequency = 2.8 GHz		1.0	–	
Input Return Loss (On-State) Common Port RL	Frequency = 0.15 GHz		35	–	dB
	Frequency = 1.0 GHz		33	–	
	Frequency = 2.8 GHz		12.5	–	
Output Return Loss (On-State) Switched Port RL	Frequency = 0.15 GHz		34.5	–	dB
	Frequency = 1.0 GHz		32	–	
	Frequency = 2.8 GHz		13	–	
Isolation (Off-State)	Frequency = 0.15 GHz		57	–	dB
	Frequency = 1.0 GHz		40	–	
	Frequency = 2.8 GHz		30	–	
Output Return Loss Isolated Port	Frequency = 0.15 GHz		2.3	–	dB
	Frequency = 1.0 GHz		2.4	–	
	Frequency = 2.8 GHz		2.0	–	
Insertion Loss @ P_{IN} = 47 dBm (Pulsed RF) PW = 100us; DC = 10%	Frequency = 0.15 GHz		0.32		dB
	Frequency = 1.0 GHz		0.45		
	Frequency = 2.8 GHz		1.0		
Insertion Loss @ P_{IN} = 47 dBm (CW)	Frequency = 0.15 GHz		0.37		dB
	Frequency = 1.0 GHz		0.55		
	Frequency = 2.8 GHz		1.2		
Input Power ($P_{0.1dB}$)			47		dBm
Control Voltage			-40	-50	V
Total Supply Current			<3		mA
Switching Speed			50		nS
Insertion Loss Temperature Coefficient		–	-0.0015	–	dB/°C

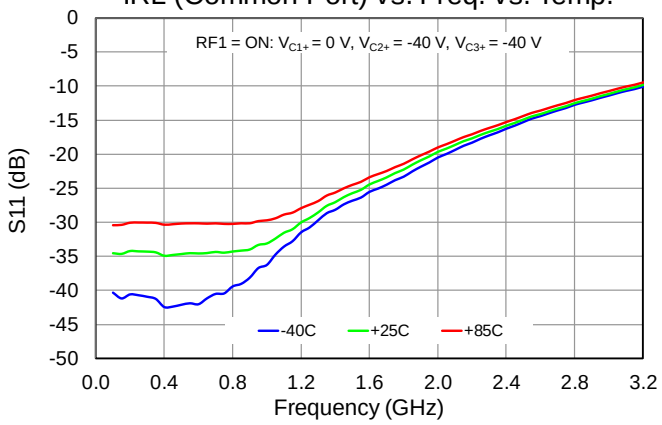
Performance Plots – Small Signal

Notes: RFC = Port1; RF1 = Port 2; RF2 = Port 3; RF3 = Port4. See Logic table on Page 13 for Voltage controls

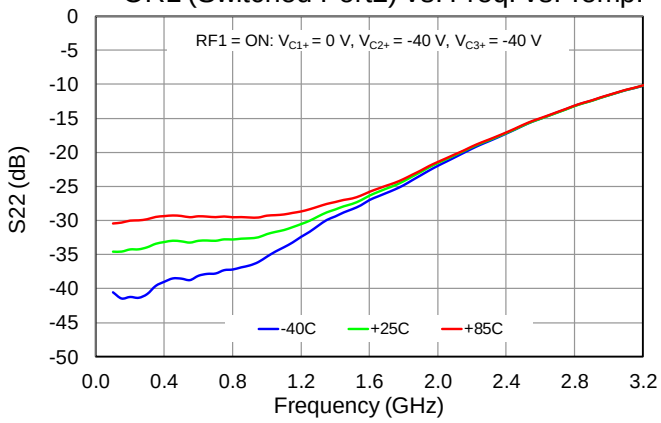
Insertion Loss vs. Freq. vs. Temp.



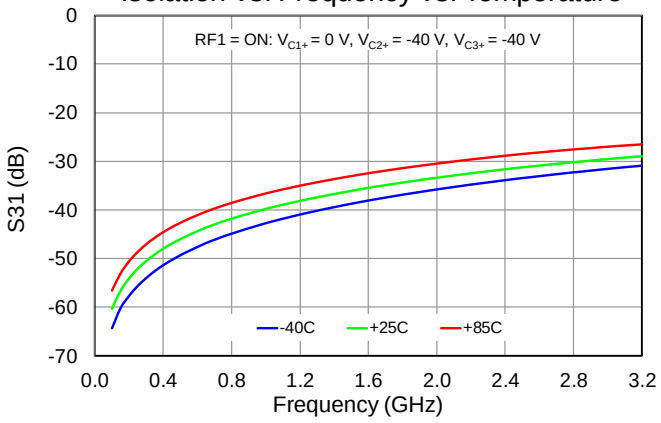
IRL (Common Port) vs. Freq. vs. Temp.



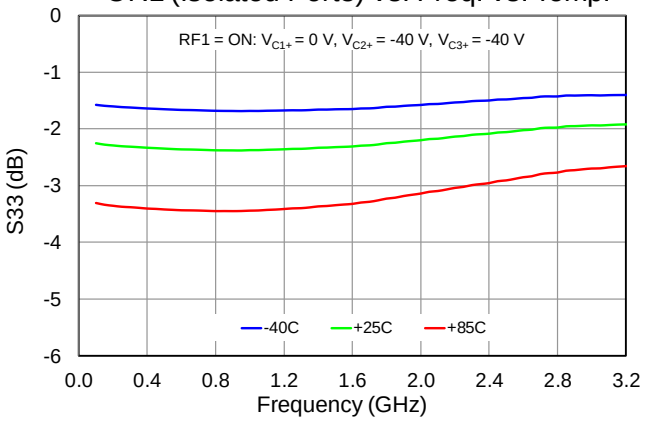
ORL (Switched Port2) vs. Freq. vs. Temp.



Isolation vs. Frequency vs. Temperature



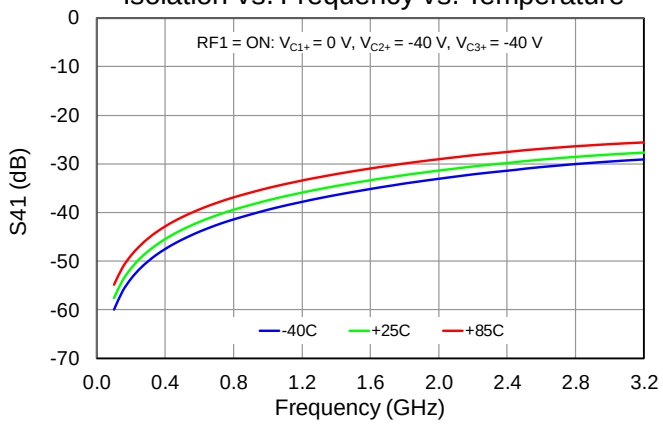
ORL (Isolated Port3) vs. Freq. vs. Temp.



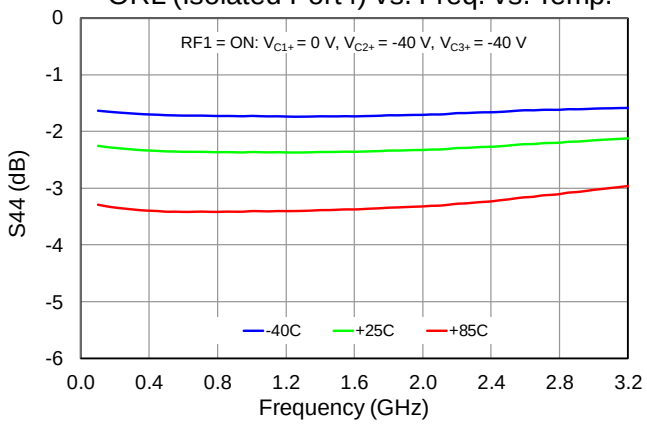
Performance Plots – Small Signal

Notes: RFC = Port1; RF1 = Port 2; RF2 = Port 3; RF3 = Port4. See Logic table on Page 13 for Voltage controls

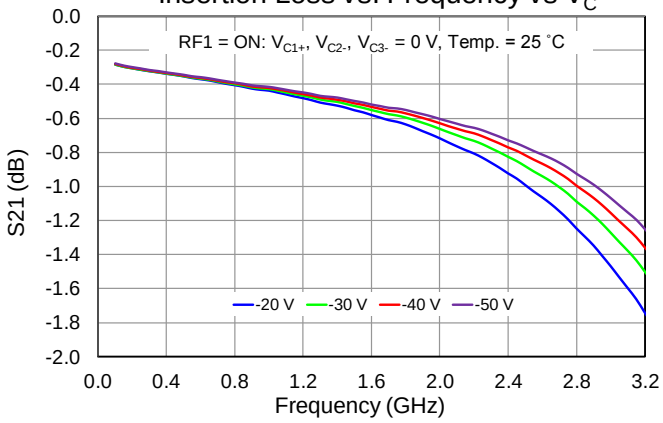
Isolation vs. Frequency vs. Temperature



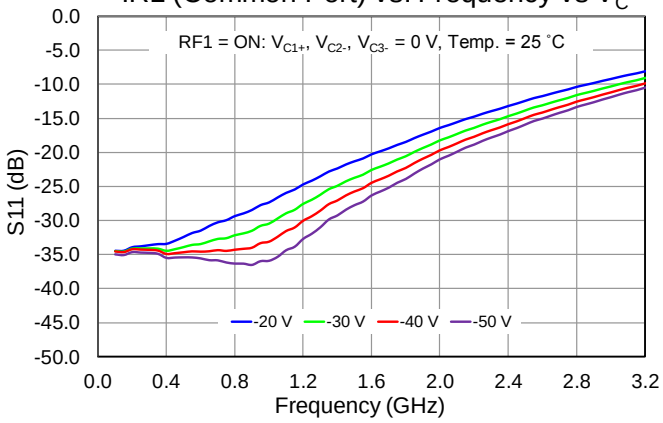
ORL (Isolated Port4) vs. Freq. vs. Temp.



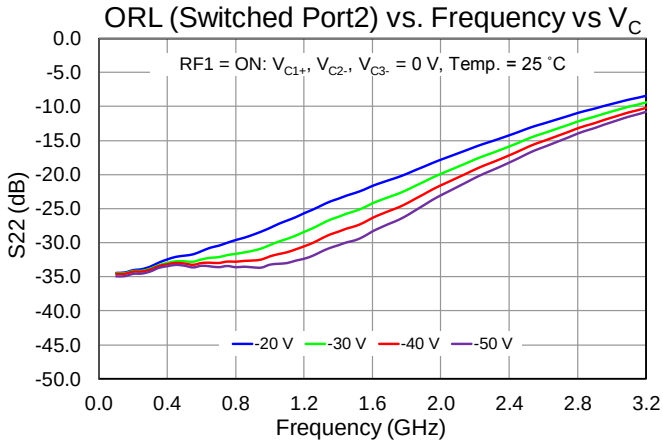
Insertion Loss vs. Frequency vs V_C



IRL (Common Port) vs. Frequency vs V_C



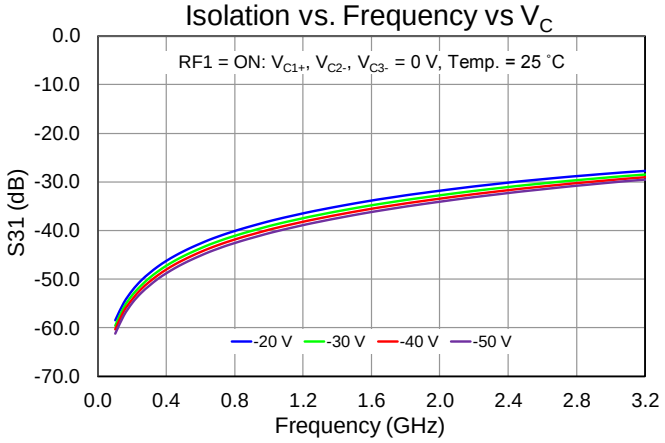
ORL (Switched Port2) vs. Frequency vs V_C



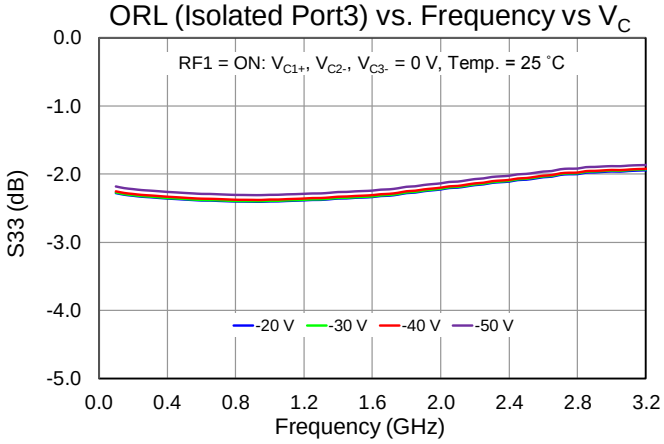
Performance Plots – Small Signal

Notes: RFC = Port1; RF1 = Port 2; RF2 = Port 3; RF3 = Port4. See Logic table on Page 13 for Voltage controls

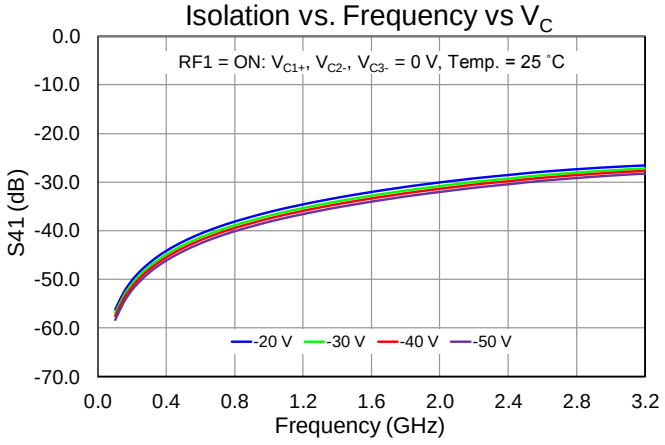
Isolation vs. Frequency vs V_C



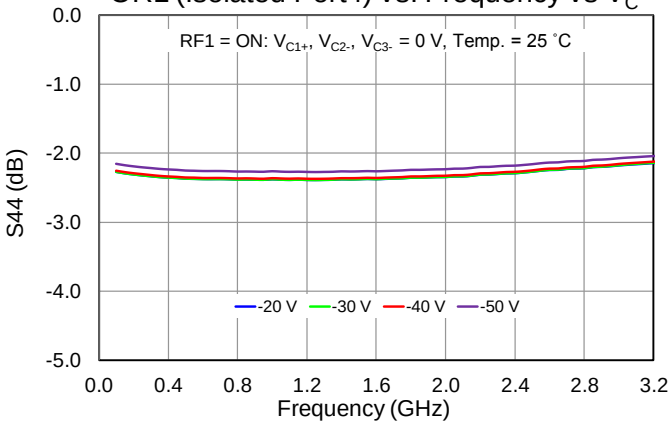
ORL (Isolated Port3) vs. Frequency vs V_C



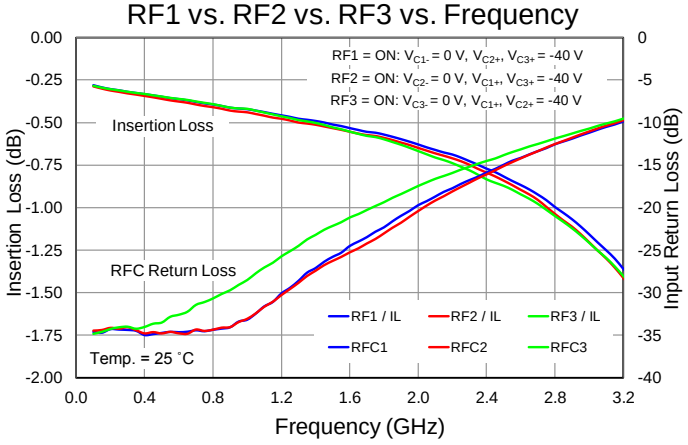
Isolation vs. Frequency vs V_C



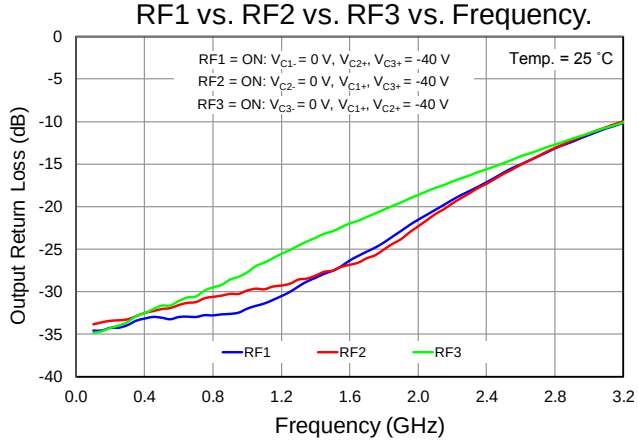
ORL (Isolated Port4) vs. Frequency vs V_C



RF1 vs. RF2 vs. RF3 vs. Frequency



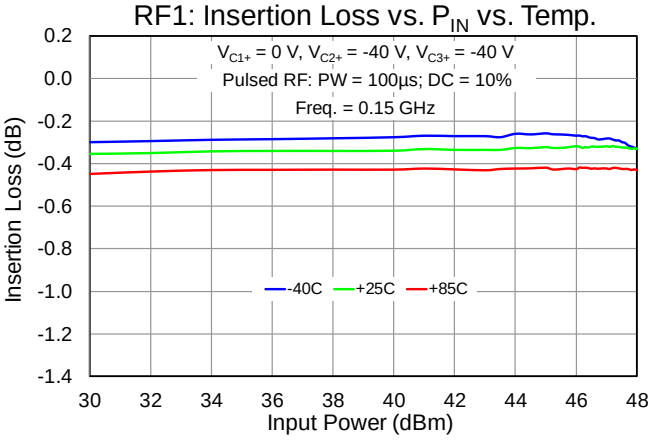
RF1 vs. RF2 vs. RF3 vs. Frequency.



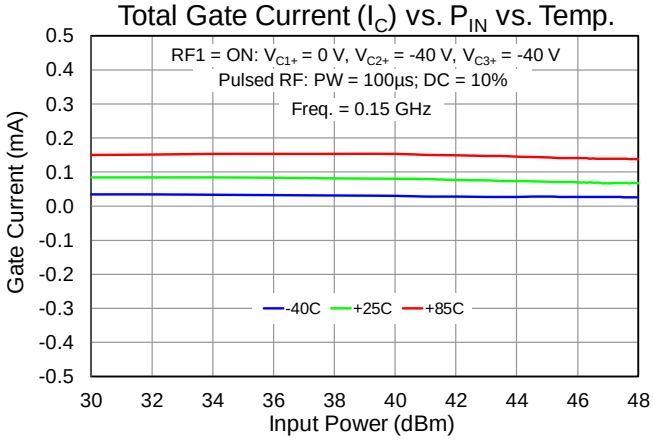
Performance Plots – Compression (Pulsed)

Notes: RFC = Port1; RF1 = Port 2; RF2 = Port 3; RF3 = Port4. See Logic table on Page 13 for Voltage controls

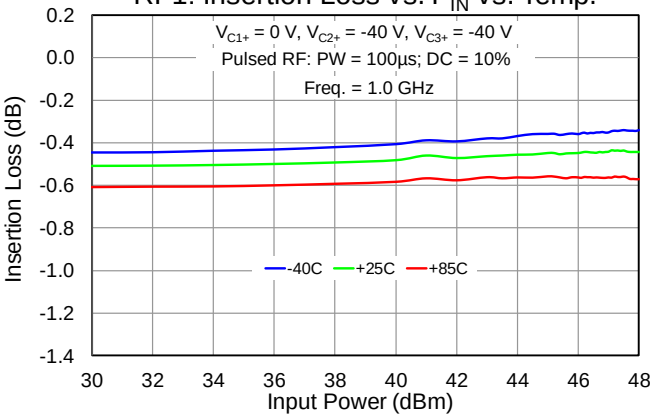
RF1: Insertion Loss vs. P_{IN} vs. Temp.



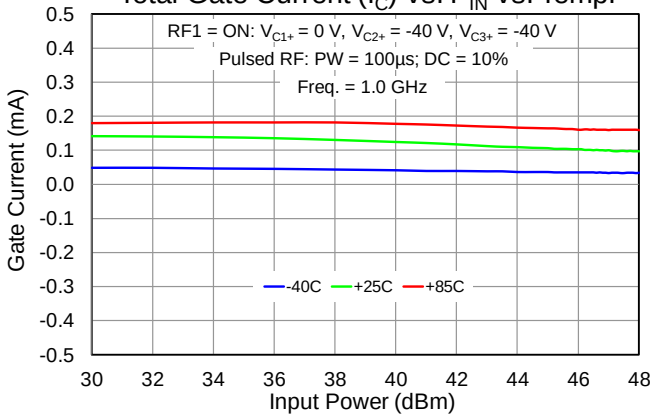
Total Gate Current (I_C) vs. P_{IN} vs. Temp.



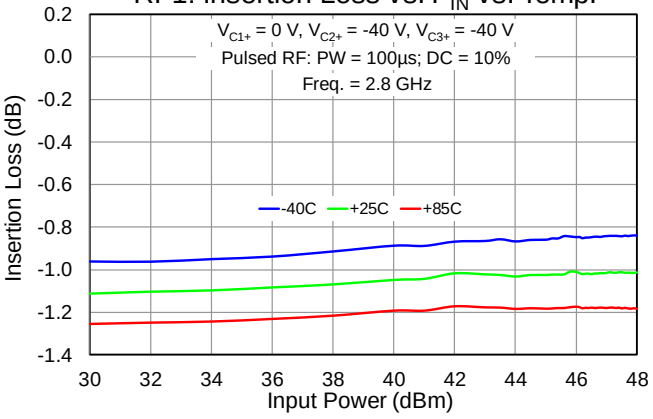
RF1: Insertion Loss vs. P_{IN} vs. Temp.



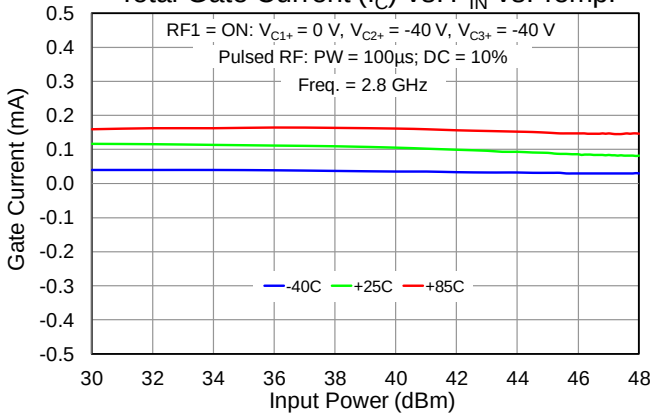
Total Gate Current (I_C) vs. P_{IN} vs. Temp.



RF1: Insertion Loss vs. P_{IN} vs. Temp.



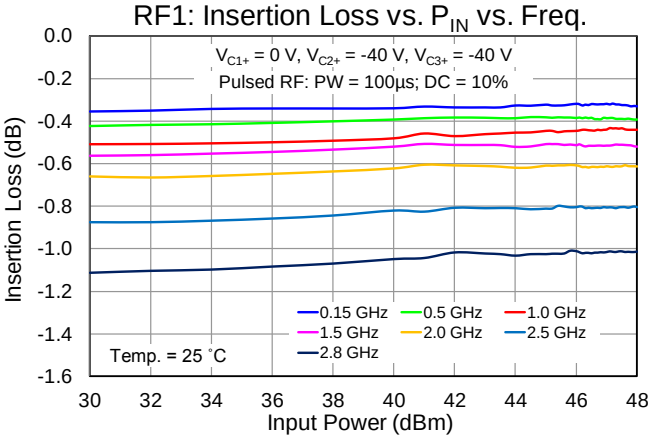
Total Gate Current (I_C) vs. P_{IN} vs. Temp.



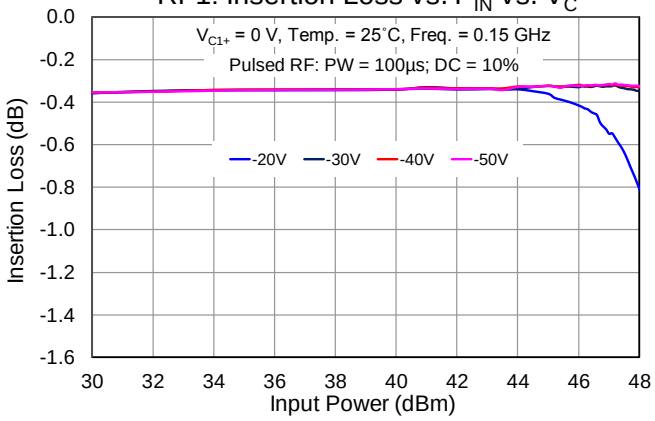
Performance Plots – Compression (Pulsed)

Notes: RFC = Port1; RF1 = Port 2; RF2 = Port 3; RF3 = Port4. See Logic table on Page 13 for Voltage controls

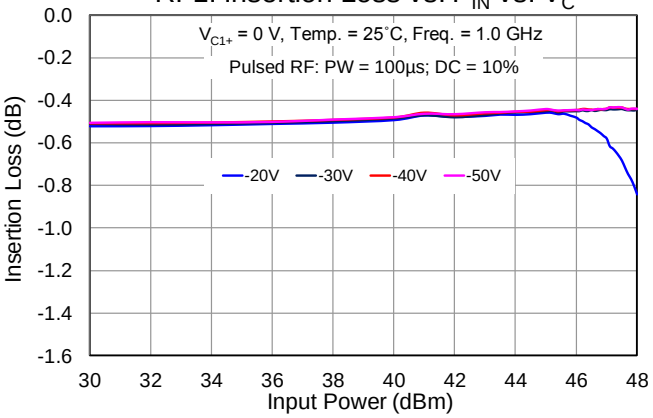
RF1: Insertion Loss vs. P_{IN} vs. Freq.



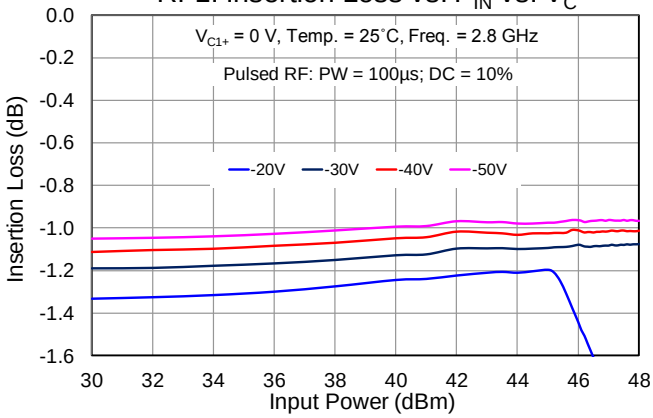
RF1: Insertion Loss vs. P_{IN} vs. V_C



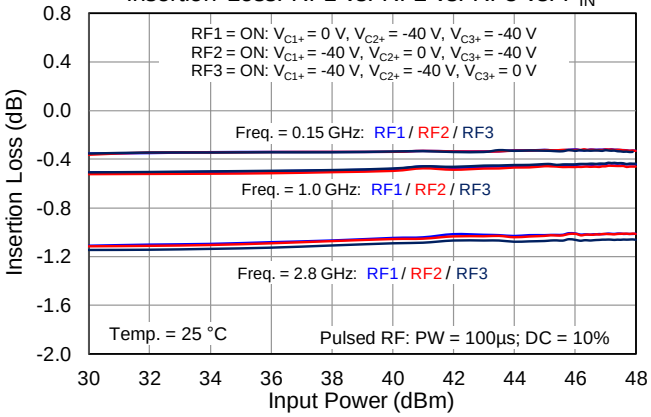
RF1: Insertion Loss vs. P_{IN} vs. V_C



RF1: Insertion Loss vs. P_{IN} vs. V_C



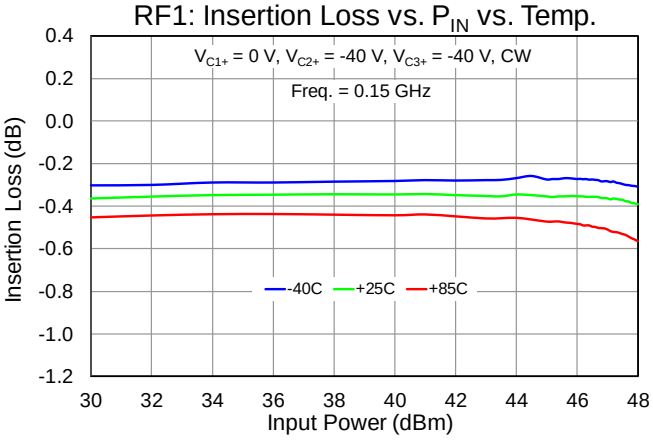
Insertion Loss: RF1 vs. RF2 vs. RF3 vs. P_{IN}



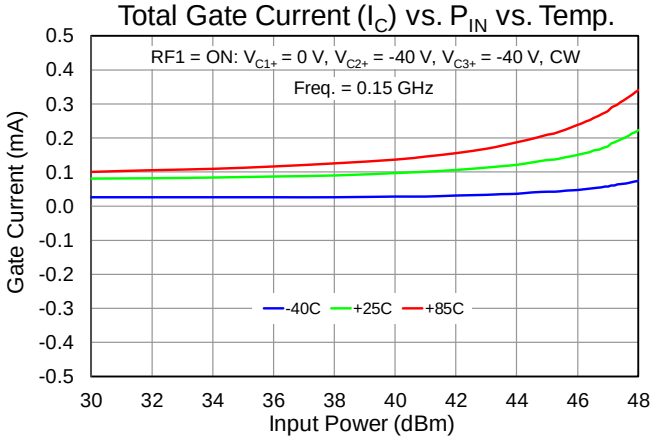
Performance Plots – Compression (CW)

Notes: RFC = Port1; RF1 = Port 2; RF2 = Port 3; RF3 = Port4. See Logic table on Page 13 for Voltage controls

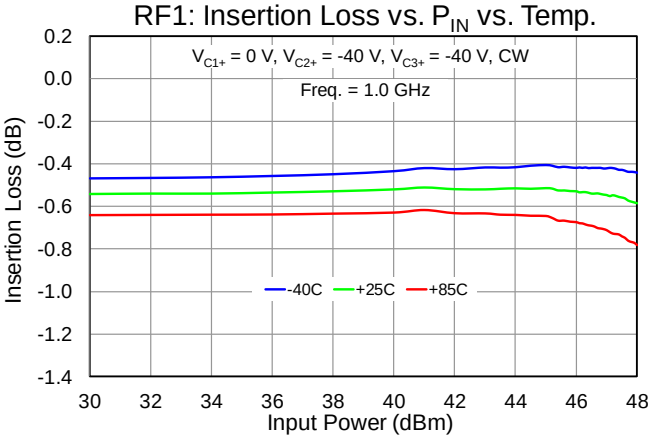
RF1: Insertion Loss vs. P_{IN} vs. Temp.



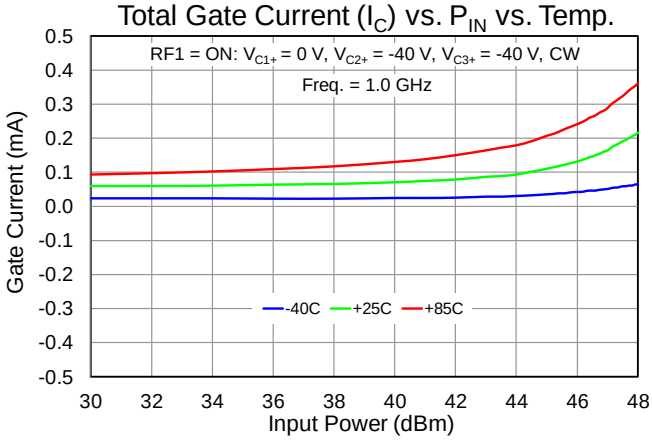
Total Gate Current (I_C) vs. P_{IN} vs. Temp.



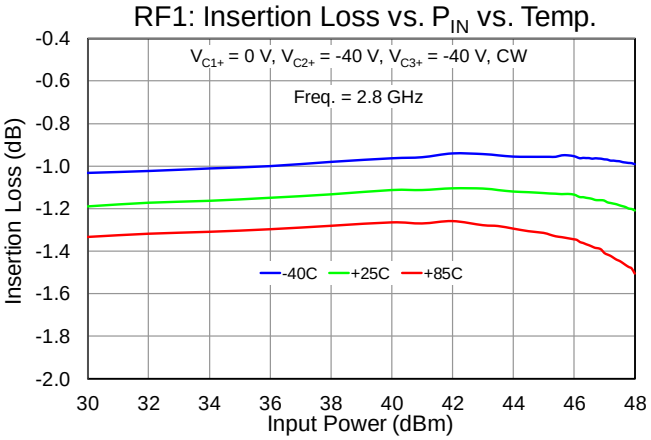
RF1: Insertion Loss vs. P_{IN} vs. Temp.



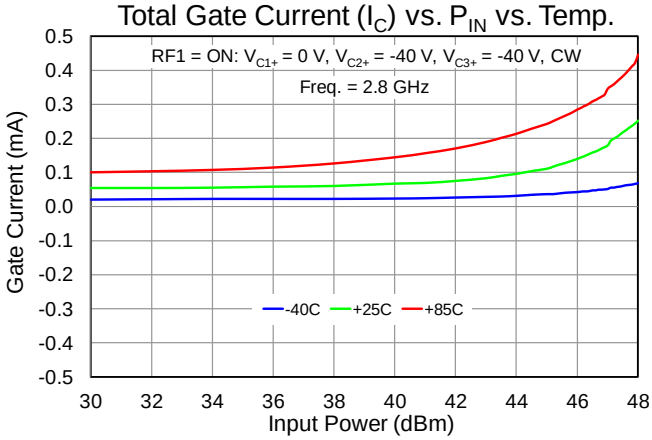
Total Gate Current (I_C) vs. P_{IN} vs. Temp.



RF1: Insertion Loss vs. P_{IN} vs. Temp.



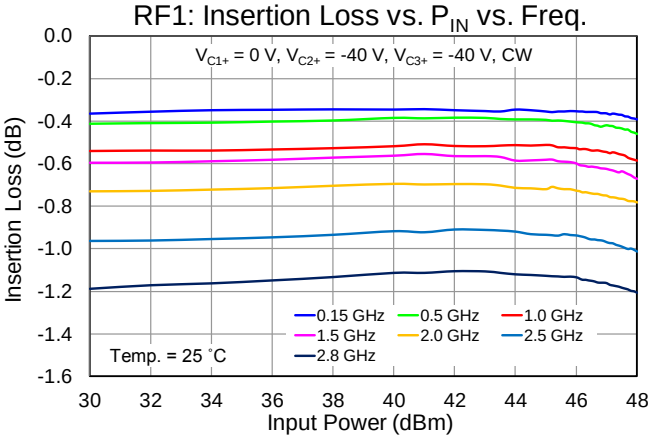
Total Gate Current (I_C) vs. P_{IN} vs. Temp.



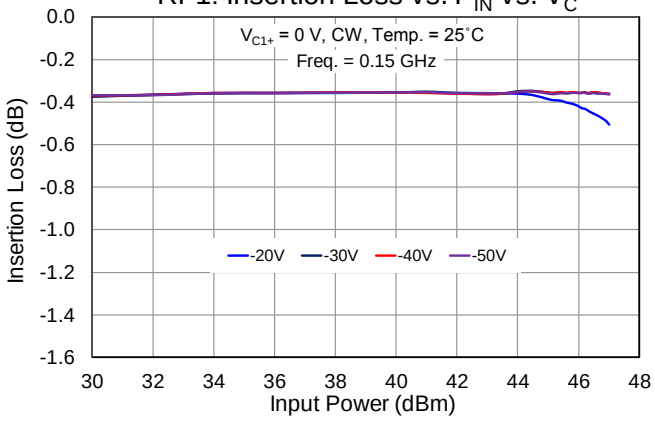
Performance Plots – Compression (CW)

Notes: RFC = Port1; RF1 = Port 2; RF2 = Port 3; RF3 = Port4. See Logic table on Page 13 for Voltage controls

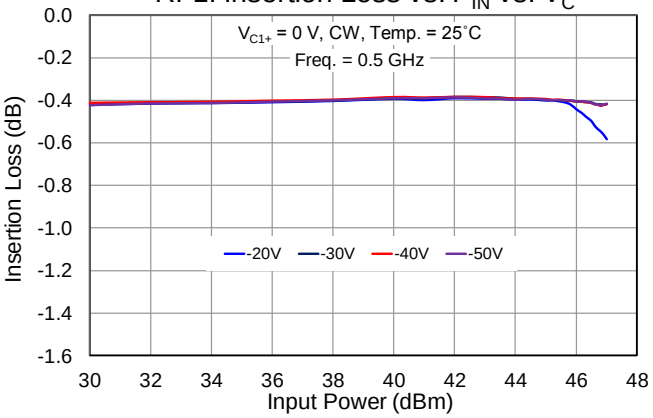
RF1: Insertion Loss vs. P_{IN} vs. Freq.



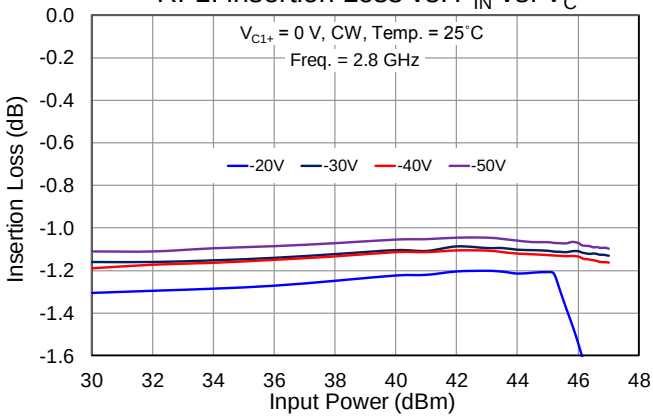
RF1: Insertion Loss vs. P_{IN} vs. V_C



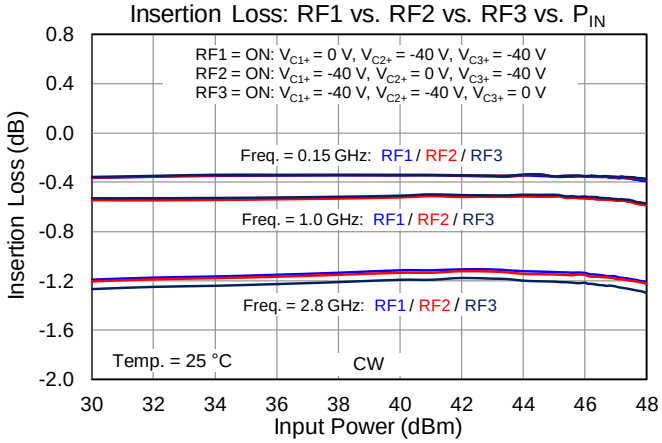
RF1: Insertion Loss vs. P_{IN} vs. V_C



RF1: Insertion Loss vs. P_{IN} vs. V_C



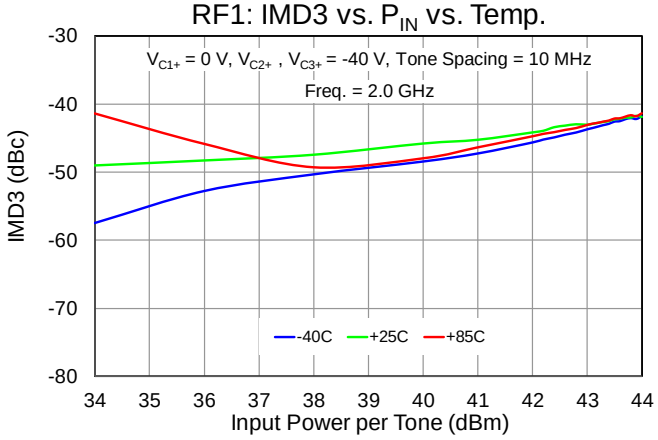
Insertion Loss: RF1 vs. RF2 vs. RF3 vs. P_{IN}



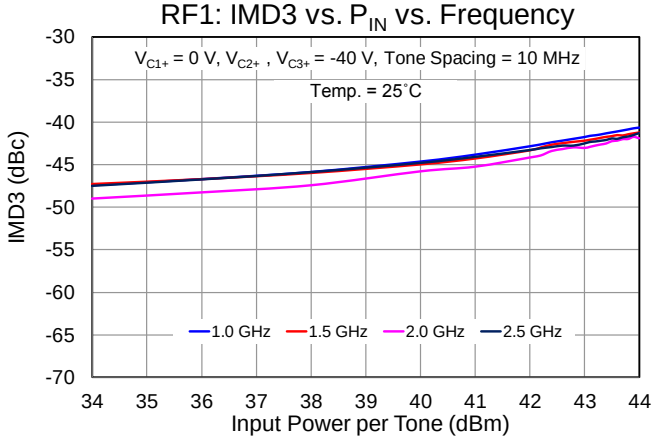
Performance Plots – Linearity

Notes: RFC = Port1; RF1 = Port 2; RF2 = Port 3; RF3 = Port4. See Logic table on Page 15 for Voltage controls

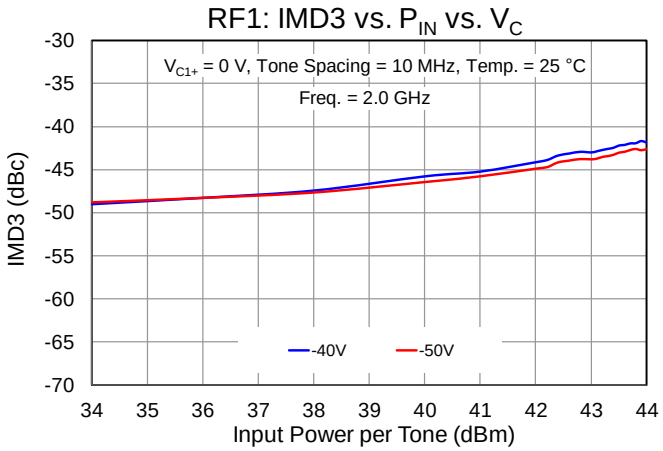
RF1: IMD3 vs. P_{IN} vs. Temp.



RF1: IMD3 vs. P_{IN} vs. Frequency



RF1: IMD3 vs. P_{IN} vs. V_C



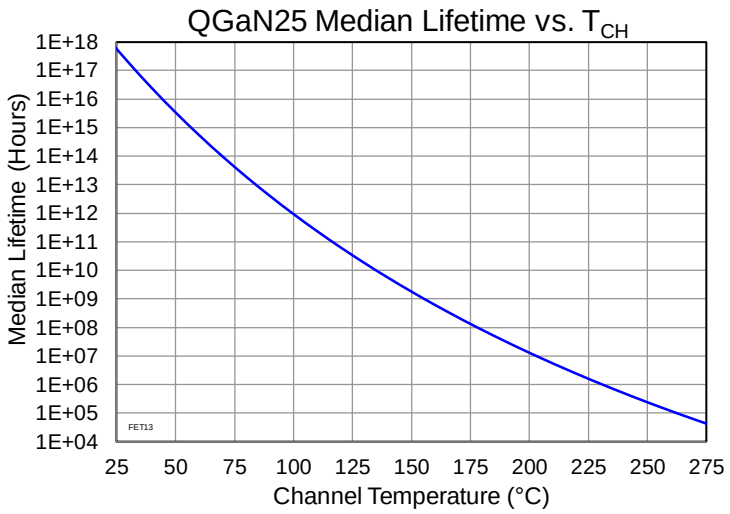
Thermal and Reliability Information

Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) (1)	T_{BASE} = 85 °C, V_{C1+} = 0 V, V_{C2+} = -40 V,, V_{C3+} = -40 V Freq. = 2.8 GHz, P_{IN} = 50 W, P_{DISS} (2) = 5.8 W, CW	7.93	ºC/W
Channel Temperature (T_{CH}) (1)		131	°C
Median Lifetime (T_M)		1.57 x 10^10	Hrs

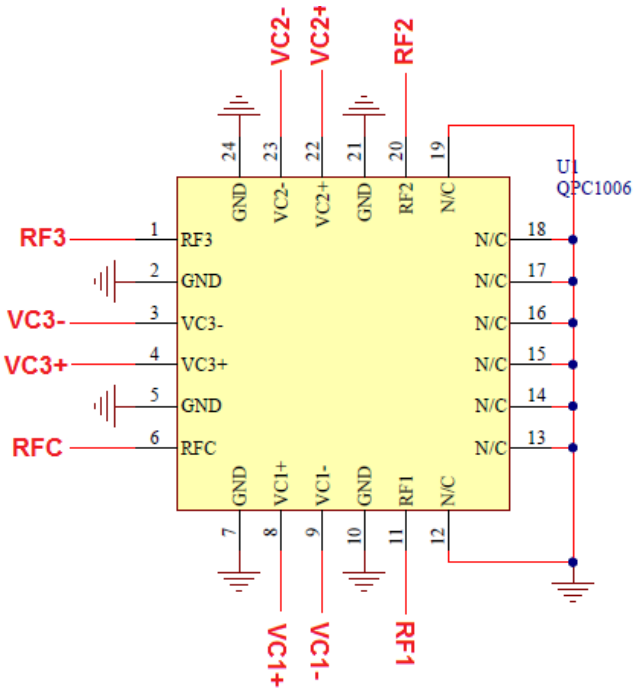
Notes:
1. Measured to the back of the package.
2. This is a total P_{DISS} in the FETs.

Median Lifetime and Channel Temperature

Test Conditions: V_D = +40 V; Failure Criteria = 10% reduction in I_{D_MAX} during DC Life Testing



Application Circuit



Notes:

1. This switch can be configured as a Single Pole, Single Throw (SPST) by terminating two unused RF switched ports with a 50 Ohm load.
2. External components are not required.

Bias Up Procedure

1. V_{C1+} or V_{C2+} or V_{C3+} set to 0 V (see Logic Table for RF Path)
2. V_{C1-} or V_{C2-} or V_{C3-} set to -40 V (see Logic Table for RF Path)
3. Apply RF signal to RF Input

Bias Up Down

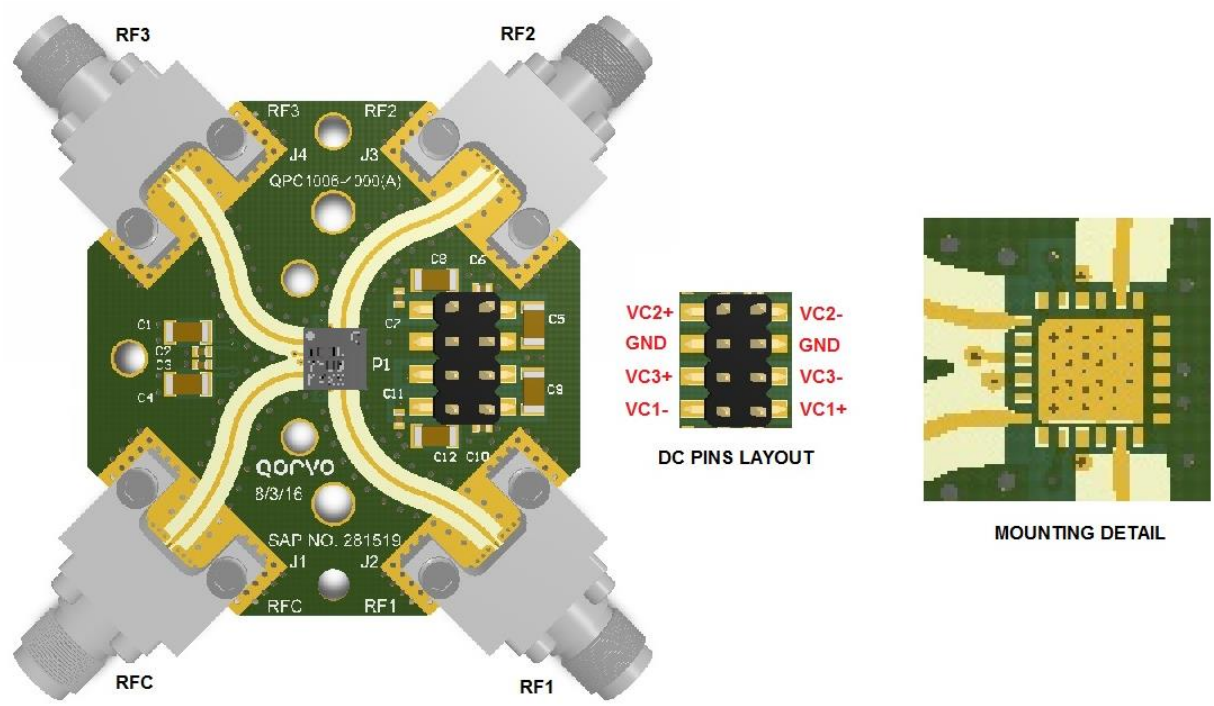
1. Turn off RF supply
2. Turn V_{C1-} or V_{C2-} or V_{C3-} to 0 V
3. Turn V_{C1+} or V_{C2+} or V_{C3+} to 0 V

Logic Table (SP3T Truth Table)

RF Path	State	V_{C1+}	V_{C1-}	V_{C2+}	V_{C2-}	V_{C3+}	V_{C3-}
RFC to RF1 ON	On-State (Insertion Loss), RF2 & RF3 = OFF	H	L	L	H	L	H
RFC to RF2 ON	On-State (Insertion Loss), RF1 & RF3 = OFF	L	H	H	L	L	H
RFC to RF3 ON	On-State (Insertion Loss), RF1 & RF2 = OFF	L	H	L	H	H	L

- VC High (H) = 0 V
- VC Low (L) = -20, -30, -40 or -50 V

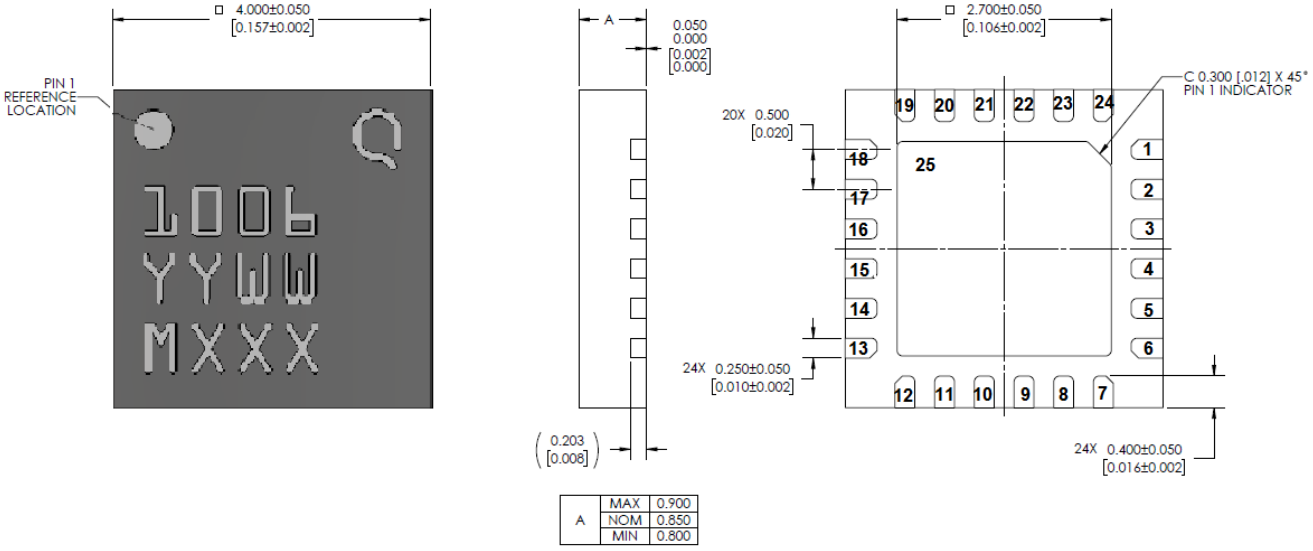
Evaluation Board (EVB) Assembly Layout.



Notes:

1. This switch can be configured as a Single Pole, Single Throw (SPST) by terminating one unused RF switched port with a 50 Ohm load.
2. See Logic Table on page 13 for biasing the voltage controls.
3. External components are not required

Mechanical Information

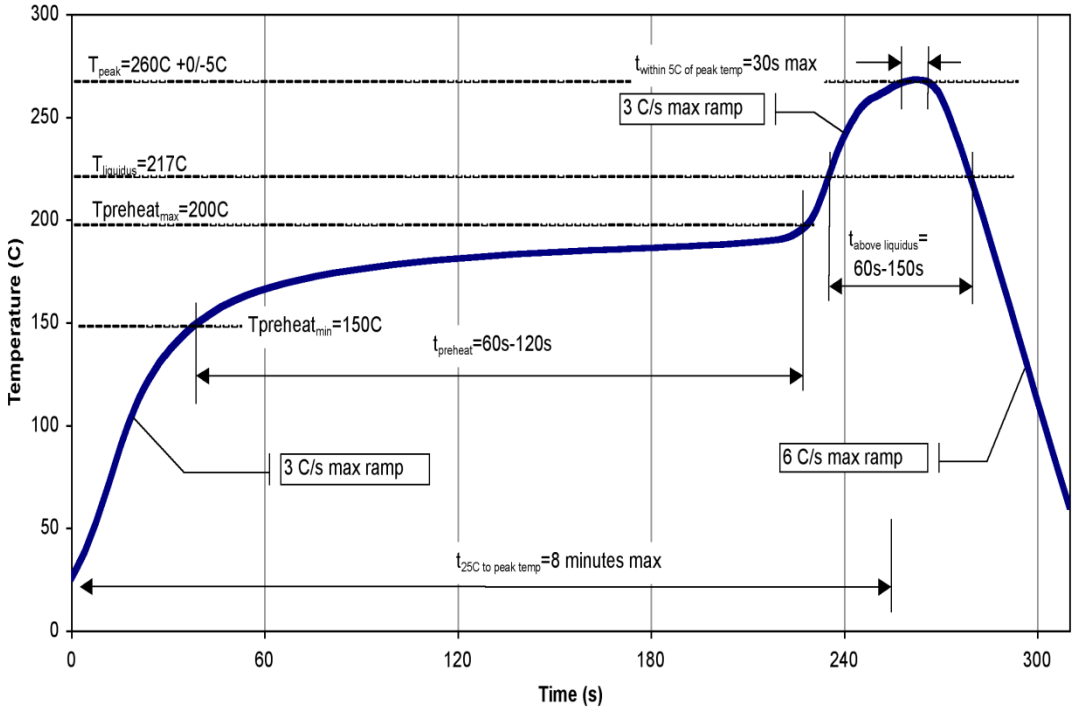


Units: millimeters
Tolerances: unless specified
x.xx = ± 0.25
x.xxx = ± 0.100
Materials:
Base: Laminate
Packaged Exposed Metallization is gold plated
Marking:
QPC1006: Part number
YY: Part Assembly year
WW: Part Assembly week
MXXX: Batch ID

Pin Description

Pad No.	Symbol	Description
1	RF3	RF switched port 3; matched to 50 Ω; DC coupled
2, 5, 7, 10, 21, 24	GND	Ground. Connected to GND paddle (pin 25); should be grounded on PCB to improve isolation
3	V_{C3-}	Control voltage #3; External components are not required
4	V_{C3+}	Control voltage #3; External components are not required
6	RFC	RF common port; matched to 50 Ω; DC coupled
8	V_{C1+}	Control voltage #1; External components are not required
9	V_{C1-}	Control voltage #1; External components are not required
11	RF1	RF switched port 1; matched to 50 Ω; DC coupled
12 - 19	N/C	Not connected internally. Recommended to be grounded at EVB level
20	RF2	RF switched port 2; matched to 50 Ω; DC coupled
22	V_{C2+}	Control voltage #2; External components are not required
23	V_{C2-}	Control voltage #2; External components are not required
25	GND	Backside Paddle. Multiple vias should be employed to minimize inductance and thermal resistance.

Recommended Soldering Profile



Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	1A	ESDA / JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	TBD	ESDA / JEDEC JS-002-2014
MSL – Convection Reflow 260 °C	TBD	JEDEC standard IPC/JEDEC J-STD-020

Caution!
ESD-Sensitive Device

Solderability

Compatible with the latest version of J-STD-020, Lead-free solder, 260 °C

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

For technical questions and application information: **Email:** appsupport@qorvo.com

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