14 W 15 V 5 V SMPS demo board with ICE5GR4780AG

DEMO_5GR4780AG_14W1

About this document

Scope and purpose

This document is an engineering report that describes a universal-input 14 W 15 V 5 V off-line non-isolated Flyback converter using the latest fifth-generation Infineon Fixed Frequency (FF) CoolSET™ ICE5GR4780AG, which offers high-efficiency, low standby power with selectable entry and exit standby power options, wide V_{CC} operating range with fast start-up, robust line protection with input OVP and various protection modes for a highly reliable system. This demoboard is designed for users who wish to evaluate the performance of ICE5GR4780AG in terms of optimized efficiency, thermal performance and EMI.

Intended audience

This document is intended for power-supply design/application engineers, students, etc. who wish to design low-cost and highly reliable systems of off-line SMPS, either auxiliary power supplies for white goods, PCs, servers and TVs, or enclosed adapters for Blu-ray players, set-top boxes, games consoles, etc.

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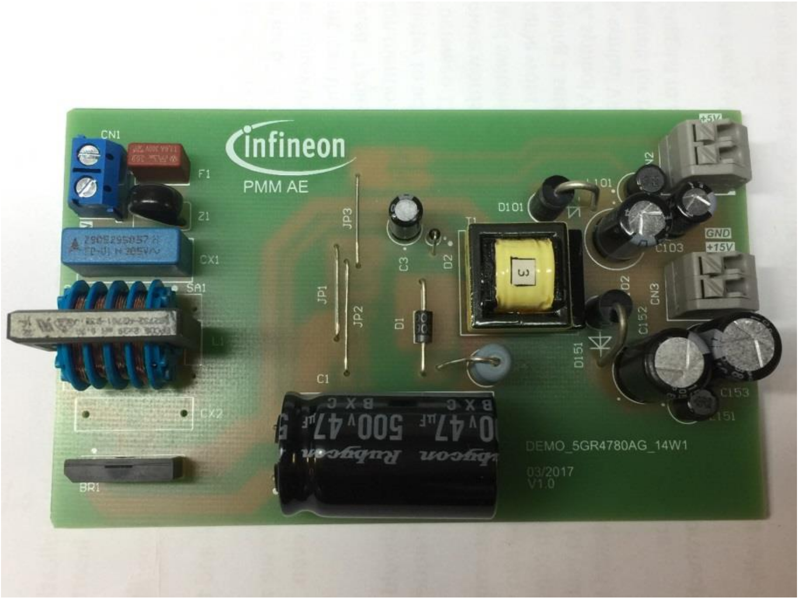
1 Abstract

This document is an engineering report for a 14 W 15 V 5 V demo board designed in an FF non-isolated Flyback converter topology with primary-side feedback (FB) using the fifth-generation FF CoolSET™ ICE5GR4780AG. The demo board is operated in Discontinuous Conduction Mode (DCM) and is running at 125 kHz fixed switching frequency. The frequency reduction with soft gate driving and frequency jittering offers lower EMI and better efficiency between medium load and 50% load. The selectable Active Burst Mode (ABM) power enables ultra-low power consumption. In addition, numerous adjustable protection functions have been implemented in ICE5GR4780AG to protect the system and customize the IC for the chosen application. In case of failure modes like line Over Voltage (OV), V_{CC} OV/Under Voltage (UV), open control-loop or over-load, over-temperature, V_{CC} short-to-GND and CS short-to-GND, the device enters protection mode. By means of the cycle-by-cycle Peak Current Limitation (PCL), the dimensions of the transformer and the current rating of the secondary diode can both be optimized. In this way, a cost-effective solution can easily be achieved. The target applications of ICE5GR4780AG are either auxiliary power supplies for white goods, PCs, servers and TVs, or enclosed adapters for Blu-ray players, set-top boxes, games consoles, etc.

2 Demo board

This document contains the list of features, the power-supply specifications, schematics, Bill of Materials (BOM) and transformer construction documentation. Typical operating characteristics such as performance curve and scope waveforms are shown at the end of the report.



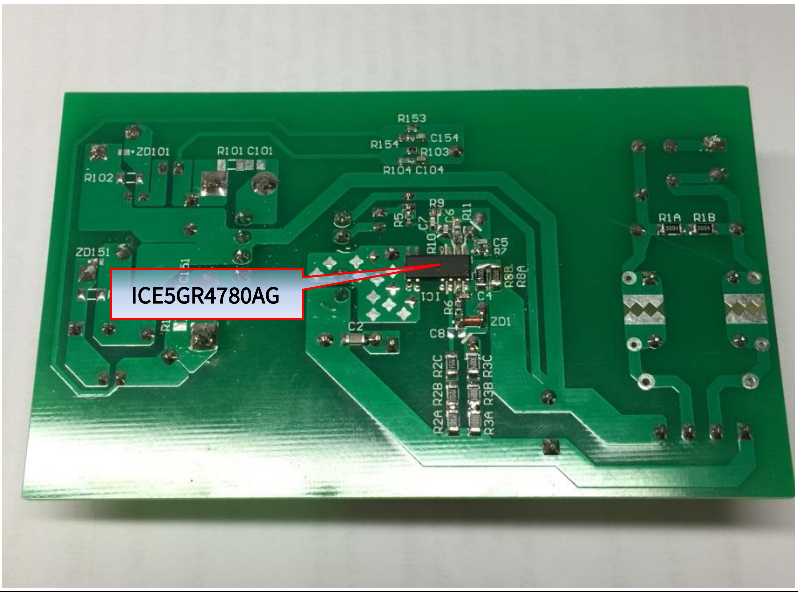


Figure 1 DEMO_5GR4780AG_14W1

3 Specifications of the demo board

Table 1 Specifications of DEMO_5GR4780AG_14W1

Input voltage and frequency	85 V AC (60 Hz) ~ 300 V AC (50 Hz)
Output voltage, current and power	(15 V × 0.83 A) + (5 V × 0.40 A) = 14.45 W
Regulation	+5 V: less than ±5% +15 V: less than ±15%
Output ripple voltage (full load, 85 V AC ~ 300 V AC)	5 $V_{ripple\_p\_p}$ < 100 mV 15 $V_{ripple\_p\_p}$ < 200 mV
Active mode four-point average efficiency (25%, 50%, 75%, 100% load)	> 82% at 115 V AC and 230 V AC
Standby power consumption	No load: P_{in} < 100 mW at 230 V AC 60 mW load: P_{in} < 170 mW at 230 V AC
Conducted emissions (EN 55022 class B)	Pass with 8.7 dB margin for 115 V AC and 7.4 dB margin for 230 V AC
Surge immunity (EN 61000-4-5)	Installation class 4 (±2 kV for line-to-line)
Form factor case size (L × W × H)	(110 × 66 × 27) mm

Note: *"The demo board is designed for dual-output with cross-regulated loop FB. It may not regulate properly if loading is applied only to single-output. If the user wants to evaluate for single-output (15 V only) conditions, the following changes are necessary on the board.*

1. Remove D101, L101, C102, C103, R102, R103, R104, C104 (to disable 5 V output).
2. Change R11 to 30 kΩ and R153 to 220 kΩ (to disable 5 V FB and enable 100% weighted factor on 15 V output).

Since the board (especially the transformer) is designed for dual-output with optimized cross-regulation, single-output efficiency might not be optimized. It is only for IC functional evaluation under single-output conditions."

4 Circuit description

4.1 Line input

The AC-line input side comprises the input fuse F1 as Over Current (OC) protection. The choke L1 and X-capacitor CX1 act as EMI suppressors. Optional spark-gap devices SA1, SA2 and varistor Z1 can absorb HV stress during a lightning surge test. A rectified DC voltage (120 ~ 424 V DC) is obtained through the bridge rectifier BR1 together with bulk capacitor C1.

4.2 Start-up

To achieve fast and safe start-up, ICE5GR4780AG is implemented with start-up resistor and V_{CC} short-to-GND protection. When V_{VCC} reaches the turn-on voltage threshold 16 V, the IC begins with a soft-start. The soft-start implemented in ICE5GR4780AG is a digital time-based function. The preset soft-start time is 12 ms with four steps. If not limited by other functions, the peak voltage on the CS pin will increase incrementally from 0.3 V to 0.8 V. After IC turn-on, the V_{CC} voltage is supplied by auxiliary windings of the transformer. V_{CC} short-to-GND protection is implemented during the start-up time.

4.3 Integrated CoolMOS™ with frequency reduction controller

ICE5GR4780AG is comprised of a CoolMOS™ and the frequency reduction controller, which enables better efficiency between light load and 50% load. This integrated solution greatly simplifies the circuit layout and reduces the cost of PCB manufacturing. The new CoolSET™ can be operated in either DCM or Continuous Conduction Mode (CCM) with frequency reduction mode. This demo board is designed to operate in DCM. When the system is operating at maximum power, the controller will switch at the FF of 125 kHz. In order to achieve better efficiency between light load and medium load, frequency reduction is implemented and the reduction curve is shown in Figure 2. The V_{CS} is clamped by the current limitation threshold or by the PWM op-amp while the switching frequency is reduced. After the maximum frequency reduction, the minimum switching frequency is f_{OSC2_MIN} (53 kHz).

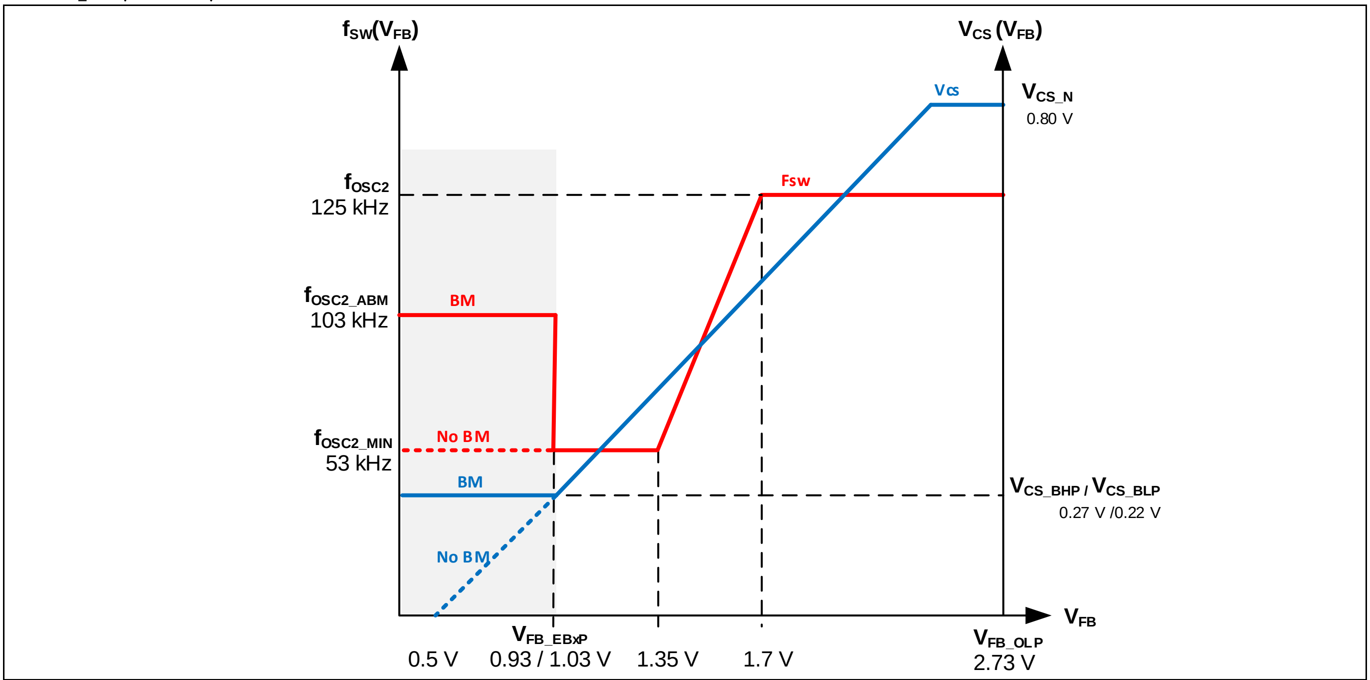


Figure 2 Frequency reduction curve

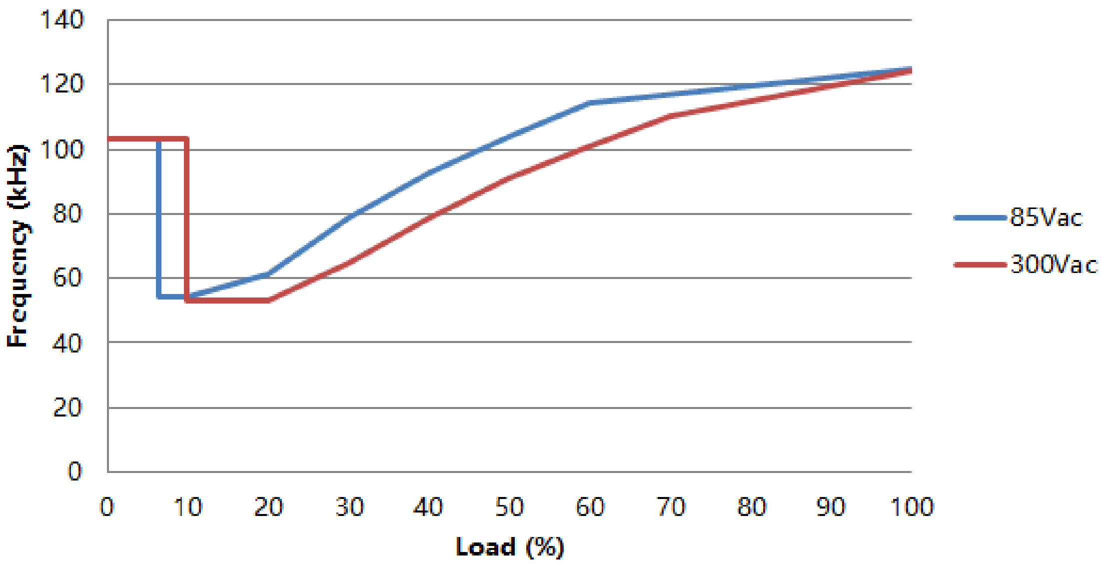


Figure 3 Frequency reduction curve of DEMO_5GR4780AG_14W1

The measured frequency reduction curve of DEMO_5GR4780AG_14W1 is shown in Figure 3.

4.4 Frequency jittering

The ICE5GR4780AG has a frequency jittering feature to reduce the EMI noise. The jitter frequency is internally set at 125 kHz (±5 kHz) and the jitter period is 4 ms.

4.5 RCD clamper circuit

A clamper network (R4, C2 and D1) dissipates the energy of the leakage inductance and suppresses ringing on the SMPS transformer.

4.6 Output stage

There are two outputs in this converter, 15 V and 5 V. The power is coupled out via Schottky diodes D151 and D101. The capacitors C152 and C102 provide energy buffering followed by the L-C filters L151-C153 and L101-C103 to reduce the output voltage ripple and reduce interference between the SMPS switching frequency and line frequency. Storage capacitors C152 and C102 are selected to have a very small internal resistance (ESR) to minimize the output voltage ripple.

4.7 FB loop

For FB, the output is sensed by the voltage divider of R11, R103, and R153 compared to the internal reference voltage of ICE5GR4780AG via the VERR pin, which is connected to the input of an integrated error amplifier internally. Connecting this pin enables non-isolated application. Feed-forward circuit R154, C154, R104 and C104 comprises the compensation network. The comparison voltage is converted to the current signal via an IC internal integrated error amplifier to the FB pin for regulation control.

4.8 ABM

ABM entry and exit power (three levels) can be selected in ICE5GR4780AG. Details are illustrated in the product datasheet. Under light-load conditions, the SMPS enters ABM. At this stage, the controller is always active but the V_{VCC} must be kept above the switch-off threshold. During ABM, the efficiency increases significantly and at the same time it supports low ripple on V_{out} and fast response on load-jump.

In order to enter ABM operation, two conditions must apply:

1. The FB voltage must be lower than the threshold of V_{FB_EBXP}.
2. There must be a certain blanking time (t_{FB_BEB} = 36 ms).

Once all of these conditions are fulfilled, the ABM flip-flop is set and the controller enters ABM operation. This dual-condition determination for entering ABM operation prevents mis-triggering of ABM, so that the controller enters ABM operation only when the output power is really low during the preset blanking time.

During ABM, the maximum Current Sense (CS) voltage is reduced from V_{CS_N} to V_{CS_BXP} to reduce the conduction loss and the audible noise. In ABM, the FB voltage is changing like a sawtooth between $V_{FB\_Bon\_NISO}$ and $V_{FB\_Boff\_NISO}$.

The FB voltage immediately increases if there is a high load-jump. This is observed by one comparator. As the current limit is 27/33% during ABM a certain load is needed so that FB voltage can exceed V_{FB_LB} (2.73 V). After leaving ABM, maximum current can now be provided to stabilize V_{out}.

5 Protection features

Protection is one of the major factors in determining whether the system is safe and robust. Therefore sufficient protection is necessary. ICE5GR4780AG provides comprehensive protection features to ensure the system is operating safely. These include line OV, V_{CC} OV and UV, over-load, over-temperature (controller junction), CS short-to-GND and V_{CC} short-to-GND. When those faults are found, the system will enter protection mode until the fault is removed, when the system resumes normal operation. A list of protections and failure conditions are shown in the table below.

Table 2 Protection functions of ICE5GR4780AG

Protection function	Failure condition	Protection mode
Line OV	V_{VIN} > 2.85 V	Non-switch auto restart
V_{CC} OV	V_{VCC} > 25.5 V	Odd-skip auto restart
V_{CC} UV	V_{VCC} < 10 V	Auto restart
Over-load	V_{FB} > 2.73 V and lasts for 54 ms	Odd-skip auto restart
Over-temperature (junction temperature of controller chip only)	T_J > 140°C	Non-switch auto restart
CS short-to-GND	V_{CS} < 0.1 V, lasts for 0.4 µs and three consecutive pulses	Odd-skip auto restart
V_{CC} short-to-GND (V_{VCC} = 0 V, $R_{Start-up}$ = 50 MΩ and V_{DRAIN} = 90 V)	V_{VCC} < 1.2 V, $I_{VCC\_Charge1}$ ≈ -0.27 mA	Cannot start up

6 Circuit diagram

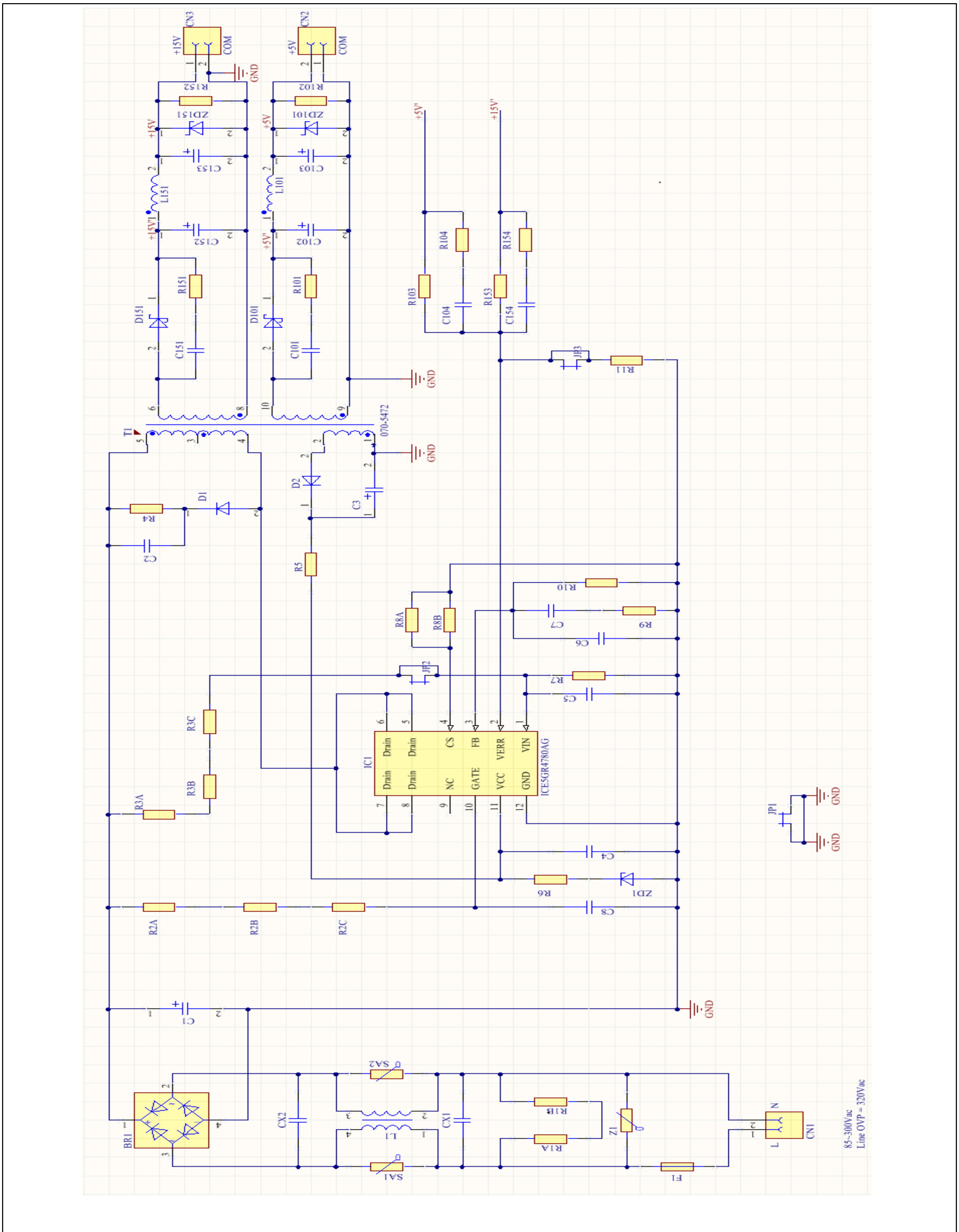


Figure 4 Schematic of DEMO_5GR4780AG_14W1

7 PCB layout

7.1 Top side

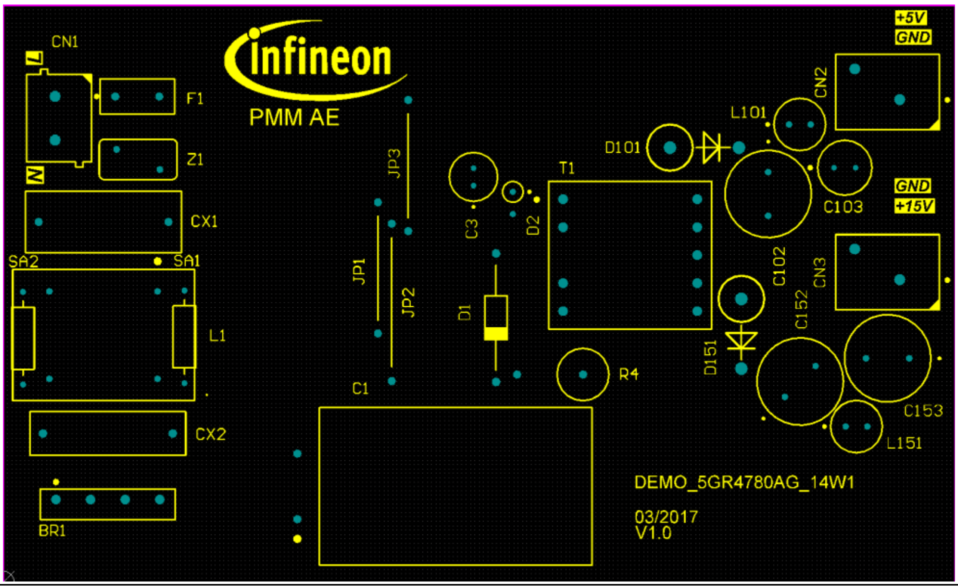


Figure 5 Top side component legend

7.2 Bottom side

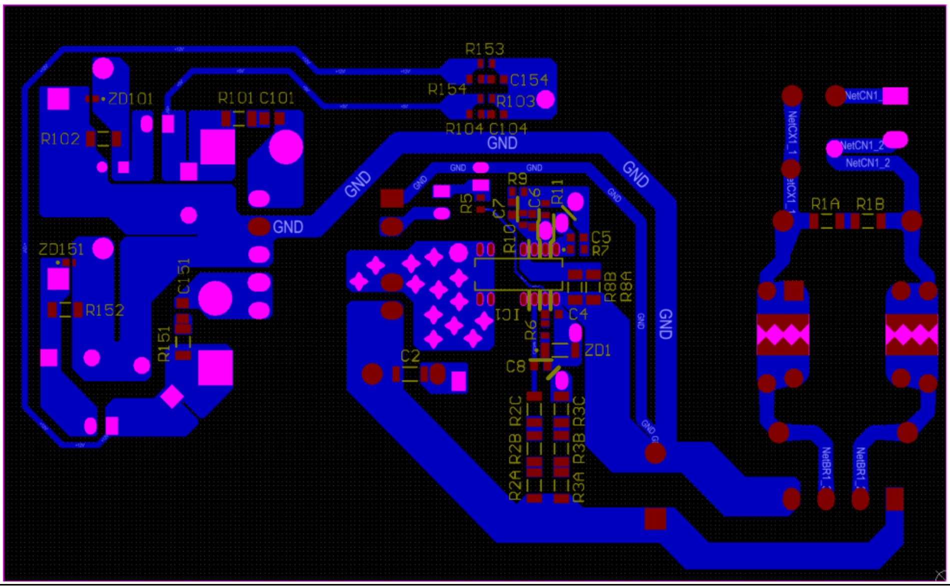


Figure 6 Bottom side copper and component legend

8 BOM

Table 3 BOM (R 1.5)

No.	Designator	Description	Part number	Manufacturer	Quantity
1	F1	1.6 A/300 V	36911600000	Littlefuse	1
2	Z1	Varistor, 0.3 W/320 V	ERZE07A511	Panasonic	1
3	BR1	600 V/1 A	S1VBA60	Shindengen	1
4	CX1	0.15 µF, X-cap	B32932A3154K189	EPCOS/TDK	1
5	C1	47 uF/500 V	500BXC47MEFC18X31.5	Rubycon	1
6	C2	1 nF/630 V (1206)	GRM31A7U2J102JW31D	Murata	1
7	C3	22 µF/50 V	50PX22MEFC5X11	Rubycon	1
8	C4	0.1 uF/50 V DC	GRM188R71H104KA93D	Murata	1
9	C5, C154	1000 pF/50 V DC	GRM1885C1H102GA01D	Murata	2
10	C6, C104	4700 pF/50 V DC	GRM188R71H472KA01D	Murata	2
11	C7	15 pF/50 V DC	GRM1885C1H150JA01D	Murata	1
12	C102	680 uF/10 V DC	10ZL680MEFC8X16	RUBYCON	1
13	C103	330 uF/10 V DC	10ZLH330MEFC6.3X11	RUBYCON	1
14	C152, C153	680 uF/25 V DC	25ZLS680MEFC10X16	RUBYCON	2
15	ZD1	22 V/500 mW	BZS55B22 RXG	Taiwan Semiconductor	1
16	D1	1 A/ 800 V	UF4006-E3/54	VISHAY	1
17	D2	0.2 A/200 V	1N485B	Fairchild	1
18	D151	3 A/150 V	STPS3150	ST	1
19	D101	3 A/60 V	MBR360	Vishay	1
20	IC1	ICE5GR4780AG	ICE5GR4780AG	Infineon	1
21	L1	39 mH/0.7 A	B82732R2701B030	EPCOS/TDK	1
22	L101, L151	2.2 uH/4.3 A	744 746 202 2	Wurth Electronics	2
23	R1A, R1B	3 MΩ/0.25 W/5%/1206			2
24	R2A, R2B, R2C	15 MΩ/0.25 W/5%/1206	RC1206JR-0715ML	Yageo	3
25	R3A, R3B, R3C	3 MΩ/0.25 W/1%/1206	RC1206FR-073ML	Yageo	3
26	R4	68 kR/2 W/500 V	MO2CT631R683J	KOA Speer	1
27	R5	4.7 Ω/0.1 W/5%/0603	RC0603JR-074R7L	Yageo	1
28	R6	0 Ω/0603	RC0603JR-070R	Yageo	1
29	R7	58.3 kR/0.1 W/0.5%/0603	RT0603DRE0758K3L	Yageo	1
30	R8A	1.8 R/0.25 W/±1%/1206			1
31	R8B	1.6R/0.25 W/±1%/1206			1
32	R9	260 kΩ/0.1 W/0603			1
33	R11	27 kΩ/0.1 W/1%/0603			1
34	R154	33 kΩ/0.1 W/1%/0603			1
35	R103	82 kΩ/0.1 W/1%/0603			1
36	R104	4.7 kΩ/0.1 W/1%/0603			1
37	R153	523 kΩ/0.1 W/1%/0603			1
38	R102	11 kΩ/0.25 W/5%/1206			1
39	R152	20 kΩ/0.25 W/5%/1206			1
40	T1	350 uH, EE16_H	750343543 (Rev 03)	Wurth Electronics	1
41	CN1	Connector	691102710002	Wurth Electronics	1
42	CN2,CN3	Connector	691 412 120 002B	Wurth Electronics	2

43	JP1-JP3	Jumper			3
44	PCB	110 mm × 66 mm (L × W), single layer, 1OZ, FR-4			1

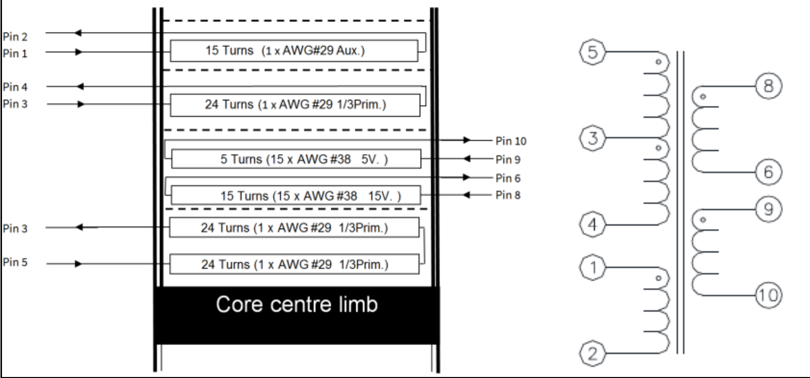
9 Transformer construction

Core and materials: EE16/7/5, TP4A (TDG)

Bobbin: 070-5472 (10-pin EXT, THT, horizontal version)

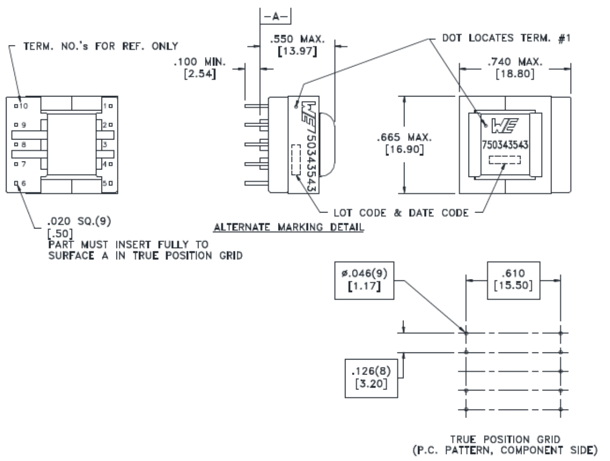
Primary inductance: Lp = 350 µH (±10%), measured between pin 4 and pin 5

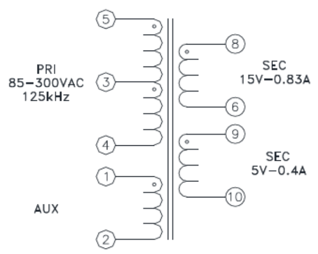
Manufacturer and part number: Wurth Electronics Midcom (750343543 R03)



Start	Stop	No. of turns	Wire size	Layer
5	-	24	1 x AWG#29	1/3 Primary
-	3	24	1 x AWG#29	1/3 Primary
8	6	15	15 x AWG #38	15V
9	10	5	15 x AWG #38	5V
3	4	24	1 x AWG#29	1/3 Primary
1	2	15	1 x AWG#29	Auxiliary

CUSTOMER TERMINAL	RoHS	LEAD(Pb)-FREE
Sn 96%, Ag 4%	Yes	Yes





WÜRTH ELEKTRONIK

ELECTRICAL SPECIFICATIONS @ 25° C unless otherwise noted:

PARAMETER		TEST CONDITIONS	VALUE
D.C. RESISTANCE	4-5	@20ºC	0.626ohms max.
D.C. RESISTANCE	1-2	@20ºC	0.171ohms max.
D.C. RESISTANCE	6-8	@20ºC	0.075ohms max.
D.C. RESISTANCE	9-10	@20ºC	0.033ohms max.
INDUCTANCE	4-5	100kHz, 100mV, Ls	350.00µH ±10%
LEAKAGE INDUCTANCE	4-5	tie(1+2+6+8+9+10),100kHz, 100mV, Ls	8.0µH max.
DIELECTRIC	5-6	tie(2+3,8+9), 1875VAC, 1 second	
DIELECTRIC	2-3	625VAC, 1 second	
TURNS RATIO		(5-4):(8-6)	4.8:1, ±2%
TURNS RATIO		(5-4):(9-10)	14.4:1, ±2%
TURNS RATIO		(5-4):(1-2)	4.8:1, ±2%

GENERAL SPECIFICATIONS:

OPERATING TEMPERATURE RANGE: -40°C to +125°C including temp rise.

Wire insulation & RoHS status not affected by wire color. Wire insulation color may vary depending on availability.

DFM		Packaging Specifications	CONVENTION PLACEMENT	Tolerances unless otherwise specified:	DRAWING TITLE	PART NO.
DATE		Method: Tray		Angles: ±1° Decimals: ±.005 [.13]	TRANSFORMER	750343543
ENG	IYU	PKG-0887		Fractions: ±1/64 Footprint: ± .001 [.03]		
REV.	02			This drawing is dual dimensioned. Dimensions in brackets are in millimeters.		
DATE	5/2/2017	www.we-online.com/midcom				SPECIFICATION SHEET 1 OF 1

Figure 7 Transformer structure

10 Test results

10.1 Efficiency, regulation and output ripple

Table 4 Efficiency, regulation and output ripple

Input (V AC/Hz)	P_{in} (W)	15 V (V)	I_{out_15V} (mA)	5 V (V)	I_{out_5V} (mA)	15 V_{RPP} (mV)	5 V_{RPP} (mV)	P_{out} (W)	Efficiency (η) (%)	Average η (%)	OLP pin (W)	OLP I_{out15V} (fixed 5 V at 0.4 A) (A)
85 V AC/60 Hz	0.0320	15.24	0	4.98	0	30	17				26.4	1.23
	0.114	17.15	0	4.78	12	22	44	0.06				
	4.430	15.06	207.5	5.00	100	34	9	3.62	81.83	81.72		
	8.81	15.08	415	5.00	200	41	10	7.26	82.39			
	13.29	15.10	622.5	5.00	300	50	11	10.90	82.01			
	18.02	15.10	830	5.00	400	57	13	14.53	80.65			
115 V AC/60 Hz	0.0370	15.26	0	4.98	0	32	18				25.5	1.26
	0.116	17.24	0	4.78	12	23	45	0.06				
	4.400	15.02	207.5	5.00	100	34	11	3.62	82.20	82.87		
	8.71	15.08	415	5.00	200	44	14	7.26	83.33			
	13.11	15.11	622.5	5.00	300	55	15	10.91	83.19			
	17.58	15.12	830	5.00	400	60	14	14.55	82.76			
230 V AC/50 Hz	0.045	15.24	0	4.99	0	39	20				25.9	1.33
	0.128	17.22	0	4.78	12	29	52	0.06				
	4.510	15.07	207.5	5.00	100	36	14	3.63	80.42	82.3		
	8.84	15.09	415	5.00	200	44	14	7.26	82.15			
	13.11	15.11	622.5	5.00	300	52	16	10.91	83.19			
	17.43	15.11	830	5.00	400	63	15	14.54	83.43			
265 V AC/50 Hz	0.051	15.25	0	4.99	0	41	20				26.4	1.36
	0.135	17.23	0	4.78	12	31	55	0.06				
	4.590	15.05	207.5	5.00	100	38	14	3.62	78.93	81.52		
	8.93	15.09	415	5.00	200	45	14	7.26	81.33			
	13.21	15.12	622.5	5.00	300	50	14	10.91	82.61			
	17.49	15.13	830	5.00	400	61	15	14.56	83.24			
300 V AC/50 Hz	0.060	15.38	0	5.05	0	44	22				27.1	1.40
	0.146	17.35	0	4.77	12	31	60	0.06				
	4.660	15.03	207.5	5.00	100	36	13	3.62	77.66	80.64		
	9.04	15.07	415	5.00	200	47	13	7.25	80.24			
	13.38	15.23	622.5	5.00	300	52	14	10.98	82.07			
	17.64	15.14	830	5.00	400	65	16	14.57	82.57			

60 mW load condition: 5 V @ 12 mA and 15 V @ 0 mA

Maximum load condition: 5 V @ 400 mA and 15 V @ 830 mA

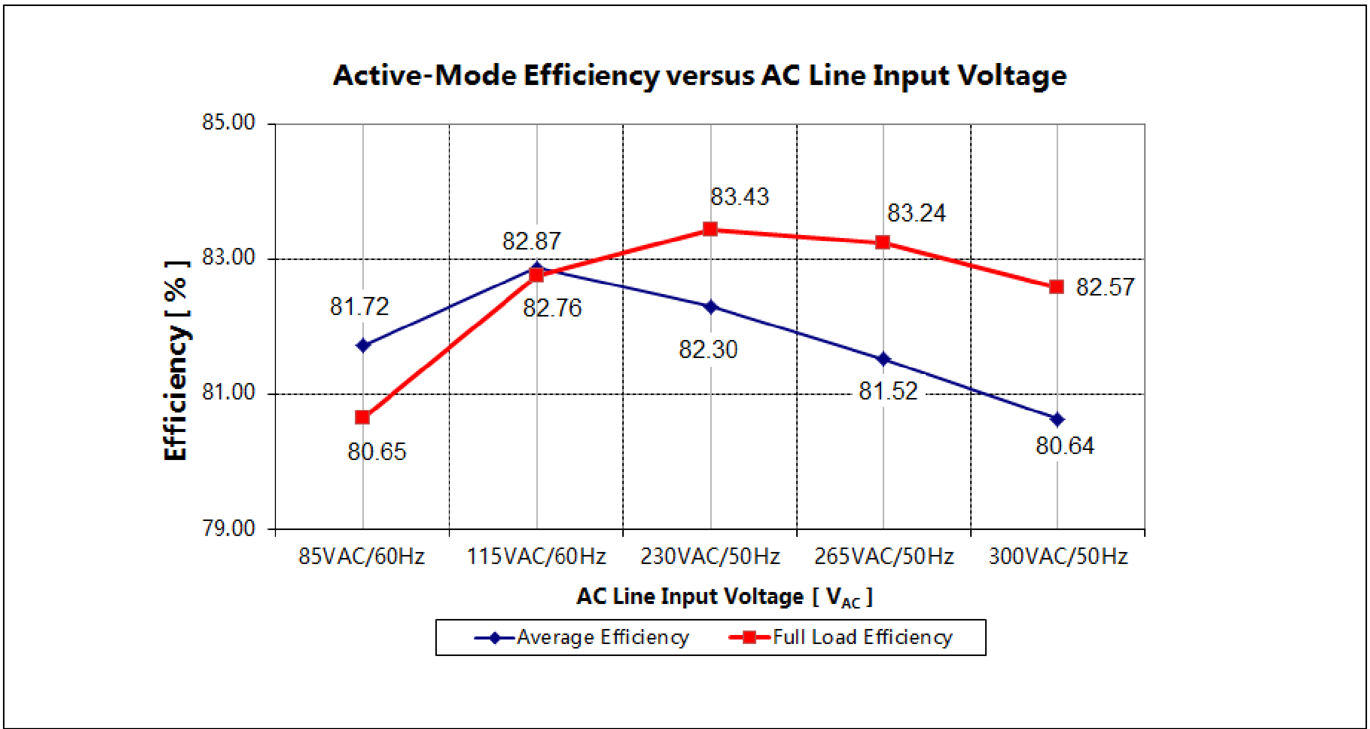


Figure 8 Efficiency vs AC-line input voltage

10.2 Standby power

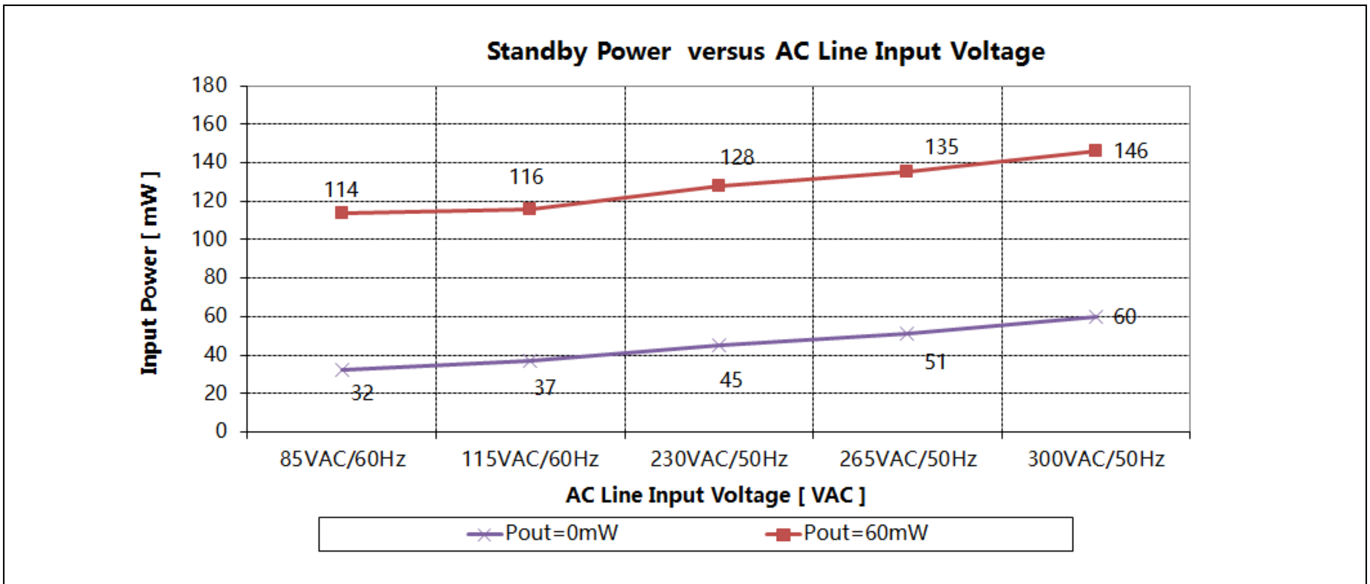


Figure 9 Standby power at no load vs AC-line input voltage (measured by Yokogawa WT210 power meter – integration mode)

10.3 Line regulation

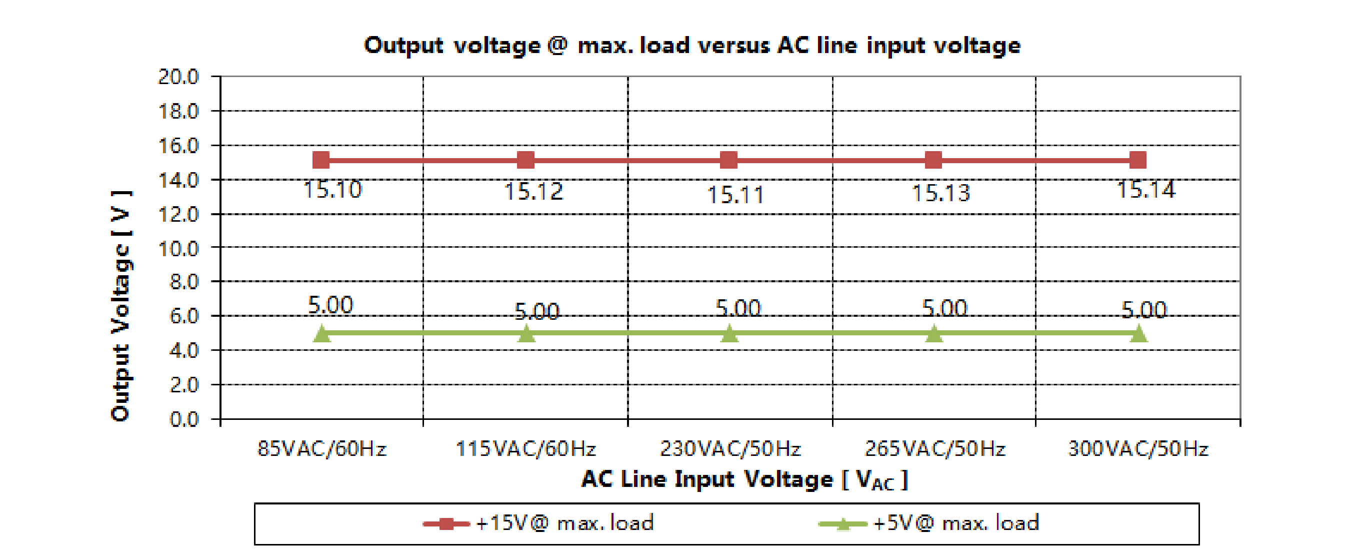


Figure 10 Line regulation V_{Out} at full load vs AC-line input voltage

10.4 Load regulation

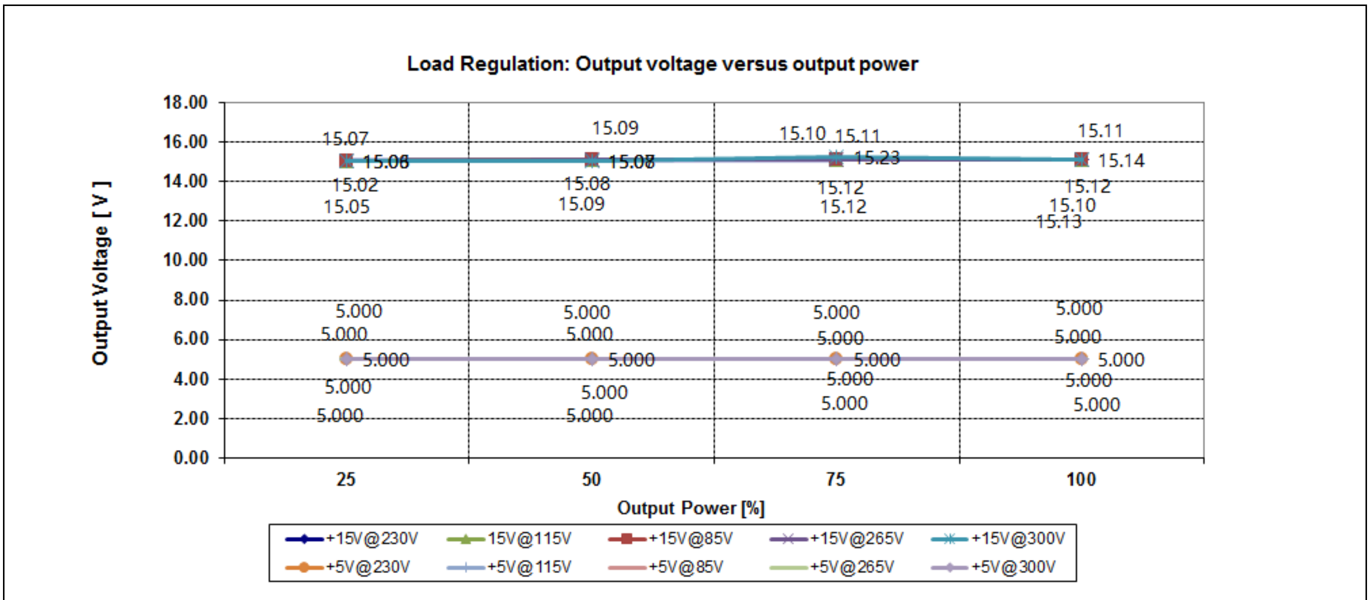


Figure 11 Load regulation V_{Out} vs output power

10.5 Maximum input power

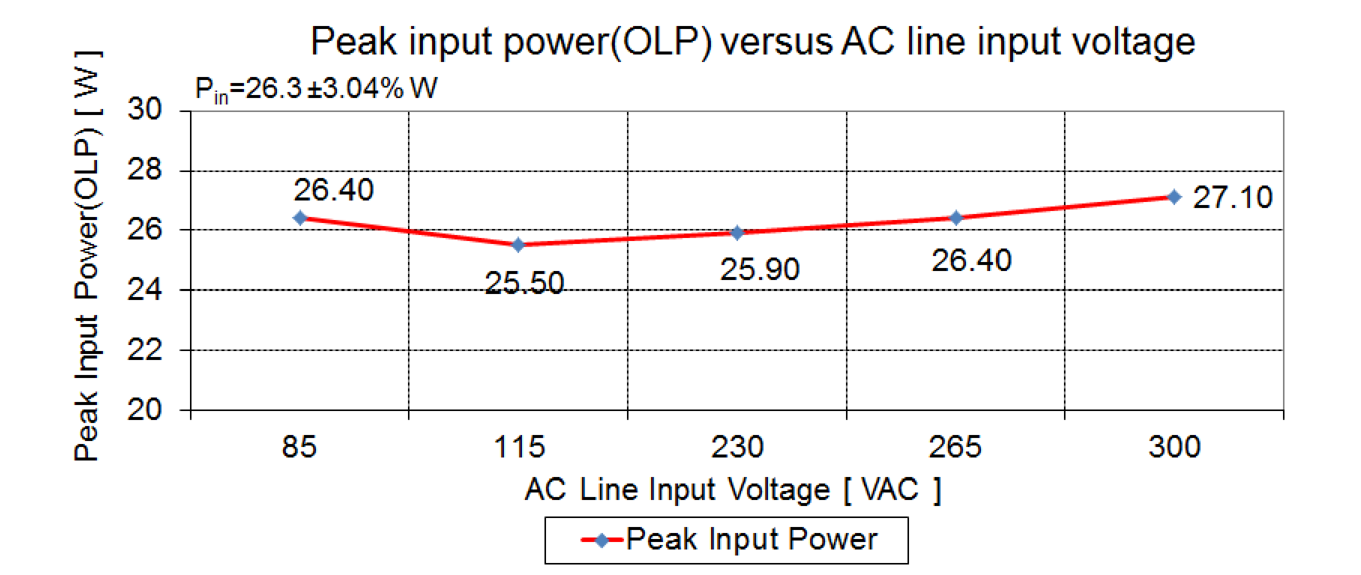


Figure 12 Maximum input power (before over-load protection) vs AC-line input voltage

10.6 Surge immunity (EN 61000-4-5)

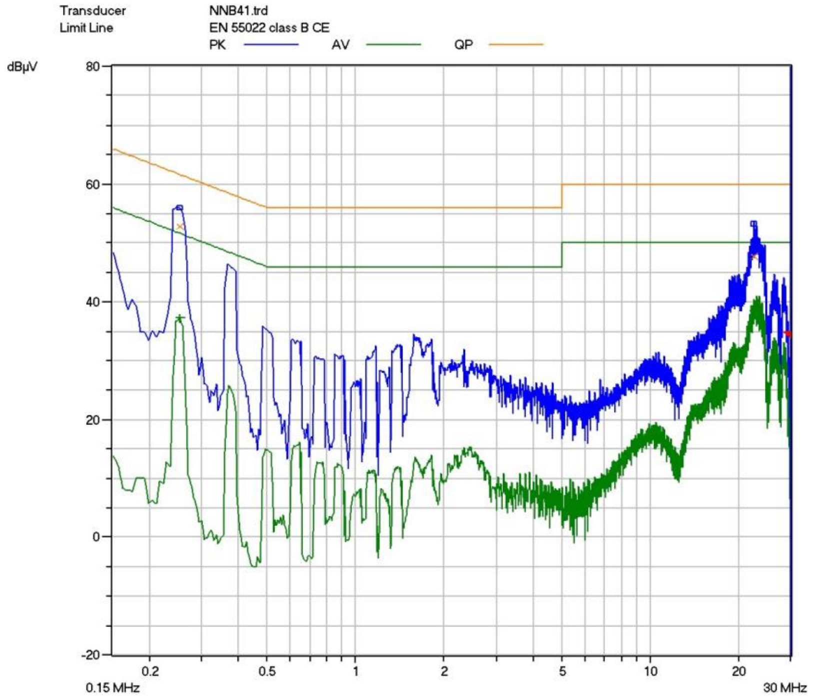
Pass EN 61000-4-5 installation class 4 (±2 kV for line-to-line)[1].

10.7 Conducted emissions (EN 55022 class B)

The conducted EMI was measured by Schaffner (SMR4503) and followed the test standard of EN 55022 (CISPR 22) class B. The demo board was set up at maximum load (14.45 W) with an input voltage of 115 V AC and 230 V AC.

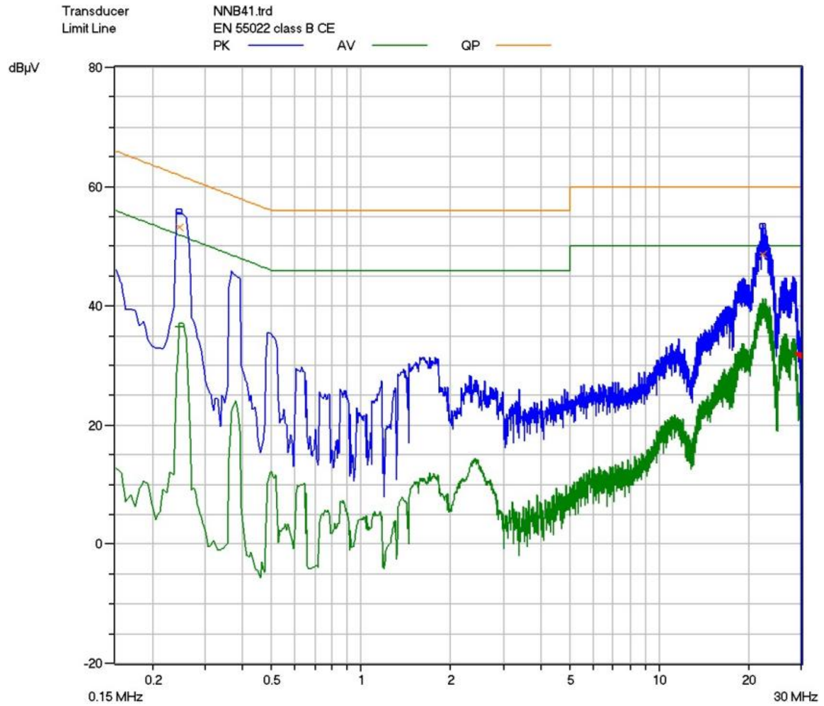
Pass conducted emissions EN 55022 (CISPR 22) class B with 8.7 dB margin at low-line (115 V AC) and with 7.4 dB margin for high-line (230 V AC).

[1] PCB spark-gap distance needs to reduce to 0.5 mm.



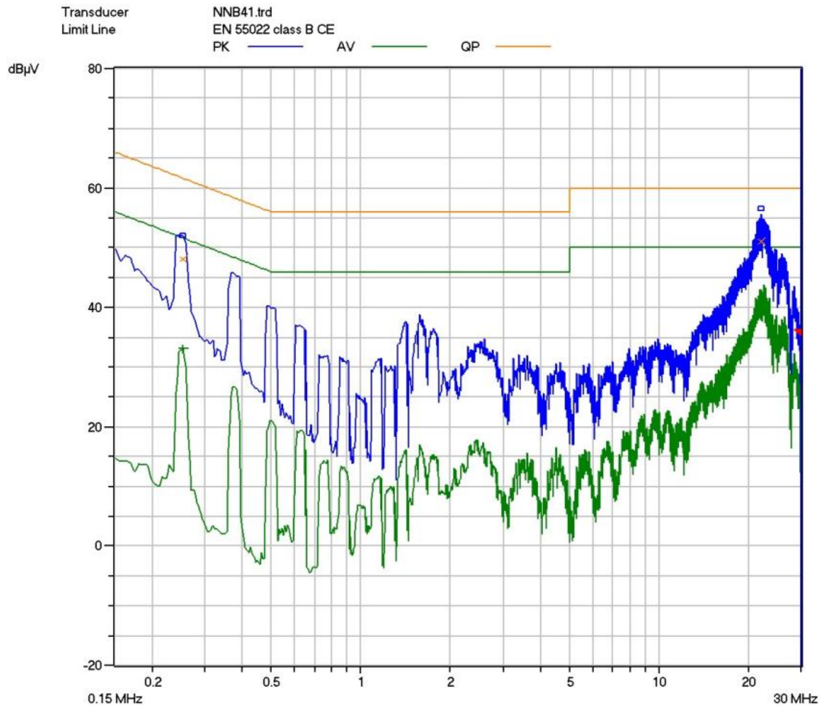
Frequency		Level Pk		Level AV		Level QP	Limit AV	Limit QP	Margin
0.2520	N	56.1	N	37.3	N	52.9	51.7	61.7	-8.8dB
22.4000	N	53.2	N	38.4	N	47.7	50.0	60.0	

Figure 13 Conducted emissions (line) at 115 V AC and maximum load



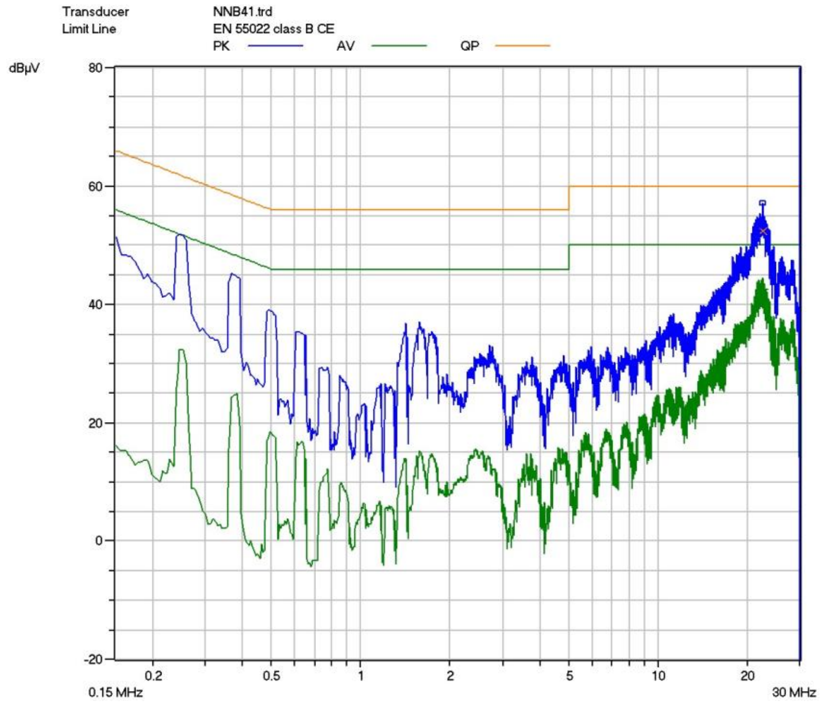
Frequency		Level Pk		Level AV		Level QP	Limit AV	Limit QP	Margin
0.2460	N	55.8	N	36.5	N	53.2	51.9	61.9	-8.7dB
22.1840	N	53.4	N	39.5	N	48.6	50.0	60.0	

Figure 14 Conducted emissions (neutral) at 115 V AC and maximum load



Frequency		Level Pk		Level AV		Level QP	Limit AV	Limit QP	Margin
0.2520	L	52.1	L	33.2	L	48.2	51.7	61.7	
21.9760	L	56.6	L	41.0	L	51.1	50.0	60.0	-8.9dB

Figure 15 Conducted emissions (line) at 230 V AC and maximum load



Frequency		Level Pk		Level AV		Level QP	Limit AV	Limit QP	Margin
22.3920	N	57.3	N	42.6	N	52.5	50.0	60.0	-7.4dB

Figure 16 Conducted emissions (neutral) at 230 V AC and maximum load

10.8 Thermal measurements

The thermal testing of the open-frame demo board was done using an infrared thermography camera (FLIR-T62101) at an ambient temperature of 25°C. The measurements were taken after one hour running at full load.

Table 5 Hottest temperature of demo board

No.	Major component	85 V AC (°C)	300 V AC (°C)
1	IC1 (ICE5GR4780AG)	87.8	74.6
2	L1 (choke)	44.7	30.4
3	T1 (transformer)	62.5	69.9
4	D151 (15 V diode)	62.1	67.2

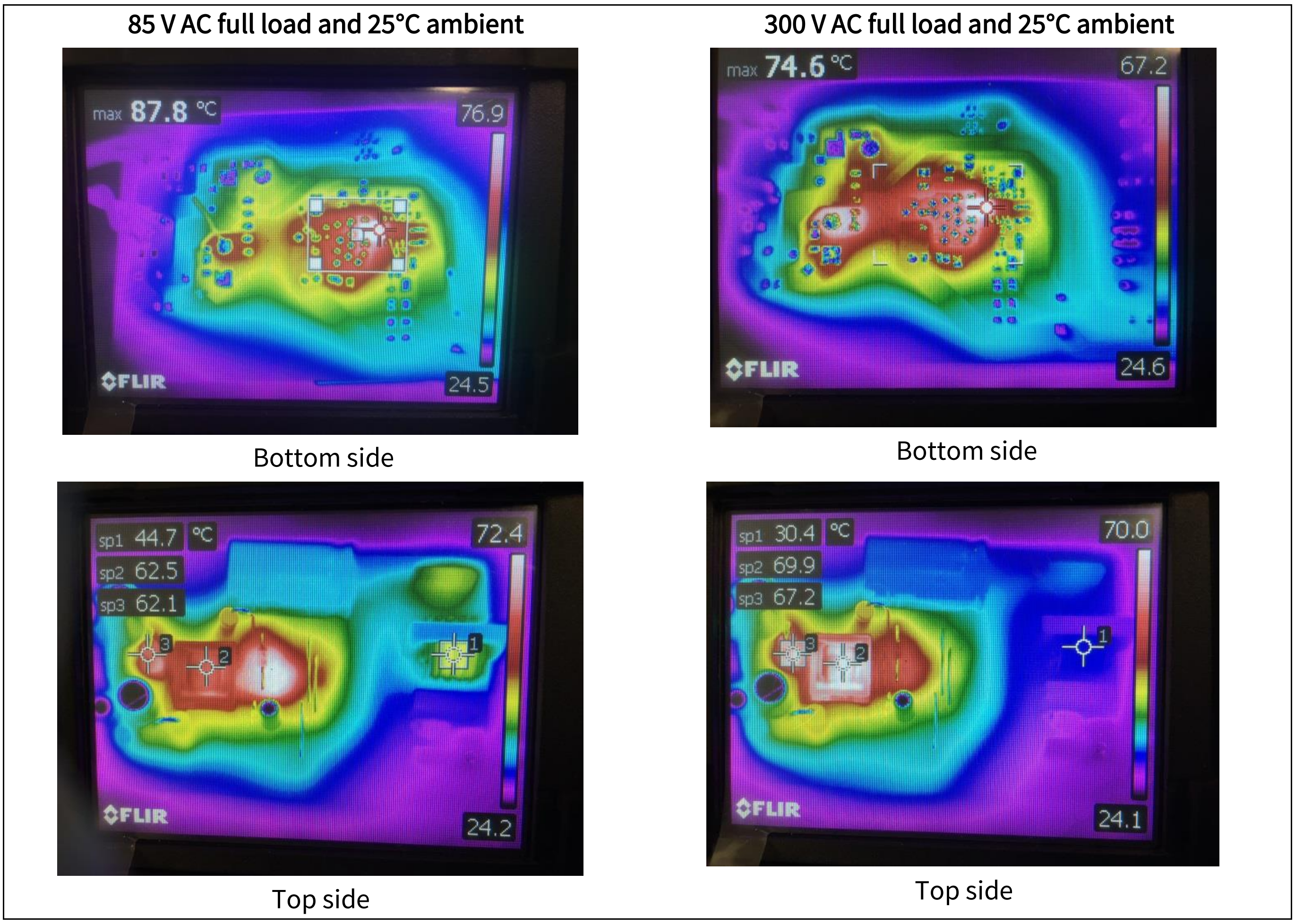


Figure 17 Infrared thermal image of DEMO_5GR4780AG_14W1

11 Waveforms and scope plots

All waveforms and scope plots were recorded with a Teledyne LeCroy 606Zi oscilloscope.

11.1 Start-up at low/high AC-line input voltage with maximum load

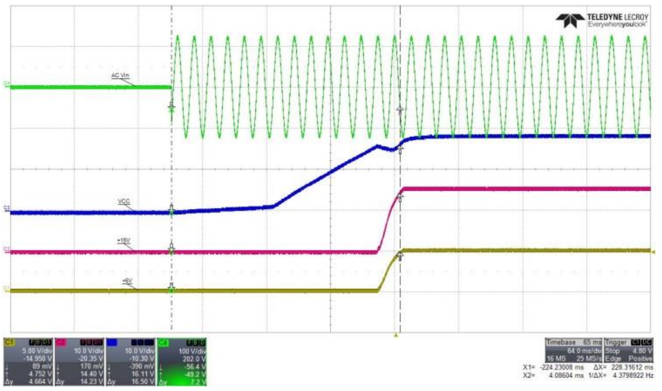
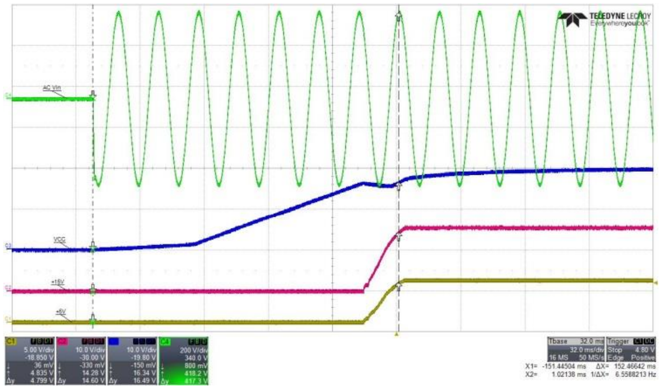
	
C1 (yellow) : 5 V output voltage (V_{Out5}) C2 (purple) : 15 V output voltage (V_{Out15}) C3 (blue) : Supply voltage (V_{VCC}) C4 (green) : AC-line voltage (V AC)	C1 (yellow) : 5 V output voltage (V_{Out5}) C2 (purple) : 15 V output voltage (V_{Out15}) C3 (blue) : Supply voltage (V_{VCC}) C4 (green) : AC-line voltage (V AC)
Start-up time at 85 V AC and maximum load ≈ 228 ms	Start-up time at 300 V AC and maximum load ≈ 152 ms

Figure 18 Start-up

11.2 Soft-start

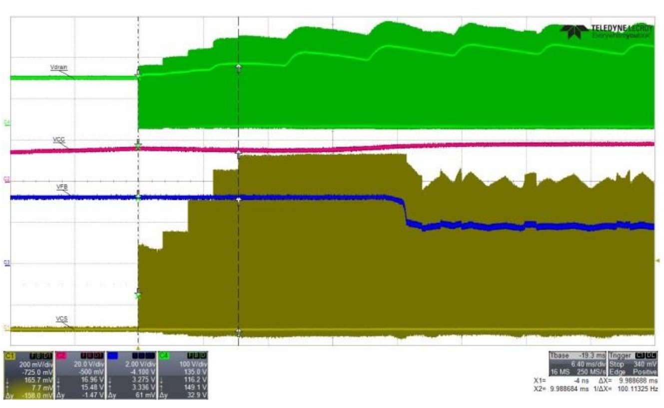
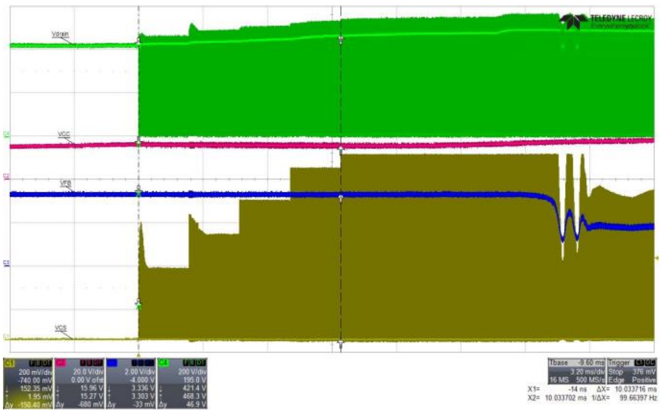
	
C1 (yellow) : CS voltage (V_{CS}) C2 (purple) : Supply voltage (V_{VCC}) C3 (blue) : FB voltage (V_{FB}) C4 (green) : Drain voltage (V_D)	C1 (yellow) : CS voltage (V_{CS}) C2 (purple) : Supply voltage (V_{VCC}) C3 (blue) : FB voltage (V_{FB}) C4 (green) : Drain voltage (V_D)
Soft-start time at 85 V AC and maximum load ≈ 10 ms	Soft-start time at 300 V AC and maximum load ≈ 10 ms

Figure 19 Soft-start

11.3 Drain and CS voltage at maximum load

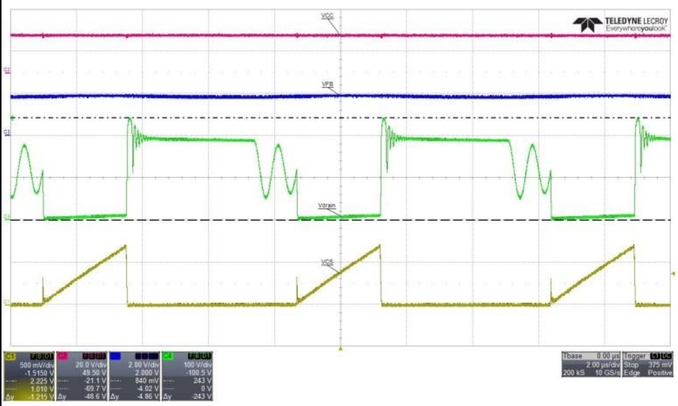
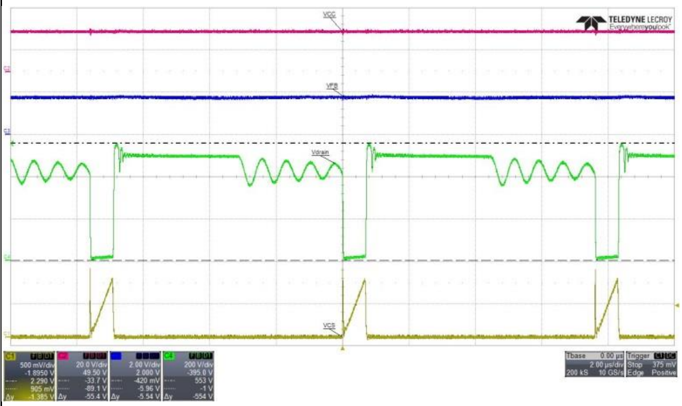
	
C1 (yellow) : CS voltage (V_{CS}) C2 (purple) : Supply voltage (V_{VCC}) C3 (blue) : FB voltage (V_{FB}) C4 (green) : Drain voltage (V_D)	C1 (yellow) : CS voltage (V_{CS}) C2 (purple) : Supply voltage (V_{VCC}) C3 (blue) : FB voltage (V_{FB}) C4 (green) : Drain voltage (V_D)
V_{Drain_peak} at 85 V AC ≈ 243 V	V_{Drain_peak} at 300 V AC ≈ 554 V

Figure 20 Drain and CS voltage at maximum load

11.4 Frequency jittering

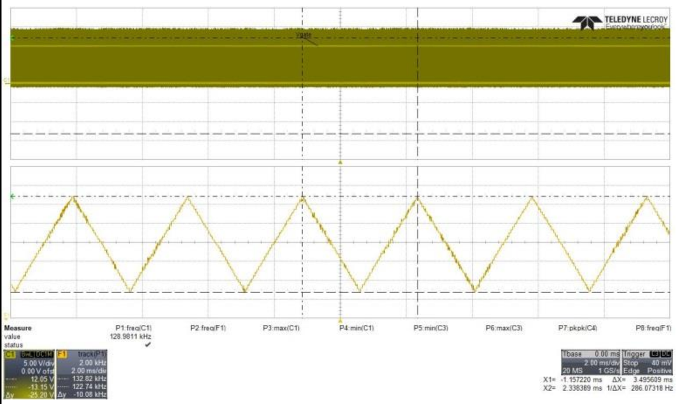
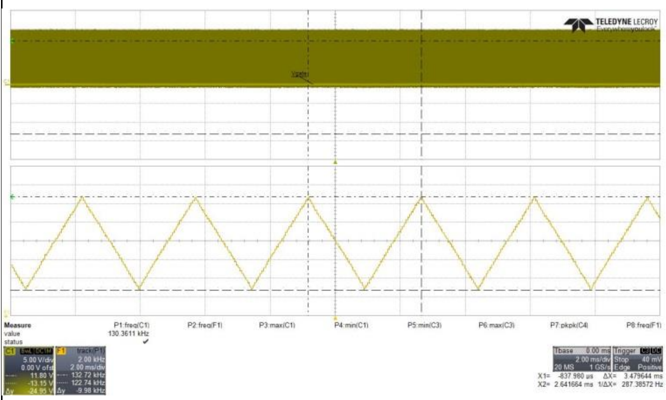
	
C1 (yellow) : Gate voltage (V_G) F1 (yellow) : Frequency track of gate (V_{GATE})	C1 (yellow) : Gate voltage (V_G) F1 (yellow) : Frequency track of gate (V_{GATE})
Frequency jittering at 85 V AC and maximum load ≈ 122 kHz ~ 132 kHz, jitter period ≈ 3.5 ms	Frequency jittering at 300 V AC and maximum load ≈ 122 kHz ~ 132 kHz, jitter period ≈ 3.5 ms

Figure 21 Frequency jittering

11.5 Load transient response (dynamic load from 10% to 100%)

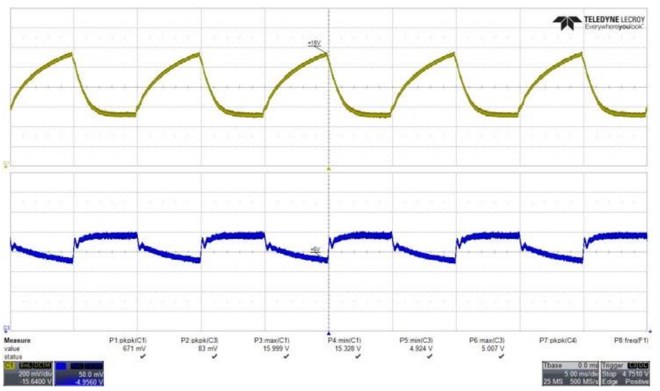
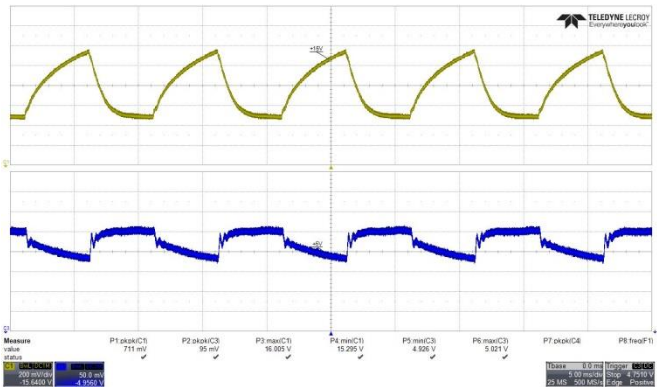
	
C1 (yellow) : 15 V output ripple voltage (V_{Out15}) C3 (blue) : 5 V output ripple voltage (V_{Out5})	C1 (yellow) : 15 V output ripple voltage (V_{Out15}) C3 (blue) : 5 V output ripple voltage (V_{Out5})
15 $V_{ripple\_pk\_pk}$ at 85 V AC ≈ 671 mV 5 $V_{ripple\_pk\_pk}$ at 85 V AC ≈ 83 mV (15 V load change from 10% to 100% and 5 V at 400 mA load at 85 V AC, 100 Hz, 0.4 A/µs slew rate) Probe terminal end with decoupling capacitor of 0.1 µF (ceramic) and 1 µF (electrolytic), 20 MHz filter	15 $V_{ripple\_pk\_pk}$ at 300 V AC ≈ 711 mV 5 $V_{ripple\_pk\_pk}$ at 300 V AC ≈ 95 mV (15 V load change from 10% to 100% and 5 V at 400 mA load at 85 V AC, 100 Hz, 0.4 A/µs slew rate) Probe terminal end with decoupling capacitor of 0.1 µF (ceramic) and 1 µF (electrolytic), 20 MHz filter

Figure 22 Load transient response

11.6 Output ripple voltage at maximum load

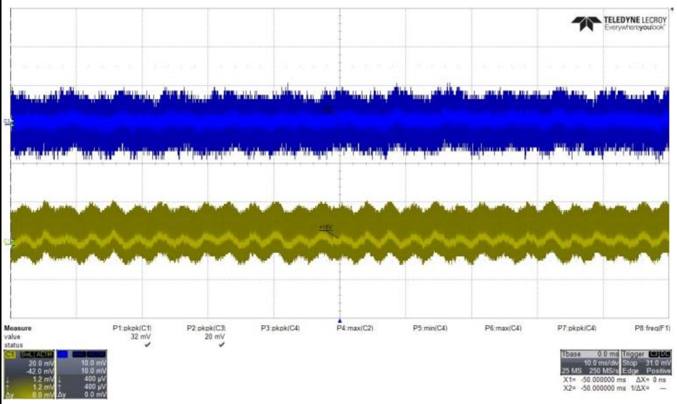
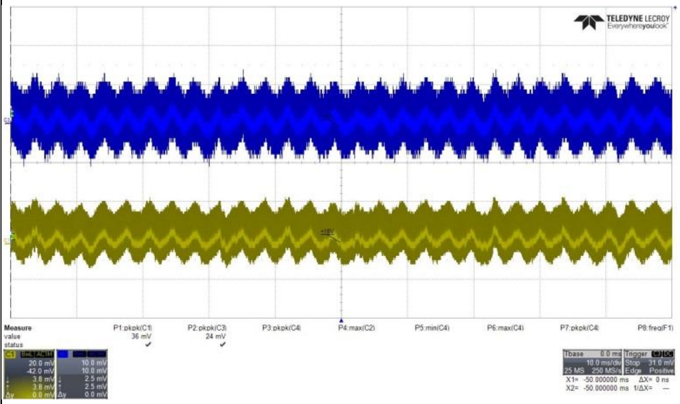
	
C1 (yellow) : 15 V output ripple voltage (V_{Out15}) C3 (blue) : 5 V output ripple voltage (V_{Out5})	C1 (yellow) : 15 V output ripple voltage (V_{Out15}) C3 (blue) : 5 V output ripple voltage (V_{Out5})
15 $V_{ripple\_pk\_pk}$ at 85 V AC ≈ 32 mV 5 $V_{ripple\_pk\_pk}$ at 85 V AC ≈ 20 mV Probe terminal end with decoupling capacitor of 0.1 µF (ceramic) and 1 µF (electrolytic), 20 MHz filter	15 $V_{ripple\_pk\_pk}$ at 300 V AC ≈ 36 mV 5 $V_{ripple\_pk\_pk}$ at 300 V AC ≈ 34 mV Probe terminal end with decoupling capacitor of 0.1 µF (ceramic) and 1 µF (electrolytic), 20 MHz filter

Figure 23 Output ripple voltage at maximum load

11.7 Output ripple voltage at ABM 1 W load

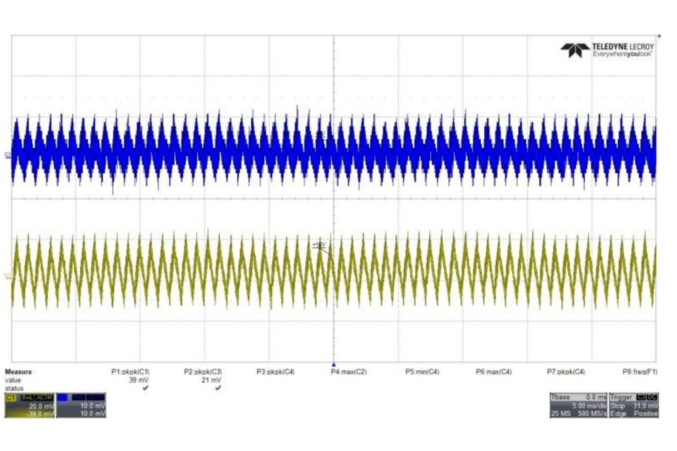
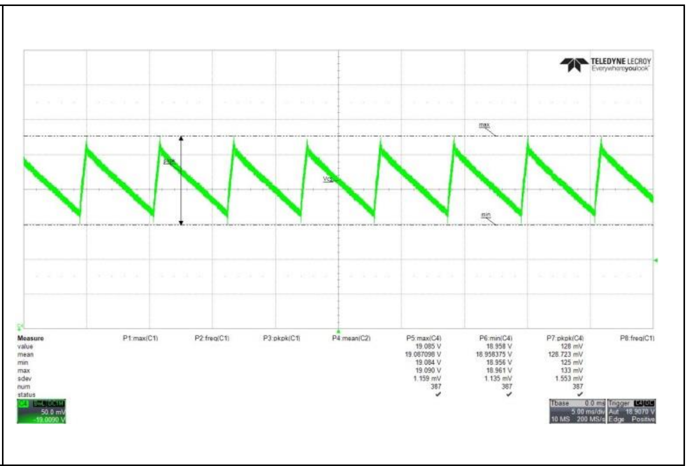
	
C1 (yellow) : 15 V output ripple voltage (V_{Out15}) C3 (blue) : 5 V output ripple voltage (V_{Out5})	C1 (yellow) : 15 V output ripple voltage (V_{Out15}) C3 (blue) : 5 V output ripple voltage (V_{Out5})
15 $V_{ripple\_pk\_pk}$ at 85 V AC ≈ 21 mV 5 $V_{ripple\_pk\_pk}$ at 85 V AC ≈ 39 mV Probe terminal end with decoupling capacitor of 0.1 µF (ceramic) and 1 µF (electrolytic), 20 MHz filter	15 $V_{ripple\_pk\_pk}$ at 300 V AC ≈ 30 mV 5 $V_{ripple\_pk\_pk}$ at 300 V AC ≈ 56 mV Probe terminal end with decoupling capacitor of 0.1 µF (ceramic) and 1 µF (electrolytic), 20 MHz filter

Figure 24 Output ripple voltage at ABM 0.8 W load

11.8 Entering ABM

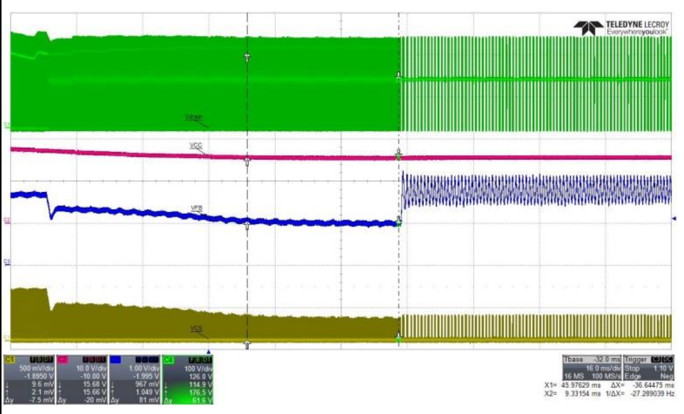
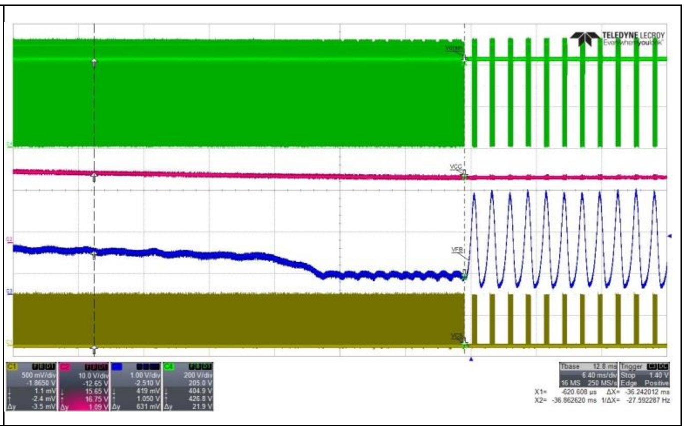
	
C1 (yellow) : CS voltage (V_{CS}) C2 (purple) : Supply voltage (V_{VCC}) C3 (blue) : FB voltage (V_{FB}) C4 (green) : Drain voltage (V_D)	C1 (yellow) : CS voltage (V_{CS}) C2 (purple) : Supply voltage (V_{VCC}) C3 (blue) : FB voltage (V_{FB}) C4 (green) : Drain voltage (V_D)
Condition to enter ABM level 3: V_{FB} < 1.03 V and $t_{blanking}$ = 36 ms (load change from full load to 0.8 W load at 85 V AC)	Condition to enter ABM level 3: V_{FB} < 1.03 V and $t_{blanking}$ = 36 ms (load change from full load to 0.8 W load at 300 V AC)

Figure 25 Entering ABM

11.9 During ABM

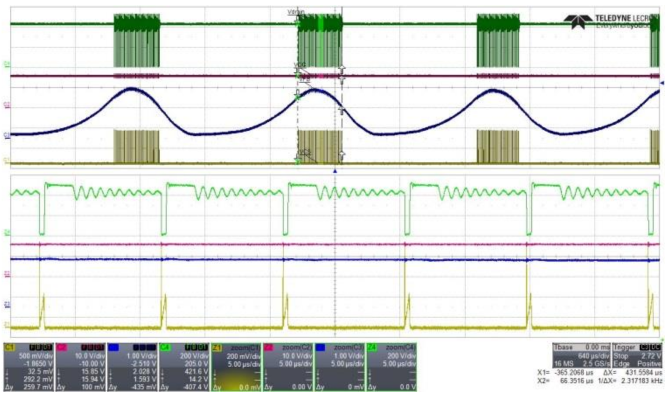
	
C1 (yellow) : CS voltage (V_{CS}) C2 (purple) : Supply voltage (V_{VCC}) C3 (blue) : FB voltage (V_{FB}) C4 (green) : Drain voltage (V_D)	C1 (yellow) : CS voltage (V_{CS}) C2 (purple) : Supply voltage (V_{VCC}) C3 (blue) : FB voltage (V_{FB}) C4 (green) : Drain voltage (V_D)
During ABM level 3: $V_{FB\_Bon\_NISO}$ = 1.95 V, $V_{FB\_BOff\_NISO}$ = 1.55 V, V_{CS_BHP} = 0.27 V (0.8 W load at 85 V AC)	During ABM level 3: $V_{FB\_Bon\_NISO}$ = 1.95 V, $V_{FB\_BOff\_NISO}$ = 1.55 V, V_{CS_BHP} = 0.27 V (0.8 W load at 300 V AC)

Figure 26 During ABM

11.10 Leaving ABM

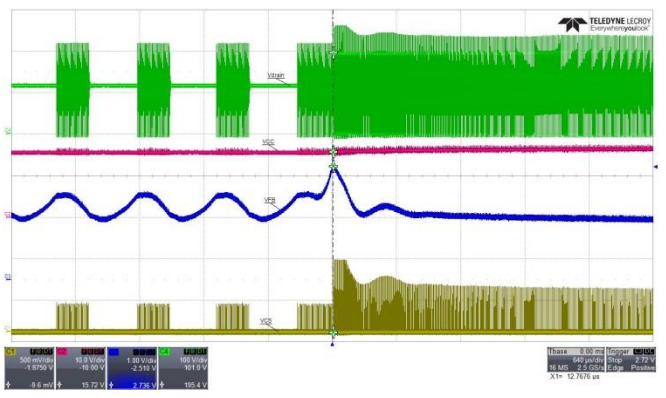
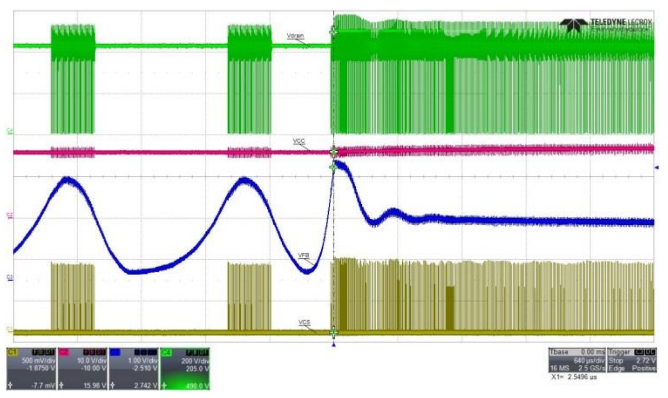
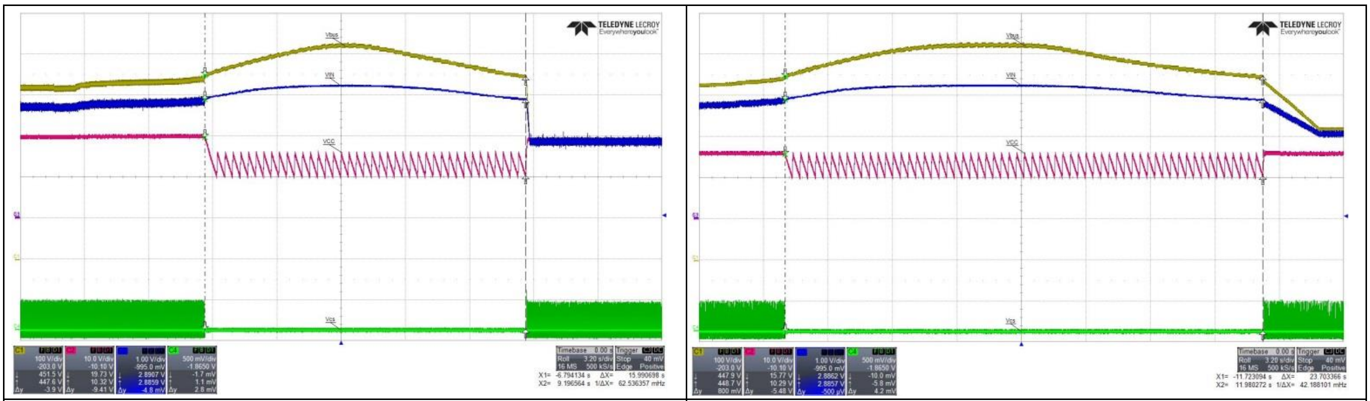
	
C1 (yellow) : CS voltage (V_{CS}) C2 (purple) : Supply voltage (V_{VCC}) C3 (blue) : FB voltage (V_{FB}) C4 (green) : Drain voltage (V_D)	C1 (yellow) : CS voltage (V_{CS}) C2 (purple) : Supply voltage (V_{VCC}) C3 (blue) : FB voltage (V_{FB}) C4 (green) : Drain voltage (V_D))
Condition to leave ABM level 3: V_{FB} >2.73 V (load change from 0.8 W to full load at 85 V AC)	Condition to leave ABM level 3: V_{FB} > 2.75 V (load change from 0.8 W to full load at 300 V AC)

Figure 27 Leaving ABM

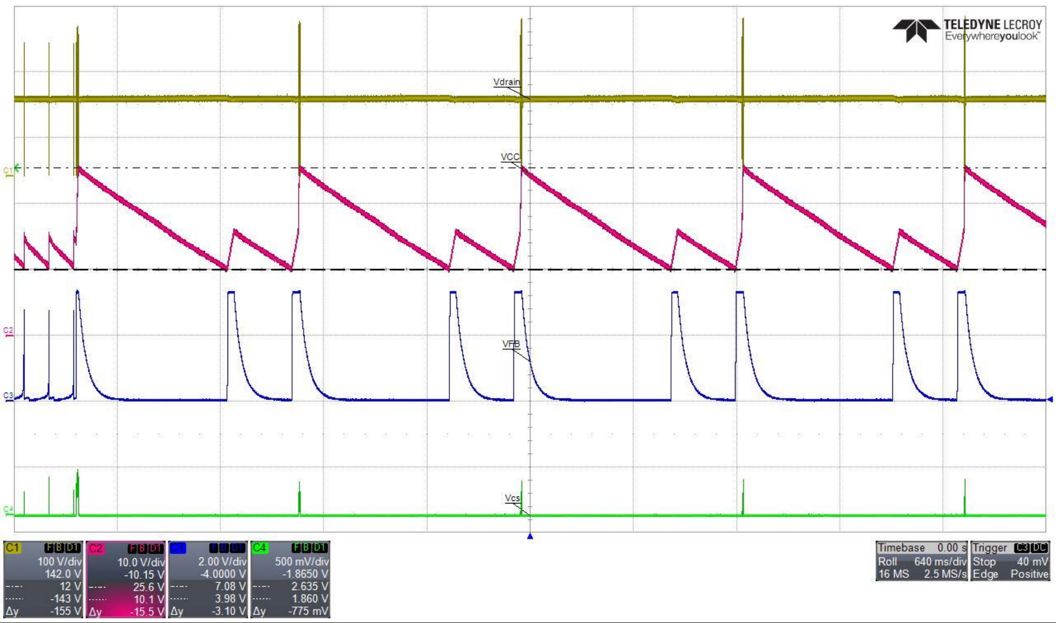
11.11 Line OVP (non-switch auto restart)



C1 (yellow) : Bus voltage (V_{Bus}) C2 (purple) : Supply voltage (V_{VCC}) C3 (blue) : V_{IN} voltage (V_{VIN}) C4 (green) : CS voltage (V_{CS})	C1 (yellow) : Bus voltage (V_{Bus}) C2 (purple) : Supply voltage (V_{VCC}) C3 (blue) : V_{IN} voltage (V_{VIN}) C4 (green) : CS voltage (V_{CS})
Condition to detect line OVP : V_{VIN} > 2.85 V (V_{BULK} > 447 V DC [≈ 320 V AC]) Condition to reset line OVP : V_{VIN} < 2.85 V (V_{BULK} < 447 V)	
(Gradually increase AC-line voltage at full load until line OVP detect and decrease AC-line until line OVP reset)	(Gradually increase AC-line voltage at 0.8 W load until line OVP detect and decrease AC-line until line OVP reset)

Figure 28 Line OVP

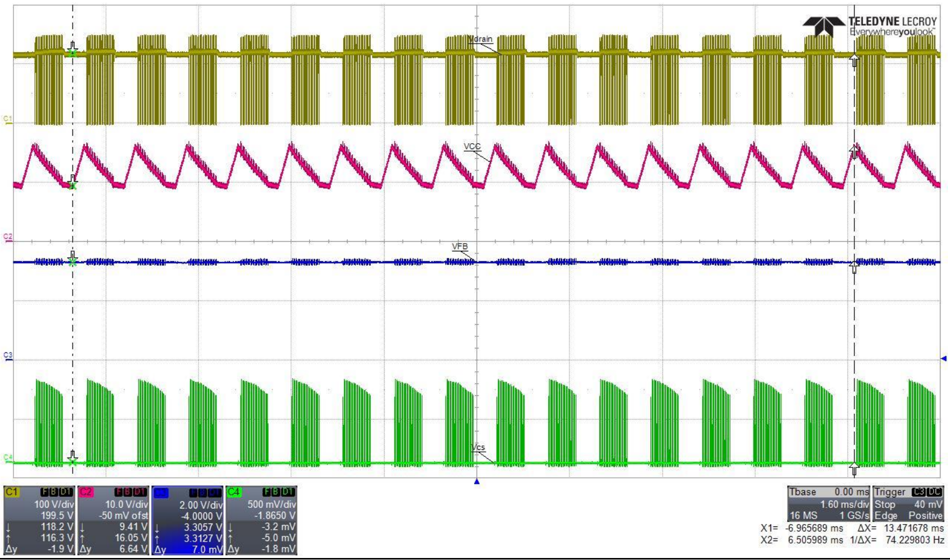
11.12 V_{CC} OVP (odd-skip auto restart)



C1 (yellow) : Drain voltage (V_D) C2 (purple) : Supply voltage (V_{VCC}) C3 (blue) : FB voltage (V_{FB}) C4 (green) : CS voltage (V_{CS})
Condition to enter V_{CC} OVP: V_{VCC} > 25.5 V (remove ZD1, R103 and R153 while system operating at 85 V AC and no load)

Figure 29 V_{CC} OVP

11.13 V_{CC} UV protection (auto restart)



C1 (yellow) : Drain voltage (V_D)
C2 (purple) : Supply voltage (V_{VCC})
C3 (blue) : FB voltage (V_{FB})
C4 (green) : CS voltage (V_{CS})

Condition to enter V_{CC} UV protection: V_{CC} < 10 V
(remove R5 and power on the system with full load at 85 V AC)

Figure 30 V_{CC} UV protection

11.14 Over-load protection (odd-skip auto restart)

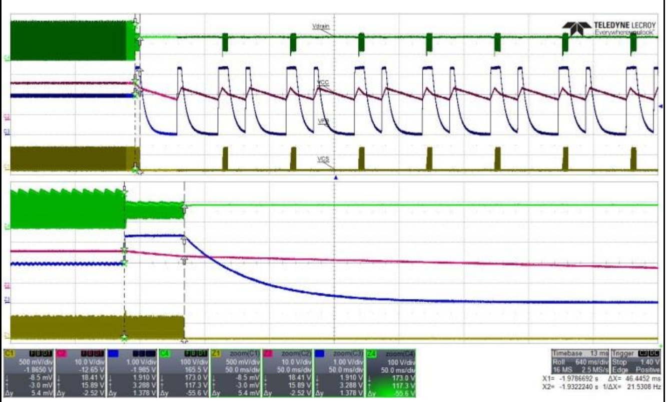
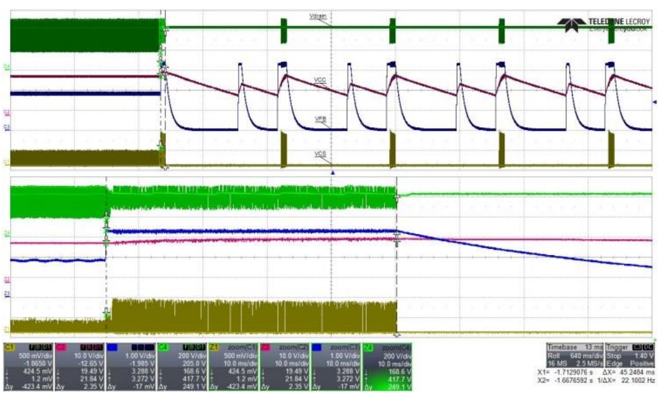
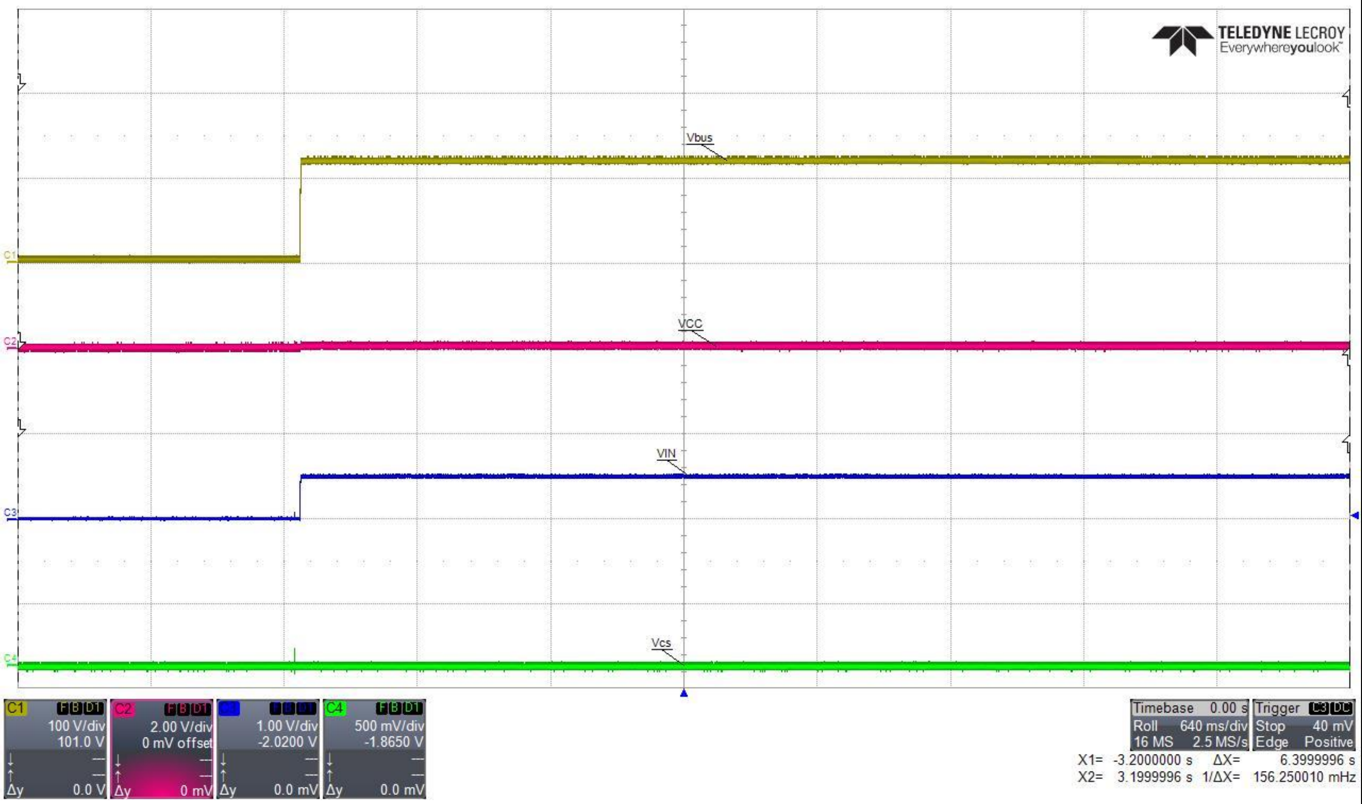
	
C1 (yellow) : CS voltage (V_{CS}) C2 (purple) : Supply voltage (V_{VCC}) C3 (blue) : FB voltage (V_{FB}) C4 (green) : Drain voltage (V_D)	C1 (yellow) : CS voltage (V_{CS}) C2 (purple) : Supply voltage (V_{VCC}) C3 (blue) : FB voltage (V_{FB}) C4 (green) : Drain voltage (V_D)
Condition to enter over-load protection: V_{FB} > 2.73 V and lasts for 54 ms blanking time (15 V output load change from full to short at 85 V AC)	Condition to enter over-load protection: V_{FB} > 2.73 V and lasts for 54 ms blanking time (15 V output load change from full to short at 300 V AC)

Figure 31 Over-load protection

11.15 V_{CC} short-to-GND protection



C1 (yellow)	: Bus voltage (V_{Bus})
C2 (purple)	: V_{CC} voltage (V_{VCC})
C3 (blue)	: V_{IN} voltage (V_{VIN})
C4 (green)	: CS voltage (V_{CS})

Condition to enter V_{CC} short-to-GND: if $V_{CC} < V_{VCC\_SCP} \rightarrow I_{VCC} = I_{VCC\_Charge1}$
(short V_{CC} pin-to-GND and measure the current with multimeter before system start-up, $I_{VCC} \approx 284$ µA at 85 V AC)

Figure 32 V_{CC} short-to-GND protection

12 References

[1] ICE5xRxxxxAG datasheet, Infineon Technologies AG

[2] 5th Generation Fixed-Frequency Design Guide

[3] Calculation Tool Fixed Frequency CoolSET™ Generation 5

Revision history

Major changes since the last revision

Page or reference	Description of change
_	First release

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