LTC6430-15
50MHz to 1000MHz
75Ω Input/Output CATV Amplifier

DESCRIPTION

Demonstration circuit 2032A is a 75Ω input and 75Ω output push-pull CATV amplifier featuring the LTC®6430-15. The LTC6430-15 has a power gain of 15.2dB and is part of the LTC643X-YY amplifier series.

The DC2032A demo board is optimized for a frequency range from 50MHz to 1000MHz. It incorporates a minimum of passive support components to configure the amplifier for the CATV applications with 75Ω input and output impedance.

Design files for this circuit board are available at http://www.linear.com/demo

PERFORMANCE SUMMARY

Specifications are at T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS	VALUE/UNIT
Power Supply			
V_{CC}	Operating Supply Range	All V_{CC} Pins Plus OUT Pins	4.75V to 5.25V
I_{CC}	Current Consumption	Total Current	160mA

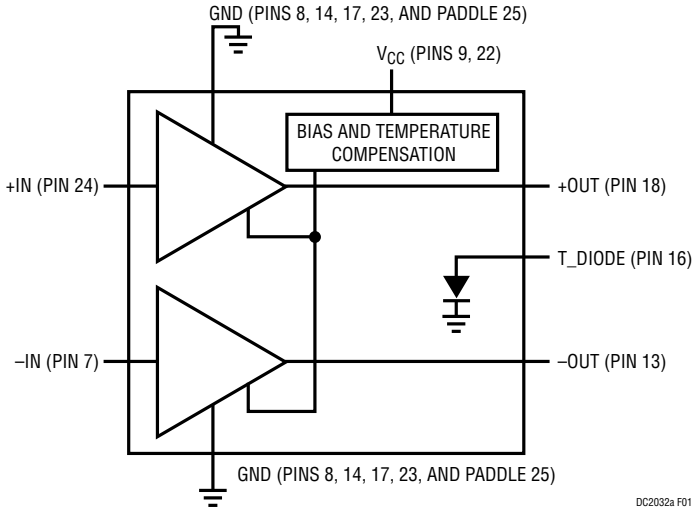


Figure 1. LTC6430-15 Device Block Diagram

QUICK START PROCEDURE

Demo circuit 2032A can be set up to evaluate the performance of the LTC6430-15. Refer to Figures 2 and 3 for proper equipment connections and follow this procedure:

Single-Tone Measurement:

Connect all test equipment as suggested in Figure 2.

1. The power labels of 5V and GND directly correspond to the power supply. Typical current consumption of the LTC6430-15 is about 160mA.
2. Apply an input signal to J1. A low distortion, low noise signal source with an external high order low pass filter will yield the best performance. The input CW signal is –10dBm.
3. Observe the output via J2. The measured power at the J2 connector should be about 4dBm.

Two-Tone Measurement:

Connect all test equipment as suggested in Figure 3.

1. The power labels of 5V and GND directly correspond to the power supply. Typical current consumption of the LTC6430-15 is about 160mA.
2. Apply to J1 two independent signals f1 and f2 from SG1 and SG2 at 400MHz and 401MHz respectively.
3. Monitor the output tone level on the spectrum analyzer. Adjust signal generator levels such that output power measures 1dBm/tone at the amplifier output J2, after correcting for external cable losses, minimum loss matching pads and attenuations.
4. Change the spectrum analyzer's center frequency and observe the two IM3 tones at 1MHz below and above the input frequencies. The frequencies of $IM3_{\_LOW}$ and $IM3_{\_HIGH}$ are 399MHz and 402MHz, respectively. The measurement levels should be approximately –90dBc; 46dBm is a typical performance of OIP3 at 400MHz. For this setup, the Rohde and Schwarz FSEM30 spectrum analyzer was used. This SA has a typical 20dBm third-order intercept point (TOI). So, the SA input attenuation is set to 20dB with an external 14dB attenuation pad (matches DUT gain), resulting in an attenuation total of 34dB. The system as described can measure OIP3 up to 50dBm.

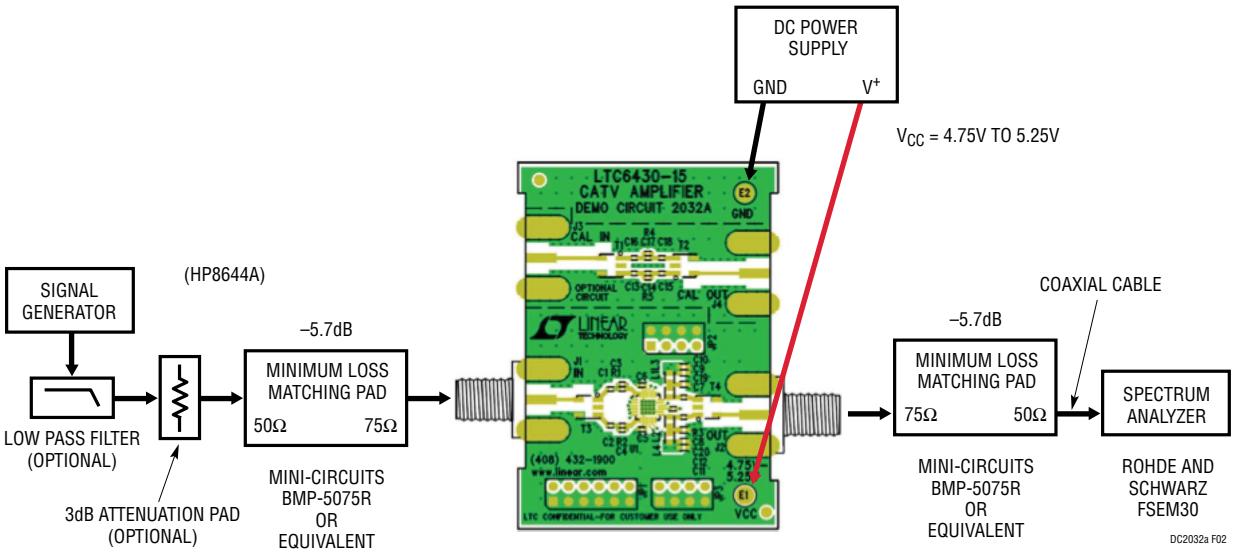


Figure 2. Proper Equipment Setup for Gain and Single-Tone Measurement

QUICK START PROCEDURE

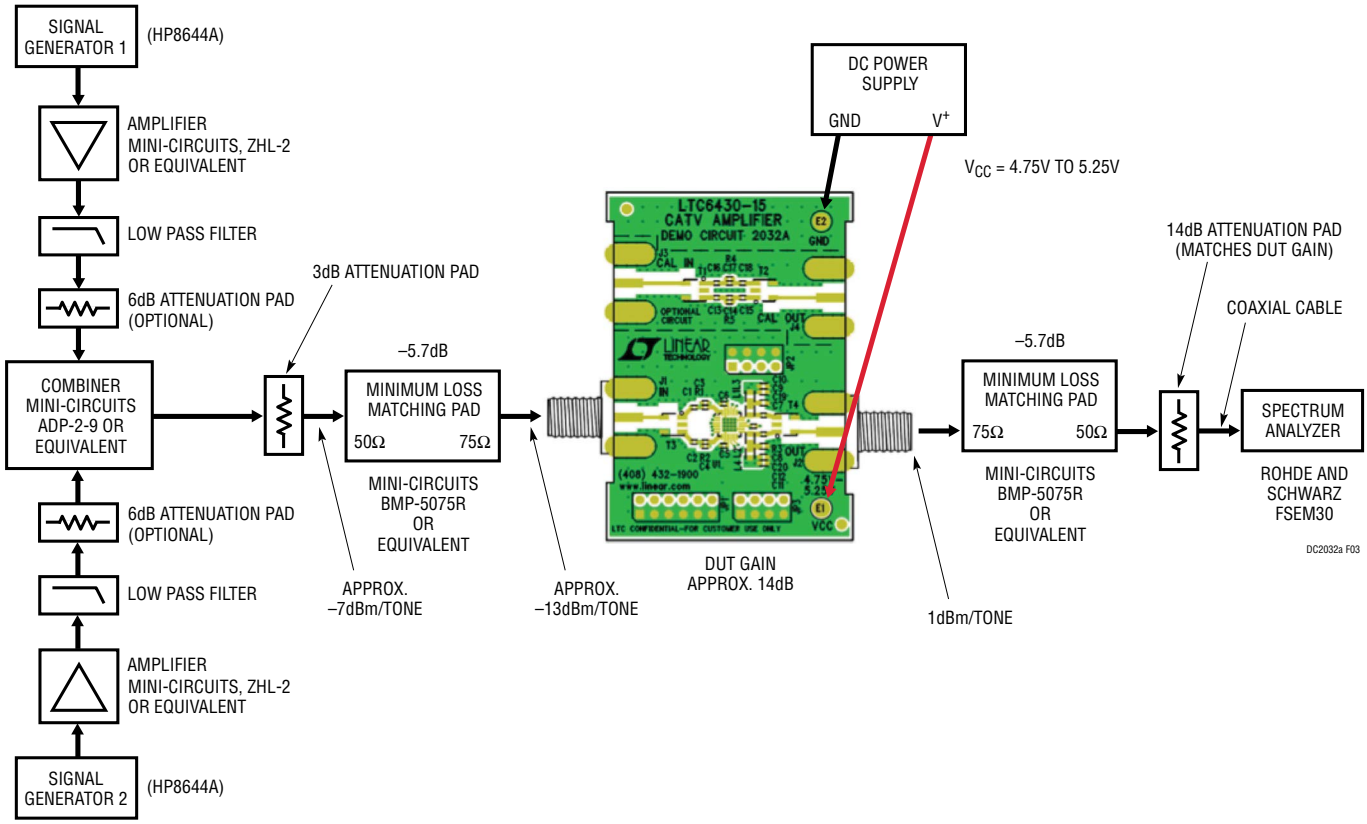


Figure 3. Proper Equipment Setup for IP3 Measurement

OPERATION

Demo circuit 2032A is a highly linear fixed gain amplifier. To configure the demo circuit 2032A for use in the 75Ω CATV environment, a transformer with 1:1.33 impedance ratio is added at the board's input and output. These transformers transform the differential 100Ω impedance of the LTC6430-15 to single-ended 75Ω impedance. The frequency range of the circuit is limited by the balun transformers. Hence, the demo board has a nominal working frequency range from 50MHz to 1000MHz. Figure 4 shows the S-parameters of demo board.

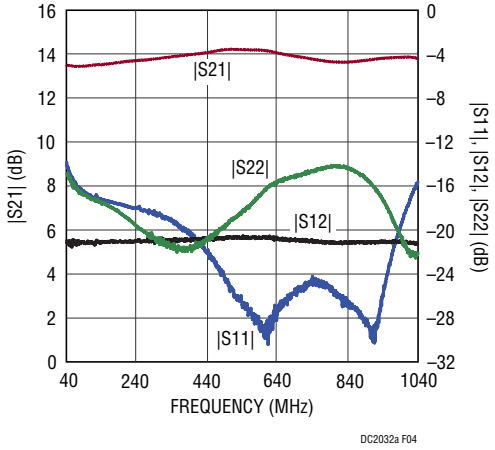


Figure 4. Demo Board DC2032A S-Parameters

Figure 6 shows the simplified demo circuit schematic. It requires a minimum of passive supporting components.

Demo circuit 2032A is shipped with 75Ω F-type connectors (J1 and J2) at both input and output. Depending on the user's preference, the board may also accept other connector types such as BNC or SMA. Please note that the use of substandard connectors can limit the usable bandwidth of the circuit.

The input and output transformers (T3 and T4) convert the differential to single-ended 75Ω for compatibility with the CATV environment, while preserving all the exceptional characteristics of the LTC6430-15. In addition, the balun's excellent phase balance and the second order linearity of the LTC6430-15 combine to further suppress second order products across the entire CATV band. Figure 5 shows the spurious products (in dBc) within the passband frequency of the output third-order intermodulation (OIM3) and the second harmonic distortion (HD2).

Table 1. Typical Demo Board Performance Summary T_A = 25°C, V_{CC} = 5V

FREQUENCY (MHz)	POWER GAIN |S21| (dB)	OUTPUT THIRD-ORDER INTERCEPT POINT[1] OIP3 (dBm)	OUTPUT THIRD-ORDER INTERMODULATION[1] OIM3 (dBc)	SECOND HARMONIC DISTORTION[2] HD2 (dBc)	THIRD HARMONIC DISTORTION[2] HD3 (dBc)	OUTPUT 1dB COMPRESSION POINT P1dB (dBm)	NOISE FIGURE[3] NF (dB)
50	13.5	46.4	–90.8	–88.1	–87.6	19.5	4.3
100	13.5	46.1	–90.2	–90.1	–82.7	21.3	4.3
200	13.7	45.1	–88.2	–83.5	–79.7	21.4	4.2
300	13.8	44.9	–87.9	–88.4	–73.8	21.4	4.1
400	14.0	45.3	–88.6	–72.0	–71.8	22.0	4.0
500	14.2	46.7	–91.4	–73.7		21.9	4.0
600	14.2	46.7	–91.5			21.9	4.1
700	13.9	46.6	–91.3			21.9	4.4
800	13.7	45.4	–88.8			21.3	4.7
900	13.7	44.9	–87.8			20.9	5.1
1000	13.9	44.5	–87.1			20.5	5.1

Notes: All figures are referenced to J1 (Input Port) and J2 (Output Port).

1. Two-tone test condition: Output power level = 1dBm/tone; Tone spacing = 1MHz.
2. Single-tone test condition: Output power level = 8dBm.
3. Small signal noise figure.

OPERATION

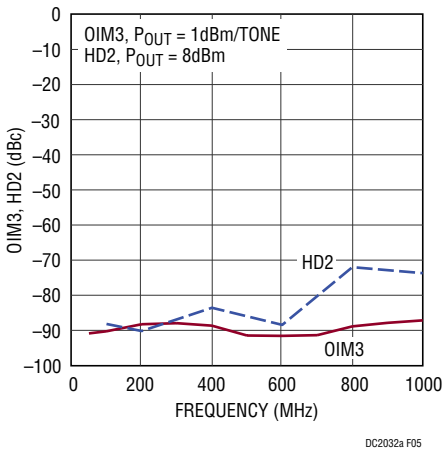


Figure 5. OIM3 and HD2 vs Frequency

The input and output DC blocking capacitors (C1, C2, C7 and C8) are required because this device is internally biased for optimal operation.

The frequency appropriate choke (L1 and L2) and the decoupling capacitors (C9, C10, C11 and C12) provide bias to the RF ±OUT nodes. Only a single 5V supply is necessary for the V_{CC} pins on the device.

The input stability networks (C3, C4, R1, R2) are not required since the LTC6430-15 is preceded by a low frequency termination from the balun transformer.

Table 2 shows the function of each input and output on the board.

Table 2. DC2032A Board I/O Descriptions

CONNECTOR	FUNCTION
J1 IN)	Single-Ended Input. Impedance Matched to 75Ω.
J2 (OUT)	Single-Ended Output. Impedance Matched to 75Ω.
E1 (V_{CC})	Positive Supply Voltage Source.
E2 (GND)	Negative Supply Ground.

Additional Information

As with any RF device, minimizing ground inductance is critical. Care should be taken with the board layout because of the exposed pad packages. The maximum number of minimum diameter vias holes should be placed underneath the exposed pad. This will ensure good RF ground and low

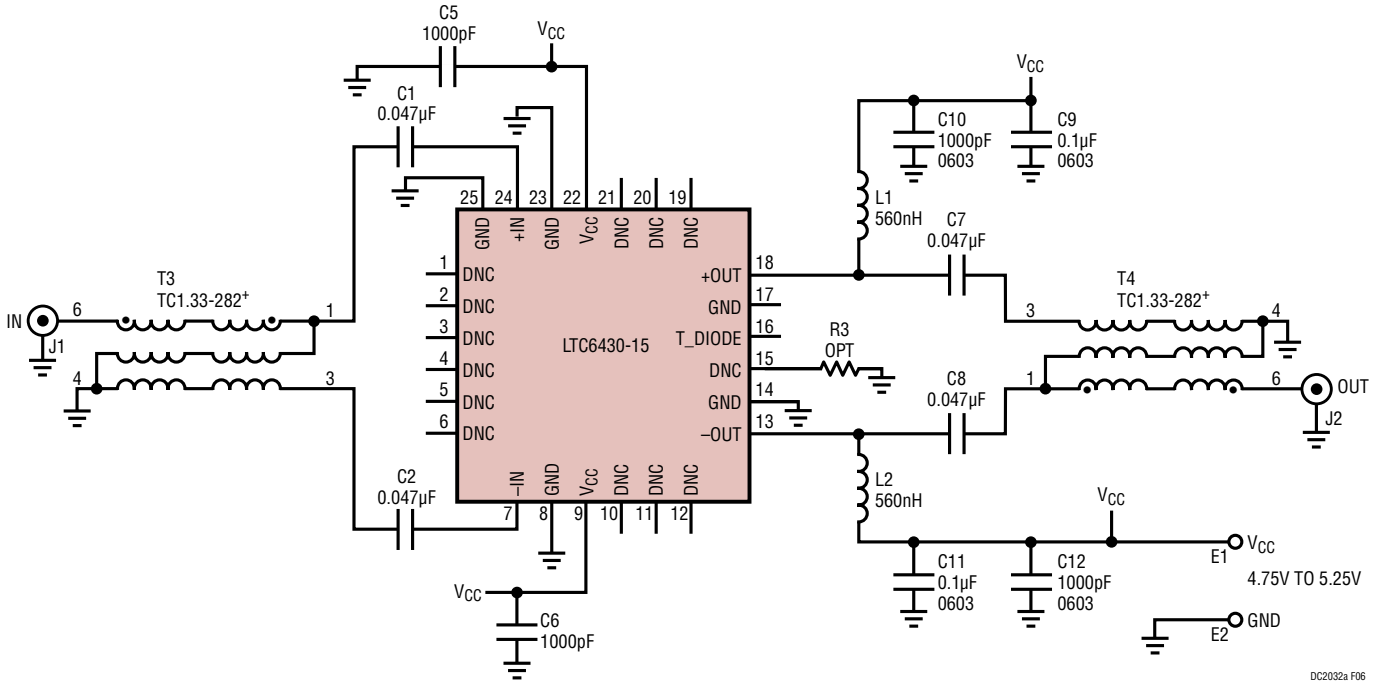


Figure 6. Demo Board DC2032A Simplified Schematic

OPERATION

thermal impedance. Maximizing the copper ground plane will also improve heat spreading and reduce inductance. It is a good idea to cover the via holes with solder mask on the back side of the PCB to prevent solder from wicking away from the critical PCB to the exposed pad interface.

The DC2032A has a nominal working frequency range from 50MHz to 1000MHz. It is not intended for operation down to DC. The lower frequency cutoff is limited by on-chip matching elements.

Setup and Testing Signal Sources

The LTC6430-15 is an amplifier with high linearity performance; therefore, output intermodulation products are very low. For this reason, it drives most test equipment and test setups to their limits. Consequently, accurate measurement of IP3 for a low distortion IC such as the LTC6430-15 requires certain precautions to be observed in the test setup and testing procedure.

Setup Signal Sources

Figure 3 shows a proposed IP3 test setup. This setup has low phase noise, good reverse isolation, high dynamic range, sufficient harmonic filtering and wideband impedance matching. The setup is outlined here:

a. High performance signal generators 1 and 2 (HP8644A) should be used in the setup. These suggested generators have low harmonic distortion and very low phase noise.

b. High linearity amplifiers to improve isolation. They prevent the two signal generators from cross talking with each other and provide higher output power.

c. A low pass filter to suppress harmonic contents from interfering with the test signal.

d. The signal combiner from Mini-Circuits ADP-2-9 combines the two isolated input signals. This combiner has a typical isolation of 27dB. For better VSWR and isolation, use the H-9 signal combiner from MA/COM, which features >40dB isolation and a wider frequency range. Passive devices (e.g., combiners) with magnetic elements can contribute nonlinearity to the signal chain and should be used cautiously.

e. The attenuator pads, on all three ports of the signal combiner, will support further isolation of the two input signal sources. They will reduce reflection and promote maximum power transfer with wideband impedance matching.

f. The minimum loss matching pads, (Mini-Circuits BMP-5075R or equivalents) are added to the test setup at the DUT input and output. These matching pads transform the DUT impedance from 75Ω to 50Ω to match the characteristic impedance of modern RF instrumentation.

Testing Signal Sources

The testing signal should be evaluated and optimized before it is used for measurements. The following outlines the necessary steps to achieve optimization.

a. Apply two independent signals f1 and f2 from signal generator 1 and signal generator 2 at 240MHz and 241MHz, while setting amplitude = –7dBm per tone at the combined output.

b. Connect the combined signal to the spectrum analyzer without the DUT (i.e. The combined signal, the minimum loss matching pad, the F-type thru adaptor, the minimum loss matching pad and the spectrum analyzer; at this point, the spectrum analyzer should read about –18dBm/tone for each main tone power).

c. Adjust the spectrum analyzer for the maximum possible resolution of the intermodulation products amplitude in dBc relative to the main tone power. A narrower resolution bandwidth will take a longer time to sweep. Optimize the dynamic range of the spectrum analyzer by adjusting input attenuation. First increase the spectrum analyzer input attenuation (normally in steps of 5dB or 10dB). If the IMD product levels decrease when the input attenuation is increased, then the input power level was too high for the spectrum analyzer to make a

OPERATION

valid measurement. In other words, the spectrum analyzer 1st mixer was overloaded and producing its own IMD products. If the IMD reading holds constant with increased input attenuation, then a sufficient amount of attenuation was present. Adding too much attenuation will raise the noise floor and bury the intended IMD signal. Therefore, select just enough attenuation to achieve a stable and valid measurement.

d. In order to achieve a valid measurement result, the test system must have lower distortion than the DUT intermodulation. For example, to measure a 46dBm OIP3, the measured intermodulation products will be –90dBc below the –19dBm per tone input level and the test system must have intermodulation products approx. –96dBc or better. For best results, the IMD or noise floor should be at least –100dBc before connecting the DUT.

Testing the DUT

At this point, the input level has been established at –7dBm per tone (–13dBm at the DUT), and the input IMD from the test setup is well suppressed at –96dBc max. Furthermore, the SA is setup to measure very low level IMD components.

a. Insert the DUT, minimum loss matching pads and output attenuator into the setup, inline between the signal source and SA. The output attenuator should match the DUT gain.

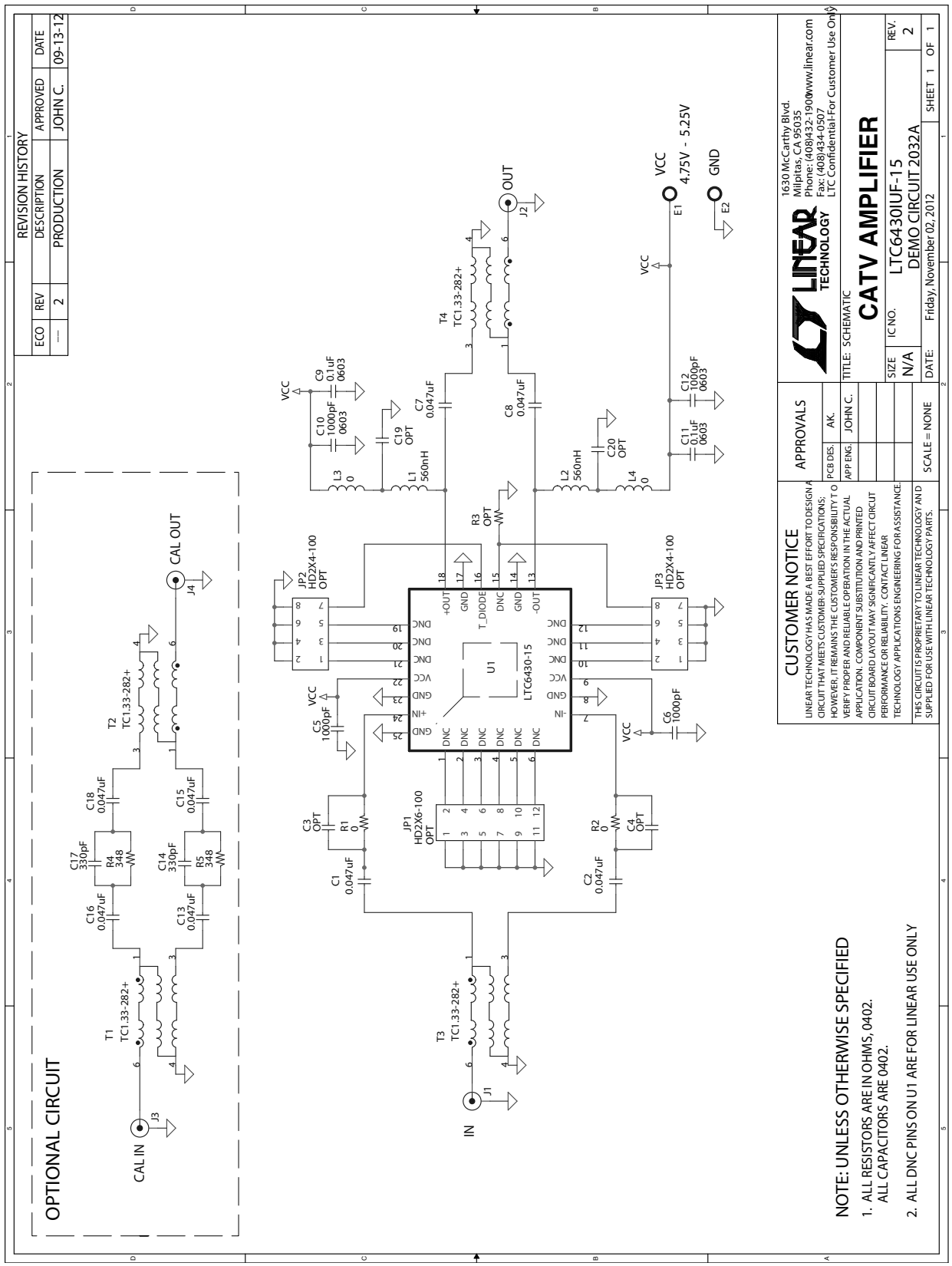
b. Fine tune the signal generator levels by a small amount if necessary (<1dB), to keep output power at 1dBm per tone at the amplifier output.

c. Measure output IMD level using the same optimized setup as previous. Based on the output power level of 1dBm per tone, and knowing the IMD level, OIP3 can be calculated.

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
1	4	C1, C2, C7, C8,	CAP, X5R, 0.047µF, 16V 10%, 0402	AVX, 0402YD473KAT2A
2	0	C13, C15, C16, C18	CAP, X5R, 0.047µF, 16V 10%, 0402	OPT
3	0	C3, C4,	CAP, COG, 330pF, 25V 10%, 0402	OPT
4	0	C14, C17	CAP, COG, 330pF, 25V 10%, 0402	OPT
5	2	C5, C6	CAP, X7R, 1000pF, 50V 5%, 0402	AVX, 04025C102JAT2A
6	2	C9, C11	CAP, X5R, 0.1µF, 10V, 10%, 0603	AVX, 0603ZD104KAT2A
7	2	C10, C12	CAP, X7R, 1000pF, 50V 5%, 0603	AVX, 06035C102JAT2A
8	0	C19, C20	CAP, OPT 0603	
9	2	E1, E2	TESTPOINT, TURRET, 0.064"	MILL-MAX, 2308-2-00-80-00-00-07-0
10	0	JP1	HEADER, 2X6, 0.1"	OPT
11	0	JP2, JP3	HEADER, 2X4, 0.1"	OPT
12	2	J1, J2,	F TYPE END LAUNCH JACK FOR 0.062" PCB, 75Ω	AMPHENOL CONNEX, 222181
13	0	J3, J4	F TYPE END LAUNCH JACK FOR 0.062" PCB, 75Ω	OPT
14	0	ALTERNATIVE FOR J1, J2, J3, J4	BNC END LAUNCH JACK FOR 0.062" PCB, 75Ω	AMPHENOL CONNEX, 112801
15	2	L1, L2	INDUCTOR, CHIP, 560nH, 5%, 0603LS-1608	COILCRAFT, 0603LS-561XJLB
16	2	L3, L4	RES, CHIP, 0Ω, 0603	VISHAY, CRCW06030000Z0ED
17	2	R1, R2	RES, CHIP, 0Ω, 0402	VISHAY, CRCW04020000Z0ED
18	0	R4, R5	RES, CHIP, 348, 1%, 0402	OPT
19	0	R3	RES, CHIP, 0Ω, 0402	OPT
20	2	T3, T4,	RF TRANSFORMER TC1.33-282+, CASE STYLE: AT 224-1	MINI-CIRCUITS, TC1.33-282+
21	0	T1, T2,	RF TRANSFORMER TC1.33-282+, CASE STYLE: AT 224-1	OPT
22	1	U1	BALANCED AMPLIFIER LTC6430AIUF-15, QFN24UF-4X4	LINEAR TECHNOLOGY, LTC6430AIUF-15
	0	ALTERNATIVE FOR U1	BALANCED AMPLIFIER LTC6430BIUF-15, QFN24UF-4X4	LINEAR TECHNOLOGY, LTC6430BIUF-15

SCHEMATIC DIAGRAM



DEMONSTRATION BOARD IMPORTANT NOTICE

Linear Technology Corporation (LTC) provides the enclosed product(s) under the following **AS IS** conditions:

This demonstration board (DEMO BOARD) kit being sold or provided by Linear Technology is intended for use for **ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY** and is not provided by LTC for commercial use. As such, the DEMO BOARD herein may not be complete in terms of required design-, marketing-, and/or manufacturing-related protective considerations, including but not limited to product safety measures typically found in finished commercial goods. As a prototype, this product does not fall within the scope of the European Union directive on electromagnetic compatibility and therefore may or may not meet the technical requirements of the directive, or other regulations.

If this evaluation kit does not meet the specifications recited in the DEMO BOARD manual the kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY THE SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE. EXCEPT TO THE EXTENT OF THIS INDEMNITY, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user releases LTC from all claims arising from the handling or use of the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge. Also be aware that the products herein may not be regulatory compliant or agency certified (FCC, UL, CE, etc.).

No License is granted under any patent right or other intellectual property whatsoever. **LTC assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or any other intellectual property rights of any kind.**

LTC currently services a variety of customers for products around the world, and therefore this transaction **is not exclusive**.

Please read the DEMO BOARD manual prior to handling the product. Persons handling this product must have electronics training and observe good laboratory practice standards. **Common sense is encouraged**.

This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact a LTC application engineer.

Mailing Address:

Linear Technology
1630 McCarthy Blvd.
Milpitas, CA 95035