EL5104, EL5105, EL5204, EL5205, EL5304

700MHz Slew-Enhanced VFAs

FN7332
Rev 8.00
May 25, 2016

The EL5104, EL5105, EL5204, EL5205, and EL5304 represent high speed voltage feedback amplifiers based on the current feedback amplifier architecture. This gives the typical high slew rate benefits of a CFA family along with the stability and ease of use associated with the VFA type architecture. This family is available in single, dual, and triple versions, with 200MHz, 400MHz, and 700MHz versions. This family operates on single 5V or ±5V supplies from minimum supply current. The EL5104 and EL5204 also feature an output enable function, which can be used to put the output in to a high-impedance mode. This enables the outputs of multiple amplifiers to be tied together for use in multiplexing applications.

Features

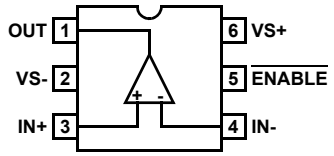
- Specified for 5V or ±5V applications
- Power-down to 17µA
- -3dB bandwidth = 700MHz
- ±0.1dB bandwidth = 45MHz
- Low supply current = 9.5mA
- Slew rate = 7000V/µs
- Low offset voltage = 10mV max
- Output current = 160mA
- A_{VOL} = 1400
- Diff gain/phase = 0.01%/0.02°
- Pb-free plus anneal available (RoHS compliant)

Applications

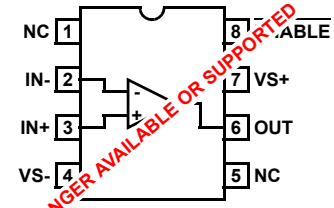
- Video amplifiers
- PCMCIA applications
- A/D drivers
- Line drivers
- Portable computers
- High speed communications
- RGB applications
- Broadcast equipment
- Active filtering

Pinouts

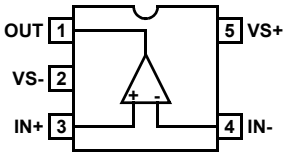
EL5104
(6 LD SOT-23)
TOP VIEW



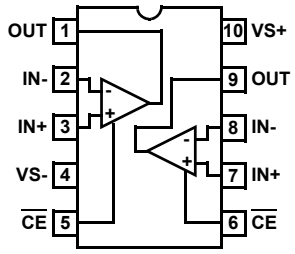
EL5104
(8 LD SOIC)
TOP VIEW



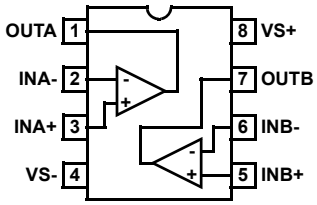
EL5105
(5 LD SOT-23, SC-70)
TOP VIEW



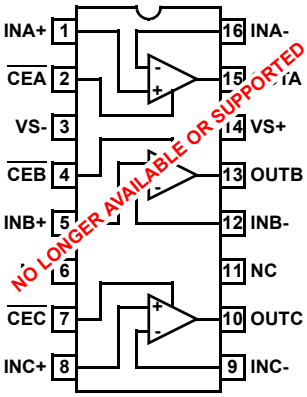
EL5204
(10 LD MSOP)
TOP VIEW



EL5205
(8 LD SOIC, MSOP)
TOP VIEW



EL5304
(16 LD QSOP)
TOP VIEW



Ordering Information

PART NUMBER	PART MARKING	TAPE & REEL	PACKAGE	PKG. DWG. #
EL5104ISZ (Note) **(No longer available, recommended replacement: EL5104IWZ-T7)**	5104ISZ	-	8 Ld SOIC (150 mil) (Pb-Free)	MDP0027
EL5104ISZ-T7 (Note) **(No longer available, recommended replacement: EL5104IWZ-T7)**	5104ISZ	7”	8 Ld SOIC (150 mil) (Pb-Free)	MDP0027
EL5104ISZ-T13 (Note) **(No longer available, recommended replacement: EL5104IWZ-T7)**	5104ISZ	13”	8 Ld SOIC (150 mil) (Pb-Free)	MDP0027
EL5104IWZ-T7 (Note)	BAEA	7” (3k pcs)	6 Ld SOT-23 (Pb-Free)	P5.064A
EL5104IWZ-T7A (Note)	BAEA	7” (250 pcs)	6 Ld SOT-23 (Pb-Free)	P5.064A
EL5105IC **(No longer available or supported)**	C	-	5 Ld SC-70 (1.25mm)	P5.049
EL5105IWZ-T7 (Note)	BBMA	7” (3k pcs)	5 Ld SOT-23 (Pb-Free)	P5.064A
EL5105IWZ-T7A (Note)	BBMA	7” (250 pcs)	5 Ld SOT-23 (Pb-Free)	P5.064A
EL5204IYZ (Note)	BAAAF	-	10 Ld MSOP (3.0mm) (Pb-Free)	MDP0043
EL5204IYZ-T7 (Note)	BAAAF	7”	10 Ld MSOP (3.0mm) (Pb-Free)	MDP0043
EL5204IYZ-T13 (Note)	BAAAF	13”	10 Ld MSOP (3.0mm) (Pb-Free)	MDP0043

Ordering Information (Continued)

PART NUMBER	PART MARKING	TAPE & REEL	PACKAGE	PKG. DWG. #
EL5205ISZ (Note)	5205ISZ	-	8 Ld SOIC (150 mil) (Pb-Free)	MDP0027
EL5205ISZ-T7 (Note)	5205ISZ	7”	8 Ld SOIC (150 mil) (Pb-Free)	MDP0027
EL5205ISZ-T13 (Note)	5205ISZ	13”	8 Ld SOIC (150 mil) (Pb-Free)	MDP0027
EL5304IU **(No longer available or supported)**	5304IU	-	16 Ld QSOP (150 mil)	MDP0040
EL5304IU-T7 **(No longer available or supported)**	5304IU	7”	16 Ld QSOP (150 mil)	MDP0040
EL5304IU-T13 **(No longer available or supported)**	5304IU	13”	16 Ld QSOP (150 mil)	MDP0040
EL5304IUZ (Note) **(No longer available or supported)**	5304IUZ	-	16 Ld QSOP (150 mil) (Pb-Free)	MDP0040
EL5304IUZ-T7 (Note) **(No longer available or supported)**	5304IUZ	7”	16 Ld QSOP (150 mil) (Pb-Free)	MDP0040
EL5304IUZ-T13 (Note) **(No longer available or supported)**	5304IUZ	13”	16 Ld QSOP (150 mil) (Pb-Free)	MDP0040

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage between V_S+ and GND. 13.2V
Input Voltage . . . . . .$\pm V_S$
Differential Input Voltage . . . . . .±4V
Maximum Output Current. 80mA
V_S+ to V_S- Maximum Slew Rate 1V/µs

Thermal Information

Storage Temperature Range . . . . . .-65°C to +150°C
Ambient Operating Temperature Range . . . . . .-40°C to +85°C
Operating Junction Temperature . . . . . .+150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

DC Electrical Specifications

V_S = ±5V, GND = 0V, T_A = +25°C, V_{CM} = 0V, V_{OUT} = 0V, V_{ENABLE} = GND or OPEN, Unless Otherwise Specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
V_{OS}	Offset Voltage	EL5104, EL5105, EL5204, EL5205	-10	3	10	mV
		EL5304	-18	5	18	mV
TCV_{OS}	Offset Voltage Temperature Coefficient	Measured from T_{MIN} to T_{MAX}		10		µV/°C
IB	Input Bias Current	V_{IN} = 0V		8	30	µA
I_{OS}	Input Offset Current	V_{IN} = 0V		4	15	µA
TCI_{OS}	Input Bias Current Temperature Coefficient	Measured from T_{MIN} to T_{MAX}		50		nA/°C
PSRR	Power Supply Rejection Ratio		60	70		dB
CMRR	Common Mode Rejection Ratio	V_{CM} from -3V to +3V	56	62		dB
CMIR	Common Mode Input Range	Guaranteed by CMRR test	-3		+3	V
R_{IN}	Input Resistance	Common mode	50	120		kΩ
C_{IN}	Input Capacitance	SO package		1		pF
$I_{S,ON}$	Supply Current - Enabled	Per amplifier	8.5	9.5	11	mA
$I_{S,OFF}$	Supply Current - Shut Down	V_S+, per amplifier	+1	0	+25	µA
		V_S-, per amplifier	-25	17	-1	µA
PSOR	Power Supply Operating Range		4		13.2	V
AVOL	Open Loop Gain	R_L = 1kΩ to GND	55	65		dB
		R_L = 150Ω to GND		60		dB
V_{OP}	Positive Output Voltage Swing	R_L = 150Ω to 0V	3.6	3.8		V
V_{ON}	Negative Output Voltage Swing	R_L = 150Ω to 0V		-3.8	-3.6	V
I_{OUT}	Output Current	R_L = 10Ω to 0V	±90	±160		mA
V_{IH-EN}	ENABLE Pin Voltage for Power Up		(V_S+) -5		(V_S+) -3	V
V_{IL-EN}	ENABLE Pin Voltage for Shut Down		(V_S+) -1		V_S+	V

Closed Loop AC Electrical Specifications

V_S = +5V, GND = 0V, T_A = +25°C, V_{CM} = +1.5V, V_{OUT} = +1.5V, V_{CLAMP} = +5V, V_{ENABLE} = 0V, A_V = +1, R_F = 0Ω, R_L = 150Ω to GND pin, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
BW	-3dB Bandwidth (V_{OUT} = 200mV_{P-P})	V_S = ±5V, A_V = 1, R_F = 0Ω		700		MHz
SR	Slew Rate	R_L = 100Ω, V_{OUT} = -3V to +3V	2000	3000	7000	V/µs
t_R, t_F	Rise Time, Fall Time	±0.1V step		0.4		ns
OS	Overshoot	±0.1V step		10		%
t_{PD}	Propagation Delay	±0.1V step		0.4		ns
t_S	0.1% Settling Time	V_S = ±5V, R_L = 500Ω, A_V = 1, V_{OUT} = ±2.5V		7		ns
dG	Differential Gain	A_V = 2, R_L = 150Ω, V_{INDC} = -1 to +1V		0.01		%
dP	Differential Phase	A_V = 2, R_L = 150Ω, V_{INDC} = -1 to +1V		0.02		°
e_N	Input Noise Voltage	f = 10kHz		10		nV/√Hz
i_N	Input Noise Current	f = 10kHz		54		pA/√Hz
t_{DIS}	Disable Time			180		ns
t_{EN}	Enable Time			650		ns
I_{EN}	Enable Pin Current	Enabled, V_{EN} = 0V	-1		1	µA
		Disabled, V_{EN} = 5V	1		25	µA

Typical Performance Curves

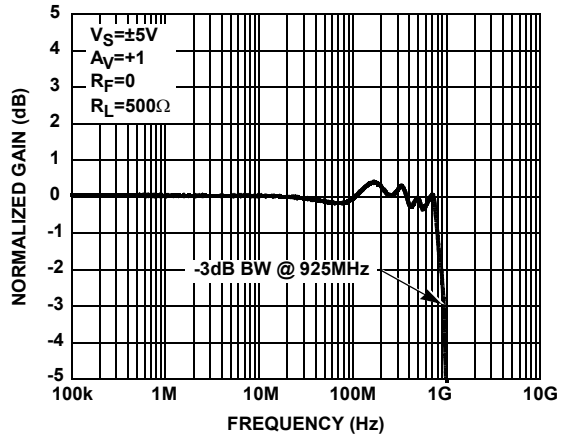


FIGURE 1. GAIN vs FREQUENCY (-3dB BANDWIDTH)

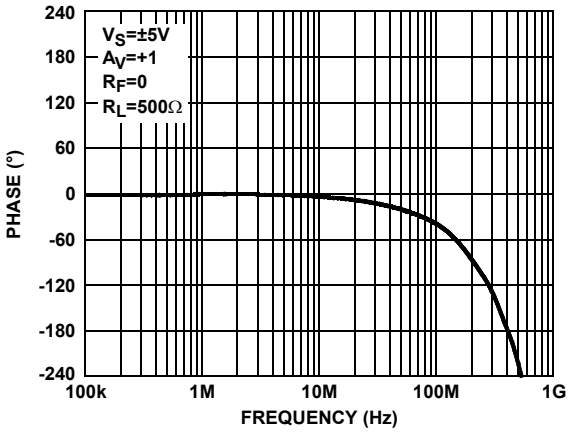


FIGURE 2. PHASE vs FREQUENCY

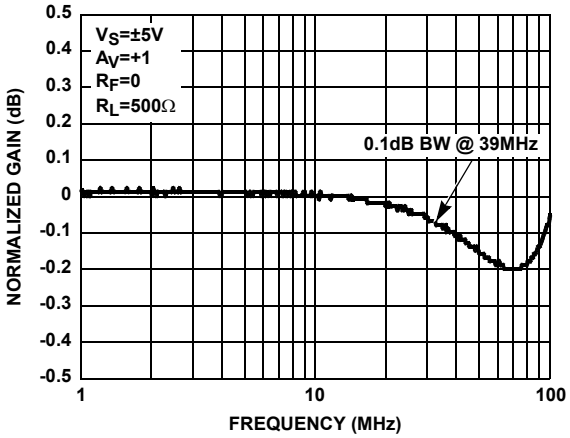


FIGURE 3. 0.1dB BANDWIDTH

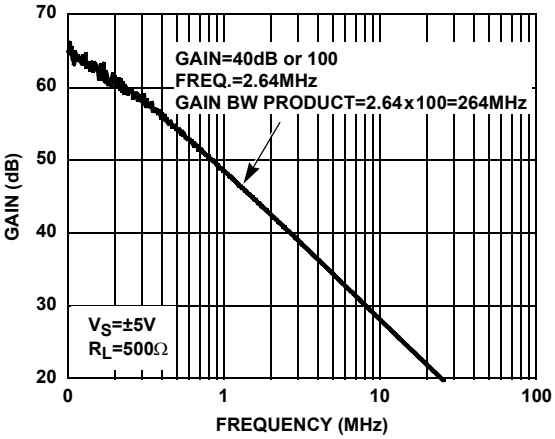


FIGURE 4. GAIN BANDWIDTH PRODUCT

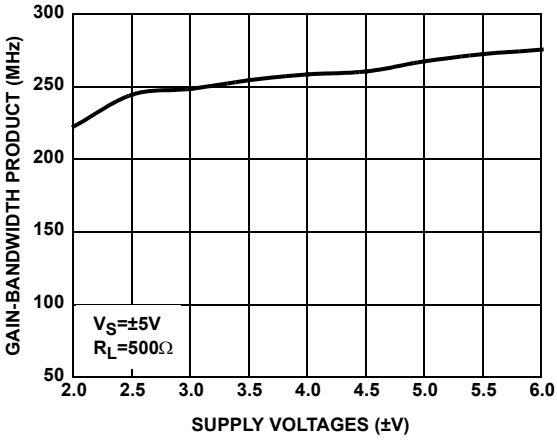


FIGURE 5. GAIN BANDWIDTH PRODUCT vs SUPPLY VOLTAGES

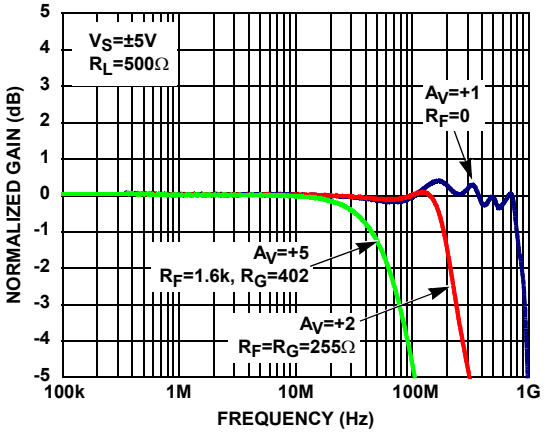


FIGURE 6. GAIN vs FREQUENCY FOR VARIOUS +A_V

Typical Performance Curves (Continued)

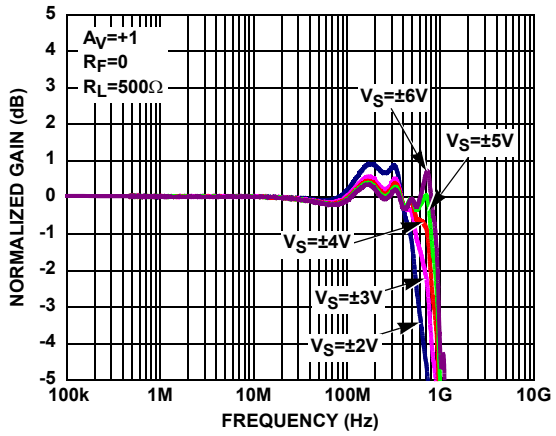


FIGURE 7. GAIN vs FREQUENCY FOR VARIOUS ±Vs

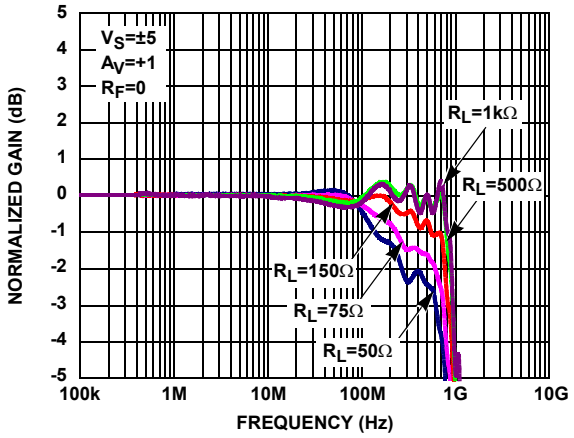


FIGURE 8. GAIN vs FREQUENCY FOR VARIOUS R_L (A_V=+1)

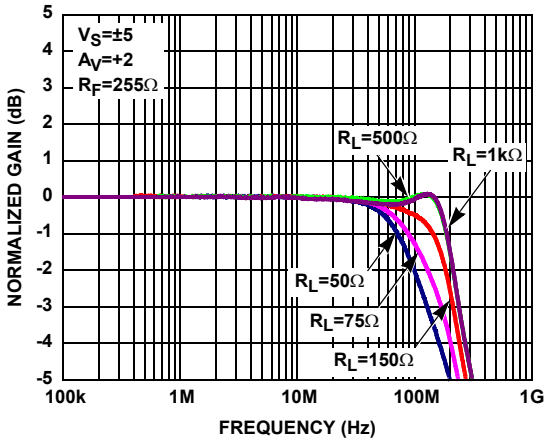


FIGURE 9. GAIN vs FREQUENCY FOR VARIOUS R_L (A_V=+2)

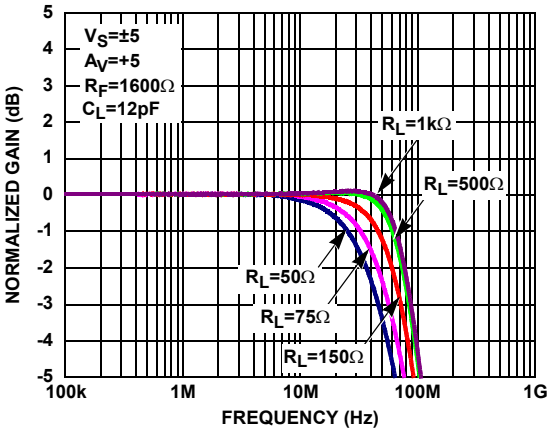


FIGURE 10. GAIN vs FREQUENCY FOR VARIOUS R_L (A_V=+5)

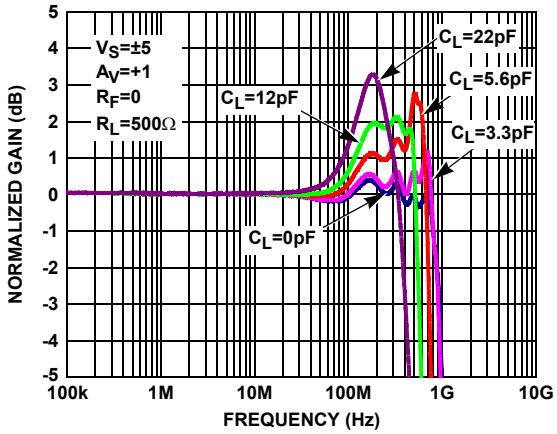


FIGURE 11. GAIN vs FREQUENCY FOR VARIOUS C_L (A_V=+1)

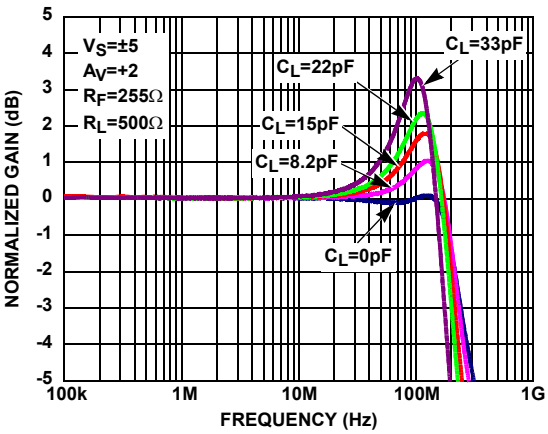


FIGURE 12. GAIN vs FREQUENCY FOR VARIOUS C_L (A_V=+2)

Typical Performance Curves (Continued)

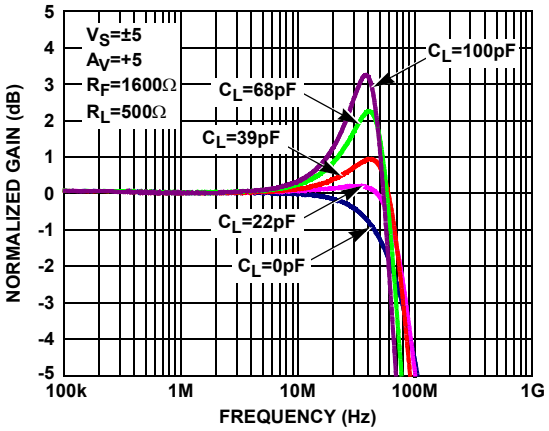


FIGURE 13. GAIN vs FREQUENCY FOR VARIOUS C_L (A_V=+5)

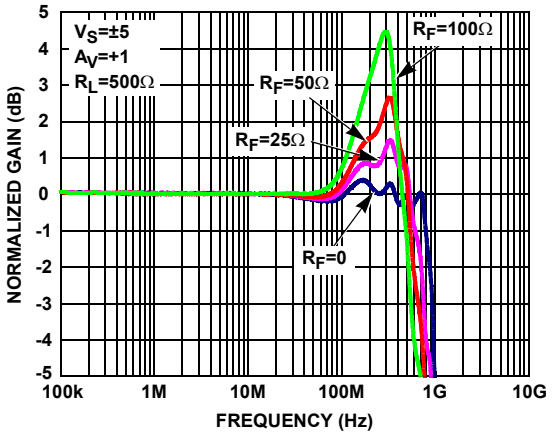


FIGURE 14. GAIN vs FREQUENCY FOR VARIOUS R_F (A_V=+1)

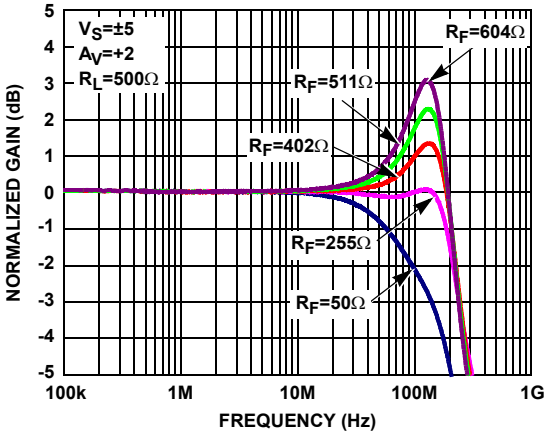


FIGURE 15. GAIN vs FREQUENCY FOR VARIOUS R_F (A_V = +2)

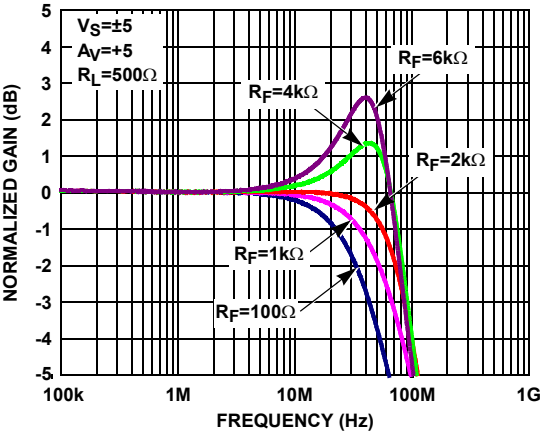


FIGURE 16. GAIN vs FREQUENCY FOR VARIOUS R_F (A_V = +5)

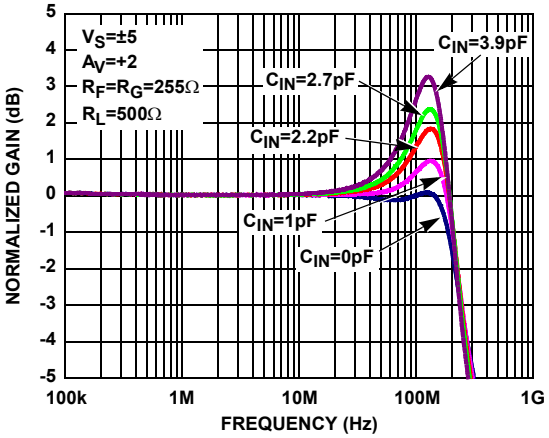


FIGURE 17. GAIN vs FREQUENCY FOR VARIOUS $C_{IN(-)}$ (A_V = +2)

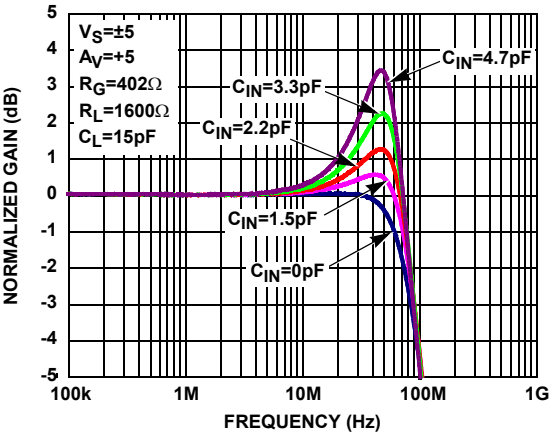


FIGURE 18. GAIN vs FREQUENCY FOR VARIOUS $C_{IN(-)}$ (A_V = +5)

Typical Performance Curves (Continued)

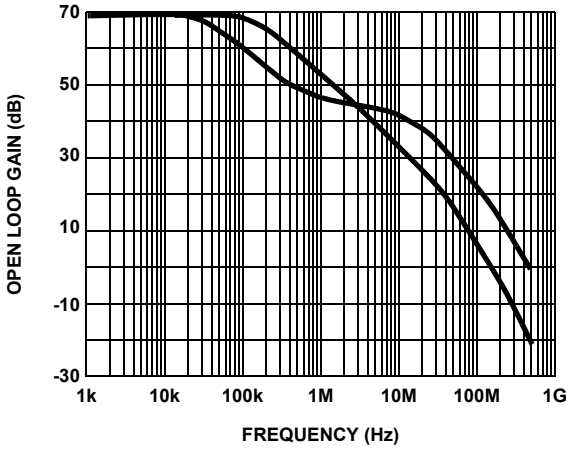


FIGURE 19. OPEN LOOP GAIN AND PHASE vs FREQUENCY

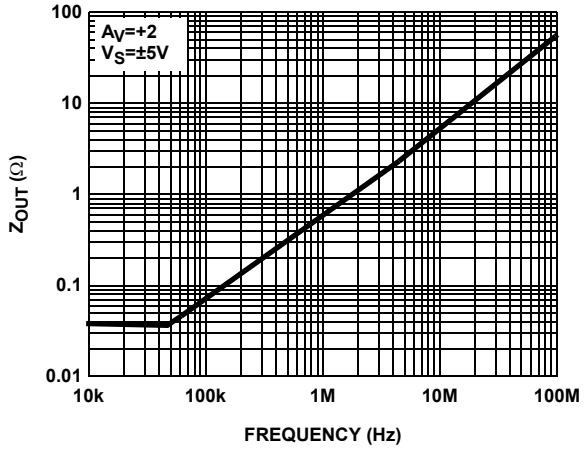


FIGURE 20. Z_{OUT} vs FREQUENCY

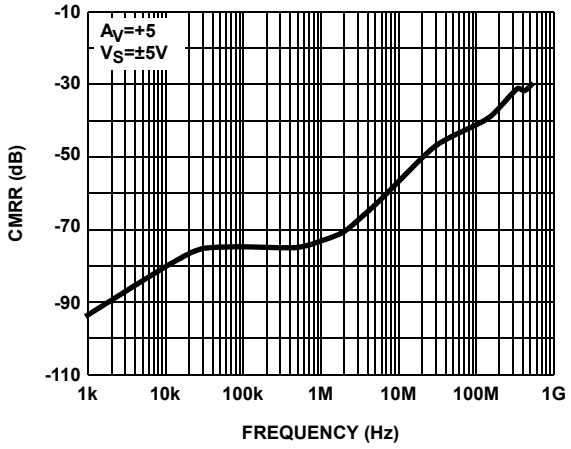


FIGURE 21. CMRR vs FREQUENCY

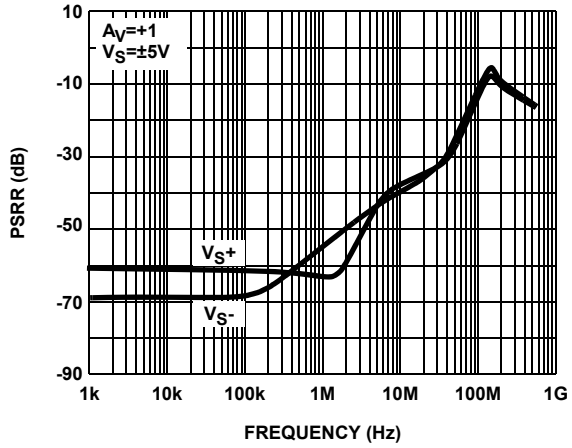


FIGURE 22. PSRR vs FREQUENCY

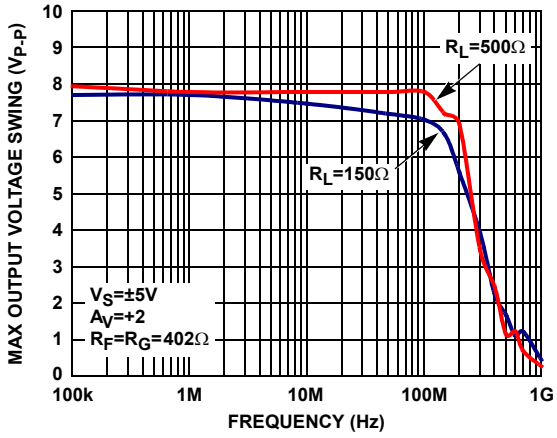


FIGURE 23. MAX OUTPUT VOLTAGE SWING vs FREQUENCY

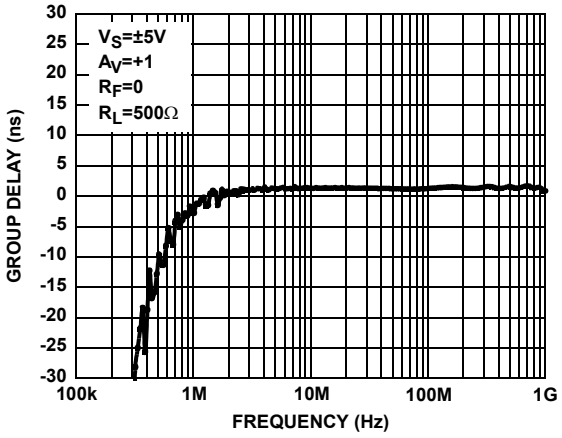


FIGURE 24. GROUP DELAY vs FREQUENCY

Typical Performance Curves (Continued)

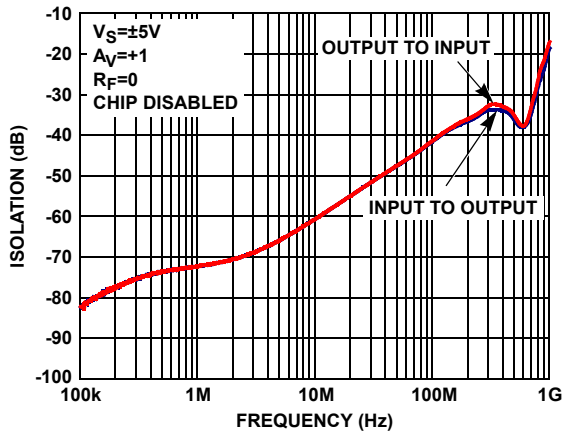


FIGURE 25. INPUT AND OUTPUT ISOLATION

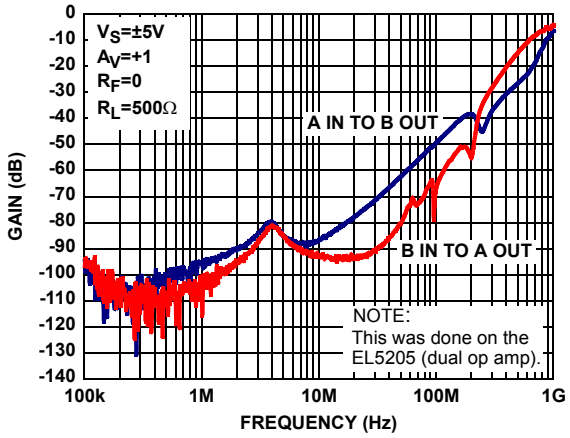


FIGURE 26. CHANNEL TO CHANNEL ISOLATION

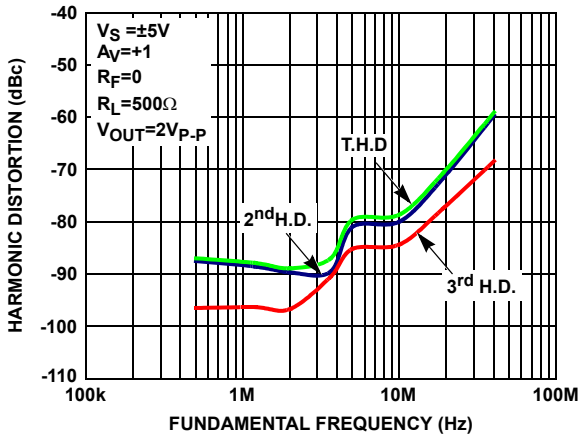


FIGURE 27. HARMONIC DISTORTION vs FREQUENCY

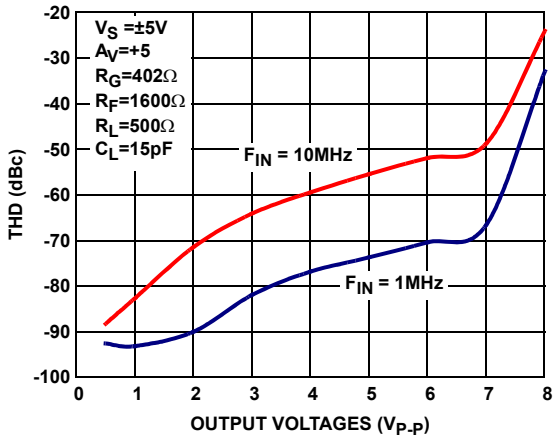


FIGURE 28. TOTAL HARMONIC DISTORTION vs OUTPUT VOLTAGES

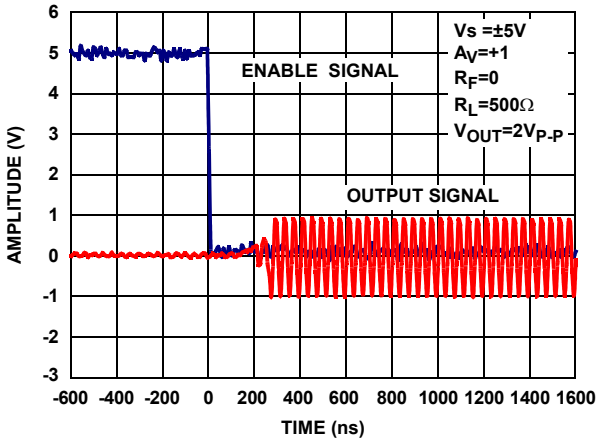


FIGURE 29. TURN-ON TIME

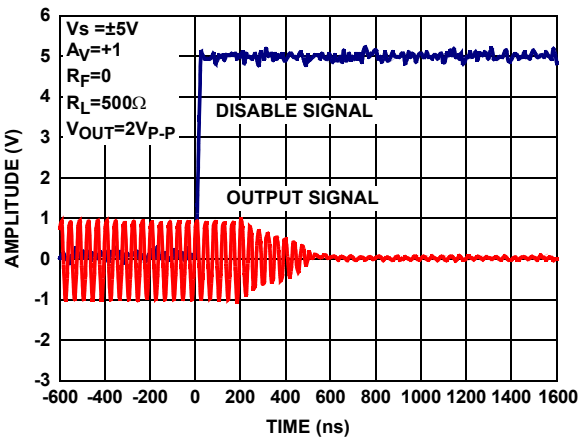


FIGURE 30. TURN-OFF TIME

Typical Performance Curves (Continued)

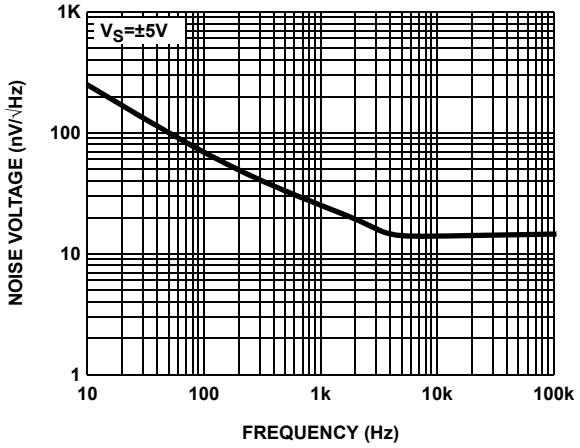


FIGURE 31. EQUIVALENT NOISE VOLTAGE vs FREQUENCY

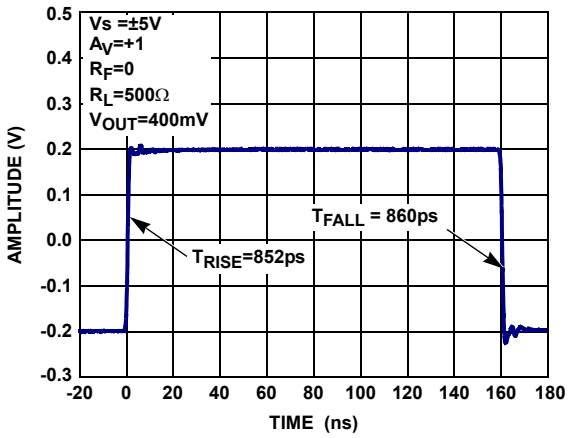


FIGURE 32. SMALL SIGNAL STEP RESPONSE_RISE & FALL TIME

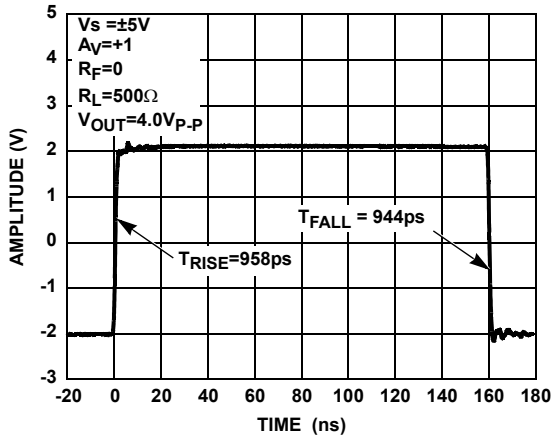


FIGURE 33. LARGE SIGNAL STEP RESPONSE_RISE & FALL TIME

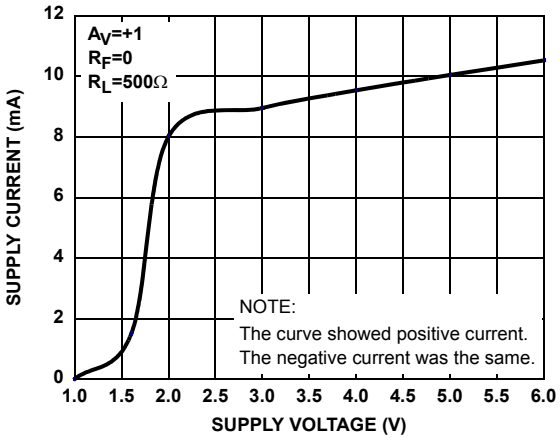


FIGURE 34. SUPPLY CURRENT vs SUPPLY VOLTAGE

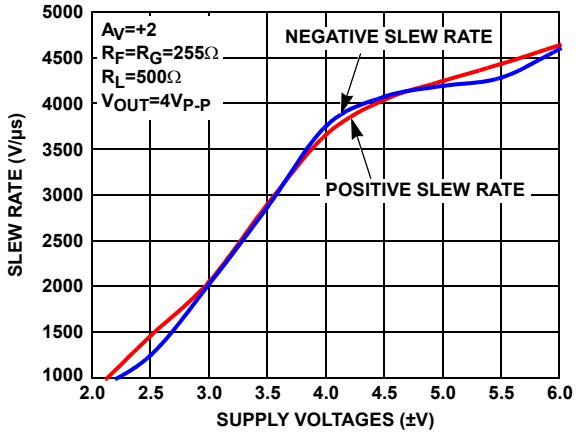


FIGURE 35. SLEW RATE vs SUPPLY VOLTAGES

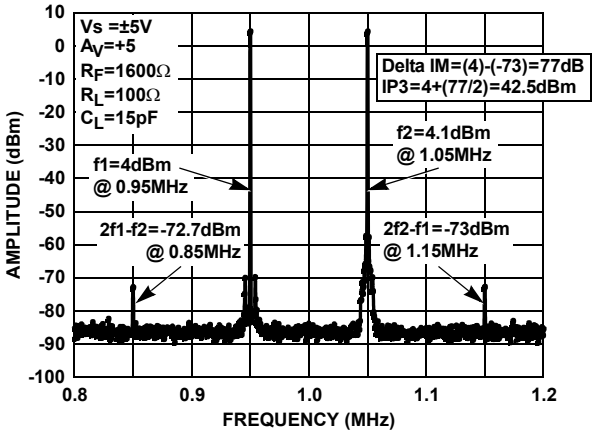


FIGURE 36. THIRD ORDER IMD INTERCEPT (IP3)

Typical Performance Curves (Continued)

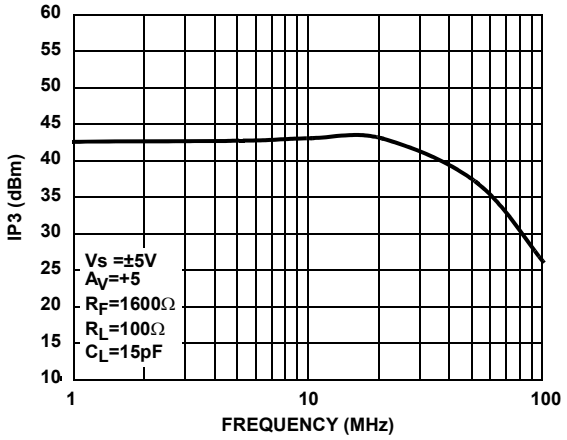


FIGURE 37. THIRD ORDER IMD INTERCEPT vs FREQUENCY

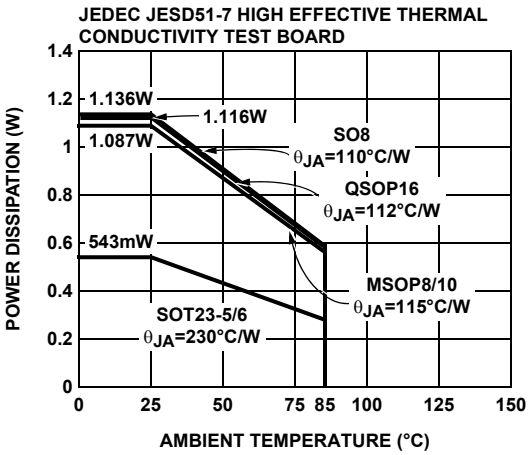


FIGURE 38. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

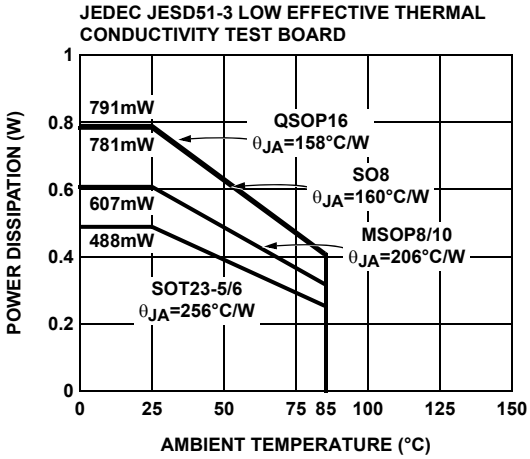


FIGURE 39. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
May 25, 2016	FN7332.8	- Updated Ordering Information Table on page 2.
October 20, 2015	FN7332.7	- Updated Ordering Information Table on page 2. - Added Revision History. - Added About Intersil Verbiage. - POD MDP0038 obsoleted and replaced by P5.064A latest revision.

About Intersil

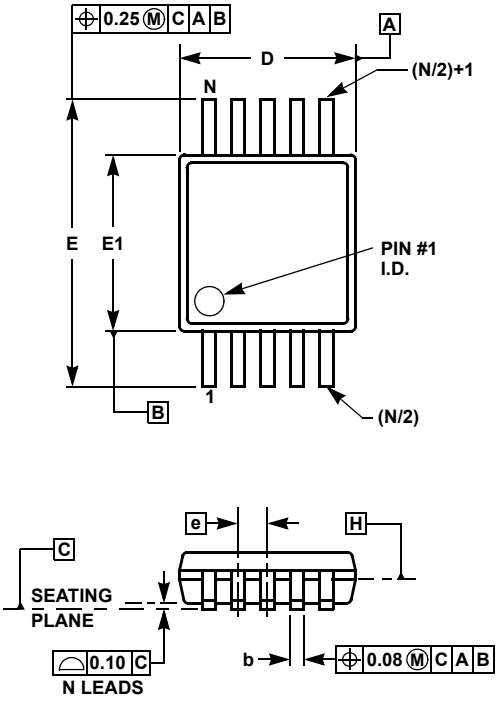
Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support.

Mini SO Package Family (MSOP)



MDP0043

MINI SO PACKAGE FAMILY

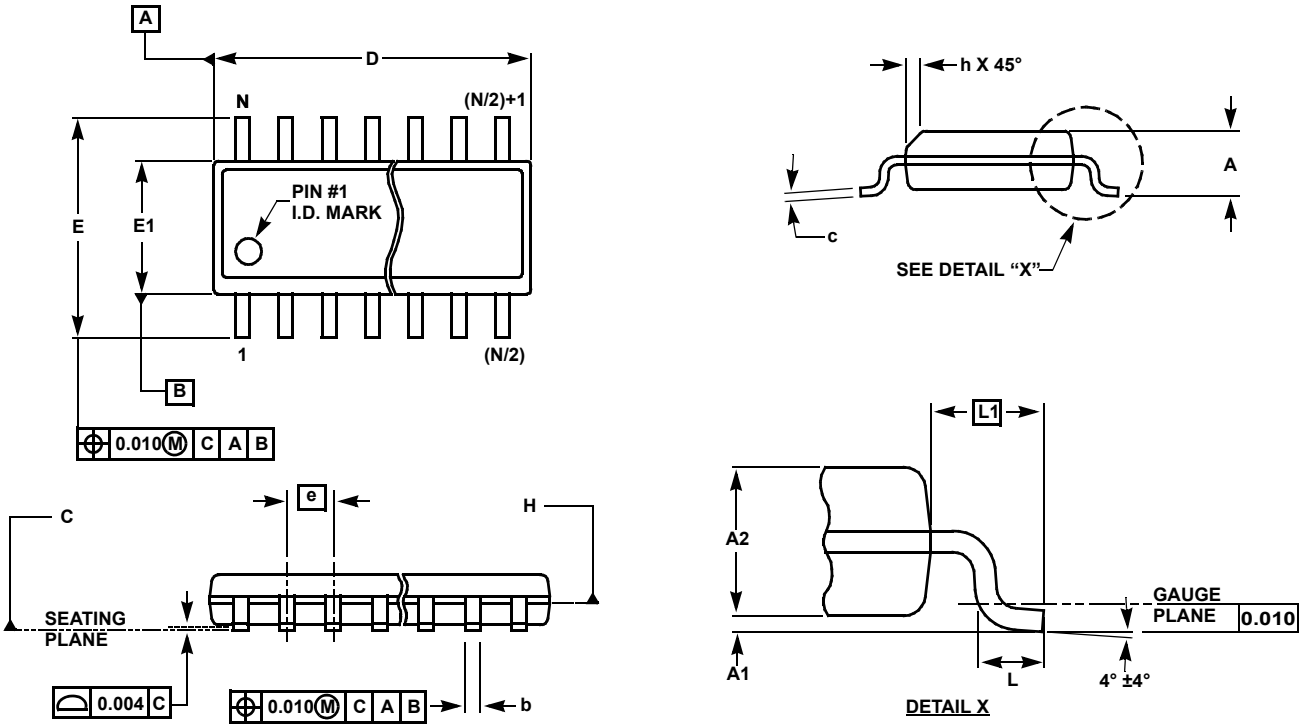
SYMBOL	MILLIMETERS		TOLERANCE	NOTES
	MSOP8	MSOP10		
A	1.10	1.10	Max.	-
A1	0.10	0.10	±0.05	-
A2	0.86	0.86	±0.09	-
b	0.33	0.23	+0.07/-0.08	-
c	0.18	0.18	±0.05	-
D	3.00	3.00	±0.10	1, 3
E	4.90	4.90	±0.15	-
E1	3.00	3.00	±0.10	2, 3
e	0.65	0.50	Basic	-
L	0.55	0.55	±0.15	-
L1	0.95	0.95	Basic	-
N	8	10	Reference	-

Rev. D 2/07

NOTES:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. Dimensions “D” and “E1” are measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.

Small Outline Package Family (SO)



MDP0027

SMALL OUTLINE PACKAGE FAMILY (SO)

SYMBOL	INCHES							TOLERANCE	NOTES
	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)		
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	±0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	±0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	±0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	±0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	±0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	±0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	±0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	±0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

Rev. M 2/07

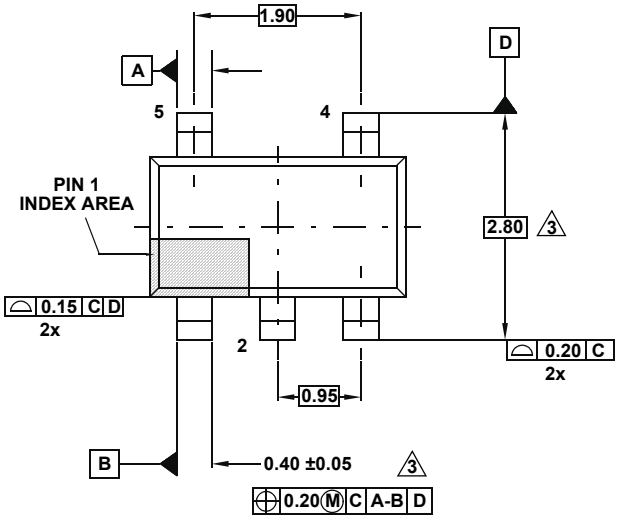
NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994

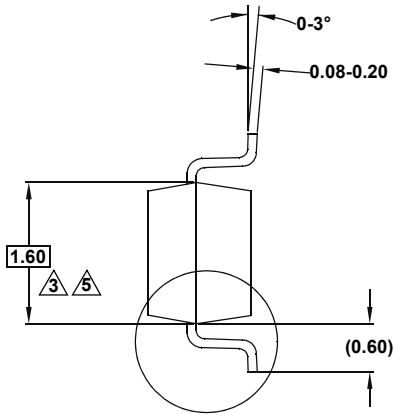
Package Outline Drawing

P5.064A

5 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE
Rev 0, 2/10

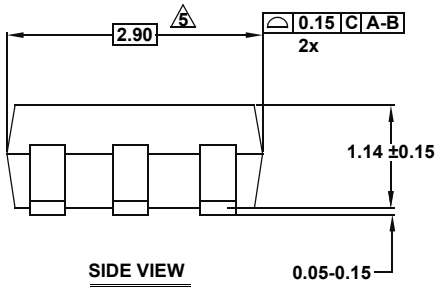


TOP VIEW

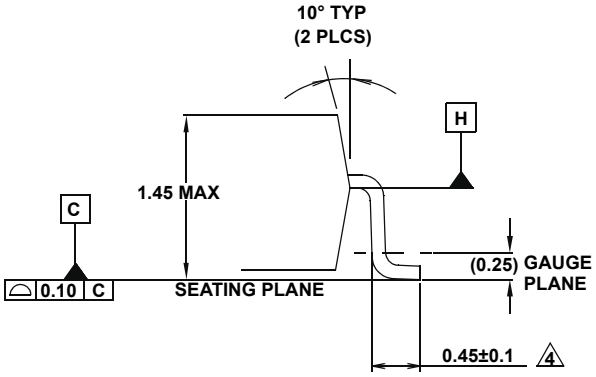


SEE DETAIL X

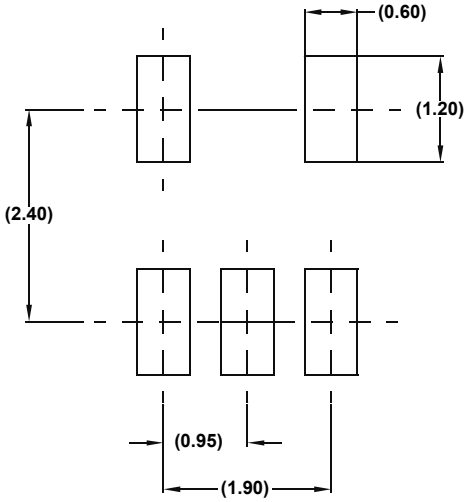
END VIEW



SIDE VIEW



DETAIL "X"

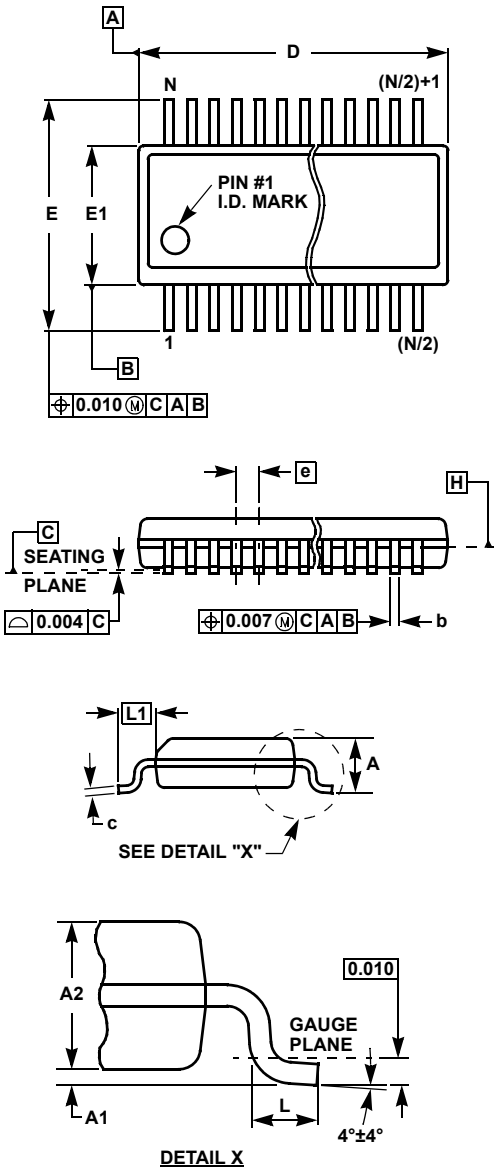


TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
3. Dimension is exclusive of mold flash, protrusions or gate burrs.
4. Foot length is measured at reference to guage plane.
5. This dimension is measured at Datum “H”.
6. Package conforms to JEDEC MO-178AA.

Quarter Size Outline Plastic Packages Family (QSOP)



MDP0040

QUARTER SIZE OUTLINE PLASTIC PACKAGES FAMILY

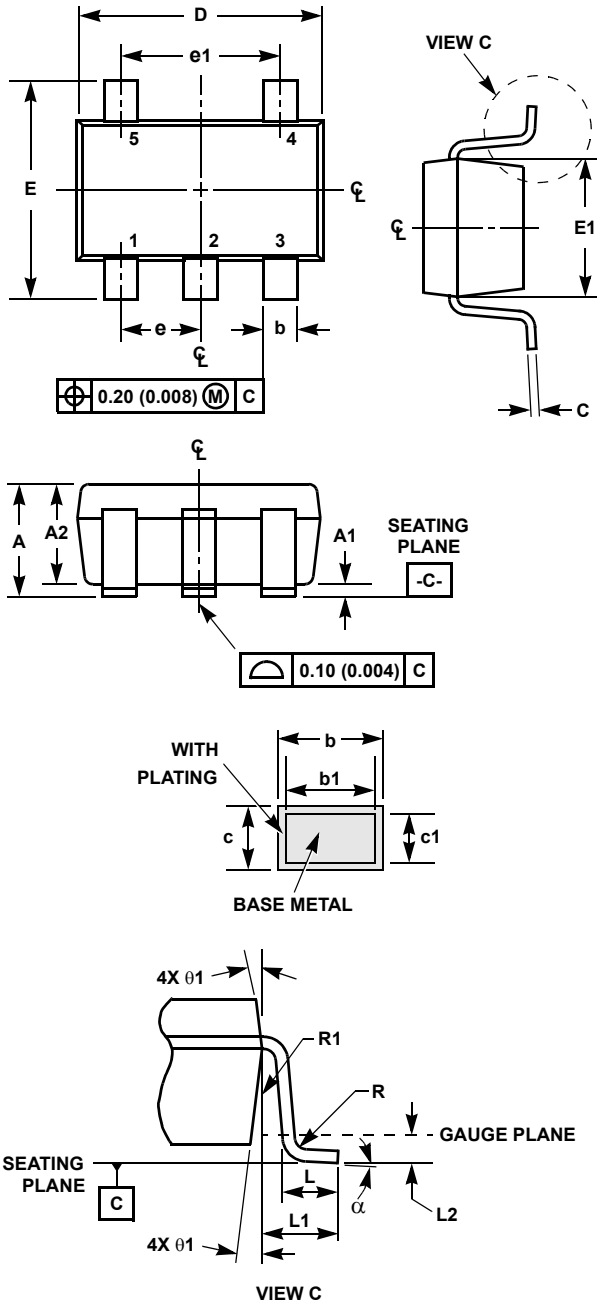
SYMBOL	INCHES			TOLERANCE	NOTES
	QSOP16	QSOP24	QSOP28		
A	0.068	0.068	0.068	Max.	-
A1	0.006	0.006	0.006	±0.002	-
A2	0.056	0.056	0.056	±0.004	-
b	0.010	0.010	0.010	±0.002	-
c	0.008	0.008	0.008	±0.001	-
D	0.193	0.341	0.390	±0.004	1, 3
E	0.236	0.236	0.236	±0.008	-
E1	0.154	0.154	0.154	±0.004	2, 3
e	0.025	0.025	0.025	Basic	-
L	0.025	0.025	0.025	±0.009	-
L1	0.041	0.041	0.041	Basic	-
N	16	24	28	Reference	-

Rev. F 2/07

NOTES:

1. Plastic or metal protrusions of 0.006” maximum per side are not included.
2. Plastic interlead protrusions of 0.010” maximum per side are not included.
3. Dimensions “D” and “E1” are measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.

Small Outline Transistor Plastic Packages (SC70-5)



P5.049

5 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.031	0.043	0.80	1.10	-
A1	0.000	0.004	0.00	0.10	-
A2	0.031	0.039	0.80	1.00	-
b	0.006	0.012	0.15	0.30	-
b1	0.006	0.010	0.15	0.25	
c	0.003	0.009	0.08	0.22	6
c1	0.003	0.009	0.08	0.20	6
D	0.073	0.085	1.85	2.15	3
E	0.071	0.094	1.80	2.40	-
E1	0.045	0.053	1.15	1.35	3
e	0.0256 Ref		0.65 Ref		-
e1	0.0512 Ref		1.30 Ref		-
L	0.010	0.018	0.26	0.46	4
L1	0.017 Ref.		0.420 Ref.		-
L2	0.006 BSC		0.15 BSC		
α	0^o	8^o	0^o	8^o	-
N	5		5		5
R	0.004	-	0.10	-	
R1	0.004	0.010	0.15	0.25	

Rev. 2 9/03

NOTES:

1. Dimensioning and tolerances per ASME Y14.5M-1994.
2. Package conforms to EIAJ SC70 and JEDEC MO-203AA.
3. Dimensions D and E1 are exclusive of mold flash, protrusions, or gate burrs.
4. Footlength L measured at reference to gauge plane.
5. “N” is the number of terminal positions.
6. These Dimensions apply to the flat section of the lead between 0.08mm and 0.15mm from the lead tip.
7. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only.