

ISL6731A, ISL6731B

Power Factor Correction Controllers

FN8582
Rev 1.00
February 13, 2015

The ISL6731A and ISL6731B are active power factor correction (PFC) controller ICs that use a boost topology. The controllers are suitable for AC/DC power systems up to 2kW and over the universal line input.

The ISL6731A and ISL6731B operate in Continuous Current Mode (CCM). Accurate input current shaping is achieved with a current error amplifier. A patent pending breakthrough negative capacitance technology minimizes zero crossing distortion and reduces the magnetic components size. The small external components result in lower design cost without sacrificing performance.

The internally clamped 12.5V gate driver delivers 1.5A peak current to the external power MOSFET. The ISL6731A and ISL6731B provide a highly reliable system that is fully protected. Protection features include cycle-by-cycle overcurrent, over power limit, over-temperature, input brownout, output overvoltage and undervoltage protection.

The ISL6731A and ISL6731B provide excellent power efficiency and transitions into a power saving skip mode during light load conditions, thus improving efficiency automatically. The ISL6731A and ISL6731B can be shut down by pulling the FB pin below 0.5V or grounding the BO pin.

Two switching frequency options are provided. The ISL6731B switches at 62kHz, and the ISL6731A switches at 124kHz.

Related Literature

- [AN1884](#), "ISL6731AEVAL1Z and ISL6731BEVAL1Z: Boost CCM PFC for 300W Universal Input Adaptors"
- [AN1885](#), "ISL6731AEVAL2Z and ISL6731BEVAL2Z: High Performance Boost CCM PFC Front End for Server Power Applications"

Features

- Reduced component size requirements
 - Enables smaller, thinner AC/DC adapters
 - Choke and cap size can be reduced
 - Lower cost of materials
- Excellent power factor and THD over line and load
 - CCM mode with negative capacitance generator for smaller EMI filter and improved performance
 - Built-in current amplifier with flexibility of gain change
- Better light-load efficiency
 - Automatic pulse skipping with programmable threshold
 - Programmable or automatic shutdown
- Highly reliable design
 - Cycle-by-cycle current limit
 - Input average power limit
 - OVP and OTP protection
 - Input brownout protection
- Small 14 Ld SOIC package

Applications

- Desktop computer AC/DC adaptor
- Laptop computer AC/DC adaptor
- TV AC/DC power supply
- AC/DC brick converters

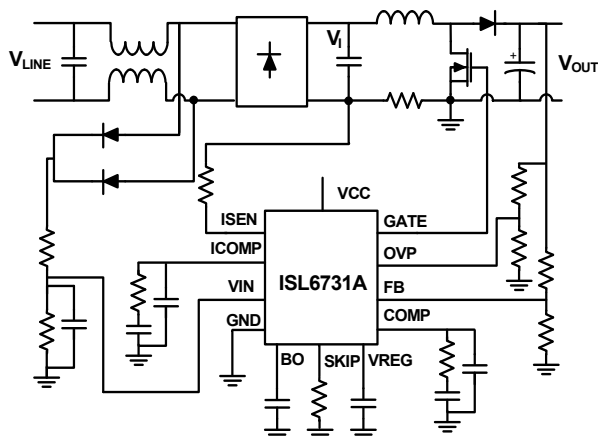


FIGURE 1. TYPICAL APPLICATION

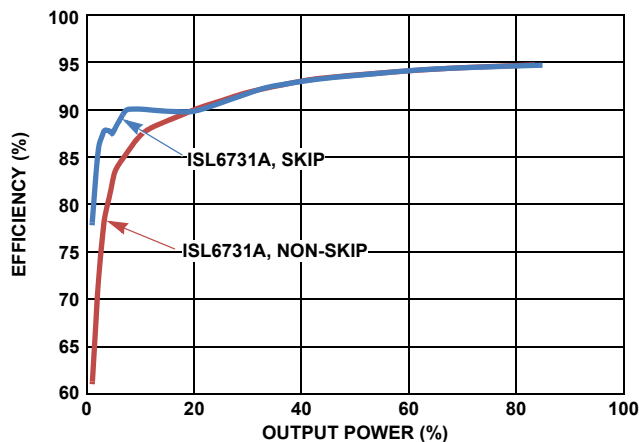
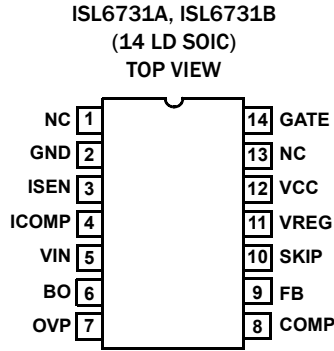


FIGURE 2. PFC EFFICIENCY

Pin Configuration



Pin Descriptions

| PIN # | I/O | SYMBOL | DESCRIPTION |
|-------|-----|--------|--|
| 1, 13 | - | NC | Not Connected. Must be floating. |
| 2 | - | GND | Ground pin. All voltage levels refer to this pin. |
| 3 | I | ISEN | Current sense pin. The current through this pin is proportional to the inductor current. |
| 4 | I/O | ICOMP | Current error amplifier output pin. |
| 5 | I | VIN | Input voltage sense. This pin provides the reference voltage to shape inductor current. Connect this pin to a resistor divider from the rectified input voltage. The resistor divider ratio is used to adjust the phase lag between input voltage and the input current. The phase lag is required to compensate the phase lead generated by the EMI filter. |
| 6 | I/O | BO | This pin should be decoupled to GND with a minimum 0.1 μ F ceramic capacitor. The BO pin is a voltage follower, which will follow the DC voltage of the VIN pin. The BO pin is internally tied to GND through a resistor R _{IS} . The decoupling capacitor provides ripple filtering. When the voltage at the BO pin (V _{BO}) drops below brownout voltage threshold, the controller enters shutdown mode and the gate drive is disabled. The BO pin will be disabled when the FB pin drops below the enabling threshold. |
| 7 | I | OVP | Overvoltage protection pin. Connect this pin to a resistor divider from the output. The resistor divider sets the OVP set point. When the OVP pin voltage exceeds 104.5% of the reference voltage V _{REF} , OVP is triggered and the gate drive is disabled. |
| 8 | I/O | COMP | Output of the error amplifier. The voltage of the COMP pin sets the input power. During start-up, a small charge current will slowly ramp up the voltage of the COMP pin. |
| 9 | I | FB | Voltage feedback pin. Connect this pin to a resistor divider from the output. The resistor divider sets the output voltage. When the FB pin voltage exceeds 104% of V _{REF} , OVP is triggered and gate drive is disabled. When the FB pin drops below 10% of V _{REF} , the device is put into shutdown mode. There is an internal pull-down current source for open loop protection. |
| 10 | I/O | SKIP | This pin has dual functions. Connecting this pin to ground disables the light load skip function. An internal 20 μ A current sources out of this pin. Connect a resistor from this pin to the ground to set the average power trip point. The converter exits the skip mode when either the VFB drops below 88% of V _{REF} or the ISEN current goes above 29 μ A. |
| 11 | - | VREG | Output of internal regulator. The voltage having a \pm 2% tolerance over line, load and operating temperature. Bypass to GND with a 47nF low ESR capacitor. VREG can source up to 10mA. This pin is not recommended for usage other than bypass. |
| 12 | I | VCC | Power supply pin. The VCC pin should be decoupled to GND with a minimum 0.1 μ F ceramic capacitor. |
| 14 | O | GATE | Push-pull gate drive for the external MOSFET. Output voltage is clamped at 12.5V. This pin provides typically 2A sink and 1.5A source capability. |

Ordering Information

| PART NUMBER (Notes 1, 2, 3) | PART MARKING | TEMP. RANGE (°C) | PACKAGE (Pb-Free) | PKG. DWG. # |
|--------------------------------|-----------------|---------------------|----------------------|----------------|
| ISL6731AFBZ | ISL 6731AFBZ | -40 to +125 | 14 Ld SOIC | M14.15 |
| ISL6731BFBZ | ISL 6731BFBZ | -40 to +125 | 14 Ld SOIC | M14.15 |

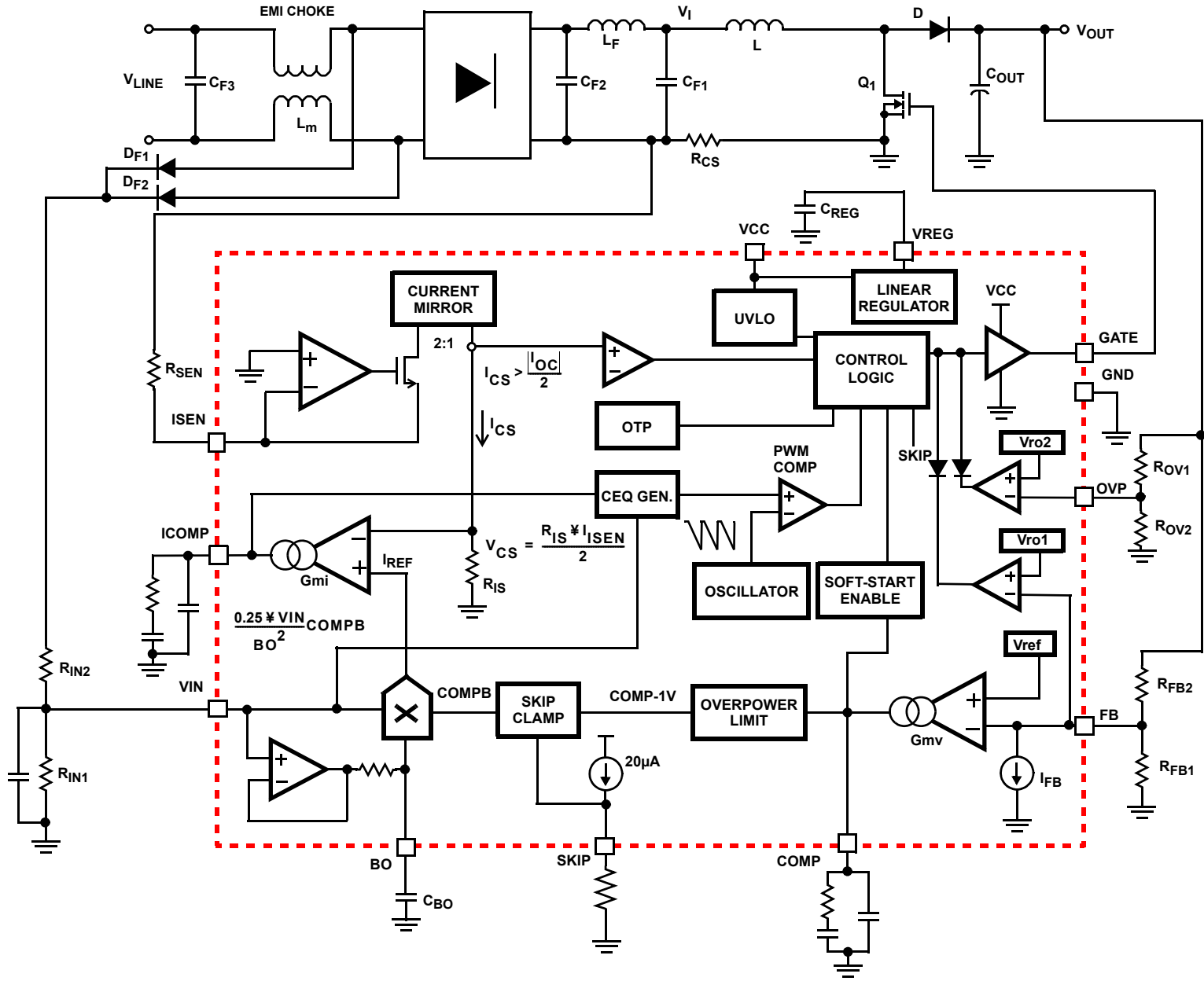
NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to [TB347](#) for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for [ISL6731A](#), [ISL6731B](#). For more information on MSL please see techbrief [TB363](#).

TABLE 1. KEY DIFFERENCES IN FAMILY OF ISL6731

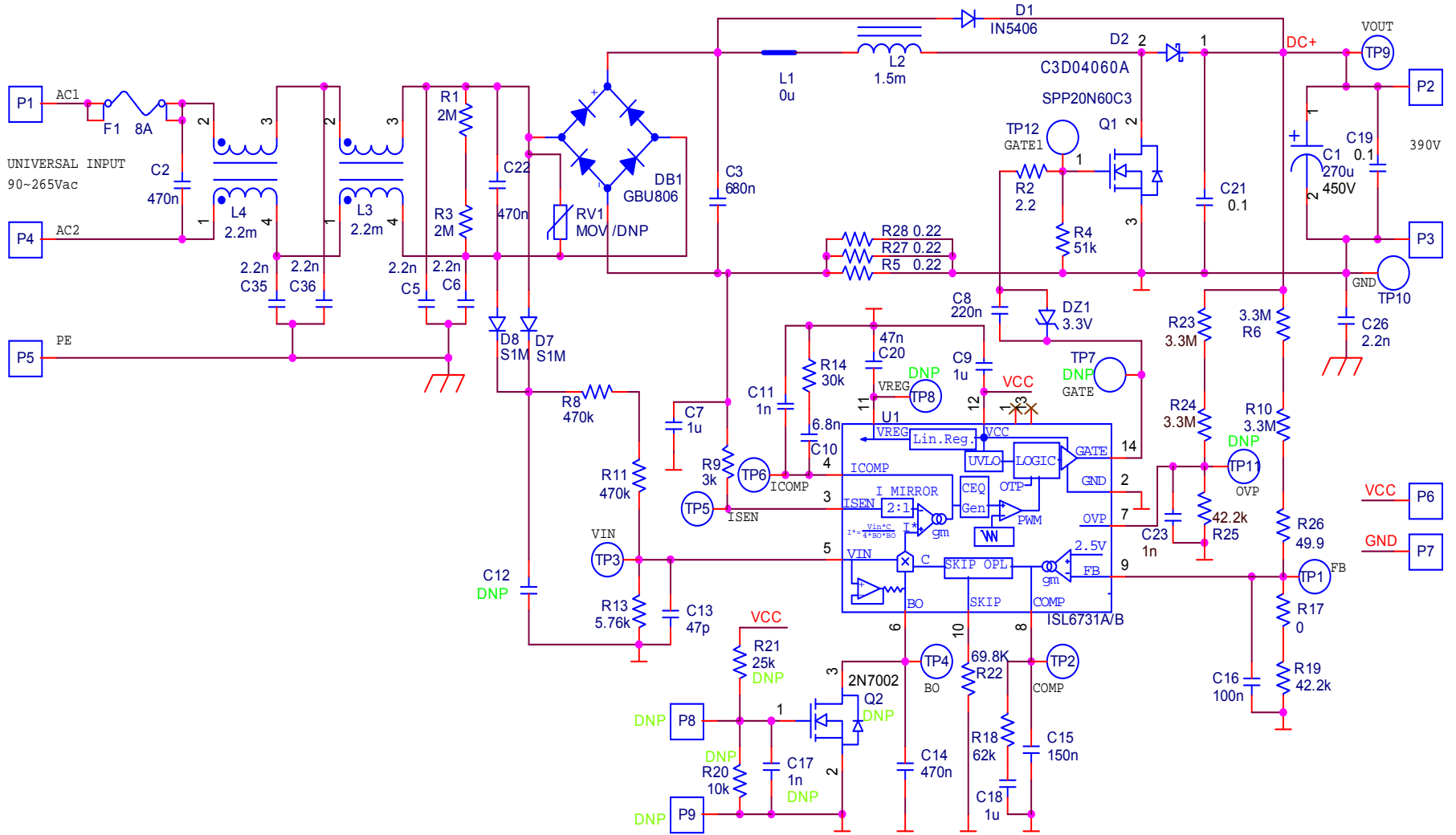
| VERSION | ISL6731A | ISL6731B |
|---------------------|----------|----------|
| Switching Frequency | 124kHz | 62kHz |

Block Diagram



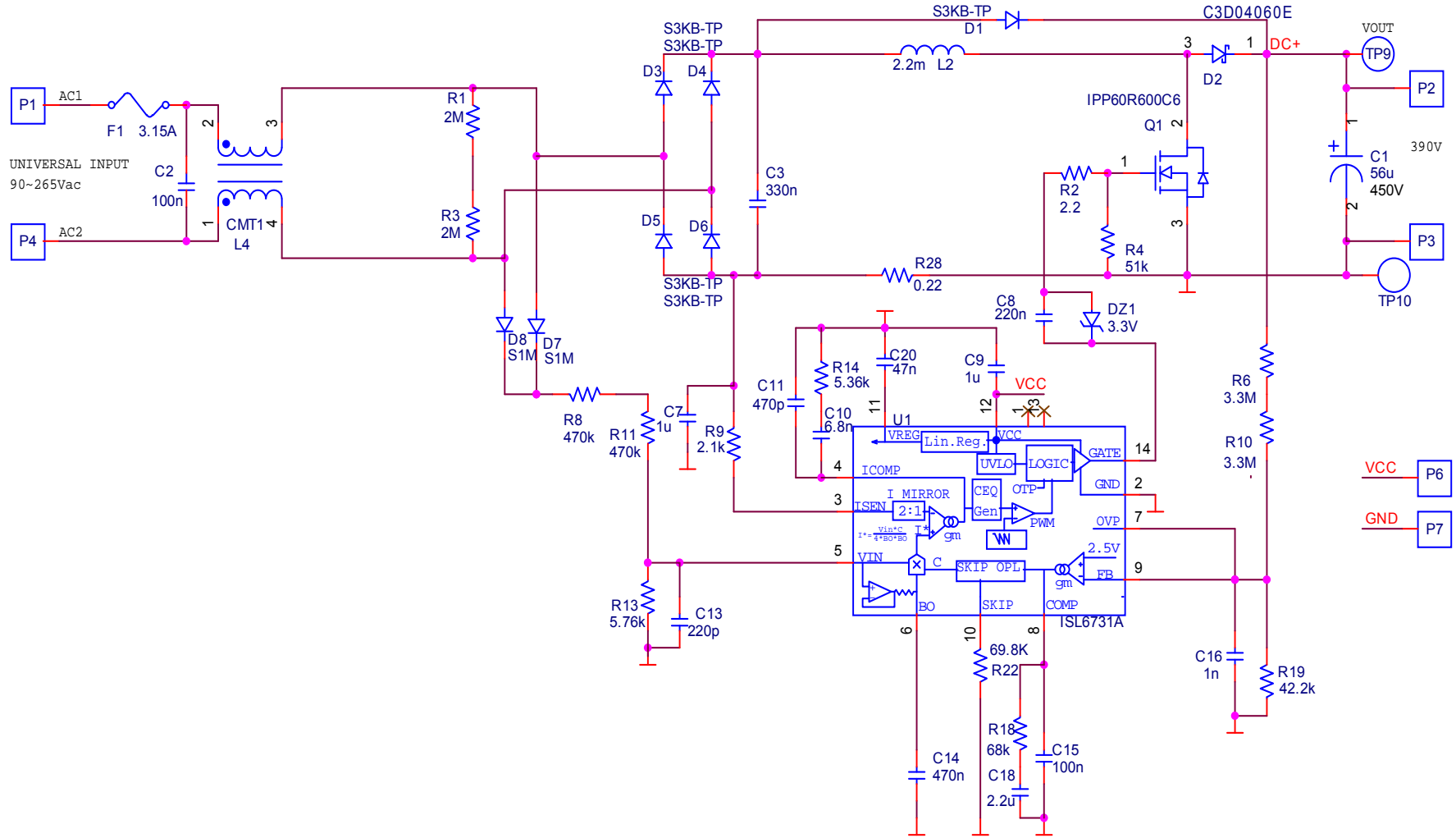
Application Schematics

Typical 300W Application Schematic



Application Schematics (Continued)

Typical 85W Application Schematic



Absolute Maximum Ratings

| | |
|--|----------------|
| VCC to GND | -0.3V to +28V |
| GATE to GND | -0.3V to +18V |
| VIN, BO, ISEN, FB, OVP, ICOMP, SKIP, VREG and COMP to GND | -0.3V to +6.3V |
| ESD Rating | |
| Human Body Model (Tested per JESD22-A114) | 2.5kV |
| Machine Model (Tested per JESD22-A115) | 200V |
| Charged Device Model (Tested per JESD-C101E) | 1kV |
| Latch-Up (Tested per JESD-78B; Class 2, Level A) | 100mA |

Thermal Information

| | | |
|--|---------------------------|----------------------|
| Thermal Resistance (Typical) | θ_{JA} (°C/W) | θ_{JC} (°C/W) |
| SOIC Package (Notes 4, 5) | 77 | 38 |
| Maximum Junction Temperature (Plastic Package) | +150°C | |
| Maximum Storage Temperature Range | -65°C to +150°C | |
| Ambient Temperature Range | -40°C to +125°C | |
| Junction Temperature Range | -40°C to +125°C | |
| Pb-Free Reflow Profile | see TB493 | |

Recommended Operating Conditions

| | |
|---------------------------|-----------------|
| VCC to GND | 12V to +20V |
| Ambient Temperature Range | -40°C to +125°C |

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

- θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief [TB379](#) for details.
- For θ_{JC} , the “case temp” location is taken at the package top center.

Electrical Specifications

Operating Conditions: $V_{CC} = 15V$, $T_A = +25^\circ C$. **Boldface limits apply across the operating temperature range, -40°C to +125°C.**

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN (Note 8) | TYP | MAX (Note 8) | UNITS |
|----------------------------------|---------------|---|-----------------|------|-----------------|---------|
| VCC SUPPLY CURRENT | | | | | | |
| Start-Up Current | I_{START} | $V_{FB} = 1V, V_{CC} < V_{CC(ON)}$ | 73 | 106 | 139 | μA |
| Standby Current | I_{STDN} | $V_{FB} = GND, V_{CC} > V_{CC(ON)}$ | 179 | 237 | 295 | μA |
| Skip Mode Current | I_{CCSKIP} | $V_{FB} = 2.5V, COMP = SKIP * 0.25 + 1V$ | 580 | 690 | 850 | μA |
| Operating Current (Note 6) | I_{CC} | GATE is floating | 3.0 | 3.7 | 4.5 | mA |
| VCC UVLO | | | | | | |
| UVLO Rising Threshold | $V_{CC(ON)}$ | | 9 | 10 | 11 | V |
| UVLO Falling Threshold | $V_{CC(OFF)}$ | | 6.7 | 7.5 | 8.3 | V |
| UVLO Threshold Hysteresis | $V_{CC(HYS)}$ | | | 2.5 | | V |
| REGULATOR VOLTAGE VREG | | | | | | |
| Overall Accuracy | V_{REG} | $I_{REG} = 0$ to $-10mA, V_{CC} = 15V$, load capacitor = 47nF | 5.1 | 5.4 | 5.6 | V |
| Current Limit | | | 30 | 50 | 70 | mA |
| PWM CONVERTERS | | | | | | |
| Maximum Duty Cycle | | $f_{SW} = 124kHz$ for ISL6731A and $f_{SW} = 62kHz$ for ISL6731B | 94.8 | 96.5 | | % |
| OSCILLATOR | | | | | | |
| Free Running Frequency, ISL6731A | | $T_A = -40^\circ C$ to $+125^\circ C, V_{IN} = 0.6V$ | 95.5 | 107 | 117 | kHz |
| Free Running Frequency, ISL6731A | | $T_A = -40^\circ C$ to $+125^\circ C, V_{IN} = 2.5V$ | 111 | 125 | 138 | kHz |
| Free Running Frequency, ISL6731B | | $T_A = -40^\circ C$ to $+125^\circ C, V_{IN} = 0.6V$ | 43.5 | 54 | 63.7 | kHz |
| Free Running Frequency, ISL6731B | | $T_A = -40^\circ C$ to $+125^\circ C, V_{IN} = 2.5V$ | 56.5 | 64 | 70.7 | kHz |
| PWM Ramp Amplitude | V_m | | 1.33 | 1.46 | 1.59 | V |

Electrical Specifications Operating Conditions: $V_{CC} = 15V$, $T_A = +25^\circ C$. **Boldface limits apply across the operating temperature range, $-40^\circ C$ to $+125^\circ C$.** (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN (Note 8) | TYP | MAX (Note 8) | UNITS |
|---|-----------------|---|-----------------|------|-----------------|-----------|
| GATE DRIVER | | | | | | |
| Gate Drive Pull-Down Resistance | | $V_{CC} = 15V$, $I_{GATE} = 15mA$ | | 2.33 | 4.46 | Ω |
| Gate Drive Pull-Up Voltage Drop | | $V_{CC} = 9V$, $I_{GATE} = 15mA$ | 0.15 | 0.3 | 0.45 | V |
| Gate Drive Max. Sourcing/Sinking Current | | | | 1.5 | | A |
| Rise Time | | $C_O = 2.2nF$, $V_{CC} = 15V$, gate voltage rise time from 10% to 90% of V_{GC} | | 34 | 62 | ns |
| Fall Time | | $C_O = 2.2nF$, $V_{CC} = 15V$, gate voltage fall time from 10% to 90% of V_{GC} | | 34 | 57 | ns |
| Gate Clamp Voltage | V_{GC} | | 10.5 | 12 | 13.5 | V |
| VOLTAGE REFERENCE | | | | | | |
| Reference Voltage | V_{REF} | | 2.48 | 2.5 | 2.52 | V |
| Feedback Pin Pull-Down Current | I_{FB} | | | 65 | | nA |
| Rising Threshold to Enable Converter | FB_EN | | 280 | 300 | 320 | mV |
| Falling Threshold to Disable Converter | FB_DIS | | 190 | 202 | 214 | mV |
| Enable Hysteresis | FB_Hys | | | 100 | | mV |
| VOLTAGE ERROR AMPLIFIER | | | | | | |
| Error Amp Transconductance | Gmv | | 50 | 77 | 104 | $\mu A/V$ |
| ISource/Sink | | | | 13 | | μA |
| COMP Offset Voltage | V_{COMP_OFF} | | 0.95 | 1.01 | 1.07 | V |
| COMP Soft-Start Enable Voltage | V_{COMP_EN} | | 0.58 | 0.64 | 0.75 | V |
| INPUT VOLTAGE SENSING | | | | | | |
| VIN Leakage Current | | | | 9 | | nA |
| MULTIPLIER GAIN | | | | | | |
| GMUL | | COMP = 2.5V, $V_{IN} = 1.0V$, $B_O = 1.0V$, $I_{SEN} = 50\mu A$ | 0.196 | 0.25 | 0.296 | V/V |
| CURRENT ERROR AMPLIFIER | | | | | | |
| Current DC Gain | A_{IDC} | $\Delta I_{ICOMP}/\Delta I_{ISEN}$ | 1.6 | 1.9 | 2.2 | A/A |
| Error Amp Transconductance | Gmi | $I_{ICOMP} = \pm 20\mu A$ | 205 | 268 | 331 | $\mu A/V$ |
| ICOMP Source/Sink Current (Note 7) | | | | 60 | | μA |
| Current Sensing Input Offset | | | -3 | 2 | 7 | mV |
| LIGHT LOAD EFFICIENCY ENHANCEMENT AND OVERPOWER PROTECTION | | | | | | |
| Skip Current Reference (Note 7) | I_{SKIP} | $V_{SKIP} = 2V$ | -23 | -20 | -17 | μA |
| Skip Falling Threshold | V_{SKIP_THf} | | 450 | 498 | 550 | mV |
| Skip Rasing Threshold | V_{SKIP_Thr} | | 570 | 616 | 690 | mV |
| COMP Upper Limit | V_{CUL} | | 3.53 | 3.85 | 4.17 | V |
| COMP Valid Range | V_{CUL-1V} | | 2.5 | 2.83 | 3.16 | V |
| FB Exit Threshold Voltage | V_{FB_EXIT} | Fraction of V_{REF} , $I_{ISEN} = 0\mu A$ | 87 | 88 | 89 | % |
| ISEN Exit Threshold Current | I_{SEN_EXIT} | $V_{FB} = 2.5V$ | -38 | -29 | -20 | μA |

Electrical Specifications Operating Conditions: $V_{CC} = 15V$, $T_A = +25^\circ C$. **Boldface limits apply across the operating temperature range, $-40^\circ C$ to $+125^\circ C$.** (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN (Note 8) | TYP | MAX (Note 8) | UNITS |
|--------------------------------------|-------------|--|-----------------|-------|-----------------|------------|
| BROWNOUT DETECTION | | | | | | |
| Brownout Rising Threshold | V_{BO_R} | | 478 | 494 | 510 | mV |
| Brownout Falling Threshold | V_{BO_F} | | 387 | 401 | 415 | mV |
| OVERVOLTAGE PROTECTION | | | | | | |
| Overvoltage Protection, FB pin | V_{RO1} | Fraction of V_{REF} ; $\sim 1\mu s$ noise filter | 103 | 104.1 | 106 | % |
| Overvoltage Protection, OVP pin | V_{RO2} | Fraction of V_{REF} ; $\sim 1\mu s$ noise filter | 103 | 104.2 | 106 | % |
| OVERCURRENT PROTECTION | | | | | | |
| Overcurrent Threshold | I_{OC} | | -197 | -177 | -159 | μA |
| THERMAL SHUTDOWN | | | | | | |
| Shutdown Temperature (Note 7) | | | | 160 | | $^\circ C$ |
| Thermal Shutdown Hysteresis (Note 7) | | | | 25 | | $^\circ C$ |

NOTES:

- 6. This is the V_{CC} current consumed when the device is active but not switching. Does not include gate drive current.
- 7. Limits should be considered typical and are not production tested.
- 8. Parameters with MIN and/or MAX limits are 100% tested at $+25^\circ C$, unless otherwise specified.

Typical Performance Curves

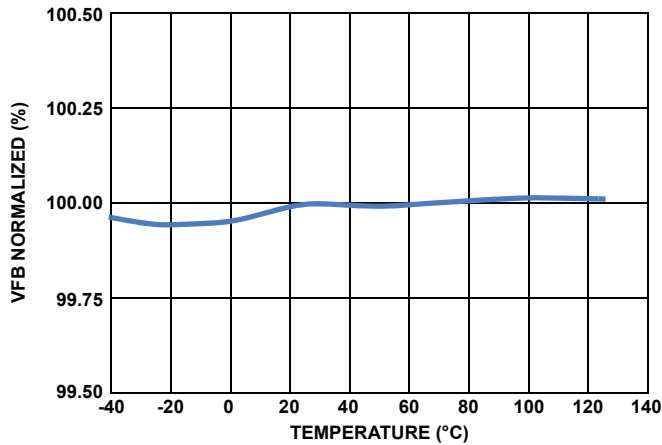


FIGURE 3. FEEDBACK ACCURACY

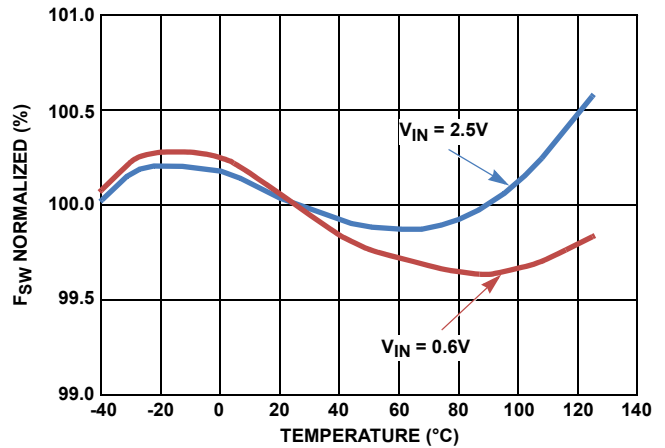


FIGURE 4. F_{SW} vs TEMPERATURE, $V_{CC} = 15V$

Typical Performance Curves (Continued)

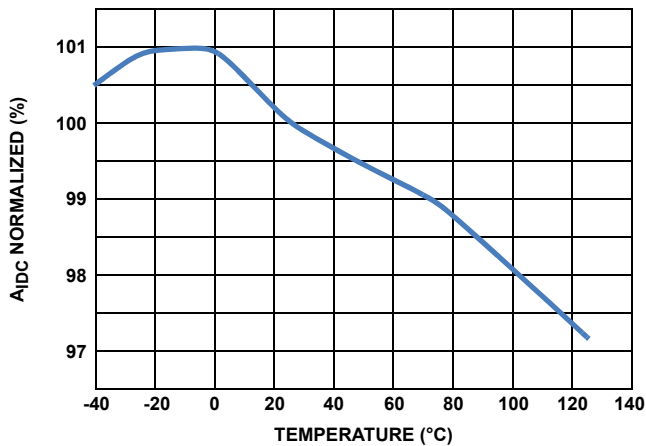


FIGURE 5. A_{IDC} vs TEMPERATURE

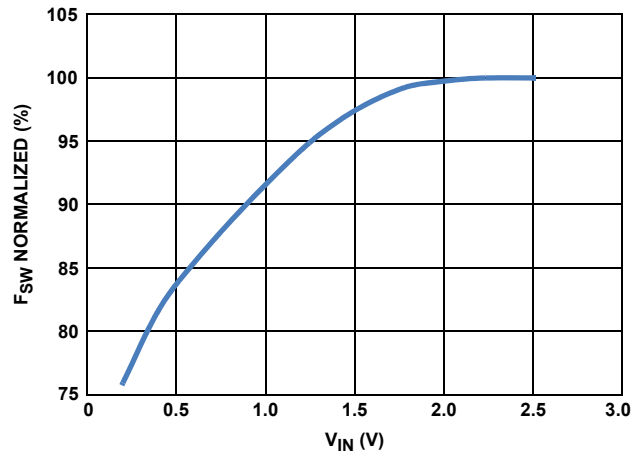


FIGURE 6. F_{SW} vs V_{IN}, T_A = +25°C

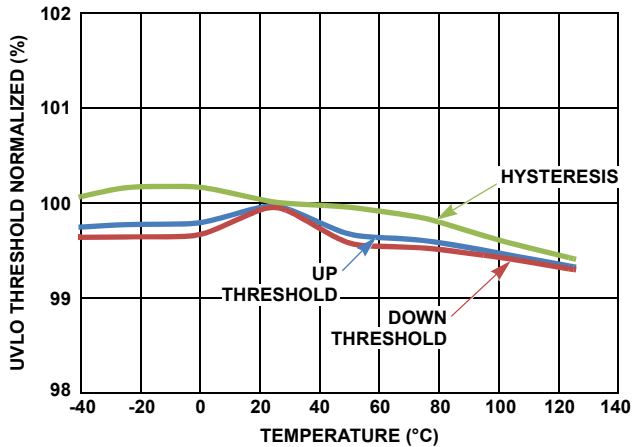


FIGURE 7. UVLO THRESHOLDS vs TEMPERATURE

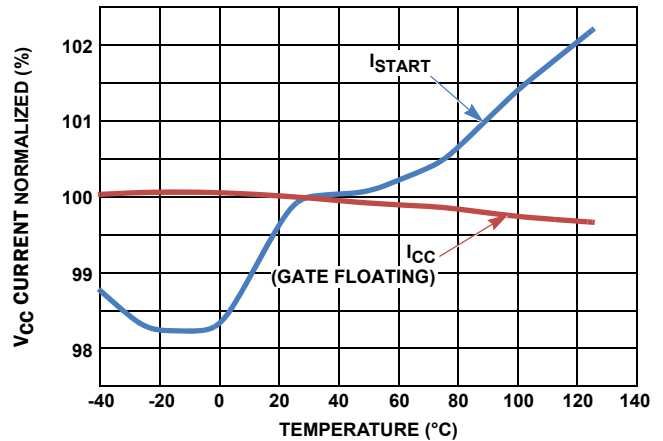


FIGURE 8. V_{CC} SUPPLY CURRENT vs TEMPERATURE

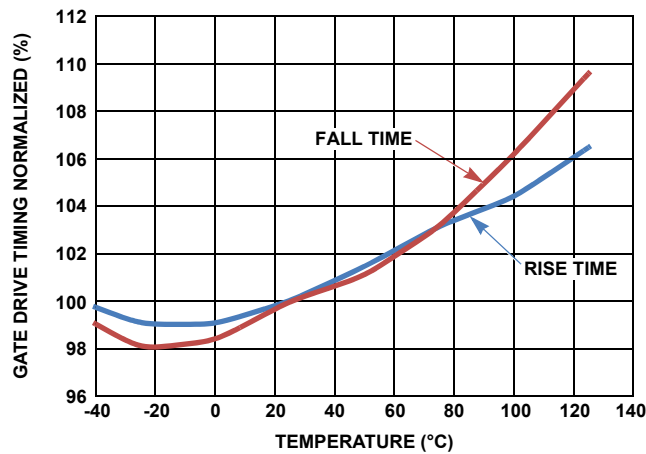


FIGURE 9. GATE DRIVE TIMING vs TEMPERATURE (LOAD = 2.2nF)

Functional Description

VCC Undervoltage Lockout (UVLO)

The ISL6731A and ISL6731B start automatically once the voltage at VCC exceeds the UVLO threshold.

Shutdown

When the VFB pin is below 0.2V, the controller is disabled and the PWM output driver is tri-stated. When disabled, the IC power will be reduced. During shutdown, the COMP pin is discharged to GND and the controller is disabled. The Over-Temperature Protection (OTP) is still alive to prevent the controller from starting up in a high temperature ambient condition.

In the event that the FB pin is disconnected from the feedback resistors, the FB pin is pulled to ground by an internal current source I_{FB} . When the FB pin voltage drops below 0.2V, the gate driver is disabled. The ISL6731A or ISL6731B enters shutdown mode.

Soft-Start

The COMP pin is released once the soft-start operation begins. A 13µA current sources out to the RC network connected from the COMP pin until the FB pin voltage reaches 90% of the reference voltage.

Switching is inhibited when the COMP pin voltage is below 1V. When the COMP pin reaches 1V, the current error amplifier and the gate driver are activated and the converter starts switching.

During UVLO, brownout and shutdown, the COMP is pulled to the ground.

Input Voltage Sensing

The VIN pin is needed to sense the rectified input voltage. The sensed semi-sinusoidal waveform is needed to shape the inductor current, which helps achieves unity power factor. At the same time, the voltage on the VIN pin is used to generate the negative capacitive element at the input. This will cancel the input filter capacitor, C_F . Canceling the effect of C_F will increase the displacement power factor and alleviate the zero crossing distortion, which is related to the distortion power factor.



FIGURE 10. INPUT VOLTAGE SENSING SCHEMATIC

The BO pin also utilizes the VIN resistor divider for voltage sensing. Set the resistor divider ratio to satisfy the brownout requirement.

First, calculate the resistor divider ratio, K_{BO} .

$$K_{BO} = \frac{V_{BORMAX}}{V_{RMSmin} - 2V_F} \quad (EQ. 1)$$

Where V_F is the forward voltage drop of the bridge rectifier and the voltage drop of D_{F1} ; D_{F2} .

Then, select the R_{IN2} based on the highest reasonable resistance value. Then select the R_{IN1} based upon the desirable minimum RMS value of the line voltage for the PFC operation.

$$R_{IN1} = \frac{K_{BO}}{1 - K_{BO}} \cdot R_{IN2} \quad (EQ. 2)$$

Inductor Current Sensing

The current sensing of the converter has two purposes. One is to force the inductor current to track the input semi-sinusoidal waveform. The other purpose is for overcurrent protection. Refer to [Figure 11](#) for the current sensing scheme. The sensed current I_{CS} is in proportion to the inductor current, I_L as described in [Equation 3](#):

$$I_{CS} = \frac{1}{2} \cdot \frac{R_{CS}}{R_{SEN}} \cdot I_L \quad (EQ. 3)$$

where:

R_{CS} is the current sensing resistor with low value in the return path to the bridge rectifier.

R_{SEN} is the current scaling resistor connected between ISEN to the R_{CS} .

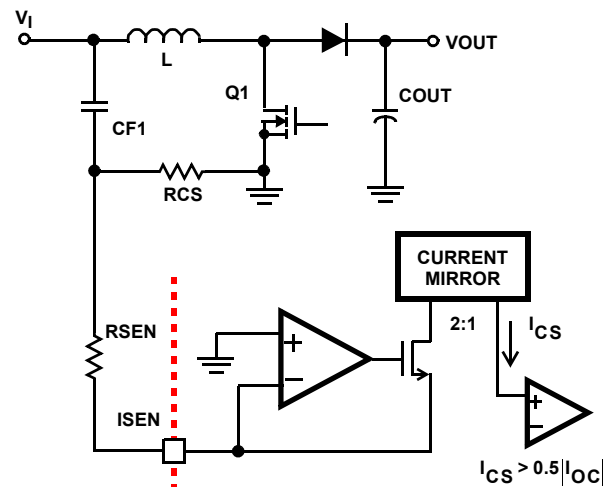


FIGURE 11. INDUCTOR CURRENT SENSING SCHEME

A high value R_{CS} renders more accurate current sensing. It is recommended to use the R_{CS} to render 120mV peak voltage at the maximum line voltage during full load condition.

$$R_{CS} > \frac{120mV \cdot V_{RMSMAX} \cdot \eta}{\sqrt{2} \cdot P_{Omax}} \quad (EQ. 4)$$

Where η is the efficiency of the converter at the maximum line input with full load.

Since the R_{CS} sees the average input current, high value R_{CS} generates high power dissipation on the R_{CS} . Use a reasonable R_{CS} according to the resistor power rating. The worst-case power dissipation occurs at the input low line when input current is at its maximum. Power dissipation by the resistor is:

$$P_{RCS} = (I_{RMSMAX})^2 \cdot R_{CS} \quad (EQ. 5)$$

where:

I_{RMSMAX} is the maximum input RMS current at the minimum input line voltage, V_{RMSmin} .

Select the R_{SEN} according to the peak current limit requirement. The resistor is sized for an overload current 25% more than the peak inductor peak current.

Negative Input Capacitor Generation

(Patent Pending)

The patent pending negative capacitor generation capability of ISL6731A and ISL6731B allow the capacitor C_{F2} to be moved from before the bridge rectifier (Figure 12) to after the bridge rectifier (Figure 13). Thus, a smaller, lower cost C_{F2} can be used. The change in topology reduces the size of the EMI filter. Furthermore, C_{F1} can be increased thus decreasing the size of L_F (Figure 13).

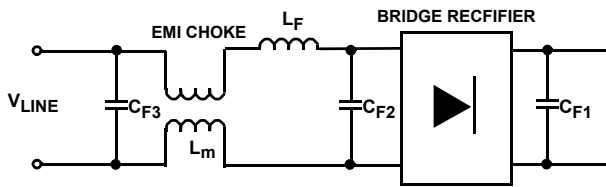


FIGURE 12. TYPICAL PFC INPUT FILTER CIRCUIT

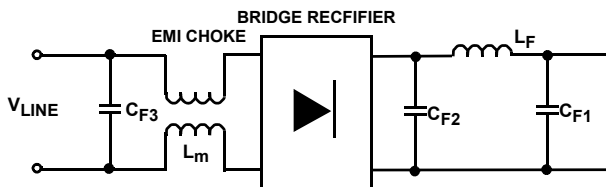


FIGURE 13. LOW COST PFC INPUT FILTER CIRCUIT

For applications where the output power is above 500W, the negative capacitance helps to improve the power factor dramatically. Refer to Table 2 for the recommended filtering capacitor to be placed after the bridge rectifier, C_{F1} .

TABLE 2. RECOMMENDED FILTERING CAPACITOR

| C_{F1} | $P_O < 100W$ | $100W < P_O < 500W$ | $P_O > 500W$ |
|----------------------------|--------------|---------------------|--------------|
| Typical $C(\mu F)/100W$ | 0.68 | 0.33 | 0.22 |

Additional C_{F1} may be used to accommodate the use of small boost inductor or to eliminate the differential mode filter inductor as long as the equipment meets the power factor or goal.

The equivalent negative capacitor is a function of the input voltage divider ratio, K_{BO} , the current sensing gain and current compensation error integration gain.

Adjusting the negative CEQ can be achieved by adjusting the current compensation network.

Frequency Modulation

The ISL6731A and ISL6731B can further reduce EMI filter size by lowering the differential noise power density. The reduction is achieved by switching frequency modulation.

The frequency varies with the VIN pin. The switching frequency reaches the peak value when the VIN pin voltage is 2V as shown in Figure 6. The peak value of ISL6731A is 124kHz, and the ISL6731B is 62kHz.

Output Voltage Regulation

The output voltage is sensed through a resistor divider. The middle point of the resistor divider is fed to the FB pin. The resistor divider ratio sets the output voltage. The transconductance error amplifier generates a current in proportion to the difference between the FB pin and the 2.5V internal reference. The PFC is stabilized by the compensation network that is connected from the COMP pin to the ground.

The voltage of the COMP sets the input average power by determining the amplitude of the current reference. To keep the harmonic distortion to a minimum, it is desirable to set the control bandwidth much lower than twice of the line frequency. The recommended voltage loop bandwidth is 10Hz.

During start-up, the compensation capacitors and the charging current from the error amplifier sets the input power increase rate. Thus, soft-start is achieved.

The COMP is discharged during shutdown and fault conditions.

Light Load Efficiency Enhancement

For PC, adaptor and TV applications, it is desirable to achieve high efficiency at light load conditions and low standby current. The ISL6731A and ISL6731B can enter light load skip mode automatically. The skip mode trigger threshold is adjustable by the SKIP pin. A 20μA current source out of the SKIP pin sets the voltage on the pin via a resistor connected between the pin and ground. Connecting this pin to ground disables the light load skip function.

The voltage error amplifier output, COMP, is an indicator of the average input power level. The controller compares the V(COMP) and V(SKIP). If $V(COMP)-1V$ is less than $V(SKIP)*0.25$, the PFC controller stops gate switching and the COMP pin voltage is clamped to $V(SKIP)+0.6V$.

The controller exits skip mode when V_{FB} drops to 88% (typical) of the reference voltage or when the sensed returned current exceeds 29μA.

Protection Circuits

Input Brownout, BO Protection

Brownout occurs when there is a drop in the line voltage. The BO pin is a dual function pin. The BO pin detects the brownout condition and shuts down the gate driver and controller. During normal operation, the BO pin is used to compensate the effect of the input line voltage change on the voltage loop. To keep the harmonic distortion low, the corner frequency formed by the R_{BO} and C_{BO} should be lower than 6Hz.

The BO pin is the output of the average voltage of the rectified voltage. The PFC controller is turned off when the BO pin drops below 0.4V. This protects the PFC power stage to enable operation at or below brownout condition for long periods of time. The controller resumes operation when the BO pin returns to 0.5V.

The BO pin is usually connected to GND through a capacitor, C_{BO} . To avoid distortion on the VIN pin, select C_{BO} so that:

$$C_{BO} \gg 0.22\mu\text{F} \quad (\text{EQ. 6})$$

Overcurrent Protection

The peak current limit function prevents the inductor from saturation. The gate driver turns off when the current goes above the current limit set point.

Overpower Protection

The overpower protection is implemented by limiting the COMP pin voltage higher than 3.85V (typical).

Overvoltage Protection

If the voltage on the FB pin exceeds the reference voltage V_{REF} by about 4%, the gate driver is turned off.

If the voltage on the OVP pin exceeds the V_{REF} by about 4.5%, the gate driver is turned off.

The controller resumes normal operation after both OVP and FB pin drops below V_{REF} .

Over-Temperature Protection

The ISL6731A and ISL6731B are protected against over-temperature conditions. When the junction temperature exceeds +160°C, the PWM shuts down. Normal operation is resumed when the junction temperature decreases below +135°C.

Application Guidelines

Layout Considerations

As in any high frequency switching converter, layout is very important. Switching current from one power device to another can generate voltage transients across the impedances of the interconnecting bond wires and circuit traces. These interconnecting impedances should be minimized by using wide, short printed circuit traces. The critical components should be located as close together as possible using ground plane construction or single point grounding.

Figure 14 shows the critical power components; Q_1 , D and C_{OUT} . To minimize the voltage overshoot, the interconnecting wires indicated by heavy lines should be part of the ground or the power plane in a printed circuit board. The components shown in Figure 14 should be located as close together as possible. Please note that the capacitors C_{VCC} and C_O each represent numerous physical capacitors. Locate the ISL6731A or ISL6731B within 2 inches of the MOSFET, Q_1 . The circuit traces for the MOSFETs' gate and source connections from the ISL6731A and ISL6731B must be sized to handle up to 1.5A peak current.

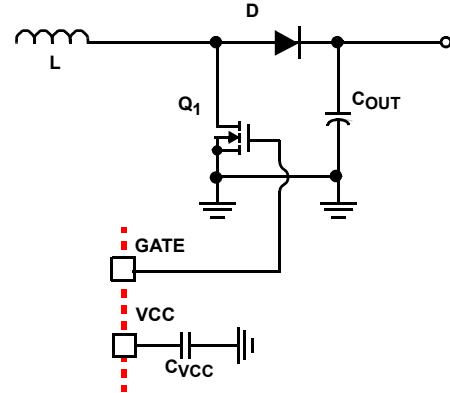


FIGURE 14. CRITICAL CURRENT POWER COMPONENTS

Component Selection Guidelines

A 300W, universal input, PFC converter design is provided for demonstration. The design method is for a continuous current mode power factor correction boost converter with the ISL6731B. The switching frequency is 62kHz.

Tables 3 shows the design parameters.

TABLE 3. CONVERTER DESIGN PARAMETERS

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|------------|------------------------|-----|---------|-----|----------|
| V_{LINE} | | 90 | 115/230 | 265 | V_{AC} |
| F_{LINE} | | 47 | | 63 | Hz |
| P_{OMAX} | Maximum Output Power | | | 300 | W |
| T_{HOLD} | Hold Up Time | | 20 | | ms |
| Efficiency | $V_{LINE} = 115V_{AC}$ | 92 | | | % |

BOOST INDUCTOR SELECTION

First, calculate the maximum input RMS current, I_{INMAX} .

$$I_{INMAX} = \frac{P_{OMAX}}{\eta \cdot V_{RMSmin}} \quad (\text{EQ. 7})$$

Where η is the converter efficiency at V_{RMSmin} . PF is the power factor at V_{RMSmin} .

$$I_{INMAX} = \frac{300\text{W}}{0.92 \cdot 90\text{V}} = 3.62\text{A} \quad (\text{EQ. 8})$$

Assuming the current is sinusoidal and the peak-to-peak ripple at line is 40%.

The boost inductor, L_{BST} , is given in [Equations 9](#) and [10](#):

$$L_{BST} \geq \frac{\sqrt{2}V_{RMSmin}}{0.4 \cdot F_{sw} \cdot \sqrt{2} \cdot I_{INMAX}} \cdot \left(1 - \frac{\sqrt{2} \cdot V_{RMSmin}}{V_{OUT}}\right) \quad (\text{EQ. 9})$$

$$L_{BST} \geq \frac{90V}{0.4 \cdot 64kHz \cdot 3.62A} \cdot \left(1 - \frac{\sqrt{2} \cdot 90V}{390V}\right) = 654\mu H \quad (\text{EQ. 10})$$

Choose inductance of 1.5mH, consider the μ_r will decrease at high current for a powder core inductor. The peak current of the inductor is the sum of the average peak inductor current and half of the peak-to-peak ripple current. Select and design the boost inductor as given by [Equation 11](#). The ISL6731A and ISL6731B provides peak current limit function that can prevent the boost inductor saturation. Assuming 25% margin is given to the OCP threshold, select and design the boost inductor with saturation current given by [Equation 11](#) with 25% margin.

$$I_{LPeak} = \sqrt{2} \cdot I_{INMAX} \cdot \left(1 + \frac{\Delta I}{2}\right) \quad (\text{EQ. 11})$$

$$I_{LPeak} = \sqrt{2} \cdot 3.88A \cdot \left(1 + \frac{1.786A}{2}\right) = 6.017A \quad (\text{EQ. 12})$$

INPUT RECTIFIER

The maximum average input current is calculated:

$$I_{INAVE(max)} = \frac{2 \cdot \sqrt{2} \cdot I_{INMAX}}{\pi} \quad (\text{EQ. 13})$$

$$I_{INAVE(max)} = \frac{2 \cdot \sqrt{2} \cdot 3.62A}{\pi} = 3.3A \quad (\text{EQ. 14})$$

Select the bridge diode using [Equation 15](#) and sufficient reverse breakdown voltage. Assuming the forward voltage, $V_{F, BR}$, is 1V across each rectifier diode. The power loss of the rectifier bridge can be calculated:

$$P_{BR} = 2 \cdot V_{F, BR} \cdot I_{INAVE(max)} \quad (\text{EQ. 15})$$

$$P_{BR} = 2 \cdot 1V \cdot 3.3A = 6.524W \quad (\text{EQ. 16})$$

INPUT CAPACITOR SELECTION

Refer to [Table 2](#) for the recommended input filter capacitor value.

$$C_{F1} = 300W \cdot \frac{0.33}{100} = 0.99\mu F \quad (\text{EQ. 17})$$

This is the recommended capacitor used after the diode bridge. For better power factor, less capacitance can be used. To lower the input filter inductor size, more capacitance can be used.

One 0.68 μ F capacitors is used for C_{F1} .

BOOST DIODE SELECTION

The boost diode loss is determined by the diode forward voltage drop, V_F and the output average current. The maximum output current is:

$$I_{OUT(max)} = \frac{P_{OMAX}}{V_{OUT}} \quad (\text{EQ. 18})$$

$$I_{OUT(max)} = \frac{300W}{390V} = 0.77A \quad (\text{EQ. 19})$$

The forward power loss on the diode is:

$$P_{FD} = I_{OUT(max)} \cdot V_F \quad (\text{EQ. 20})$$

$$P_{FD} = 0.77A \cdot 0.9V = 0.692W \quad (\text{EQ. 21})$$

The CREE C3D10060A SiC Schottky diode is selected.

The reverse recovery loss on the diode can be calculated. The Q_{RR} is found from the diode datasheet. $Q_{RR} = 25nC$.

The reverse recover loss on the diode can be estimated:

$$P_{RRD} = \frac{1}{4} \cdot Q_{RR} \cdot V_{OUT} \cdot F_{sw} \quad (\text{EQ. 22})$$

$$P_{RRD} = \frac{1}{4} \cdot 25nC \cdot 390V \cdot 62kHz = 0.156W \quad (\text{EQ. 23})$$

The total power loss on the diode is:

$$P_D = P_{FD} + P_{RRD} = (0.692 + 0.156)W = 0.848W \quad (\text{EQ. 24})$$

MOSFET POWER DISSIPATION

The power dissipation on the MOSFET is from two different types of losses; the conduction loss and the switching loss.

For the MOSFET, the worst case is at minimum line input voltage.

First, the drain-to-source RMS current is calculated:

$$I_{DS(max)} = I_{INMAX} \sqrt{1 - \frac{8\sqrt{2}}{3\pi} \cdot \frac{V_{RMSmin}}{V_{OUT}}} \quad (\text{EQ. 25})$$

$$I_{DS(max)} = 3.623A \sqrt{1 - \frac{8\sqrt{2}}{3\pi} \cdot \frac{90V}{390V}} = 3.081A \quad (\text{EQ. 26})$$

The MOSFET, SPP20N60C3 is selected.

$$P_{COND} = I_{DS(max)}^2 \cdot r_{DS(on)} \quad (\text{EQ. 27})$$

$$P_{COND} = 3.3A^2 \cdot 0.285\Omega = 2.71W \quad (\text{EQ. 28})$$

The switching loss of the MOSFET consists of three parts: the turn-on loss, the turn-off loss and the diode reverse recovery loss.

From the MOSFET datasheet, the typical switching losses curves are provided.

When $R_G = 3.6\Omega$, $I_D = 6A$, $E_{ON} = 0.013mJ$, $E_{OFF} = 0.020mJ$.

The switching loss due to transition is calculated:

$$P_{SW} = (E_{ON} + E_{OFF}) \cdot F_{sw} \quad (\text{EQ. 29})$$

$$P_{SW} = (0.013mJ + 0.020mJ) \cdot 64kHz = 2.09W \quad (\text{EQ. 30})$$

The loss caused by C_{OSS} can be estimated as:

$$P_{OSS} = \frac{2}{3} C_{OSS} \cdot V_{OUT}^2 \cdot F_{sw} \quad (\text{EQ. 31})$$

From the MOSFET datasheet, the $C_{OSS} = 197pF$ when $V_{OUT} = 390V$.

$$P_{OSS} = \frac{2}{3} 197pF \cdot 390V^2 \cdot 64kHz = 1.28W \quad (\text{EQ. 32})$$

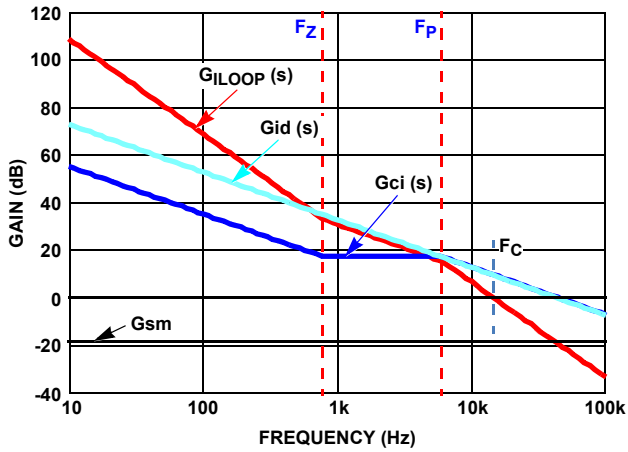


FIGURE 16. ASYMPTOTIC BODE PLOT FOR CURRENT LOOP GAIN

$$F_Z = \frac{1}{2\pi \cdot R_{ic} \cdot C_{ic}} \quad (\text{EQ. 46})$$

$$F_P = \frac{1}{2\pi \cdot R_{ic} \cdot \frac{C_{ip} \cdot C_{ic}}{C_{ip} + C_{ic}}} \quad (\text{EQ. 47})$$

Use the following guidelines for locating the poles and zeros of the compensation network.

Near the crossover frequency, the transfer function from duty cycle to inductor current is well approximated by Equation 48:

$$G_{id}(s) = \frac{V_{OUT}}{L_{BST} \cdot s} \quad (\text{EQ. 48})$$

The compensation gain uses external impedance networks as shown in Figure 15, $G_{ci}(s)$ is given by:

$$G_{ci}(s) = G_{mi} \frac{1}{(C_{ic} + C_{ip}) \cdot s} \cdot \frac{\frac{s}{2 \cdot \pi \cdot F_Z} + 1}{\frac{s}{2 \cdot \pi \cdot F_P} + 1} \quad (\text{EQ. 49})$$

The current gain and modulation gain G_{sm} is:

$$G_{sm} = \frac{R_{cs}}{R_{sen}} \cdot \frac{R_{is}}{2 \cdot V_m} \quad (\text{EQ. 50})$$

where V_m is the amplitude of the PWM carrier. The open loop gain of the current loop is:

$$G_{ILOOP}(s) = G_{id}(s) \cdot G_{sm} \cdot G_{ci}(s) \quad (\text{EQ. 51})$$

It is recommended to set the crossover frequency, F_C from 1/10 to 1/6 of the switching frequency with a phase margin of 60°. A high frequency pole, F_P , is set at 1/2 of the switching frequency for ripple filtering. In this example, we set the F_C at 14kHz.

$$F_Z = \frac{F_C}{\tan\left(\text{atan}\left(\frac{F_C}{F_P}\right) + \Phi_M\right)} \quad (\text{EQ. 52})$$

Where Φ_M is the phase margin, which is 20°. $F_P = 6\text{kHz}$. This is an aggressive example to fulfill a tight THD for light load.

Thus, the current loop compensation zero is:

$$F_Z = \frac{14\text{kHz}}{\tan\left(\text{atan}\left(\frac{14\text{kHz}}{6\text{kHz}}\right) + 20\text{deg}\right)} = 0.78\text{kHz} \quad (\text{EQ. 53})$$

The total compensation capacitance is calculated:

$$C_{ip} + C_{ic} = \left(\left(\frac{V_{OUT}}{L_{BST} \cdot (2\pi f_c)^2} \cdot \frac{A_{IDC}}{V_m} \cdot \frac{R_{CS}}{R_{SEN}} \right) \cdot \sqrt{\frac{1 + (f_c/f_z)^2}{1 + (f_c/f_p)^2}} \right) \quad (\text{EQ. 54})$$

$$C_{ip} + C_{ic} = 7.345\text{nF} \quad (\text{EQ. 55})$$

$$C_{ip} = (C_{ip} + C_{ic}) \frac{f_z}{f_p} \quad (\text{EQ. 56})$$

The value of the noise filtering capacitor is:

$$C_{ip} = 7.345\text{nF} \cdot \frac{0.78\text{kHz}}{6\text{Hz}} = 0.958\text{nF} \quad (\text{EQ. 57})$$

The value of C_{ic} is:

$$C_{ic} = 7.345\text{nF} - 0.958\text{nF} = 6.378\text{nF} \quad (\text{EQ. 58})$$

The value of R_{ic} is:

$$R_{ic} = \frac{1}{2\pi \cdot 0.78\text{kHz} \cdot 6.378\text{nF}} = 31.85\text{k}\Omega \quad (\text{EQ. 59})$$

Select the R_C value from the standard value, we have:

$R_{ic} = 30\text{k}\Omega$, $C_{ic} = 6.8\text{nF}$, $C_{ip} = 1\text{nF}$. Figure 17 shows the actual bode plot of current loop gain.

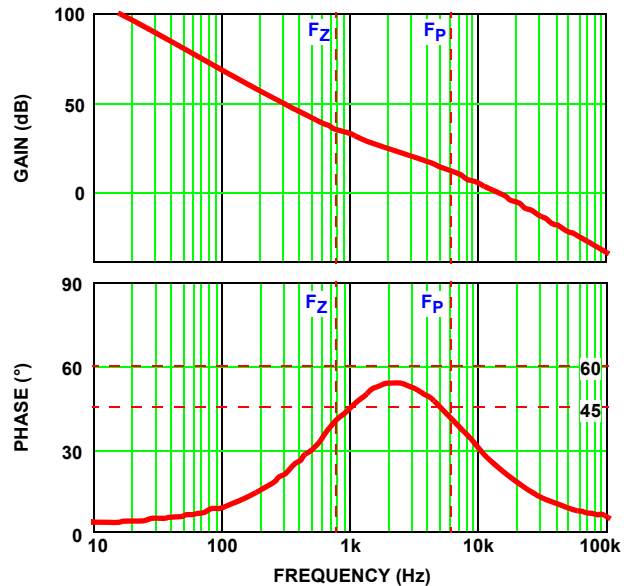


FIGURE 17. BODE PLOT OF THE ACTUAL CURRENT LOOP GAIN

INPUT VOLTAGE SETTING

First, set the B0 resistor divider gain, K_{BO} according to [Equations 1](#) and [2](#).

Assuming the converter starts at $V_{LINE} = 80V_{RMS}$, then the B0 resistor divider gain, K_{BO} , should be:

$$K_{BO} = \frac{0.5V}{80V - 2V} = 0.00641 \quad (\text{EQ. 60})$$

In this design, two 470k Ω resistors in series are used for R_{IN2} . Therefore, R_{IN1} is calculated:

$$R_{IN1} = \frac{0.00641}{1 - 0.00641} \cdot (0.94M\Omega) = 6.065k\Omega \quad (\text{EQ. 61})$$

We choose $R_{IN1} = 5.76k\Omega$, the actual K_{BO} is calculated:

$$K_{BO} = \frac{R_{IN1}}{R_{IN1} + R_{IN2}} = 0.00609 \quad (\text{EQ. 62})$$

NEGATIVE INPUT CAPACITOR GENERATION

The ISL6731A and ISL6731B generate an equivalent negative capacitance at the input to cancel the input filter capacitance. Thus, more input capacitors can be used without reducing the power factor.

The input equivalent negative capacitance is a function of the current sensing gain, B0 resistor divider gain and the compensation components.

$$C_{NEG} = \left(K_{BO} \cdot 0.8 - \frac{V_m}{V_{OUT}} \right) \frac{R_{SEN}}{R_{CS} A_{IDC}} (C_{ic} + C_{ip}) \quad (\text{EQ. 63})$$

$$C_{NEG} = \left(0.00609 \cdot 0.8 - \frac{1.5}{390} \right) \frac{3k}{0.073 \cdot 1.9} (6.8nF + 1nF) = 0.17\mu F \quad (\text{EQ. 64})$$

This equivalent negative capacitor cancels the input filter capacitor required for EMI filtering. Therefore, the displacement power factor significantly improves.

For example, $C_{F1} = 0.68\mu F$, $C_{F2} = C_{F3} = 0.47\mu F$, using the low cost EMI filter shown in [Figure 13](#). When $V_{LINE} = 230VAC$, $f_{LINE} = 50Hz$, $P_O = 300W$.

Assuming 95% efficiency under the above test condition, the resistive component of the line current, which is in phase to voltage:

$$I_a = \frac{P_O}{V_{LINE} \cdot 0.95} = 1.373A \quad (\text{EQ. 65})$$

The reactive current through the input capacitors:

$$I_c = V_{LINE} \cdot (2\pi \cdot f_{LINE}) \cdot (C_{F1} + C_{F2} + C_{F3}) = 0.14A \quad (\text{EQ. 66})$$

Thus, the displacement power factor is:

$$PF_{DIS} = \frac{I_a}{\sqrt{(I_a)^2 + (I_c)^2}} = 0.9948 \quad (\text{EQ. 67})$$

The reactive current generated by the equivalent negative capacitor is:

$$I_{cneg} = V_{LINE} \cdot (2\pi \cdot f_{LINE}) \cdot (C_{NEG}) = 0.015A \quad (\text{EQ. 68})$$

With the equivalent negative capacitor, the total reactive current reduces to:

$$I_c - I_{cneg} = 0.126A \quad (\text{EQ. 69})$$

The displacement power factor increases to:

$$PF_{DIS} = \frac{I_a}{\sqrt{(I_a)^2 + (I_c - I_{cneg})^2}} = 0.9958 \quad (\text{EQ. 70})$$

VOLTAGE LOOP COMPENSATION

The average boost diode forward current can be approximated by:

$$I_{D(ave)} = \frac{P_{in}}{V_{OUT}} \quad (\text{EQ. 71})$$

Assuming the input current traces the input voltage perfectly. The input power is in proportion to $(V_{COMP} - 1V)$.

$$I_{D(ave)} = \frac{R_{SEN}}{R_{CS} \cdot 0.5 \cdot R_{IS}} \cdot \frac{1}{V_{OUT}} \cdot \left(\frac{0.25}{((2\sqrt{2})/\pi)^2 \cdot K_{BO}} \right) \cdot \Delta_{COMP} \quad (\text{EQ. 72})$$

Where Δ_{COMP} is the $V_{COMP} - 1V$. 1V is the offset voltage.

R_{IS} is the internal current scaling resistor. $R_{IS} = 14.2k\Omega$.

$$I_{D(ave)} = 0.749 \frac{A}{V} \cdot \Delta_{COMP} \quad (\text{EQ. 73})$$

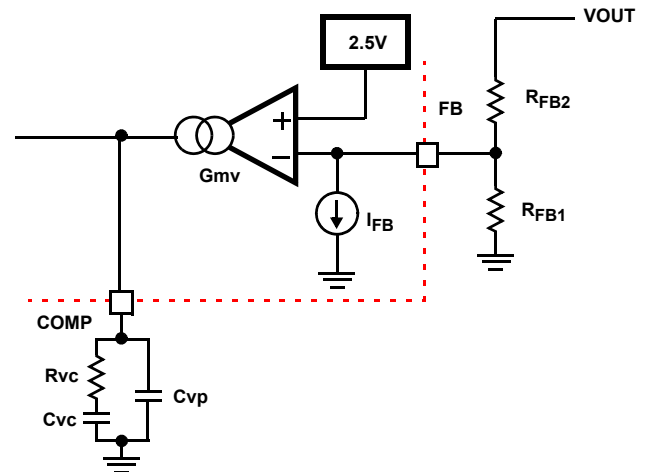


FIGURE 18. OUTPUT VOLTAGE SENSING AND COMPENSATION

Thus, the transfer function from V_{COMP} to V_{OUT} is:

$$G_{PS}(s) = \frac{V_{OUT}(s)}{\Delta_{COMP}} = \frac{1}{C_O \cdot s} \cdot \frac{I_{D(ave)}}{\Delta_{COMP}} \quad (\text{EQ. 74})$$

$$G_{PS}(s) = \left(\frac{I_{D(ave)}}{C_O \cdot s} \cdot \frac{1}{\Delta_{COMP}} \right) = \frac{0.749}{C_O \cdot s} \quad (\text{EQ. 75})$$

As shown in [Figure 18](#), the voltage loop gain is:

$$G_{VLOOP}(s) = G_{PS}(s) \cdot G_{DIV} \cdot G_{mv} \cdot Z_{COMP}(s) \quad (\text{EQ. 76})$$

The output feedback resistor divider gain, G_{DIV} is:

$$G_{DIV} = \frac{V_{REF}}{V_{OUT}} \quad (EQ. 77)$$

The compensation gain uses external impedance networks as shown in [Figure 18](#), $Z_{COMP}(s)$ is given by:

$$Z_{COMP}(s) = \frac{1}{(C_{VC} + C_{VP}) \cdot s} \cdot \frac{R_{VC} \cdot C_{VC} \cdot s + 1}{\frac{R_{VC} \cdot C_{VC} \cdot C_{VP} \cdot s + 1}{C_{VC} + C_{VP}}} \quad (EQ. 78)$$

The targeted crossover frequency, F_{CV} is 7.5Hz. The high frequency pole, F_{PV} , is required in order to reject the 2 time line frequency component. $F_{PV} = 20\text{Hz}$. The targeted phase margin is 50° .

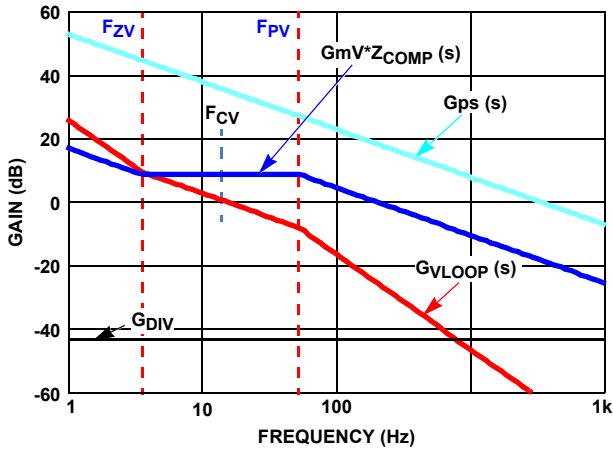


FIGURE 19. ASYMPTOTIC BODE PLOT OF VOLTAGE LOOP GAIN

The zero, F_{ZV} is calculated:

$$F_{ZV} = \frac{F_{CV}}{\tan(\Phi_m + \text{atan}(F_{CV}/(F_{PV})))} \quad (EQ. 79)$$

$$F_{ZV} = \frac{7.5\text{Hz}}{\tan(50\text{deg} + \text{atan}((7.5\text{Hz})/(20\text{Hz})))} = 2.648\text{Hz} \quad (EQ. 80)$$

Then the total capacitance used for compensation is calculated:

$$C_{VC} + C_{VP} = \frac{|G_{PS}(i \cdot (2\pi F_{CV}))| \cdot G_{DIV} \cdot G_{mv}}{(2\pi F_{CV})} \cdot \frac{\sqrt{(F_{CV}/F_{ZV})^2 + 1}}{\sqrt{(F_{CV}/F_{PV})^2 + 1}} \quad (EQ. 81)$$

Thus, the total compensation capacitance is:

$$C_{VC} + C_{VP} = 1127\text{nF} \quad (EQ. 82)$$

$$C_{VP} = 1127\text{nF} \cdot \frac{F_{ZV}}{F_{PV}} = 149\text{nF} \quad (EQ. 83)$$

$$C_{VC} = 1127\text{nF} - 149.1\text{nF} = 977\text{nF} \quad (EQ. 84)$$

$$R_{VC} = \frac{1}{2 \cdot \pi \cdot F_{ZV} \cdot C_{VC}} = 61.5\text{k}\Omega \quad (EQ. 85)$$

Choose components from the standard values. We have $C_{VP} = 150\text{nF}$, $C_{VC} = 1\mu\text{F}$, $R_{VC} = 62\text{k}\Omega$. The actual bode plot is shown in [Figure 20](#).

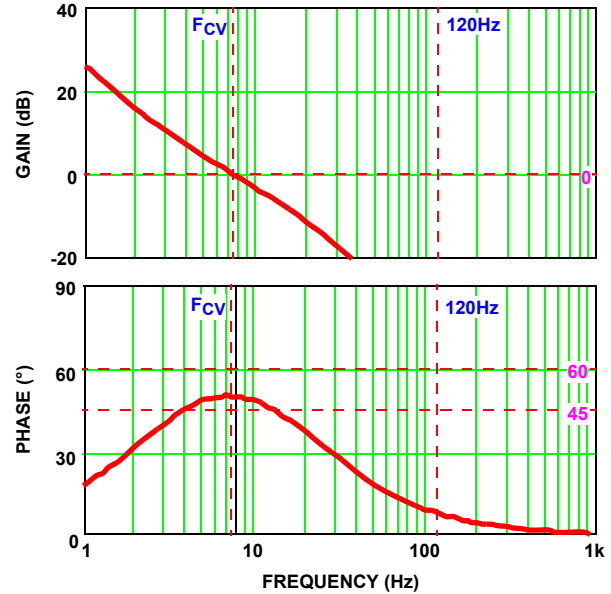


FIGURE 20. BODE PLOT OF THE ACTUAL VOLTAGE LOOP GAIN

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

| DATE | REVISION | CHANGE |
|-------------------|----------|--|
| February 13, 2015 | FN8582.1 | Recommended operating conditions on page 7: changed VCC to GND value from "15V to +20V" to "12V to +20V". Updated Equations 38 and 39 on page 15. |
| March 25, 2014 | FN8582.0 | Initial Release |

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support

© Copyright Intersil Americas LLC 2014-2015. All Rights Reserved.
All trademarks and registered trademarks are the property of their respective owners.

For additional products, see www.intersil.com/en/products.html

Intersil products are manufactured, assembled and tested utilizing ISO9001 quality systems as noted in the quality certifications found at www.intersil.com/en/support/qualandreliability.html

Intersil products are sold by description only. Intersil may modify the circuit design and/or specifications of products at any time without notice, provided that such modification does not, in Intersil's sole judgment, affect the form, fit or function of the product. Accordingly, the reader is cautioned to verify that datasheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

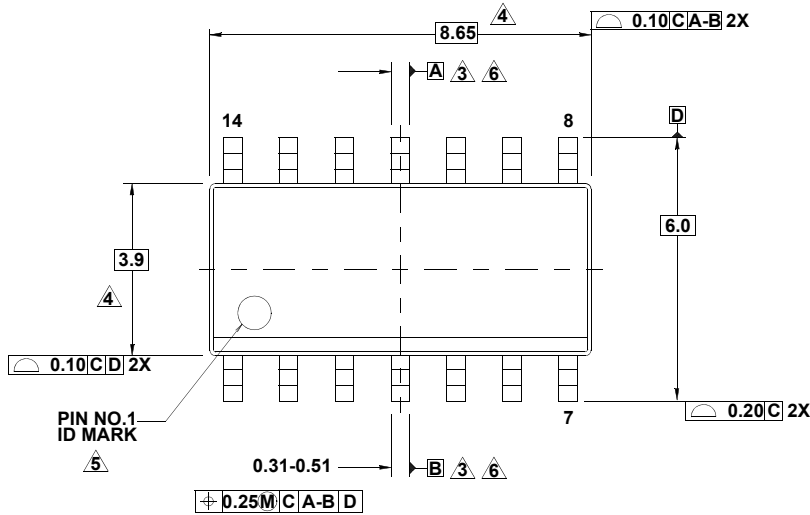
For information regarding Intersil Corporation and its products, see www.intersil.com

Package Outline Drawing

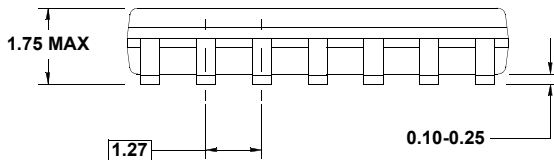
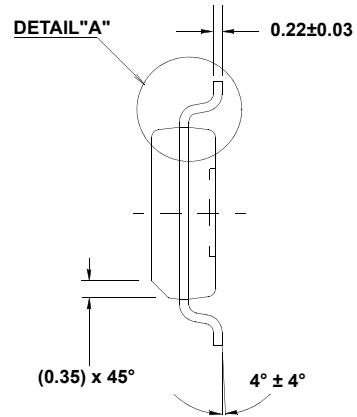
M14.15

14 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

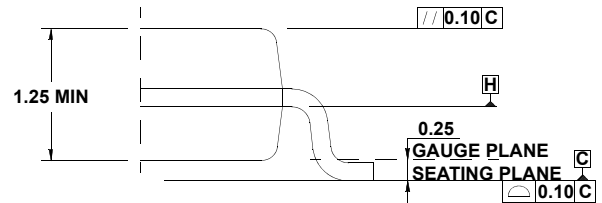
Rev 1, 10/09



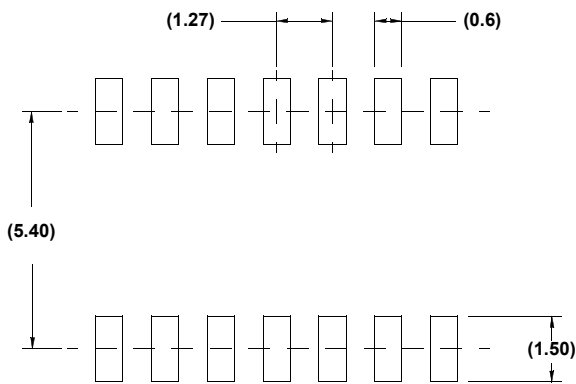
TOP VIEW



SIDE VIEW



DETAIL "A"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
Dimensions in () for Reference Only.
2. Dimensioning and tolerancing conform to AMSEY14.5m-1994.
3. Datums A and B to be determined at Datum H.
4. Dimension does not include interlead flash or protrusions.
Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm total in excess of lead width at maximum condition.
7. Reference to JEDEC MS-012-AB.