



# RF Power LDMOS Transistors

## N-Channel Enhancement-Mode Lateral MOSFETs

These 32 W RF power LDMOS transistors are designed for cellular base station applications requiring very wide instantaneous bandwidth capability covering the frequency range of 2110 to 2170 MHz.

- Typical Single-Carrier W-CDMA Performance:  $V_{DD} = 28$  Vdc,  $I_{DQ} = 800$  mA,  $P_{out} = 32$  W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

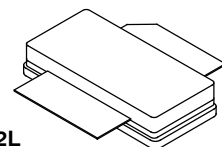
Frequency	$G_{ps}$ (dB)	$\eta_D$ (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
2110 MHz	19.0	33.9	6.7	-32.4	-15
2140 MHz	19.3	33.5	6.7	-32.6	-24
2170 MHz	19.4	33.2	6.7	-32.7	-22

### Features

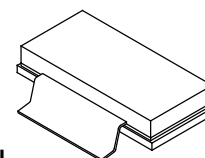
- Designed for Wide Instantaneous Bandwidth Applications
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Able to Withstand Extremely High Output VSWR and Broadband Operating Conditions
- Optimized for Doherty Applications
- In Tape and Reel. R3 Suffix = 250 Units, 56 mm Tape Width, 13-inch Reel.

**AFT21S140W02SR3**  
**AFT21S140W02GSR3**

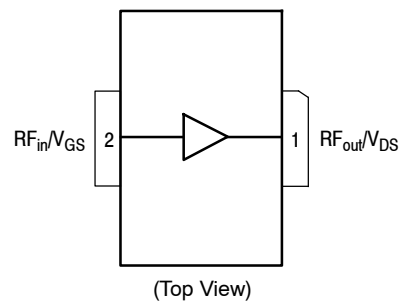
**2110–2170 MHz, 32 W AVG., 28 V**  
**AIRFAST RF POWER LDMOS**  
**TRANSISTORS**



**NI-780S-2L**  
**AFT21S140W02SR3**



**NI-780GS-2L**  
**AFT21S140W02GSR3**



**Figure 1. Pin Connections**

**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	-0.5, +65	Vdc
Gate-Source Voltage	$V_{GS}$	-6.0, +10	Vdc
Operating Voltage	$V_{DD}$	32, +0	Vdc
Storage Temperature Range	$T_{stg}$	-65 to +150	°C
Case Operating Temperature Range	$T_C$	-40 to +125	°C
Operating Junction Temperature Range (1,2)	$T_J$	-40 to +225	°C
CW Operation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	CW	124 0.70	W W/°C

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature $80^\circ\text{C}$ , 32 W CW, 28 Vdc, $I_{DQ} = 800$ mA, 2140 MHz	$R_{\theta JC}$	0.59	°C/W

**Table 3. ESD Protection Characteristics**

Test Methodology	Class
Human Body Model (per JESD22-A114)	2
Machine Model (per EIA/JESD22-A115)	B
Charge Device Model (per JESD22-C101)	IV

**Table 4. Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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**Off Characteristics**

Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 65$ Vdc, $V_{GS} = 0$ Vdc)	$I_{DSS}$	—	—	10	$\mu\text{Adc}$
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 28$ Vdc, $V_{GS} = 0$ Vdc)	$I_{DSS}$	—	—	5	$\mu\text{Adc}$
Gate-Source Leakage Current ( $V_{GS} = 5$ Vdc, $V_{DS} = 0$ Vdc)	$I_{GSS}$	—	—	1	$\mu\text{Adc}$

**On Characteristics**

Gate Threshold Voltage ( $V_{DS} = 10$ Vdc, $I_D = 146$ $\mu\text{Adc}$ )	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Gate Quiescent Voltage ( $V_{DD} = 28$ Vdc, $I_D = 800$ mAdc, Measured in Functional Test)	$V_{GS(Q)}$	1.5	1.9	2.3	Vdc
Drain-Source On-Voltage ( $V_{GS} = 10$ Vdc, $I_D = 1.4$ Adc)	$V_{DS(on)}$	0.1	0.15	0.3	Vdc

**Functional Tests (4,5)** (In Freescale Test Fixture, 50 ohm system)  $V_{DD} = 28$  Vdc,  $I_{DQ} = 800$  mA,  $P_{out} = 32$  W Avg.,  $f = 2140$  MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @  $\pm 5$  MHz Offset.

Power Gain	$G_{ps}$	18.7	19.3	21.7	dB
Drain Efficiency	$\eta_D$	32.0	33.5	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	6.2	6.7	—	dB
Adjacent Channel Power Ratio	ACPR	—	-32.6	-30.5	dBc
Input Return Loss	IRL	—	-24	-9	dB

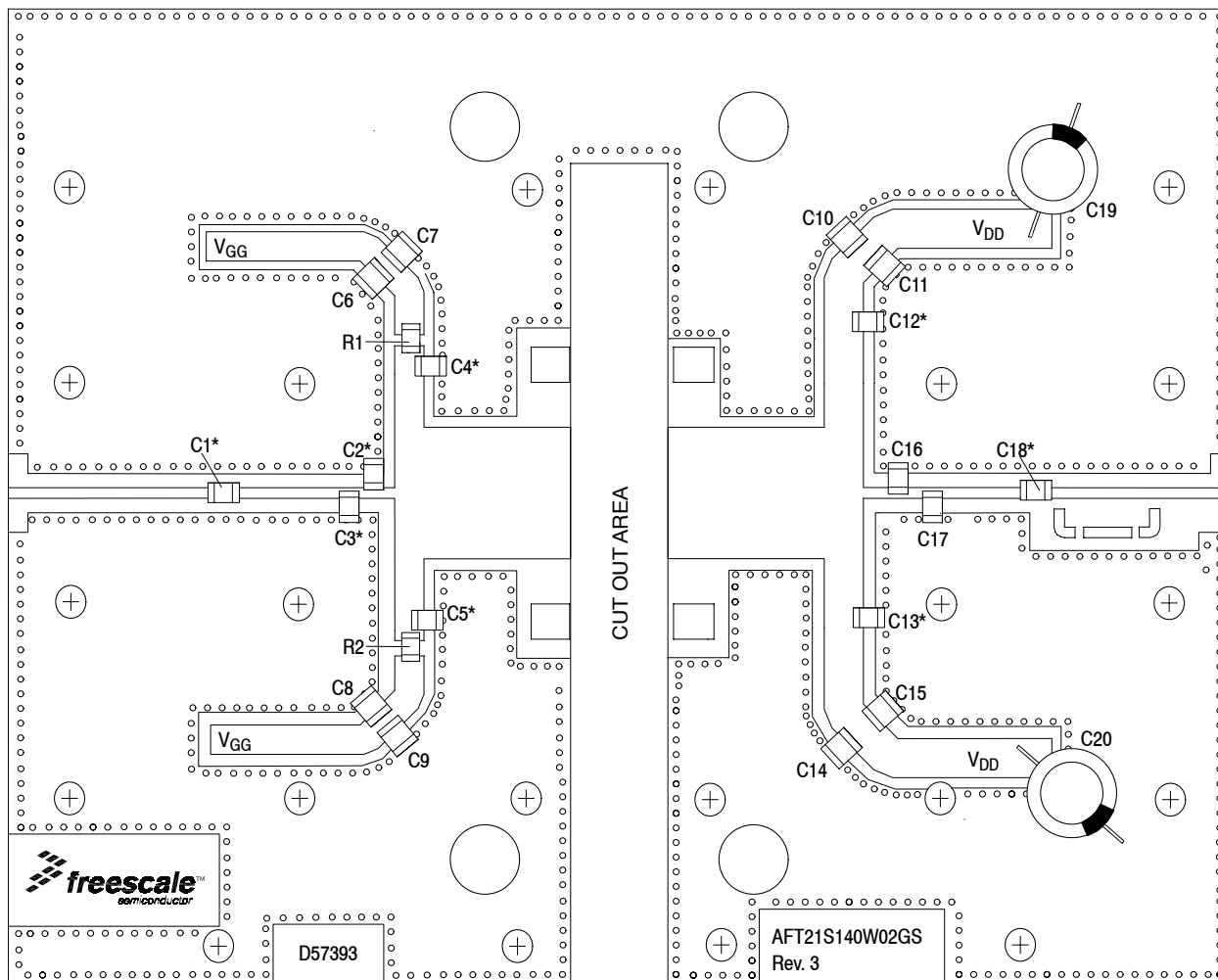
1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1955.
4. Part internally matched both on input and output.
5. Measurements made with device in straight lead configuration before any lead forming operation is applied. Lead forming is used for gull wing (GS) parts.

(continued)

**Table 4. Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
<b>Load Mismatch</b> (In Freescale Test Fixture, 50 ohm system) $I_{DQ} = 800\text{ mA}$ , $f = 2140\text{ MHz}$					
VSWR 10:1 at 32 Vdc, 158 W CW <sup>(1)</sup> Output Power (3 dB Input Overdrive from 112 W CW Rated Power)	No Device Degradation				
<b>Typical Performance</b> (In Freescale Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$ , $I_{DQ} = 800\text{ mA}$ , 2110–2170 MHz Bandwidth					
$P_{out}$ @ 1 dB Compression Point, CW	P1dB	—	112	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 2110–2170 MHz bandwidth)	$\Phi$	—	-17	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW <sub>res</sub>	—	150	—	MHz
Gain Flatness in 60 MHz Bandwidth @ $P_{out} = 32\text{ W Avg.}$	$G_F$	—	0.3	—	dB
Gain Variation over Temperature (-30°C to +85°C)	$\Delta G$	—	0.03	—	dB/°C
Output Power Variation over Temperature (-30°C to +85°C) <sup>(1)</sup>	$\Delta P1dB$	—	0.01	—	dB/°C

1. Exceeds recommended operating conditions. See CW operation data in Maximum Ratings table.



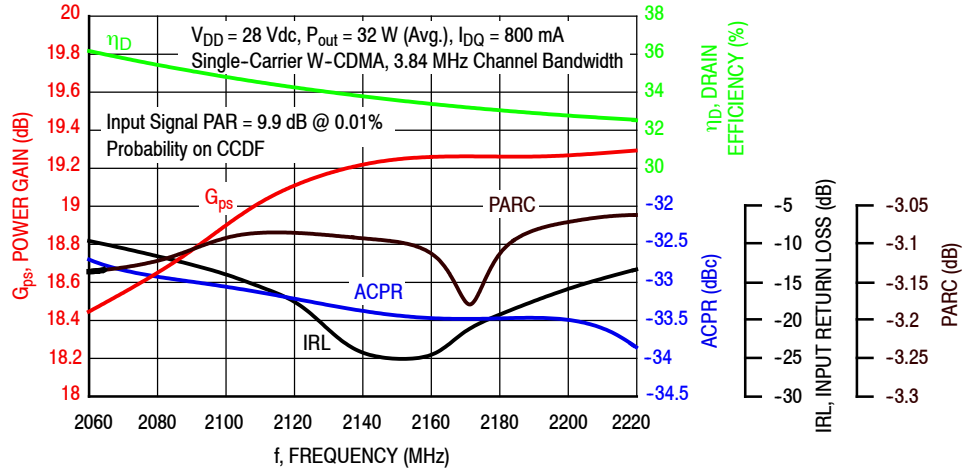
\*C1, C2, C3, C4, C5, C12, C13 and C18 are mounted vertically.

**Figure 2. AFT21S140W02SR3 Test Circuit Component Layout**

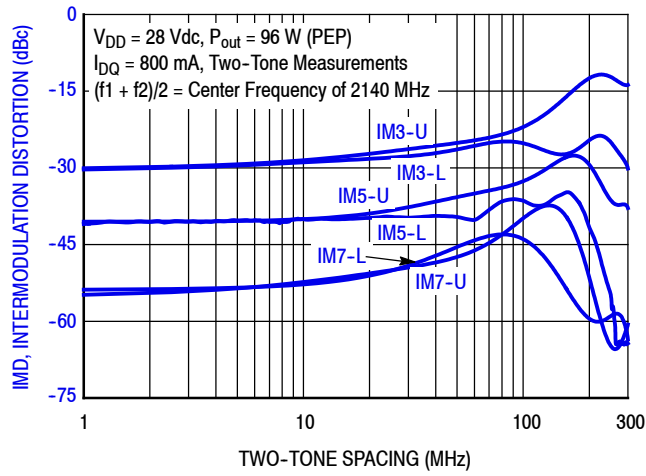
**Table 5. AFT21S140W02SR3 Test Circuit Component Designations and Values**

Part	Description	Part Number	Manufacturer
C1, C4, C5, C18	6.2 pF Chip Capacitors	ATC100B6R2BT500XT	ATC
C2	0.5 pF Chip Capacitor	ATC100B0R5BT500XT	ATC
C3	1.1 pF Chip Capacitor	ATC100B1R1BT500XT	ATC
C6, C7, C8, C9, C10, C11, C14, C15	10 $\mu$ F, Chip Capacitors	GRM32ER61H106KA12L	Murata
C12, C13	8.2 pF Chip Capacitors	ATC100B8R2CT500XT	ATC
C16	2.2 pF Chip Capacitor	ATC100B2R2JT500XT	ATC
C17	0.9 pF Chip Capacitor	ATC100B0R9BT500XT	ATC
C19, C20	470 $\mu$ F, 63 V Electrolytic Capacitors	MCGPR63V477M13X26-RH	Multicomp
R1, R2	2.37 $\Omega$ , 1/4 W Chip Resistors	CRCW12062R37FNEA	Vishay
PCB	Rogers RO4350B, 0.020", $\epsilon_r = 3.66$	D57393	MTL

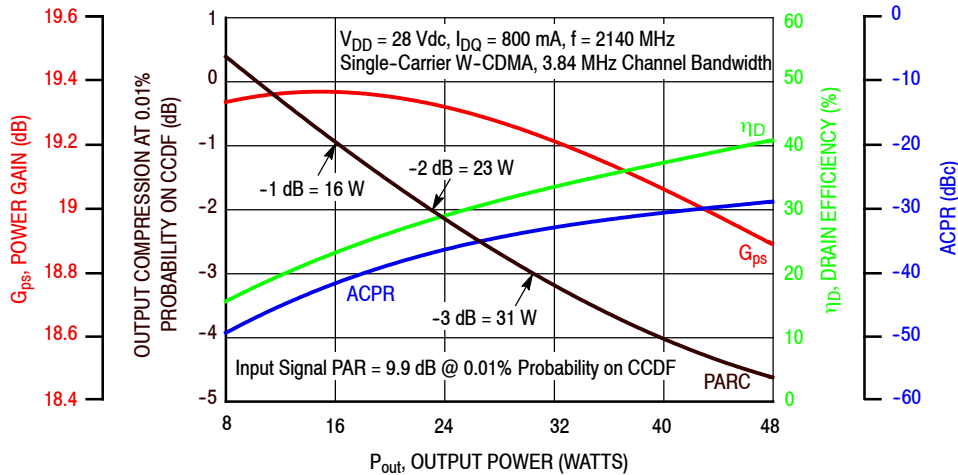
### TYPICAL CHARACTERISTICS



**Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @  $P_{out} = 32$  Watts Avg.**

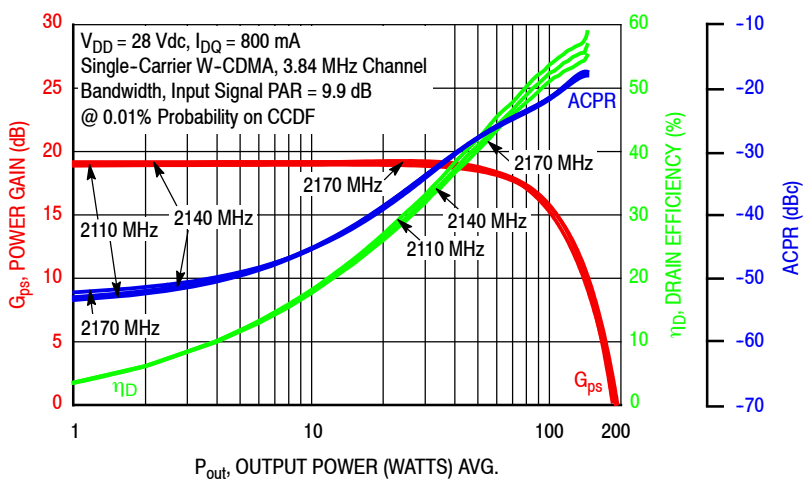


**Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing**

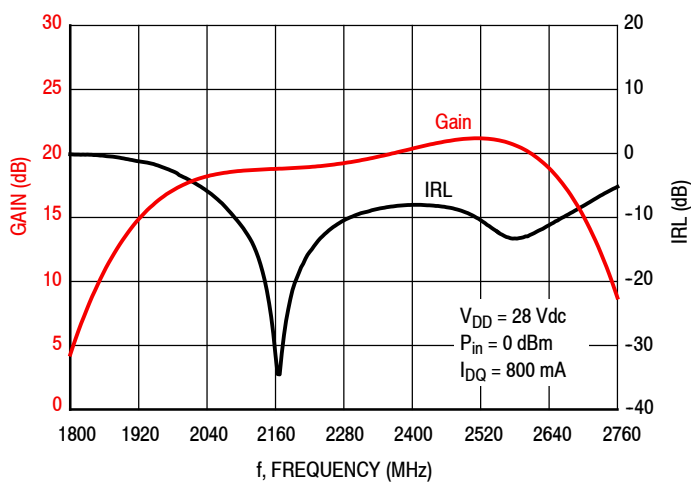


**Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power**

### TYPICAL CHARACTERISTICS



**Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power**



**Figure 7. Broadband Frequency Response**

**Table 6. Load Pull Performance — Maximum Power Tuning**
 $V_{DD} = 28 \text{ Vdc}$ ,  $I_{DQ} = 770 \text{ mA}$ , Pulsed CW, 10  $\mu\text{sec}(\text{on})$ , 10% Duty Cycle

f (MHz)	$Z_{\text{source}} (\Omega)$	$Z_{\text{in}} (\Omega)$	Max Output Power					
			P1dB					
			$Z_{\text{load}}^{(1)} (\Omega)$	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM (°)
2110	4.72 - j7.83	5.44 + j8.03	3.92 - j6.59	18.9	51.8	152	54.3	-10
2140	6.03 - j8.06	6.63 + j8.08	3.84 - j6.22	19.0	51.9	156	55.5	-11
2170	7.23 - j7.37	7.86 + j7.65	3.89 - j6.16	19.2	52.0	158	56.6	-11

f (MHz)	$Z_{\text{source}} (\Omega)$	$Z_{\text{in}} (\Omega)$	Max Output Power					
			P3dB					
			$Z_{\text{load}}^{(2)} (\Omega)$	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM (°)
2110	4.72 - j7.83	5.92 + j8.68	3.92 - j7.04	16.8	52.8	190	57.5	-16
2140	6.03 - j8.06	7.42 + j8.66	3.99 - j6.82	16.9	52.8	193	58.4	-17
2170	7.23 - j7.37	8.93 + j7.96	3.96 - j6.86	16.9	52.9	193	58.1	-17

(1) Load impedance for optimum P1dB power.

(2) Load impedance for optimum P3dB power.

 $Z_{\text{source}}$  = Measured impedance presented to the input of the device at the package reference plane.

 $Z_{\text{in}}$  = Impedance as measured from gate contact to ground.

 $Z_{\text{load}}$  = Measured impedance presented to the output of the device at the package reference plane.

**Table 7. Load Pull Performance — Maximum Drain Efficiency Tuning**
 $V_{DD} = 28 \text{ Vdc}$ ,  $I_{DQ} = 770 \text{ mA}$ , Pulsed CW, 10  $\mu\text{sec}(\text{on})$ , 10% Duty Cycle

f (MHz)	$Z_{\text{source}} (\Omega)$	$Z_{\text{in}} (\Omega)$	Max Drain Efficiency					
			P1dB					
			$Z_{\text{load}}^{(1)} (\Omega)$	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM (°)
2110	4.72 - j7.83	5.45 + j8.49	8.22 - j1.63	21.7	49.5	89	64.0	-18
2140	6.03 - j8.06	6.72 + j8.52	6.98 - j1.62	21.7	49.7	93	64.4	-18
2170	7.23 - j7.37	8.07 + j8.09	5.87 - j1.79	21.7	50.0	99	65.8	-19

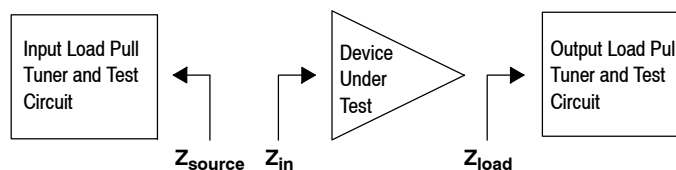
f (MHz)	$Z_{\text{source}} (\Omega)$	$Z_{\text{in}} (\Omega)$	Max Drain Efficiency					
			P3dB					
			$Z_{\text{load}}^{(2)} (\Omega)$	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM (°)
2110	4.72 - j7.83	5.83 + j8.94	6.85 - j4.39	18.9	51.6	143	66.0	-22
2140	6.03 - j8.06	7.35 + j8.95	6.31 - j4.25	18.8	51.7	148	66.5	-23
2170	7.23 - j7.37	9.04 + j8.28	6.47 - j2.38	19.6	50.9	122	67.0	-27

(1) Load impedance for optimum P1dB efficiency.

(2) Load impedance for optimum P3dB efficiency.

 $Z_{\text{source}}$  = Measured impedance presented to the input of the device at the package reference plane.

 $Z_{\text{in}}$  = Impedance as measured from gate contact to ground.

 $Z_{\text{load}}$  = Measured impedance presented to the output of the device at the package reference plane.


### P1dB - TYPICAL LOAD PULL CONTOURS — 2140 MHz

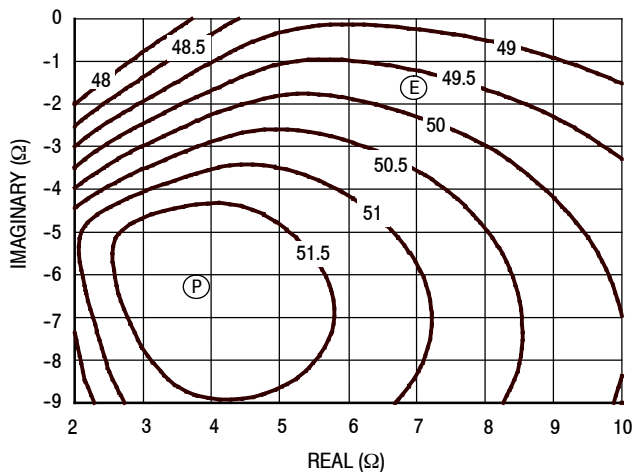


Figure 8. P1dB Load Pull Output Power Contours (dBm)

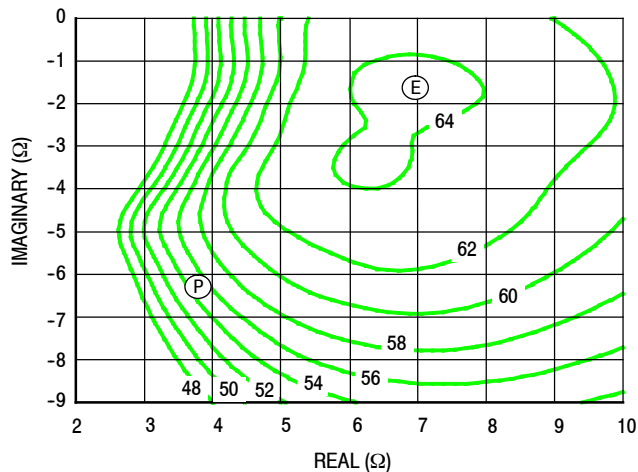


Figure 9. P1dB Load Pull Efficiency Contours (%)

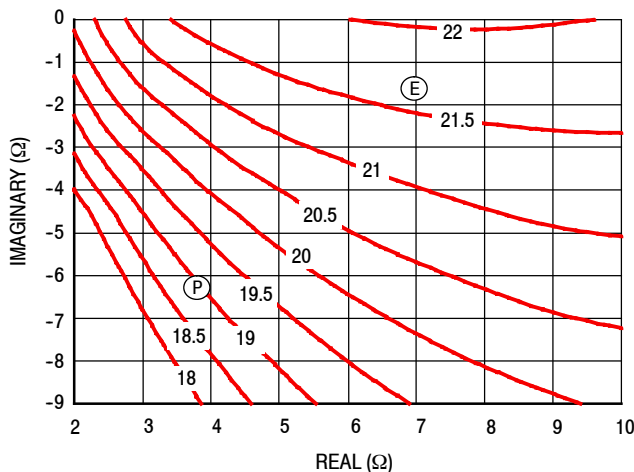


Figure 10. P1dB Load Pull Gain Contours (dB)

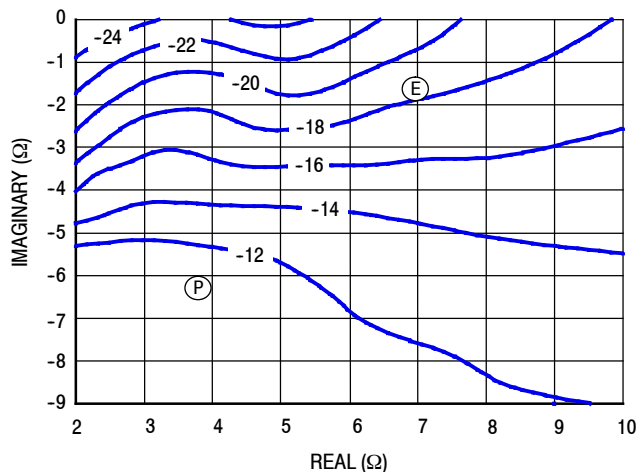


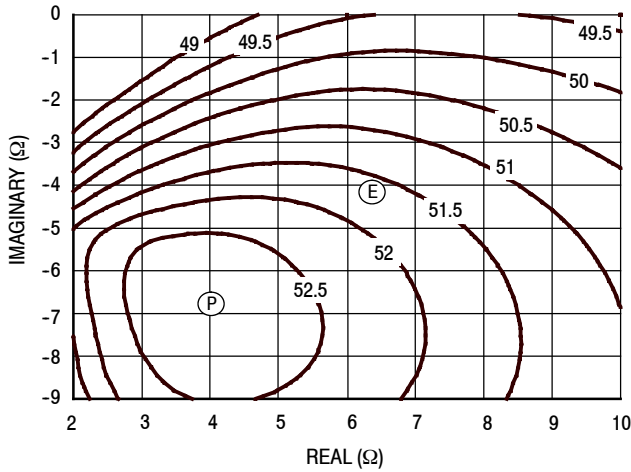
Figure 11. P1dB Load Pull AM/PM Contours (°)

**NOTE:** (P) = Maximum Output Power  
 (E) = Maximum Drain Efficiency

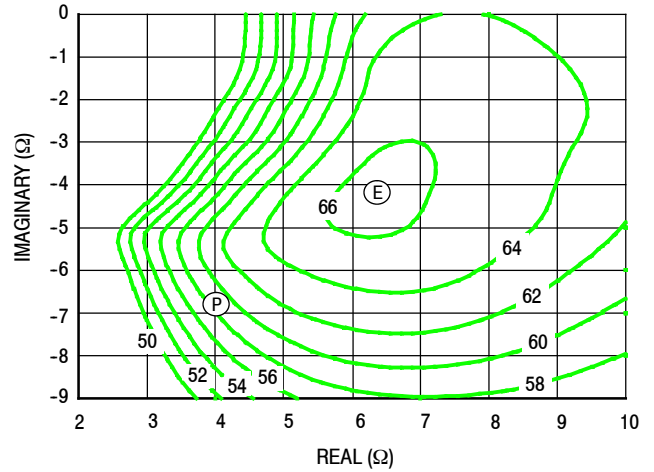
- Gain
- Drain Efficiency
- Linearity
- Output Power



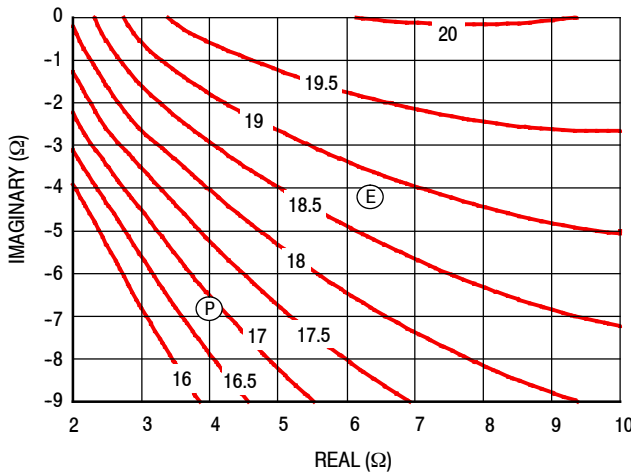
**P3dB - TYPICAL LOAD PULL CONTOURS — 2140 MHz**



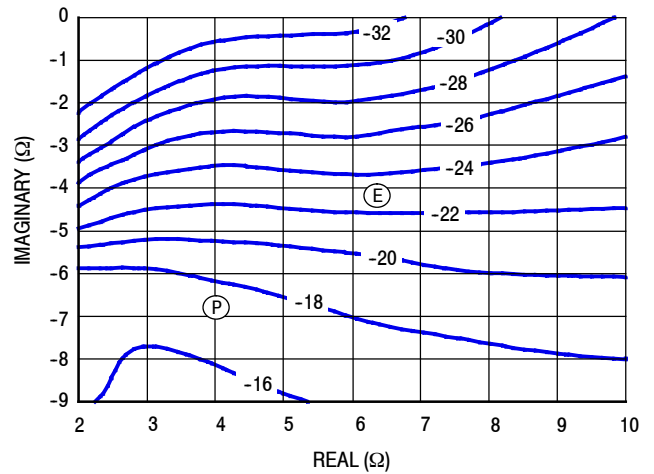
**Figure 12. P3dB Load Pull Output Power Contours (dBm)**



**Figure 13. P3dB Load Pull Efficiency Contours (%)**



**Figure 14. P3dB Load Pull Gain Contours (dB)**

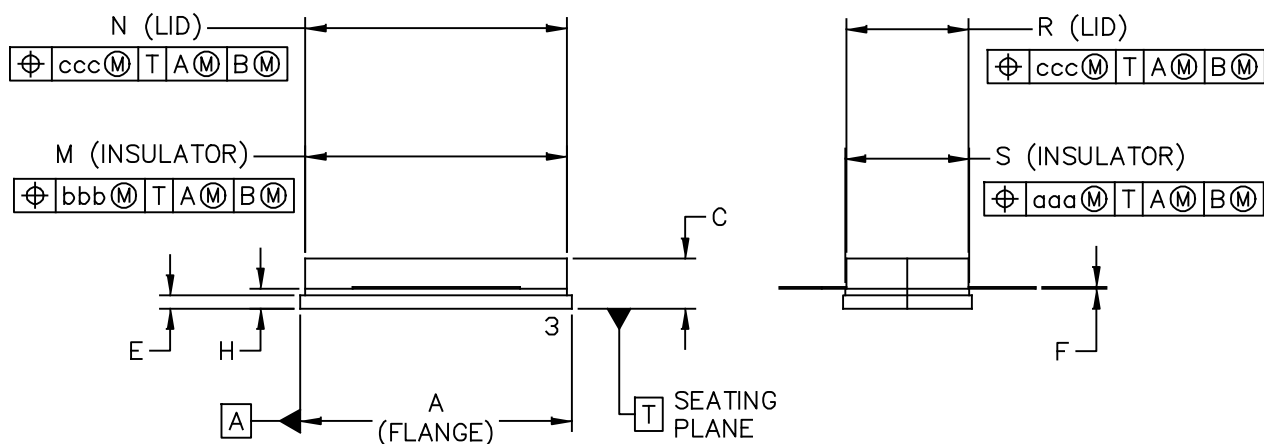
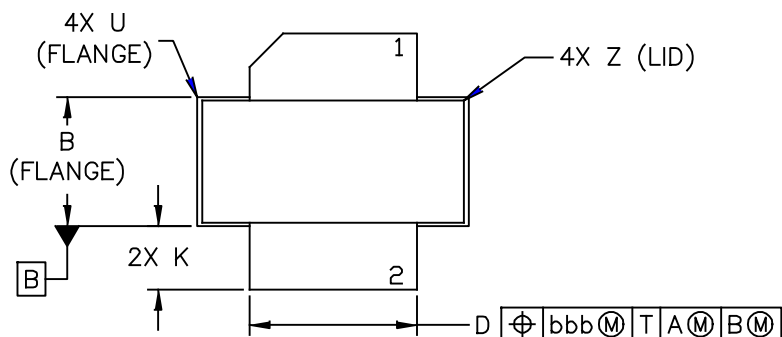


**Figure 15. P3dB Load Pull AM/PM Contours (°)**

**NOTE:** (P) = Maximum Output Power  
 (E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

### PACKAGE DIMENSIONS



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TITLE:  NI-780S	DOCUMENT NO: 98ASB16718C	REV: H	
	CASE NUMBER: 465A-06	31 MAR 2005	
	STANDARD: NON-JEDEC		

NOTES:

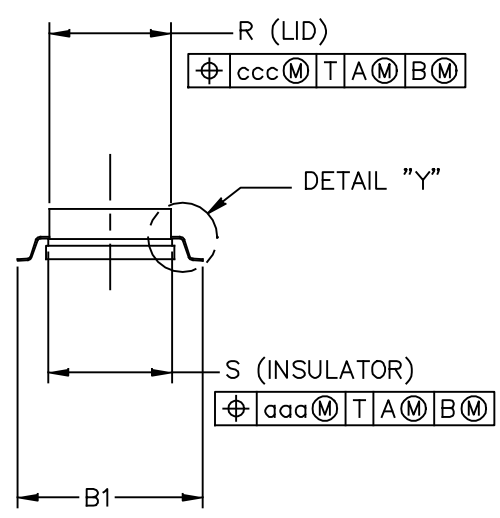
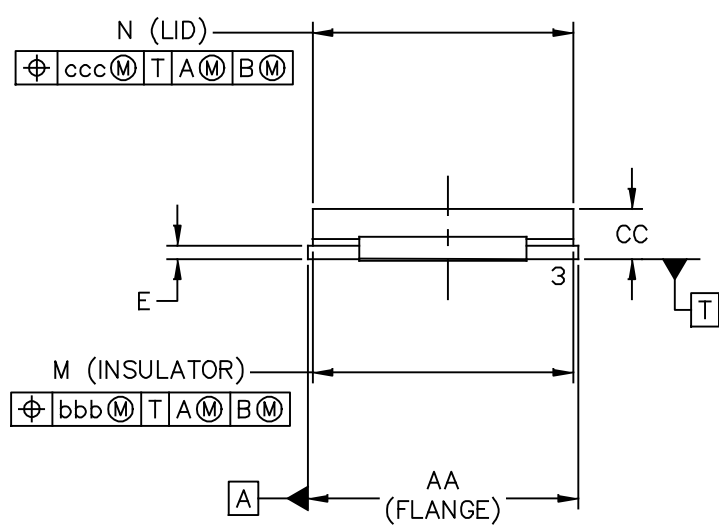
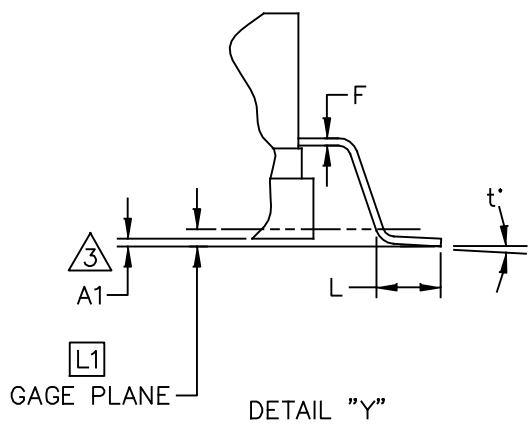
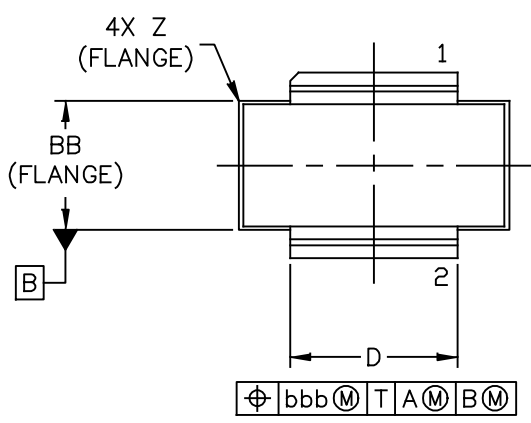
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DELETED
4. DIMENSION H IS MEASURED .030 (0.762) AWAY FROM PACKAGE BODY.

STYLE 1:

- PIN 1. DRAIN
2. GATE
3. SOURCE

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.805	-.815	20.45	20.7	U	-.040			1.02
B	.380	-.390	9.65	9.91	Z	-.030			0.76
C	.125	-.170	3.18	4.32	aaa	-.005		0.127	
D	.495	-.505	12.57	12.83	bbb	-.010		0.254	
E	.035	-.045	0.89	1.14	ccc	-.015		0.381	
F	.003	-.006	0.08	0.15	-				
H	.057	-.067	1.45	1.7	-				
K	.170	-.210	4.32	5.33	-				
M	.774	-.786	19.61	20.02	-				
N	.772	-.788	19.61	20.02	-				
R	.365	-.375	9.27	9.53	-				
S	.365	-.375	9.27	9.52	-				

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TITLE:  NI-780S		DOCUMENT NO: 98ASB16718C		REV: H	
		CASE NUMBER: 465A-06		31 MAR 2005	
		STANDARD: NON-JEDEC			



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TITLE:  NI-780GS-2L	DOCUMENT NO: 98ASA00193D	REV: B
	STANDARD: NON-JEDEC	
	05 SEP 2013	

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.

3. DIMENSION A1 IS MEASURED WITH REFERENCE TO DATUM T. THE POSITIVE VALUE IMPLIES THAT THE PACKAGE BOTTOM IS HIGHER THAN THE LEAD BOTTOM.

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
AA	.805	.815	20.45	20.70	Z	R.000	R.040	R0.00	R1.02
A1	.002	.008	0.05	0.20	t	0	8	0	8
BB	.380	.390	9.65	9.91					
B1	.546	.562	13.87	14.27					
CC	.125	.170	3.18	4.32	aaa	.005		0.13	
D	.495	.505	12.57	12.83	bbb	.010		0.25	
E	.035	.045	0.89	1.14	ccc	.015		0.38	
F	.003	.006	0.08	0.15					
L	.038	.046	0.97	1.17					
L1	.010 BSC		0.25 BSC						
M	.774	.786	19.66	19.96					
N	.772	.788	19.61	20.02					
R	.365	.375	9.27	9.53					
S	.365	.375	9.27	9.53					
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TITLE:					DOCUMENT NO: 98ASA00193D		REV: B		
NI-780GS-2L					STANDARD: NON-JEDEC				
					05 SEP 2013				

## PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following documents, software and tools to aid your design process.

### Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

### Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

### Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

### Development Tools

- Printed Circuit Boards

For Software and Tools, do a Part Number search at <http://www.freescale.com>, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

## REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Feb. 2014	• Initial Release of Data Sheet

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