

# 74LVC1G386

## 3-input EXCLUSIVE-OR gate

Rev. 4 — 9 May 2017

Product data sheet

## 1 General description

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The 74LVC1G386 provides a 3-input EXCLUSIVE-OR function.

The input can be driven from either 3.3 or 5 V devices. This feature allows the use of these devices in a mixed 3.3 and 5 V environment.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall time.

This device is fully specified for partial power-down applications using  $I_{OFF}$ . The  $I_{OFF}$  circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

## 2 Features and benefits

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- Wide supply voltage range from 1.65 to 5.5 V
- High noise immunity
- Complies with JEDEC standard:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8B/JESD36 (2.7 V to 3.6 V)
- $\pm 24$  mA output drive ( $V_{CC} = 3.0$  V)
- Latch-up performance exceeds 250 mA
- CMOS low power consumption
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- ESD protection:
  - HBM EIA/JESD22-A114E exceeds 2 000 V
  - MM EIA/JESD22-A115-A exceeds 200 V.
- SOT363 and SOT457 package
- Specified from -40 to +85 °C and -40 to +125 °C.

3 Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC1G386GW	-40 °C to +125 °C	SC-88	plastic surface-mounted package; 6 leads	SOT363
74LVC1G386GV	-40 °C to +125 °C	SC-74A	plastic surface-mounted package (TSOP6); 6 leads	SOT457

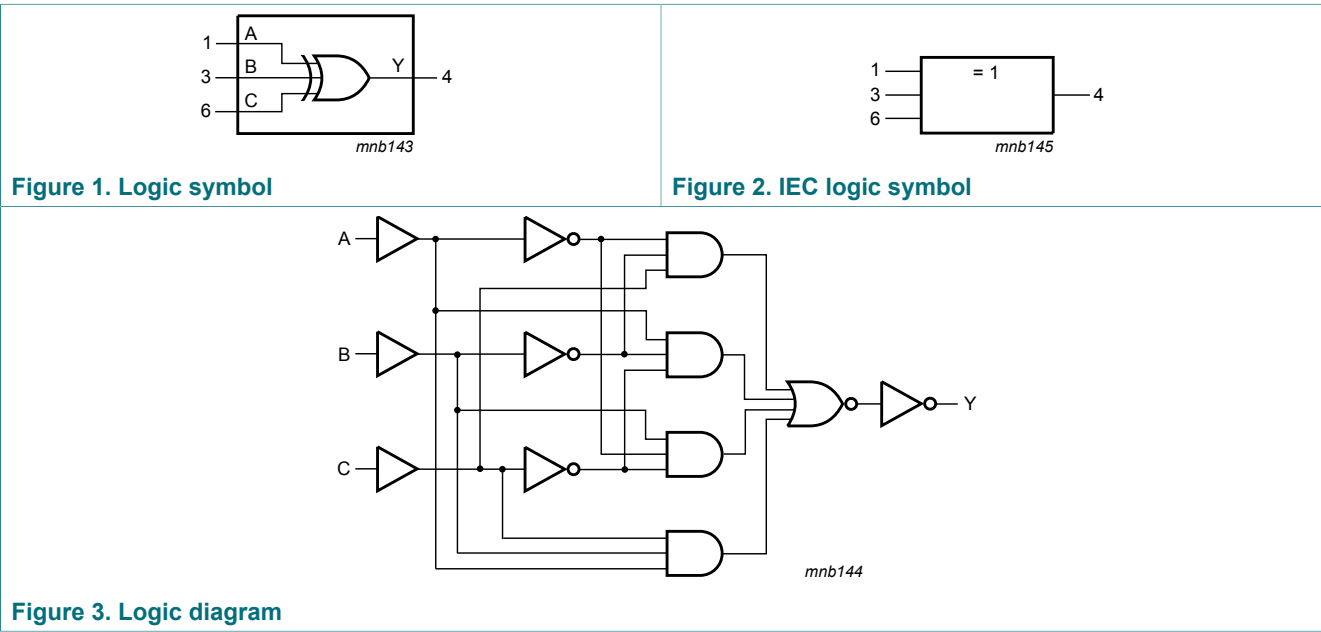
4 Marking

Table 2. Marking

Type number	Marking code <sup>[1]</sup>
74LVC1G386GW	YH
74LVC1G386GV	YH

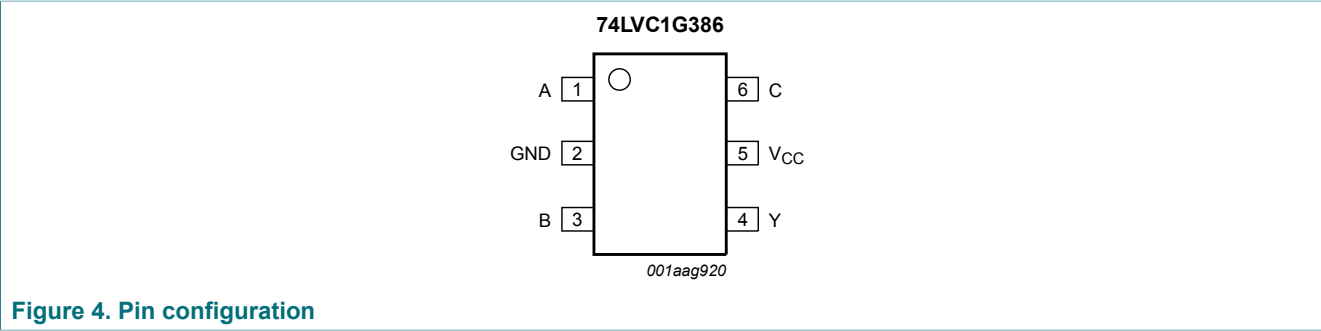
[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5 Functional diagram



6 Pinning information

6.1 Pinning



6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
A	1	data input
GND	2	ground (0 V)
B	3	data input
Y	4	data output
V <sub>CC</sub>	5	supply voltage
C	6	data input

7 Functional description

Table 4. Function table <sup>[1]</sup>

Input			Output
A	B	C	Y
L	L	L	L
L	L	H	H
L	H	L	H
L	H	H	L
H	L	L	H
H	L	H	L
H	H	L	L
H	H	H	H

[1] H = HIGH voltage level;  
L = LOW voltage level

## 8 Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+6.5	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-50	-	mA
$V_I$	input voltage	[1]	-0.5	+6.5	V
$I_{OK}$	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	$\pm 50$	mA
$V_O$	output voltage	Active mode [1] [2]	-0.5	$V_{CC} + 0.5$	V
		Power-down mode [1] [2]	-0.5	+6.5	V
$I_O$	output current	$V_O = 0$ V to $V_{CC}$	-	$\pm 50$	mA
$I_{CC}$	supply current		-	100	mA
$I_{GND}$	ground current		-100	-	mA
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to $+125$ °C [3]	-	250	mW
$T_{stg}$	storage temperature		-65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] When  $V_{CC} = 0$  V (Power-down mode), the output voltage can be 5.5 V in normal operation.

[3] For SC-74 and SC-88 packages: above 87.5 °C the value of  $P_{tot}$  derates linearly with 4.0 mW/K.

## 9 Recommended operating conditions

**Table 6. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		1.65	-	5.5	V
$V_I$	input voltage		0	-	5.5	V
$V_O$	output voltage	Active mode	0	-	$V_{CC}$	$V_O$
		$V_{CC} = 0$ V; Power-down mode	0	-	5.5	$V_O$
$T_{amb}$	ambient temperature		-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65$ V to $2.7$ V	-	-	20	ns/V
		$V_{CC} = 2.7$ V to $5.5$ V	-	-	10	ns/V

## 10 Static characteristics

**Table 7. Static characteristics**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
$T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$						
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7	-	-	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2.0	-	-	V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$0.7 \times V_{CC}$	-	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	-	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	-	-	0.7	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	-	-	0.8	V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	-	$0.3 \times V_{CC}$	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}\text{ or }V_{IL}$				
		$I_O = -100\text{ }\mu\text{A}; V_{CC} = 1.65\text{ V to }5.5\text{ V}$	$V_{CC} - 0.1$	-	-	V
		$I_O = -4\text{ mA}; V_{CC} = 1.65\text{ V}$	1.2	-	-	V
		$I_O = -8\text{ mA}; V_{CC} = 2.3\text{ V}$	1.9	-	-	V
		$I_O = -12\text{ mA}; V_{CC} = 2.7\text{ V}$	2.2	-	-	V
		$I_O = -24\text{ mA}; V_{CC} = 3.0\text{ V}$	2.3	-	-	V
		$I_O = -32\text{ mA}; V_{CC} = 4.5\text{ V}$	3.8	-	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}\text{ or }V_{IL}$				
		$I_O = 100\text{ }\mu\text{A}; V_{CC} = 1.65\text{ V to }5.5\text{ V}$	-	-	0.1	V
		$I_O = 4\text{ mA}; V_{CC} = 1.65\text{ V}$	-	-	0.45	V
		$I_O = 8\text{ mA}; V_{CC} = 2.3\text{ V}$	-	-	0.3	V
		$I_O = 12\text{ mA}; V_{CC} = 2.7\text{ V}$	-	-	0.4	V
		$I_O = 24\text{ mA}; V_{CC} = 3.0\text{ V}$	-	-	0.55	V
		$I_O = 32\text{ mA}; V_{CC} = 4.5\text{ V}$	-	-	0.55	V
$I_I$	input leakage current	$V_{CC} = 0\text{ V to }5.5\text{ V}; V_I = 5.5\text{ V or GND}$	-	$\pm 0.1$	$\pm 1$	$\mu\text{A}$
$I_{OFF}$	power-off leakage current	$V_{CC} = 0\text{ V}; V_I\text{ or }V_O = 5.5\text{ V}$	-	$\pm 0.1$	$\pm 2$	$\mu\text{A}$
$I_{CC}$	supply current	$V_I = 5.5\text{ V or GND};$ $V_{CC} = 1.65\text{ V to }5.5\text{ V}; I_O = 0\text{ A}$	-	0.1	4	$\mu\text{A}$
$\Delta I_{CC}$	additional supply current	per pin; $V_{CC} = 2.3\text{ V to }5.5\text{ V};$ $V_I = V_{CC} - 0.6\text{ V}; I_O = 0\text{ A}$	-	5	500	$\mu\text{A}$
$C_I$	input capacitance	$V_{CC} = 3.3\text{ V}; V_I = \text{GND to }V_{CC}$	-	4	-	pF
$T_{amb} = -40\text{ }^{\circ}\text{C to }+125\text{ }^{\circ}\text{C}$						
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7	-	-	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2.0	-	-	V

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	0.7 × V <sub>CC</sub>	-	-	V
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	-	0.35 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	-	0.7	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	0.8	V
		V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	0.3 × V <sub>CC</sub>	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = -100 µA; V <sub>CC</sub> = 1.65 V to 5.5 V	V <sub>CC</sub> - 0.1	-	-	V
		I <sub>O</sub> = -4 mA; V <sub>CC</sub> = 1.65 V	0.95	-	-	V
		I <sub>O</sub> = -8 mA; V <sub>CC</sub> = 2.3 V	1.7	-	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.7 V	1.9	-	-	V
		I <sub>O</sub> = -24 mA; V <sub>CC</sub> = 3.0 V	2.0	-	-	V
		I <sub>O</sub> = -32 mA; V <sub>CC</sub> = 4.5 V	3.4	-	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = 100 µA; V <sub>CC</sub> = 1.65 V to 5.5 V	-	-	0.1	V
		I <sub>O</sub> = 4 mA; V <sub>CC</sub> = 1.65 V	-	-	0.70	V
		I <sub>O</sub> = 8 mA; V <sub>CC</sub> = 2.3 V	-	-	0.45	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.7 V	-	-	0.60	V
		I <sub>O</sub> = 24 mA; V <sub>CC</sub> = 3.0 V	-	-	0.80	V
		I <sub>O</sub> = 32 mA; V <sub>CC</sub> = 4.5 V	-	-	0.80	V
I <sub>I</sub>	input leakage current	V <sub>CC</sub> = 0 V to 5.5 V; V <sub>I</sub> = 5.5 V or GND	-	-	±1	µA
I <sub>OFF</sub>	power-off leakage current	V <sub>CC</sub> = 0 V; V <sub>I</sub> or V <sub>O</sub> = 5.5 V	-	-	±2	µA
I <sub>CC</sub>	supply current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 1.65 V to 5.5 V; I <sub>O</sub> = 0 A	-	-	4	µA
ΔI <sub>CC</sub>	additional supply current	per pin; V <sub>CC</sub> = 2.3 V to 5.5 V; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A	-	-	500	µA

[1] All typical values are measured at V<sub>CC</sub> = 3.3 V and T<sub>amb</sub> = 25 °C.

## 11 Dynamic characteristics

**Table 8. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 6](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
$t_{pd}$	propagation delay	A, B, C to Y; see <a href="#">Figure 5</a> <sup>[2]</sup>						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	2.0	8.0	17.0	2.0	22.0	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.5	5.0	9.0	1.5	11.5	ns
		$V_{CC} = 2.7 \text{ V}$	1.5	5.0	8.5	1.5	11.0	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.0	4.5	7.5	1.0	9.5	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	1.0	3.5	5.5	1.0	7.0	ns
$C_{PD}$	power dissipation capacitance	$V_I = \text{GND to } V_{CC}; V_{CC} = 3.3 \text{ V}$ <sup>[3]</sup>	-	13	-	-	-	pF

[1] Typical values are measured at  $T_{amb} = 25 \text{ °C}$  and  $V_{CC} = 1.8 \text{ V}, 2.5 \text{ V}, 2.7 \text{ V}, 3.3 \text{ V}$  and  $5.0 \text{ V}$  respectively.

[2]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .

[3]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$  where:

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

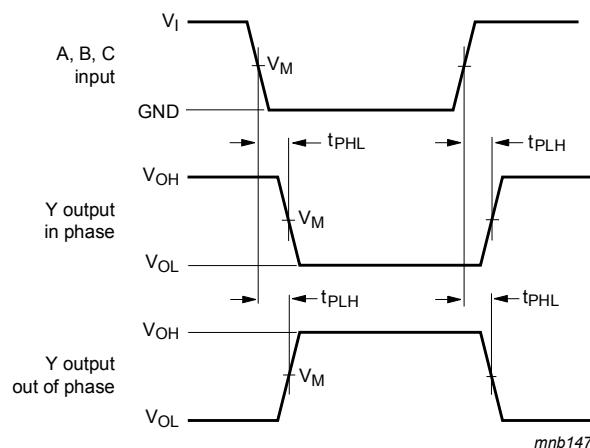
$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in V;

$N$  = number of inputs switching;

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

### 11.1 Waveforms and test circuit



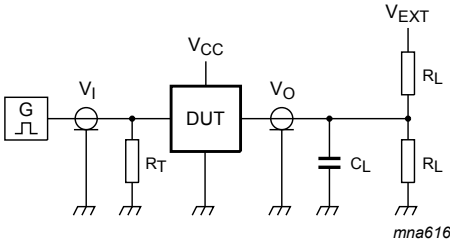
Measurement points are given in [Table 9](#).

$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Figure 5. Input A, B, C to output Y propagation delays**

Table 9. Measurement points

V <sub>CC</sub>	V <sub>M</sub>	Input	
		V <sub>I</sub>	t <sub>r</sub> = t <sub>f</sub>
1.65 V to 1.95 V	0.5 × V <sub>CC</sub>	V <sub>CC</sub>	≤ 2.0 ns
2.3 V to 2.7 V	0.5 × V <sub>CC</sub>	V <sub>CC</sub>	≤ 2.0 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 V to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns
4.5 V to 5.5 V	0.5 × V <sub>CC</sub>	V <sub>CC</sub>	≤ 2.5 ns



Test data is given in [Table 10](#).  
Definitions for test circuit:  
R<sub>L</sub> = Load resistance.  
C<sub>L</sub> = Load capacitance including jig and probe capacitance.  
R<sub>T</sub> = Termination resistance should be equal to the output impedance Z<sub>o</sub> of the pulse generator.  
V<sub>EXT</sub> = External voltage for measuring switching times.

Figure 6. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input	Load		V <sub>EXT</sub>
V <sub>CC</sub>	V <sub>I</sub>	C <sub>L</sub>	R <sub>L</sub>	t <sub>PLH</sub> , t <sub>PHL</sub>
1.65 V to 1.95 V	V <sub>CC</sub>	30 pF	1 kΩ	open
2.3 V to 2.7 V	V <sub>CC</sub>	30 pF	500 Ω	open
2.7 V	2.7 V	50 pF	500 Ω	open
3.0 V to 3.6 V	2.7 V	50 pF	500 Ω	open
4.5 V to 5.5 V	V <sub>CC</sub>	50 pF	500 Ω	open



12 Package outline

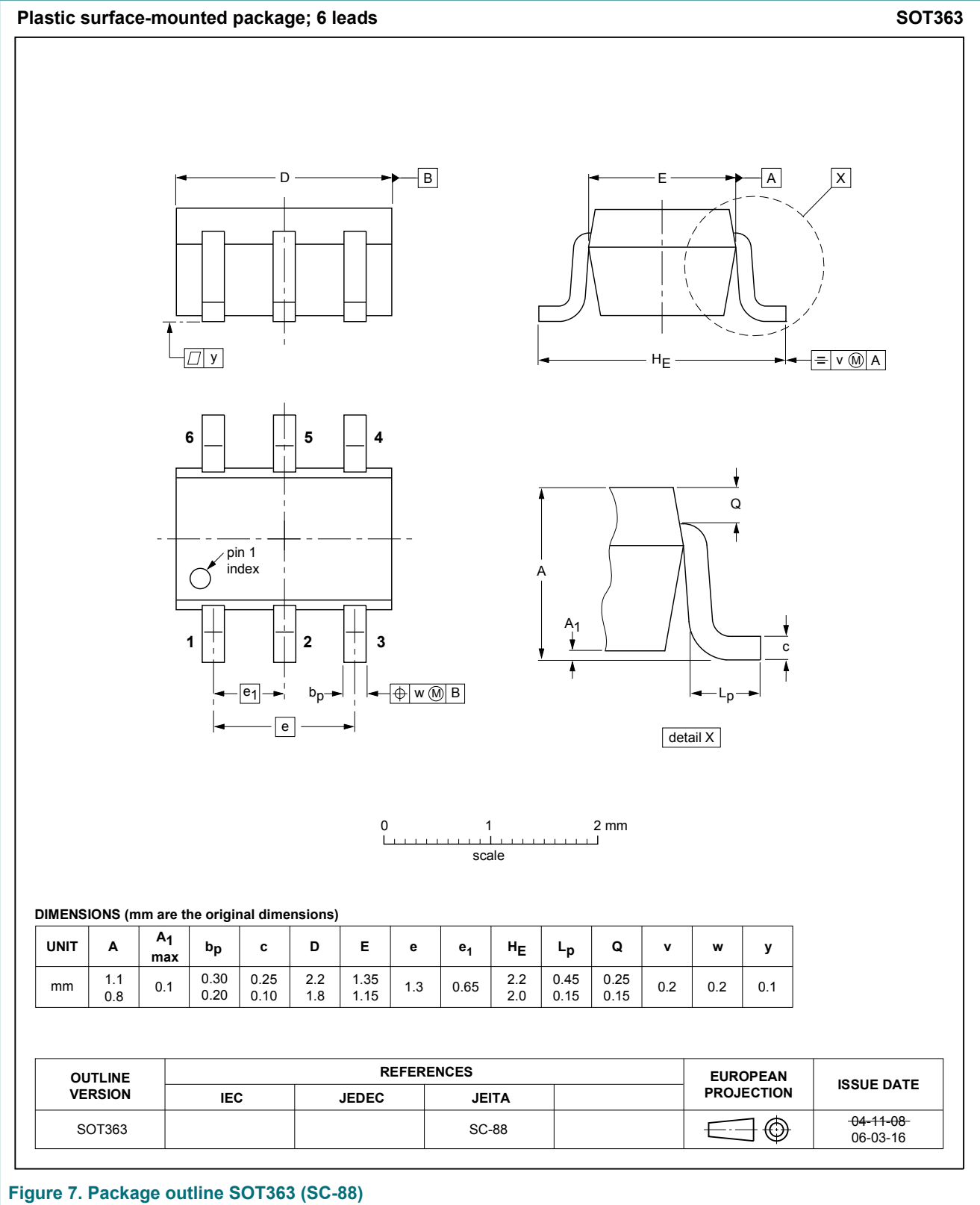
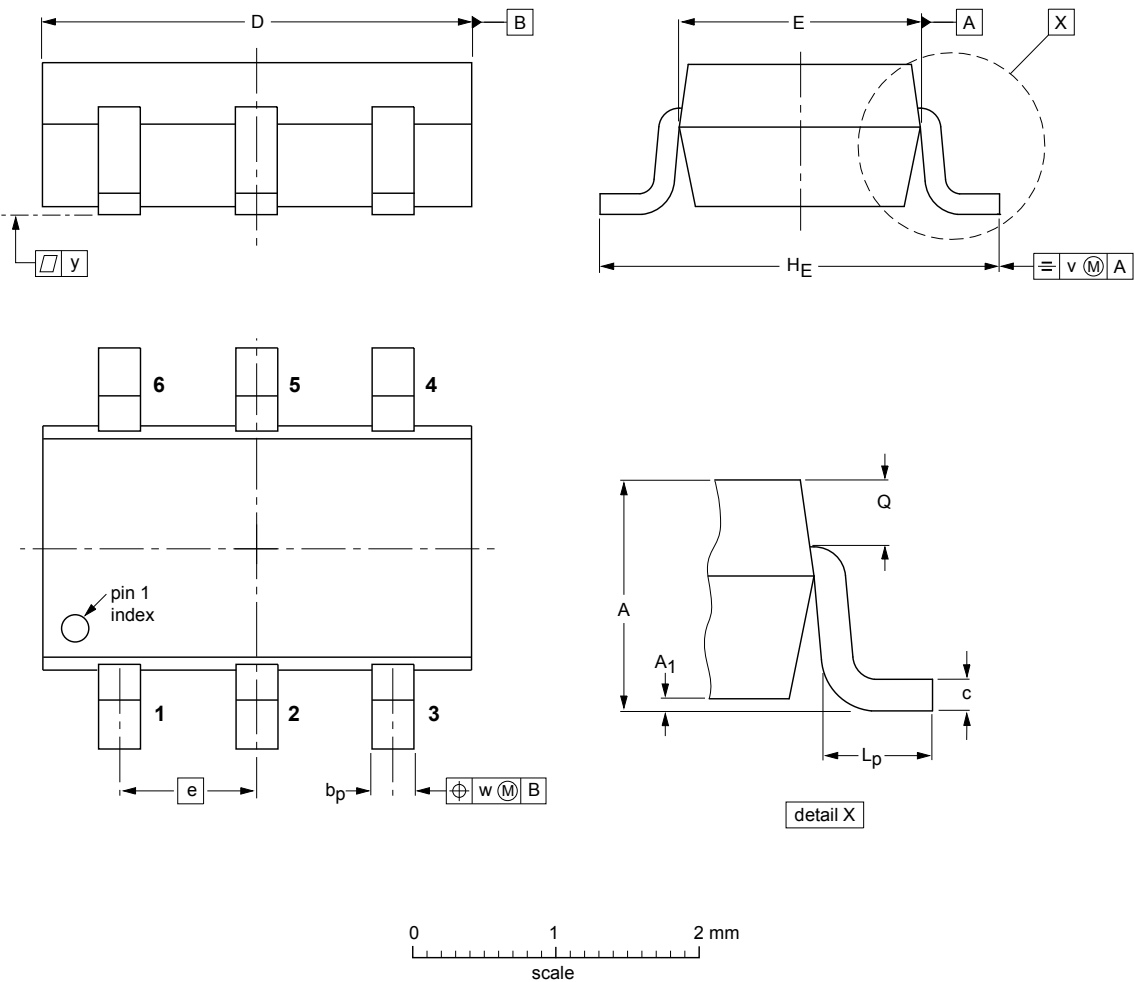


Figure 7. Package outline SOT363 (SC-88)

Plastic surface-mounted package (TSOP6); 6 leads

SOT457



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	b <sub>p</sub>	c	D	E	e	H <sub>E</sub>	L <sub>p</sub>	Q	v	w	y
mm	1.1 0.9	0.1 0.013	0.40 0.25	0.26 0.10	3.1 2.7	1.7 1.3	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT457			SC-74			05-11-07 06-03-16

Figure 8. Package outline SOT457 (SC-74)

## 13 Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 14 Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC1G386 v.4	20170509	Product data sheet	-	74LVC1G386 v.3
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate</li> </ul>			
74LVC1G386 v.3	20161207	Product data sheet	-	74LVC1G386 v.2
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Table 7</a>: The maximum limits for leakage current and supply current have changed.</li> </ul>			
74LVC1G386 v.2	20121119	Product data sheet	-	74LVC1G386 v.1
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>In <a href="#">Section 10 "Static characteristics"</a>, changed conditions for input leakage and supply current.</li> </ul>			
74LVC1G386 v.1	20031104	Product specification	-	

## 15 Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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For sales office addresses, please send an email to: [salesaddresses@nexperia.com](mailto:salesaddresses@nexperia.com)

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