MP4034

Offline LED Driver

The Future of Analog IC Technology

DESCRIPTION

The MP4034 is an offline regulator that provides accurate constant-current regulation. The LED driver circuit design is simplified by removing the opto-coupler and the secondary feedback components.

The MP4034 has an integrated 700V MOSFET. Its variable off-time control allows a flyback converter to operate in discontinuous conduction mode (DCM). The MP4034 also features complete protection functions such as VCC under-voltage lockout, over-voltage protection, over-temperature protection, and open-loop protection.

The MP4034's variable switching frequency provides natural spectrum shaping to smooth the EMI signature, which can reduce the EMI filter's size and cost.

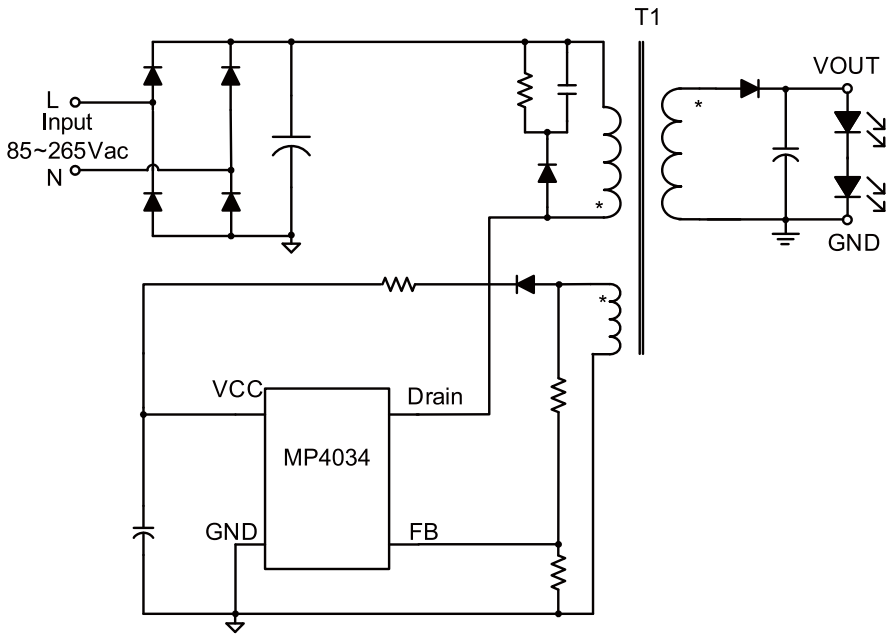
FEATURES

- Primary-Side–Control without Opto-coupler or Secondary Feedback Circuit
- Precise Constant Current Regulation
- Integrated 700V MOSFET with Minimal External Components
- Variable Off-Time and Peak-Current Control
- 550μA High-Voltage Current Source
- Up to 7W Output Power
- Over-Voltage Protection
- Over-Temperature Protection
- Open-Loop Protection
- Natural Spectrum Shaping for Improved EMI Signature
- Low Cost and Simple External circuit
- SOIC8-7A Package

APPLICATIONS

- Offline LED Driver

TYPICAL APPLICATION

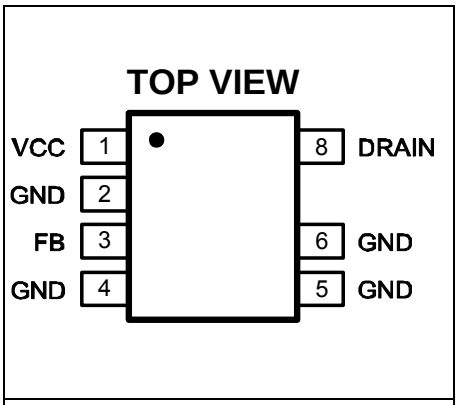


ORDERING INFORMATION

Part Number*	Package	Top Marking
MP4034GS	SOIC8-7A	MP4034

* For Tape & Reel, add suffix –Z (e.g. MP4034GS–Z);

PACKAGE REFERENCE



SOIC8-7A

ABSOLUTE MAXIMUM RATINGS (1)

Drain to GND ..... -0.7V to 700V
VCC to GND ..... -0.3V to 30V
FB Input..... -0.7V to 10V
Continuous Power Dissipation (T_A = +25°C) (2)
SOIC8-7A……...1.3W
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature.....-60°C to +150°C
ESD Capability Human Body Mode 2.0kV
ESD Capability Machine Mode 200V

Recommended Operating Conditions (3)

Operating VCC range ..... 6.6V to 28V
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
SOIC8-7A	76	45	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

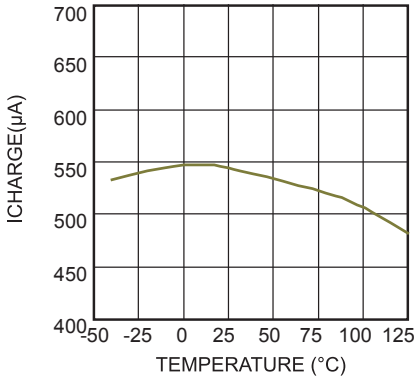
ELECTRICAL CHARACTERISTICS

V_{CC} = 15V, T_A = 25°C, unless otherwise noted.

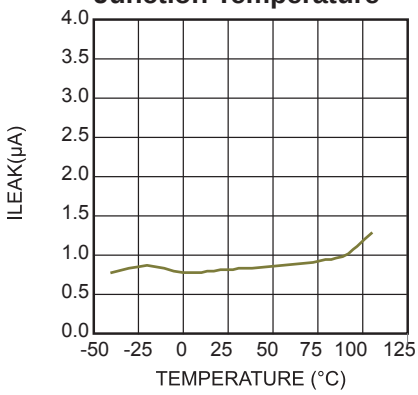
Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Voltage Management (VCC Pin)						
V_{CC} ON threshold	V_{CCH}		16.8	17.3	17.8	V
V_{CC} OFF threshold	V_{CCL}		6	6.3	6.6	V
V_{CC} operating voltage			6.6		28	V
Quiescent current	I_Q	At no load condition, V_{CC}=20V		360	410	μA
Operating current	I_{OP}	60kHz, V_{CC}=20V		500		μA
Leakage current from VCC Pin	I_{Leak_VCC}	V_{CC}=0V→16V, Drain float		0.1	1	μA
Internal MOSFET (Drain Pin)						
Break down voltage	V_{BRDSS}	V_{CC}=20V, V_{FB}=7V	700			V
Supply Current from Drain Pin	I_{Charge}	V_{CC}=4V, V_{Drain}=100V	450	550	750	μA
Leakage current from Drain Pin	I_{Leak_Drain}	V_{DS}=500V_{DC}		1	10	μA
On-state resistance	R_{ON}	I_D=10mA, T_J=20 degree		10	13	Ω
Internal Current Sense						
Current Limit	I_{Limit}	V_{FB}=-0.5V	365	380	395	mA
Leading-edge blanking	t_{LEB}		230	300	370	ns
Feedback input (FB Pin)						
FB pin input current	I_{FB}	V_{FB}=4V		0.2	0.5	μA
DCM detect threshold	V_{DCM}		80	120	160	mV
FB open-circuit threshold	V_{FBOPEN}		-0.22	-0.15	-0.08	V
First-level FB OVP threshold	V_{FBOVP1}		3.93	4	4.07	V
Second-level FB OVP threshold	V_{FBOVP2}		6.2	6.35	6.5	V
OVP sampling delay	t_{OVP}			3.5		μs
Thermal Shutdown						
Thermal shutdown threshold				150		°C
Thermal shutdown recovery threshold				120		°C

TYPICAL CHARACTERISTICS

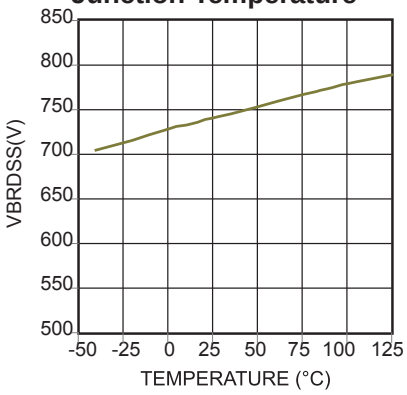
Charge Current vs. Junction Temperature



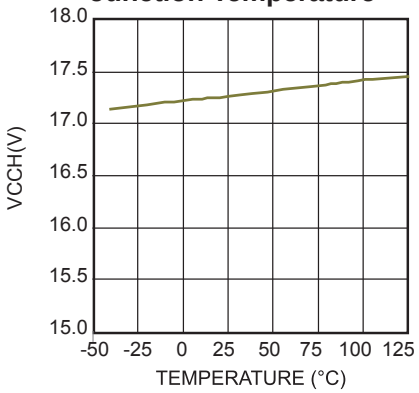
Leakage Current vs. Junction Temperature



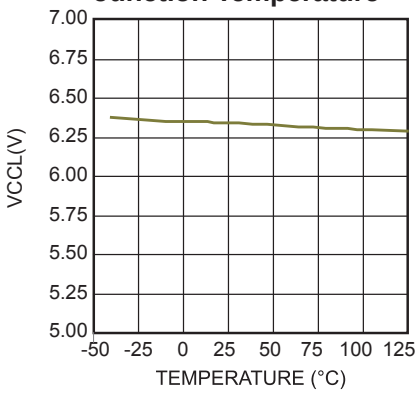
Breakdown Voltage vs. Junction Temperature



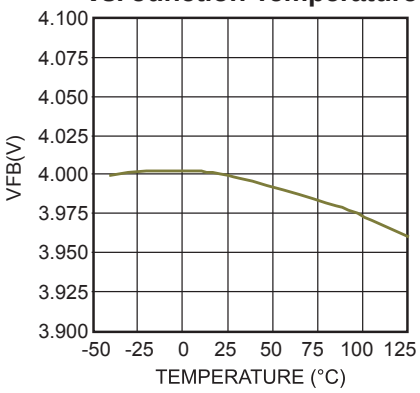
V_{CC} ON Threshold vs. Junction Temperature



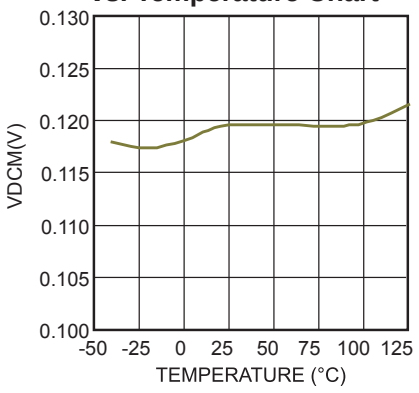
V_{CC} OFF Threshold vs. Junction Temperature



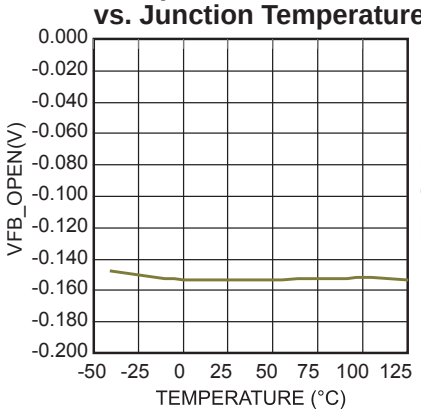
First-Level OVP Threshold vs. Junction Temperature



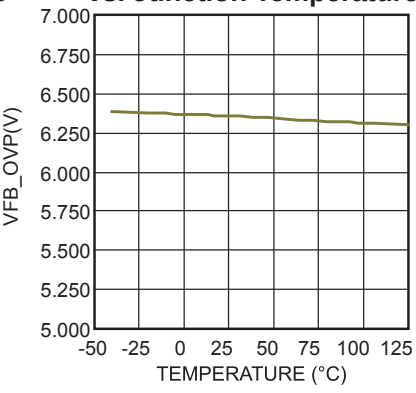
DCM Detect Threshold vs. Temperature Chart



FB Open Circuit Threshold vs. Junction Temperature

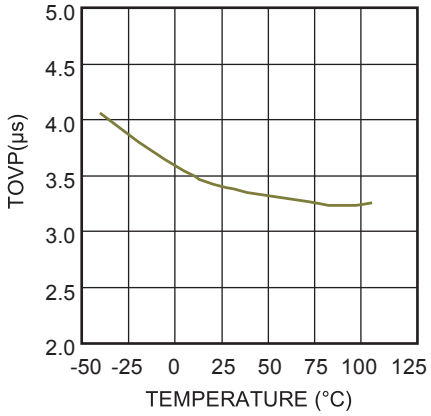


Second-Level OVP Threshold vs. Junction Temperature

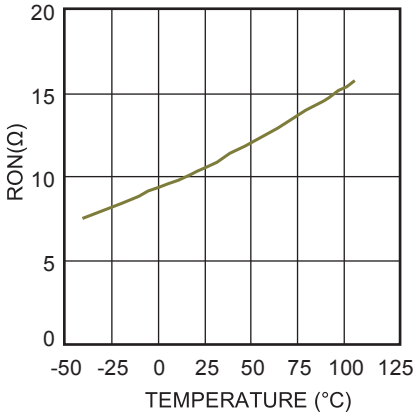


TYPICAL CHARACTERISTICS *(continued)*

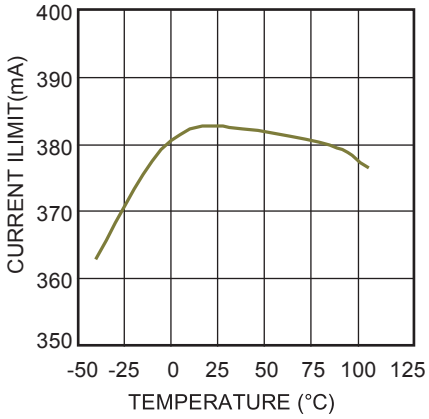
OVP Sample Delay vs. Junction Temperature



On State Resistance vs. Junction Temperature



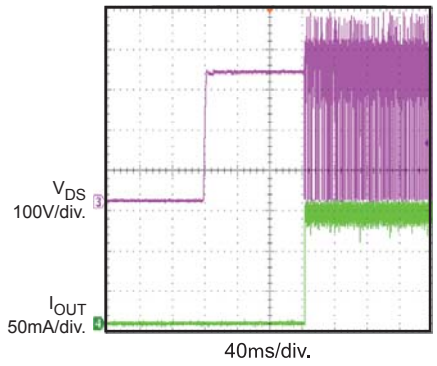
Current I_{Limit} vs. Junction Temperature



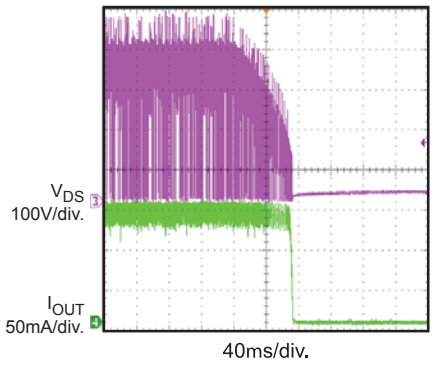
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 230VAC, V_{OUT} = 40V, I_{OUT}=0.13A, L = 1.2mH, T_A = 25°C, unless otherwise noted.

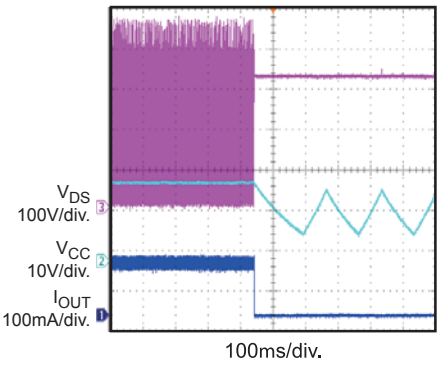
Input Power Startup



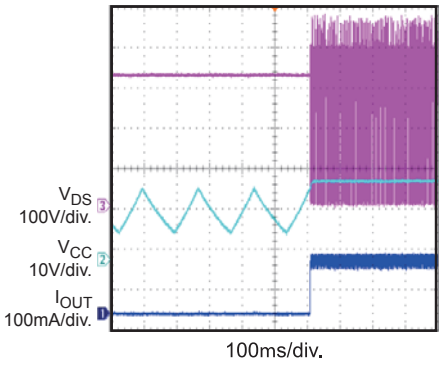
Input Power Shut Down



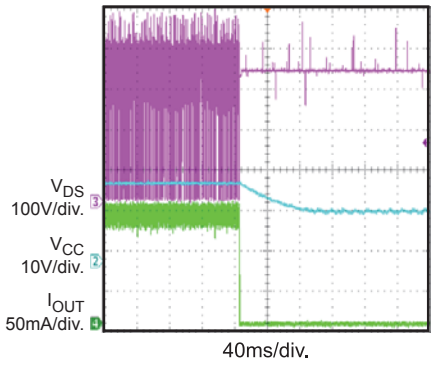
OCkP Entry



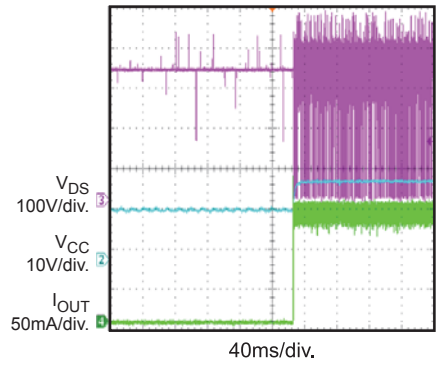
OCkP Recovery



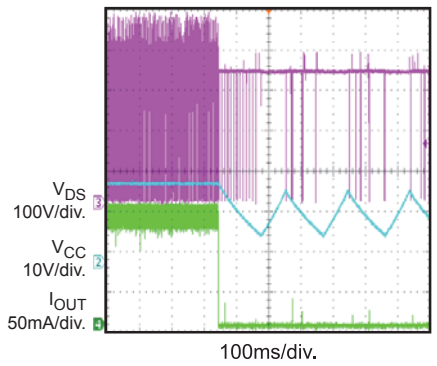
OVP Entry



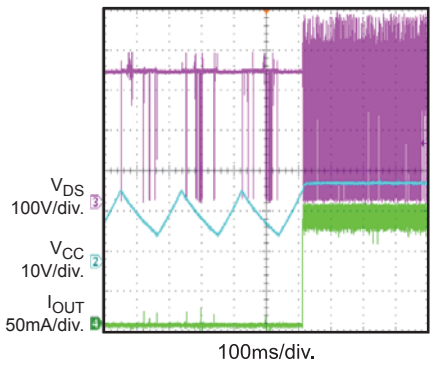
OVP Recovery



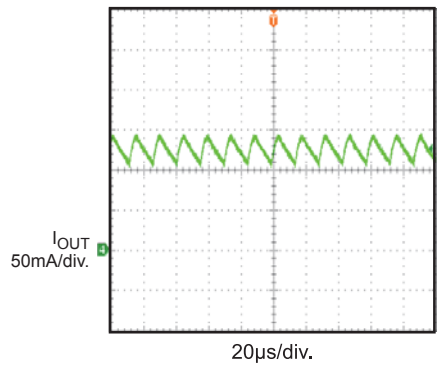
SCP Entry



SCP Recovery



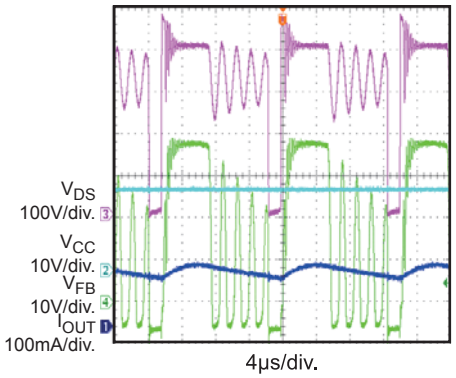
Output Current Ripple



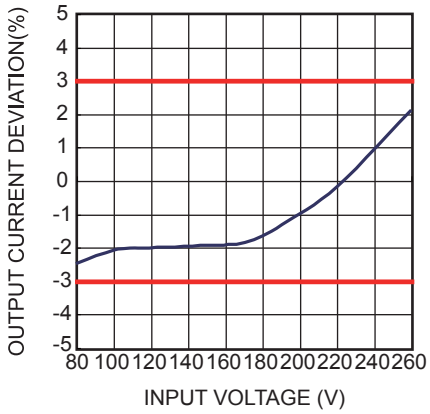
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 230VAC, V_{OUT} = 40V, I_{OUT}=0.13A, L = 1.2mH, T_A = 25°C, unless otherwise noted.

Normal Operation



Output Current Regulation



PIN FUNCTIONS

SOIC8-7A Pin #	Name	Description
1	VCC	Supply. An internal high-voltage current source charges VCC voltage to V_{CCH} to start the IC. The internal high-voltage current source will also turn on when V_{CC} falls below V_{CCL} to charge VCC. Connect a 0.1μF ceramic decoupling capacitor as close as possible to this pin.
3	FB	Feedback. Controls the OVP function. If V_{FB}=4.0V, the first-level OVP triggers and output voltage remains constant. If V_{FB}=6.35V, the second-level OVP triggers, switch immediately shuts off, and IC restarts.
2, 4, 5, 6	GND	Ground.
8	Drain	Internal MOSFET Drain. Input for the startup high-voltage current source.

FUNCTIONAL BLOCK DIAGRAM

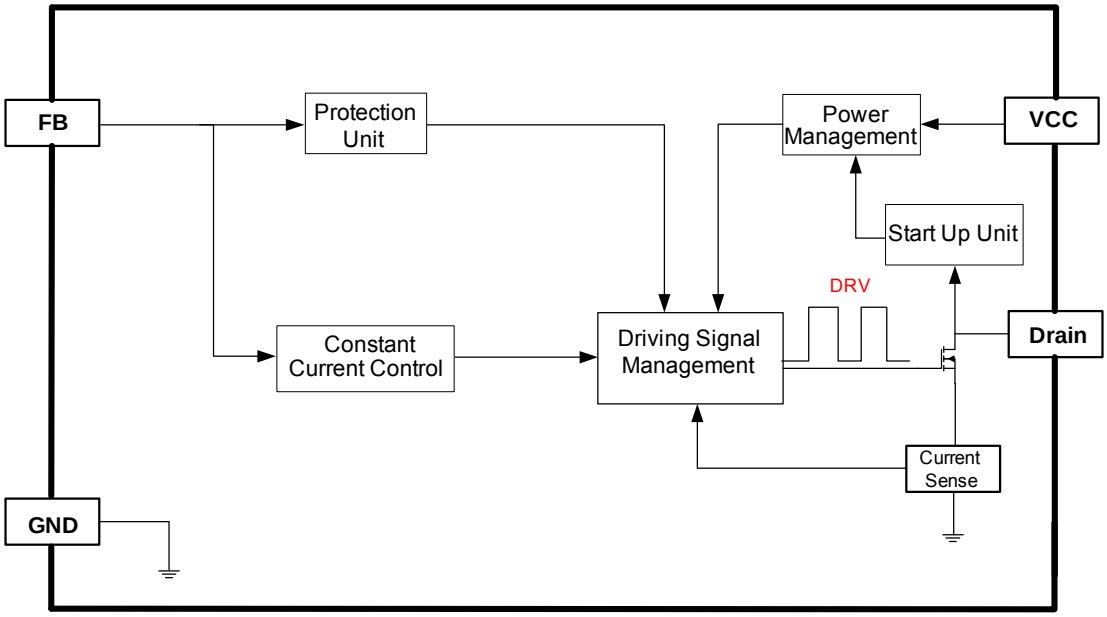


Figure 1: Functional Block Diagram

OPERATION

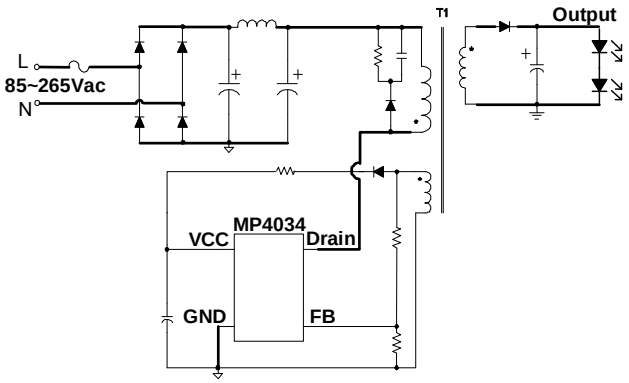


Figure 2: Simplified Flyback Converter

Startup

Initially, the IC is self-supplying through the internal high-voltage current source, which is drawn from the Drain pin. The internal high-voltage current source will turn off for better efficiency when V_{CC} reaches the V_{CC} ON threshold. Then the transformer's auxiliary winding takes over as the power source. When V_{CC} falls below the V_{CC} OFF threshold, the IC stops switching and the internal high-voltage current source turns on again. See Figure 3 for the start-up waveform.

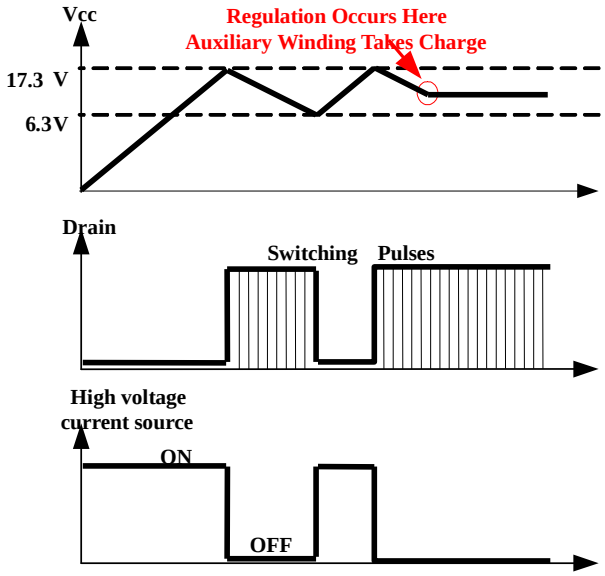


Figure 3: VCC UVLO

Transformer Design

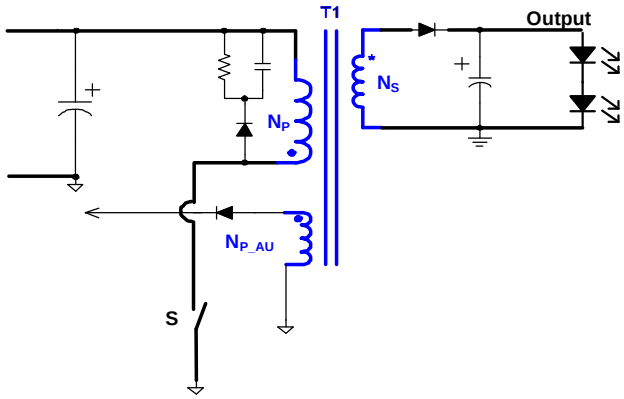


Figure 4: Isolated Flyback LED Driver

The MP4034 ensures that the circuit operates in discontinues conduction mode (DCM). When the IC internal MOSFET turns on, the current (i_P) flowing through transformer's primary-side winding (N_P) increases linearly until it reaches its peak current limit (I_{PK})

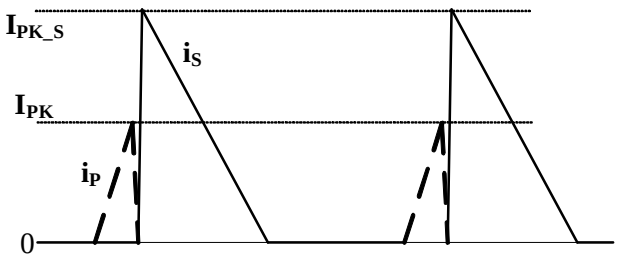


Figure 5: Current Waveform

Assume switching frequency is f_s, the power stored in the inductor is given by:

$$P = \frac{1}{2} L_M \times I_{PK}^2 \times f_S$$

Then inductance of coupling inductor is then:

$$L_M = \frac{2 \times P_O}{I_{PK}^2 \times f_S \times \eta}$$

Where P_O is output power and η is the estimated efficiency.

When MP4034's internal switch turns off, the freewheeling current (i_S) will flow through secondary-side diode and decrease linearly, as shown in Figure 5.

The relationship of peak current at ON period and OFF period is:

$$I_{PK\_S} = \frac{N_P}{N_S} \times I_{PK}$$

Where N_P is the number of primary winding turns, and N_S is the number of secondary winding turns.

The MP4034 detects the secondary side diode duty cycle by sampling the auxiliary winding voltage and generates a ZCD signal as shown in Figure 6.

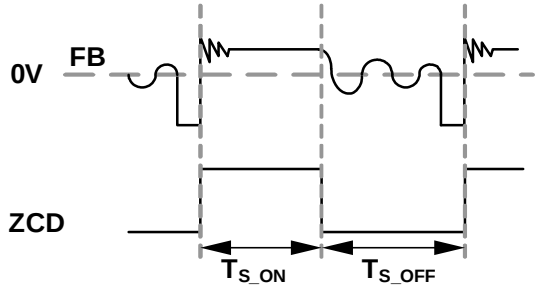


Figure 6: VFB and ZCD Waveforms

When the FB voltage is high—which means that the current is flowing through secondary-side diode—the ZCD signal goes high. Conversely, when the FB voltage is low—which means no current flows through the secondary-side diode—the ZCD signal goes low, meaning the secondary-side diode duty cycle (D_S) is:

$$D_S = \frac{T_{S\_ON}}{T_{S\_ON} + T_{S\_OFF}}$$

Then the average output current is:

$$I_{OUT} = \frac{1}{2} \times I_{PK\_S} \times D_S$$
$$= \frac{1}{2} \times \frac{N_P}{N_S} \times I_{PK} \times \frac{T_{S\_ON}}{T_{S\_ON} + T_{S\_OFF}}$$

The MP4034 keeps D_S at 0.4. Thus the output current is:

$$I_{OUT} = \frac{1}{2} \times \frac{N_P}{N_S} \times I_{PK} \times D_S = \frac{1}{5} \times \frac{N_P}{N_S} \times I_{PK}$$

This provides enough information to design the transformer turn ratio.

Leading-Edge Blanking

Turning the power switch on induces a spike on the sense resistor. To avoid falsely terminating the switching pulse, the MP4034 includes a 300ns leading-edge blanking period. During this blanking period, the current sense comparator is disabled and the gate driver can not switch off.

DCM Detection

The MP4034 is designed to operate in discontinuous conduction mode (DCM). To avoid operating in continuous conduction mode (CCM), the MP4034 detects the falling edge of the FB input voltage with each cycle. If the chip does not detect a 120mV falling edge, it will stop switching.

Over Voltage Protection

The MP4034 has two levels of over-voltage protection based on the FB voltage.

In normal operation, MP4034 samples the FB pin voltage 3.5μs after the primary switch turns off, as shown in Figure 6.

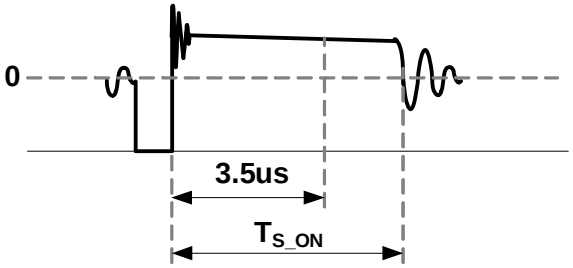


Figure 7: Auxiliary Voltage Waveform

The relationship of output voltage and V_{FB} is :

$$V_{FB} = \frac{N_{P\_AU}}{N_S} \times \frac{R_{DOWN}}{R_{UP} + R_{DOWN}} \times (V_O + V_D)$$

Where V_D is the secondary-diode forward-drop voltage.

When the MP4034 detects that the FB voltage equals 4.0V, the first level OVP triggers. The switching frequency drops to maintain the output voltage at a constant value. If V_{FB} voltage exceeds 6.35V for 3.5μs, it will shut down immediately and discharge the VCC

voltage. When V_{CC} drops to UVLO, the MP4034 will restart.

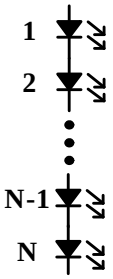


Figure 8: LED String

Assume the forward voltage of one LED is V_F and the total number of LEDs on the string is N. So the output voltage can be calculated as $N \times V_F$. To ensure that OVP won't trigger during normal operation; the V_{FB} should not exceed V_{FBOVP1} (typical 4.0V). However, avoid a large output voltage when OVP occurs. So the voltage reflected on the FB pin should be:

$$V_{FB} = \frac{N_{P\_AU}}{N_S} \times \frac{R_{DOWN}}{R_{DOWN} + R_{UP}} \times (N \times V_F + V_D) = 0.85 V_{FBOVP1}$$

Open-Circuit Protection (OCkP)

The MP4034 has open-circuit protection (OCkP). If the −0.15V falling edge of V_{FB} can not be monitored—which means the feedback loop is open—the MP4034 immediately shuts off the driving signals and enters hiccup mode. The MP4034 resumes normal operation when the fault has been removed.

Thermal Shutdown (TSD)

When the temperature of the IC exceeds 150°C, the over-temperature protection is enacted and the IC enters auto-recovery mode. When the temperature falls below 120°C, the IC resumes working.

APPLICATION INFORMATION

COMPONENT SELECTION

Input Filter

Input filter produces a DC source through the rectifier from the AC input power Figure 9 shows the input filter and Figure 10 shows the typical DC bus voltage waveform.

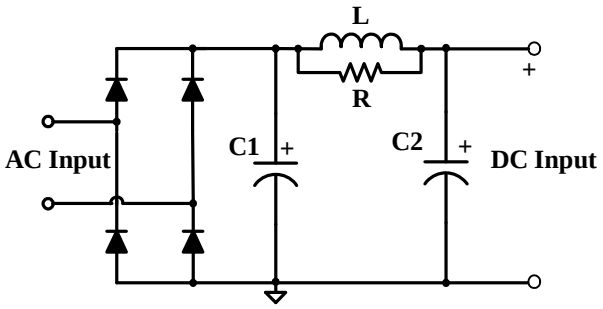


Figure 9: Input Filter

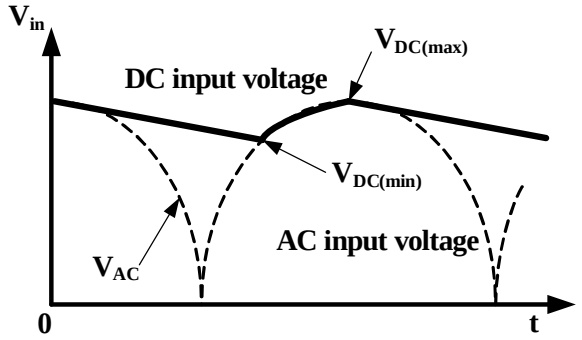


Figure 10: DC Input-Voltage Waveform

Bulk capacitors C1 and C2 filter the rectified AC. Inductor L forms a π filter with C1 and C2 to restrain the differential-mode EMI noise. The resistor (R) in parallel with the inductor (L) restrains the mid-frequency-band EMI noise. Normally, R is selected between 1kΩ and 10kΩ.

The DC input capacitors, C1 and C2, are usually 2μF/W to 3μF/W for the universal input condition. For a 230VAC single-range application, the capacitor can be half that value. Normally, the minimum DC voltage should not be too low to ensure the converter can supply the maximum power to the load which can be express as follows:

$$V_{DC(min)} \geq \frac{N_P}{N_S} \cdot (N \cdot V_F + V_D) \cdot \frac{D_S}{1 - D_S}$$

If the $V_{DC(min)}$ can not satisfy this express, increase the value of the input capacitors to increase the $V_{DC(min)}$.

Output Diode

Use a Schottky diode because of its fast switching speed and low forward voltage drop for better efficiency.

If a lower average efficiency (3%-4%) is acceptable, replace the output diode with a PN-junction diode or other non-Schottky diode to lower costs.

Leakage Inductance

The transformer leakage inductance will decrease the system efficiency and affect the output current constant precision. The transformer structure should be optimized to improve the primary side and secondary side coupling and minimize the transformer leakage inductance of transformer. Aim for a leakage inductance that is less than 5% inductance.

RCD Snubber

The transformer leakage inductance causes the MOSFET drain voltage spike and the excessive ringing on the drain voltage waveform.

The RCD snubber circuit can limit this Drain voltage spike. Figure 11 shows the RCD snubber circuit.

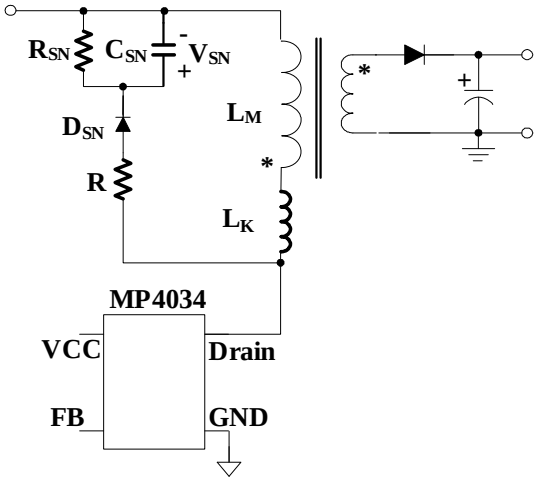


Figure 11: RCD Snubber

Select R_{SN} and C_{SN} for an acceptable voltage spike and better system operation.

The power dissipated in the snubber circuit is approximately:

$$P_{SN} = \frac{1}{2} \cdot L_K \cdot I_{PK}^2 \cdot \frac{V_{SN}}{V_{SN} - N_{PS} \times V_O} \times f_S$$

Where:

- L_K is the leakage inductance,
- V_{SN} is the clamp voltage,
- N_{PS} is the turn ratio of primary and secondary side.

The power consumed in the snubber resistor (R_{SN}), the resistor (R_{SN}) is:

$$R_{SN} = \frac{V_{SN}^2}{P_{SN}}$$

The maximum ripple of the snubber capacitor voltage is:

$$\Delta V_{SN} = \frac{V_{SN}}{C_{SN} \cdot R_{SN} \cdot f_S}$$

Generally, a 15% ripple is reasonable. Use the previous equation to approximate C_{SN}.

The damping resistor (R) in series with the RCD has a relatively large value to prevent any excessive ringing voltage that can affect the EMI. Use a damping resistor of about 200Ω to 500Ω to limit the drain voltage ringing.

Resistor Divider

For better application performance, use a resistor divider with values in the range of 10kΩ to 100kΩ to limit noise from adjacent components on the FB pin. Connect a resistor with a value ranging from 1kΩ to 2kΩ from the FB pin to the resistor divider to limit substrate injection current effects, as shown in Figure 12.

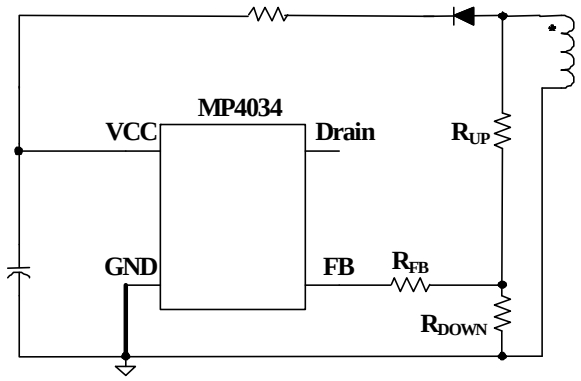


Figure 12: FB Pin in Series with ON Resistor

Dummy Load

A dummy load is required in open-output applications for good over-voltage protection. Use a dummy load of ~10mW for good load regulation.

Maximum Switching Frequency

Because of the parameter tolerance of the sampling detecting time and inductance tolerances, select a secondary-side-diode conduction time that exceeds 5.4μs as follows.

$$T_{S\_ON} = I_{PK} \cdot \frac{N_S \cdot L_M}{N_P \cdot (V_O + V_D)} > 5.4\mu s$$

For high or low temperature operation, select a maximum switching frequency below 75kHz.

PCB Layout Guide

PCB layout is very important to achieve reliable operation, and good EMI and thermal performance. The use design guide as follows to help optimize performance.

1. Minimize the loop area formed by the input capacitor, the MP4034 drain-source, and the primary winding to reduce EMI noise.

2. The copper area connected to source pins acts as a heat sink. Provide a large copper area to improve the thermal performance.

3. Minimize the clamp circuit loop to reduce EMI.

4. Minimize the secondary loop area of the output diode and output filter to reduce the EMI noise. In addition, provide a sufficient copper area at the anode and cathode terminal of the output diode for heat dissipation.

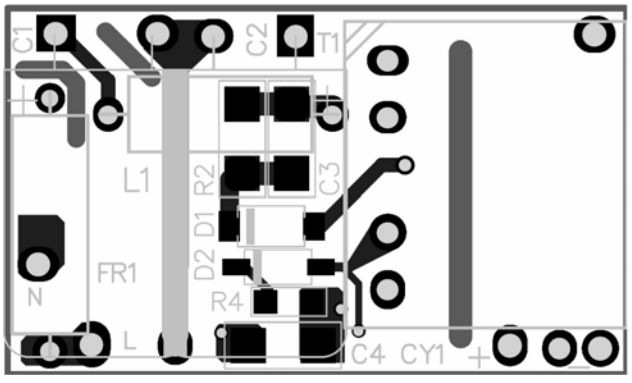
5. Place the AC input away from the switching nodes to minimize the noise coupling that may bypass the input filter.

6. Place the bypass capacitor as close as possible to the IC and source.

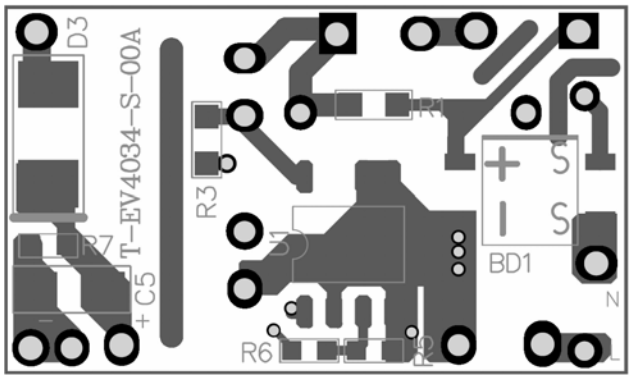
7. Place the feedback resistors at the FB pin and minimize the feedback sampling loop area to minimize noise coupling.

8. Use a single point connection at the negative terminal of the input filter capacitor for the MP4034 source pin and bias winding return.

Figure 13 shows a layout example.



Top Layer



Bottom Layer

Figure 13: PCB Layout

Design Example

Below are design examples following the application guidelines for the given specifications:

Table 1: Design Example

Example 1	
V_{IN}	85VAC-265VAC
V_{OUT}	40V
I_{OUT}	0.13A
Example 2	
V_{IN}	85VAC-265VAC
V_{OUT}	10V
I_{OUT}	0.35A

Figure 14 and Figure 15 show the detailed isolated application, while Figure 16 and Figure 17 show the detailed non-isolated application. These examples were used in the Typical Performance Characteristics section. For more applications, please refer to the related evaluation board datasheets.

TYPICAL APPLICATION CIRCUITS

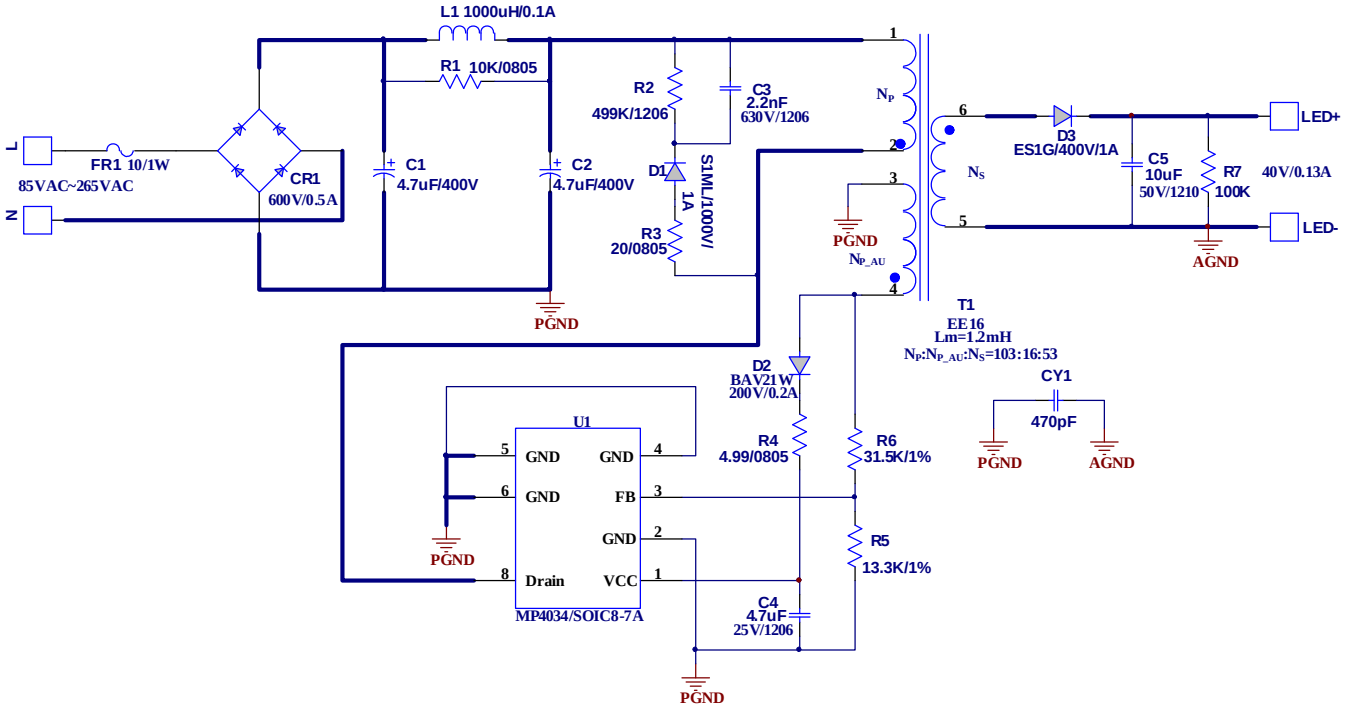


Figure 14: Typical Application Example
Universal Input, Driving 14 LEDs in Series, 130mA LED Current, 6W Isolation Flyback Converter

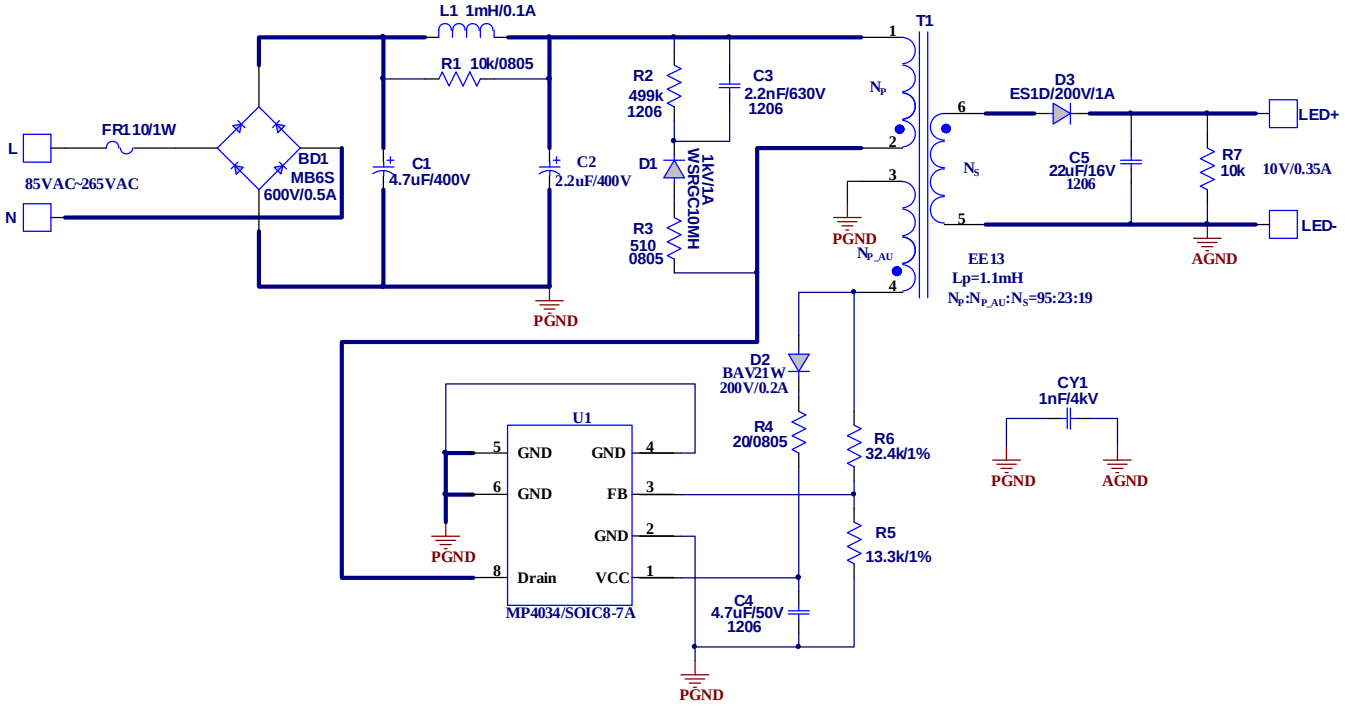


Figure 15: Typical Application Example
Universal Input, Driving 3 LEDs in Series, 350mA LED Current, 3.5W Isolation Flyback Converter

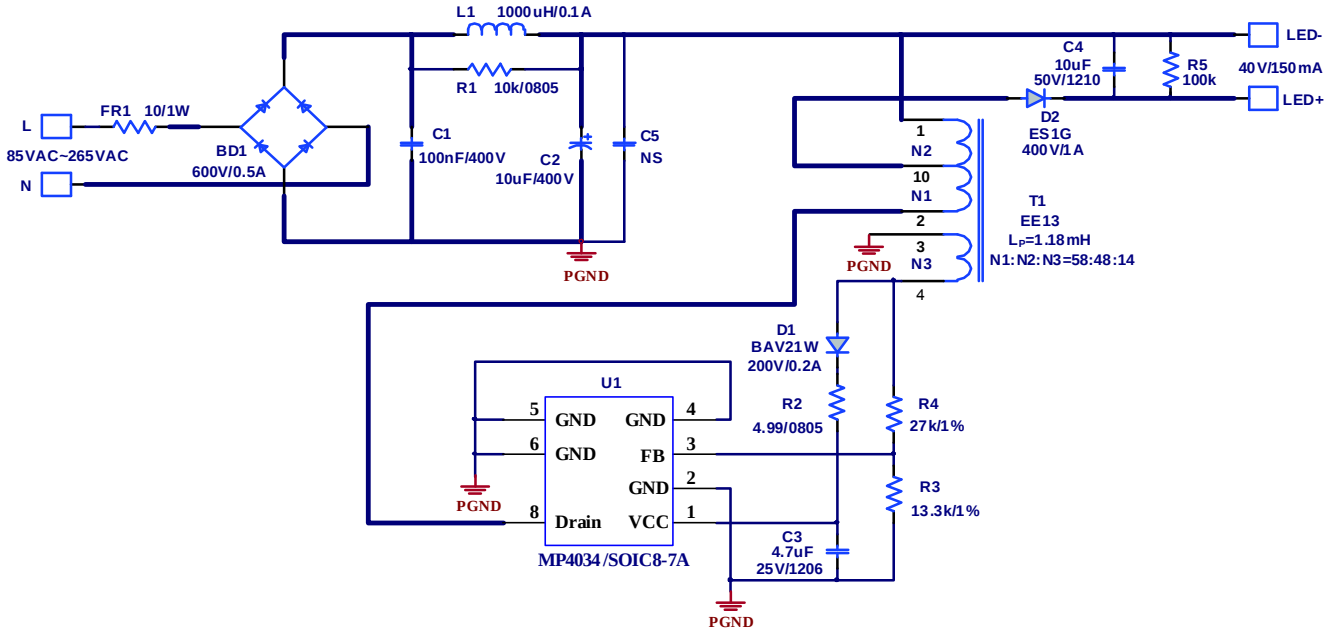


Figure 16: Typical Application Example
Universal Input, Driving 14 LEDs in Series, 150mA LED Current, 6W Non-isolated Buck-Boost Converter

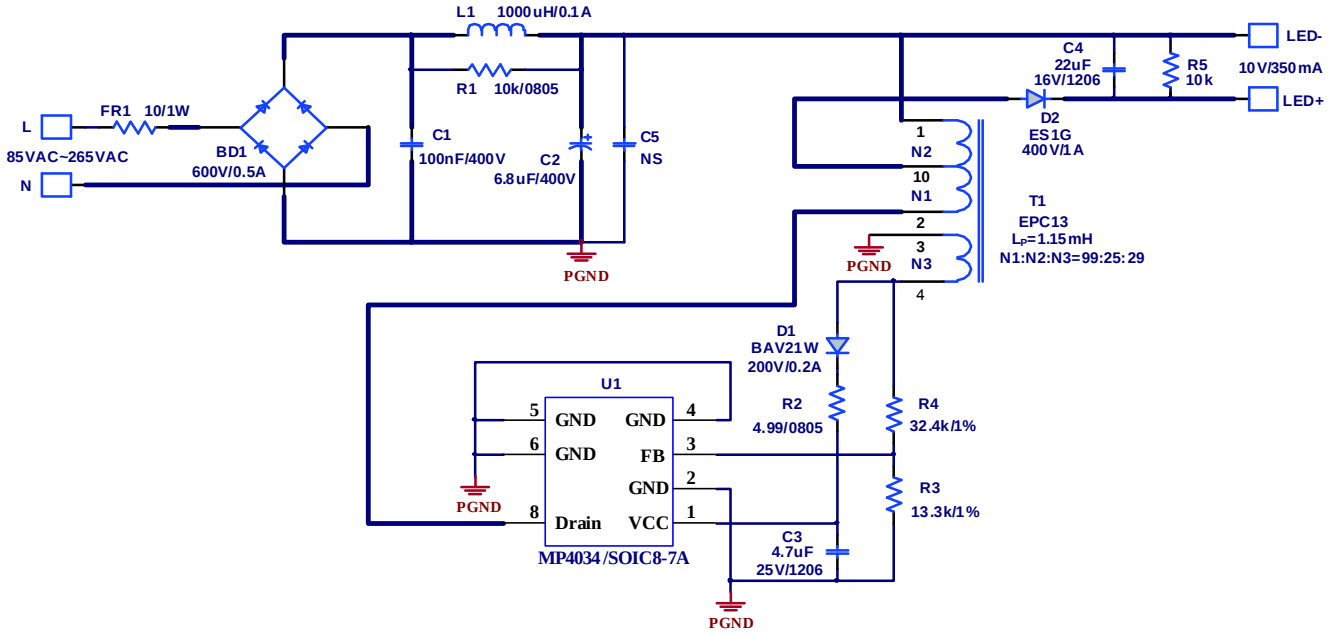
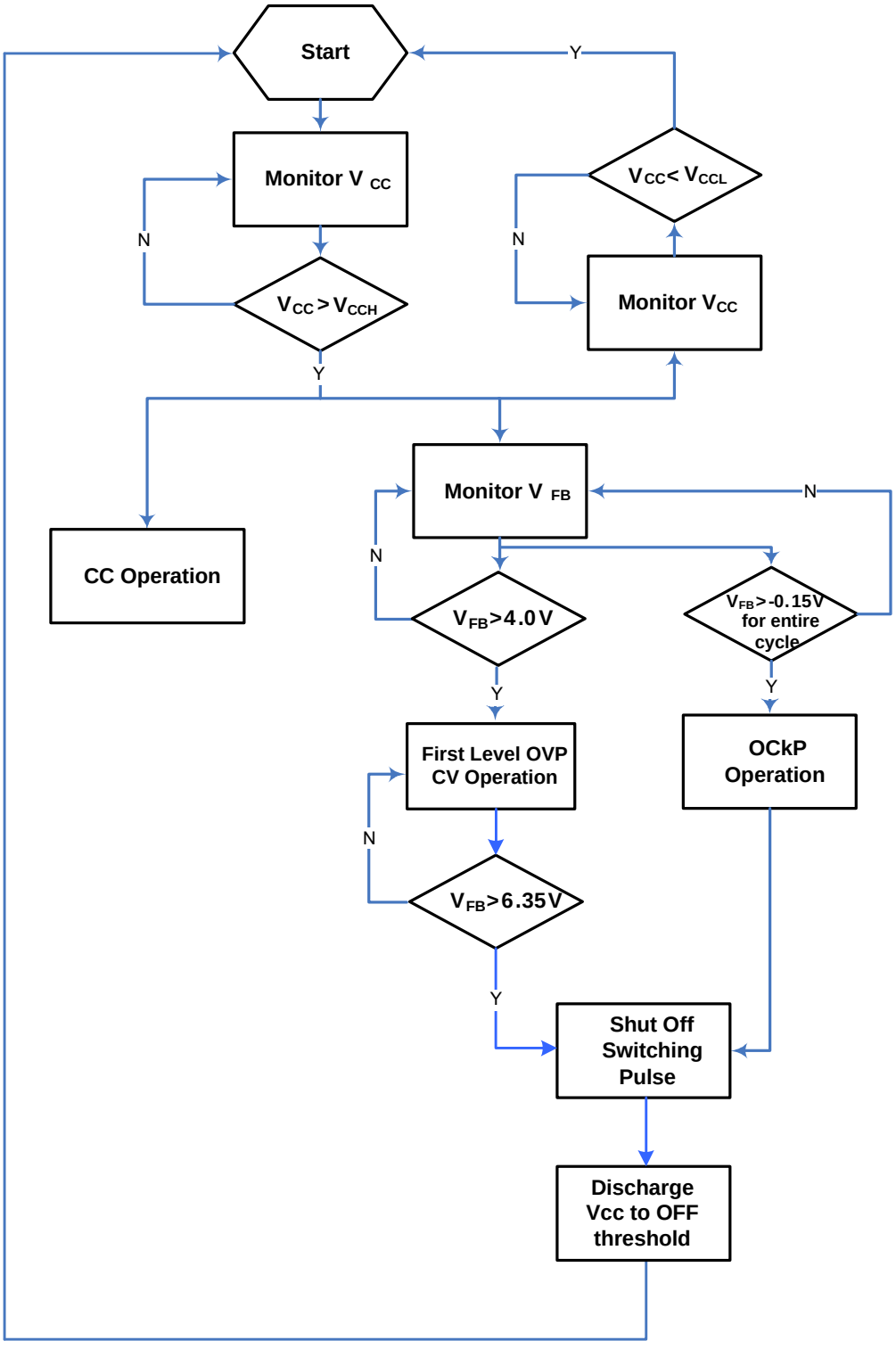


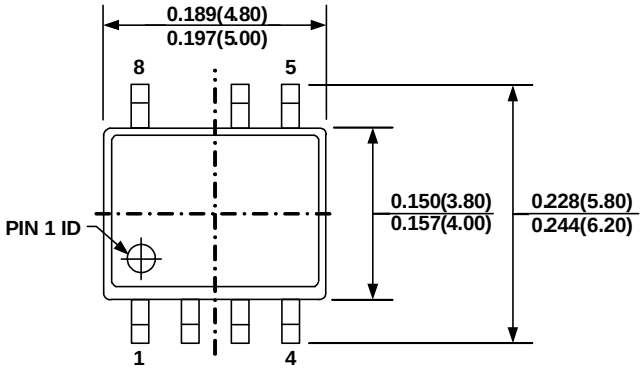
Figure 17: Typical Application Example
Universal Input, Driving 3 LEDs in Series, 350mA LED Current, 3.5W Non-isolated Buck-Boost Converter

FLOW CHART

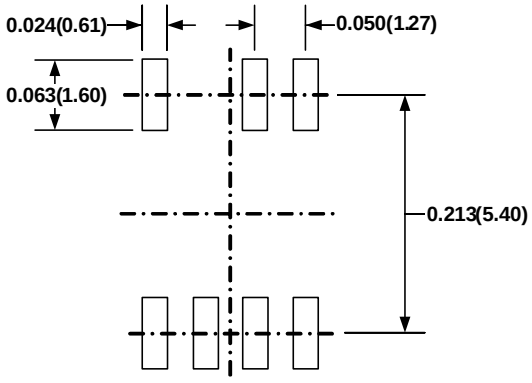


PACKAGE INFORMATION

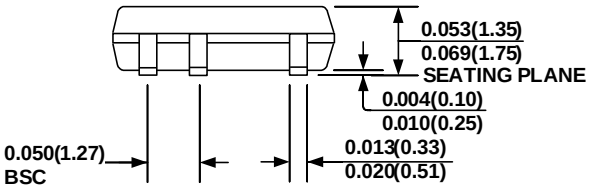
SOIC8-7A



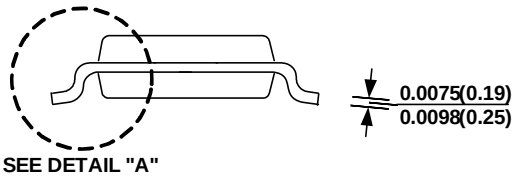
TOP VIEW



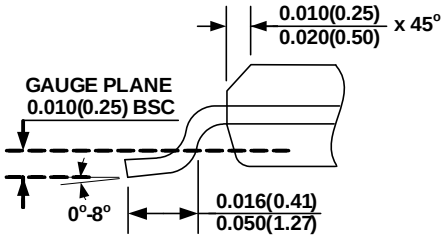
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY(BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) JEDEC REFERENCE IS MS-012.
6) DRAWING IS NOT TO SCALE