

74ALVC16245; 74ALVCH16245

16-bit transceiver with direction pin; 3-state

Rev. 4 — 21 November 2017

Product data sheet

1 General description

The 74ALVC16245; 74ALVCH16245 is a 16-bit transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions.

The 74ALVC16245; 74ALVCH16245 features two output enable inputs (pins \overline{nOE}) for easy cascading and two send or receive inputs (pins $nDIR$) for direction control. Pins \overline{nOE} control the outputs so that the buses are effectively isolated. This device can be used as two 8-bit transceivers or one 16-bit transceiver.

The 74ALVCH16245 has an active bushold circuitry which is provided to hold unused or floating data inputs at a valid logic level. This feature eliminates the need for external pull-up or pull-down resistors.

2 Features and benefits

- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- MULTIBYTE flow-through standard pin-out architecture
- Low inductance multiple V_{CC} and GND pins for minimize noise and ground bounce
- Direct interface with TTL levels
- All data inputs have bushold (74ALVCH16245 only)
- Output drive capability 50 Ω transmission lines at 85 °C
- Current drive ± 24 mA at $V_{CC} = 3.0$ V.
- Complies with JEDEC standards:
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - HBM ANSI/ESDA/JEDEC JS-001 exceeds 2000 V
 - CDM JESD22-C101E exceeds 1000 V

3 Ordering information

Table 1. Ordering information

| Type number | Package | | | |
|-----------------|-------------------|---------|--|----------|
| | Temperature range | Name | Description | Version |
| 74ALVC16245DL | -40 °C to +85 °C | SSOP48 | plastic shrink small outline package; 48 leads; body width 7.5 mm | SOT370-1 |
| 74ALVCH16245DL | | | | |
| 74ALVC16245DGG | -40 °C to +85 °C | TSSOP48 | plastic thin shrink small outline package; 48 leads; body width 6.1 mm | SOT362-1 |
| 74ALVCH16245DGG | | | | |

4 Functional diagram

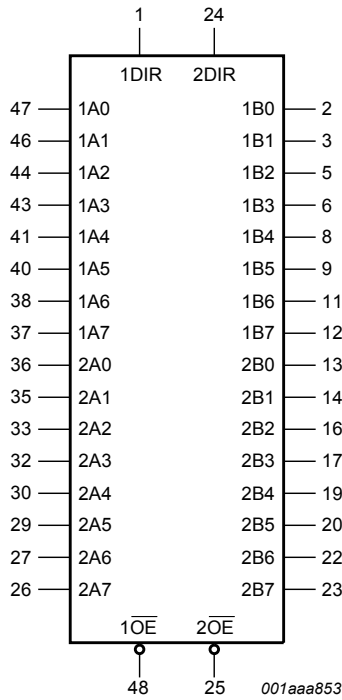


Figure 1. Logic symbol

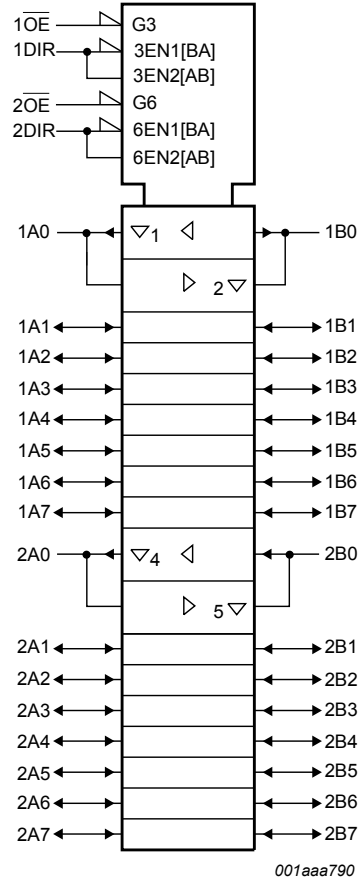


Figure 2. IEC logic symbol

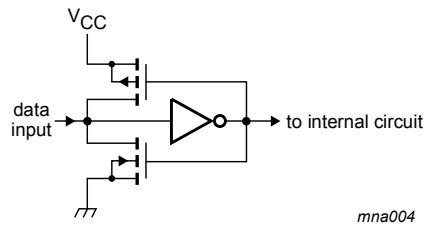


Figure 3. Bushold circuit



Figure 4. Logic diagram

5 Pinning information

5.1 Pinning



Figure 5. Pin configuration (T)SSOP48

5.2 Pin description

Table 2. Pin description

| Pin | Symbol | Description |
|--------------------------------|--|----------------------------------|
| 1, 24 | 1DIR, 2DIR | direction control inputs |
| 2, 3, 5, 6, 8, 9, 11, 12 | 1B0, 1B1, 1B2, 1B3, 1B4, 1B5, 1B6, 1B7 | data output or input |
| 4, 10, 15, 21, 28, 34, 39, 45 | GND | ground (0 V) |
| 7, 18, 31, 42 | V _{CC} | positive supply voltage |
| 13, 14, 16, 17, 19, 20, 22, 23 | 2B0, 2B1, 2B2, 2B3, 2B4, 2B5, 2B6, 2B7 | data output or input |
| 48, 25 | 1 \overline{OE} , 2 \overline{OE} | output enable input (active LOW) |
| 36, 35, 33, 32, 30, 29, 27, 26 | 2A0, 2A1, 2A2, 2A3, 2A4, 2A5, 2A6, 2A7 | data input or output |
| 47, 46, 44, 43, 41, 40, 38, 37 | 1A0, 1A1, 1A2, 1A3, 1A4, 1A5, 1A6, 1A7 | data input or output |

6 Functional description

Table 3. Function table ^[1]

| Input | | Input or output | |
|-------|------|------------------|------------------|
| nOE | nDIR | nAn | nBn |
| L | L | output nAn = nBn | input |
| L | H | input | output nBn = nAn |
| H | X | Z | Z |

- [1] H = HIGH voltage level
 L = LOW voltage level
 X = don't care
 Z = high-impedance OFF-state.

7 Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|-------------------------|--|------|-----------------------|------|
| V _{CC} | supply voltage | | -0.5 | +4.6 | V |
| V _I | input voltage | data inputs with bushold ^[1] | -0.5 | V _{CC} + 0.5 | V |
| | | data inputs without bushold ^[1] | -0.5 | +4.6 | V |
| | | control pins ^[1] | -0.5 | +4.6 | V |
| V _O | output voltage | ^[1] | -0.5 | V _{CC} + 0.5 | V |
| I _{IK} | input clamping current | V _I < 0 V | -50 | - | mA |
| I _{OK} | output clamping current | V _O > V _{CC} or V _O < 0 V | - | ±50 | mA |
| I _O | output current | V _O = 0 V to V _{CC} | - | ±50 | mA |
| I _{CC} | supply current | | - | 100 | mA |
| I _{GND} | ground current | | -100 | - | mA |
| T _{stg} | storage temperature | | -65 | +150 | °C |
| P _{tot} | total power dissipation | T _{amb} = -40 °C to +85 °C | | | |
| | | SSOP package ^[2] | - | 850 | mW |
| | | TSSOP package ^[3] | - | 600 | mW |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] Above 55 °C the value of P_{tot} derates linearly with 11.3 mW/K.

[3] Above 55 °C the value of P_{tot} derates linearly with 8 mW/K.

8 Recommended operating conditions

Table 5. Recommended operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------|-------------------------------------|----------------------------------|-----|-----|-----------------|------|
| V _{CC} | supply voltage | maximum speed performance | | | | |
| | | C _L = 30 pF | 2.3 | - | 2.7 | V |
| | | C _L = 50 pF | 3.0 | - | 3.6 | V |
| | | low-voltage applications | 1.2 | - | 3.6 | V |
| V _I | input voltage | | 0 | - | V _{CC} | V |
| V _O | output voltage | | 0 | - | V _{CC} | V |
| T _{amb} | ambient temperature | | -40 | - | +85 | °C |
| Δt/ΔV | input transition rise and fall rate | V _{CC} = 2.3 V to 3.0 V | - | - | 20 | ns/V |
| | | V _{CC} = 3.0 V to 3.6 V | - | - | 10 | ns/V |

9 Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Typ ^[1] | Max | Unit |
|---|---------------------------|---|-----------------------|------------------------|------|------|
| T_{amb} = -40 °C to +85 °C | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 2.3 V to 2.7 V | 1.7 | 1.2 | - | V |
| | | V _{CC} = 2.7 V to 3.6 V | 2.0 | 1.5 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 2.3 V to 2.7 V | - | 1.2 | 0.7 | V |
| | | V _{CC} = 2.7 V to 3.6 V | - | 1.5 | 0.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} | | | | |
| | | I _O = -100 μA; V _{CC} = 2.3 V to 3.6 V | V _{CC} - 0.2 | V _{CC} | - | V |
| | | I _O = -6 mA; V _{CC} = 2.3 V | V _{CC} - 0.3 | V _{CC} - 0.08 | - | V |
| | | I _O = -12 mA; V _{CC} = 2.3 V | V _{CC} - 0.6 | V _{CC} - 0.26 | - | V |
| | | I _O = -12 mA; V _{CC} = 2.7 V | V _{CC} - 0.5 | V _{CC} - 0.14 | - | V |
| | | I _O = -12 mA; V _{CC} = 3.0 V | V _{CC} - 0.6 | V _{CC} - 0.09 | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | |
| | | I _O = 100 μA; V _{CC} = 2.3 V to 3.6 V | - | GND | 0.20 | V |
| | | I _O = 6 mA; V _{CC} = 2.3 V | - | 0.07 | 0.40 | V |
| | | I _O = 12 mA; V _{CC} = 2.3 V | - | 0.15 | 0.70 | V |
| | | I _O = 12 mA; V _{CC} = 2.7 V | - | 0.14 | 0.40 | V |
| I _I | input leakage current | I _O = 24 mA; V _{CC} = 3.0 V | - | 0.27 | 0.55 | V |
| | | V _{CC} = 2.3 V to 3.6 V; V _I = V _{CC} or GND | - | 0.1 | 5 | μA |
| I _{OZ} | OFF-state output current | V _{CC} = 2.3 V to 3.6 V; V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND | - | 0.1 | 10 | μA |

| Symbol | Parameter | Conditions | Min | Typ ^[1] | Max | Unit |
|-----------------|---------------------------------|---|------|--------------------|-----|---------------|
| I_{CC} | supply current | $V_{CC} = 2.3\text{ V to }3.6\text{ V}; V_I = V_{CC}\text{ or GND}; I_O = 0\text{ A}$ | - | 0.2 | 40 | μA |
| ΔI_{CC} | additional supply current | 74ALVCH16245; per data I/O pin; $V_{CC} = 2.3\text{ V to }3.6\text{ V}; V_I = V_{CC} - 0.6\text{ V}; I_O = 0\text{ A}$ | - | 150 | 750 | μA |
| I_{BHL} | bus hold LOW current | $V_{CC} = 2.3\text{ V}; V_I = 0.7\text{ V}$ ^[2] | 45 | - | - | μA |
| | | $V_{CC} = 3.0\text{ V}; V_I = 0.8\text{ V}$ ^[2] | 75 | 150 | - | μA |
| I_{BHH} | bus hold HIGH current | $V_{CC} = 2.3\text{ V}; V_I = 1.7\text{ V}$ ^[2] | -45 | - | - | μA |
| | | $V_{CC} = 3.0\text{ V}; V_I = 2.0\text{ V}$ ^[2] | -75 | -175 | - | μA |
| I_{BHLO} | bus hold LOW overdrive current | $V_{CC} = 3.6\text{ V}$ ^[2] | 500 | - | - | μA |
| I_{BHHO} | bus hold HIGH overdrive current | $V_{CC} = 3.6\text{ V}$ ^[2] | -500 | - | - | μA |
| C_I | input capacitance | | - | 4.0 | - | pF |
| $C_{I/O}$ | input/output capacitance | | - | 8.0 | - | pF |

[1] All typical values are measured at $T_{amb} = 25\text{ }^\circ\text{C}$.

[2] Valid for data inputs of bushold parts.

10 Dynamic characteristics

Table 7. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 8](#).

| Symbol | Parameter | Conditions | Min | Typ ^[1] | Max | Unit |
|---|-------------------------------|---|-----|--------------------|-----|------|
| T_{amb} = -40 °C to +85 °C | | | | | | |
| t _{pd} | propagation delay | nAn to nBn; nBn to nAn; see Figure 6 ^[2] | | | | |
| | | V _{CC} = 2.3 V to 2.7 V | 1.0 | 2.0 | 3.7 | ns |
| | | V _{CC} = 2.7 V | 1.0 | 2.1 | 3.6 | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 1.0 | 1.9 | 3.0 | ns |
| t _{en} | enable time | n $\overline{\text{OE}}$ to nAn; n $\overline{\text{OE}}$ to nBn; see Figure 7 ^[3] | | | | |
| | | V _{CC} = 2.3 V to 2.7 V | 1.0 | 2.7 | 5.7 | ns |
| | | V _{CC} = 2.7 V | 1.0 | 3.0 | 5.4 | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 1.0 | 2.3 | 4.4 | ns |
| t _{dis} | disable time | n $\overline{\text{OE}}$ to nAn; n $\overline{\text{OE}}$ to nBn; see Figure 7 ^[4] | | | | |
| | | V _{CC} = 2.3 V to 2.7 V | 1.0 | 2.2 | 5.2 | ns |
| | | V _{CC} = 2.7 V | 1.0 | 3.1 | 4.6 | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 1.0 | 2.8 | 4.1 | ns |
| C _{PD} | power dissipation capacitance | per buffer; V _I = GND to V _{CC} ^[5] | | | | |
| | | outputs enabled | - | 29 | - | pF |
| | | outputs disabled | - | 5 | - | pF |

[1] Typical values are measured at T_{amb} = 25 °C

Typical values for V_{CC} = 2.3 V to 2.7 V are measured at V_{CC} = 2.5 V.

Typical values for V_{CC} = 3.0 V to 3.6 V are measured at V_{CC} = 3.3 V.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] t_{en} is the same as t_{PZL} and t_{PZH}.

[4] t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in Volts;

N = total load switching outputs;

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

10.1 Waveforms and test circuit



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 6. Input (nAn, nBn) to output (nBn, nAn) propagation delay times



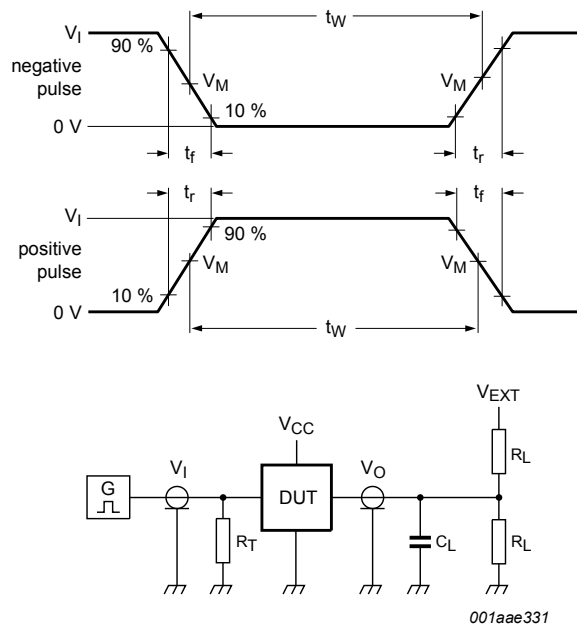
Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 7. 3-state enable and disable times

Table 8. Measurement points

| Supply voltage | Input | Output | | |
|---------------------|---------------------|---------------------|--------------------------|--------------------------|
| V_{CC} | V_M | V_M | V_X | V_Y |
| $< 2.7\text{ V}$ | $0.5 \times V_{CC}$ | $0.5 \times V_{CC}$ | $V_{OL} + 0.15\text{ V}$ | $V_{OH} - 0.15\text{ V}$ |
| $\geq 2.7\text{ V}$ | 1.5 V | 1.5 V | $V_{OL} + 0.3\text{ V}$ | $V_{OH} - 0.3\text{ V}$ |



Test data is given in [Table 9](#).

Definitions test circuit:

R_L = Load resistance.

C_L = Load capacitance includes jig and probe capacitance.

R_T = Termination resistance should be equal to Z_0 of pulse generator.

V_{EXT} = Test voltage for switching times.

Figure 8. Test circuit for measuring switching times

Table 9. Test data

| Supply voltage | Input | | Load | | V_{EXT} | | |
|----------------|----------|---------------|-------|--------------|--------------------|--------------------|--------------------|
| V_{CC} | V_I | t_r, t_f | C_L | R_L | t_{PLH}, t_{PHL} | t_{PHZ}, t_{PZH} | t_{PLZ}, t_{PZL} |
| < 2.7 V | V_{CC} | ≤ 2.0 ns | 30 pF | 500 Ω | open | GND | $2 \times V_{CC}$ |
| 2.7 V to 3.6 V | 2.7 V | ≤ 2.5 ns | 50 pF | 500 Ω | open | GND | $2 \times V_{CC}$ |

11 Package outline

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm

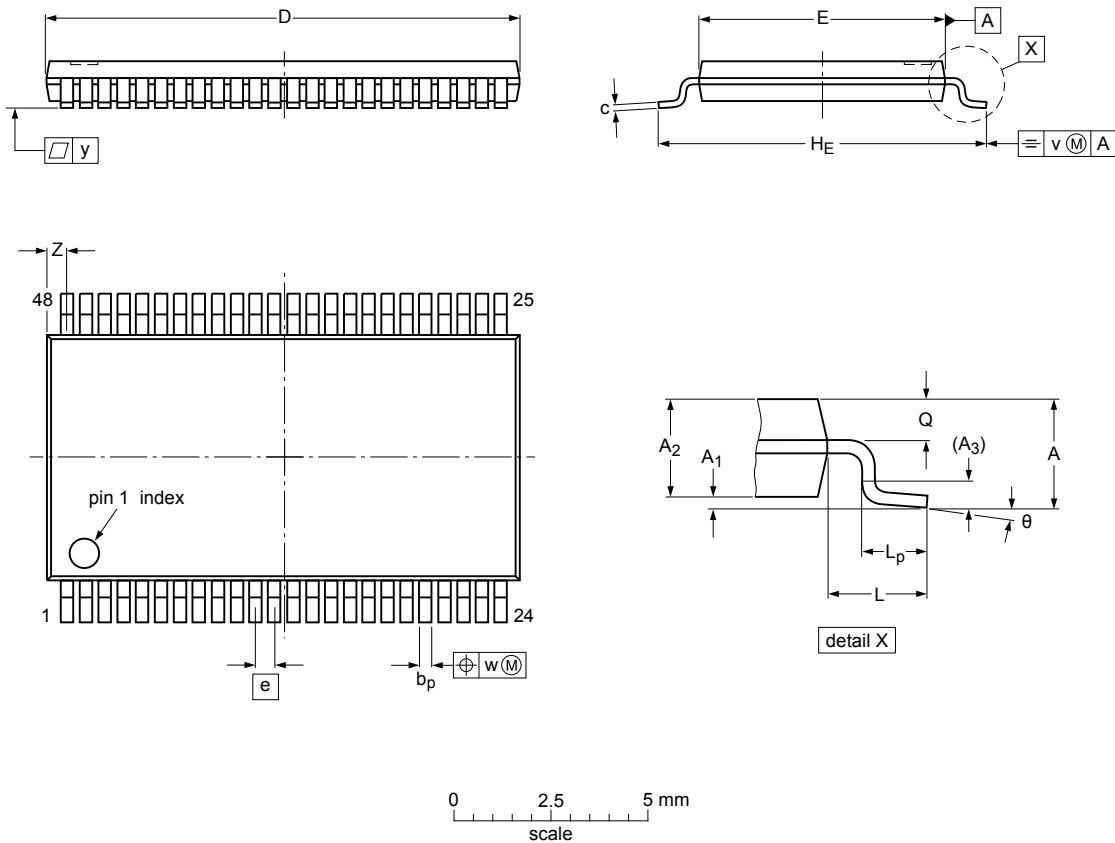
SOT370-1



Figure 9. Package outline SOT370-1 (SSOP48)

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1



Dimensions (mm are the original dimensions)

| Unit | A | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽²⁾ | e | H _E | L | L _p | Q | v | w | y | Z | θ |
|------|-----|----------------|----------------|----------------|----------------|-----|------------------|------------------|-----|----------------|---|----------------|------|------|------|-----|-----|----|
| max | | 0.15 | 1.05 | | 0.28 | 0.2 | 12.6 | 6.2 | | 8.3 | | 0.8 | 0.50 | | | | 0.8 | 8° |
| nom | 1.2 | | | 0.25 | | | | | 0.5 | | 1 | | | 0.25 | 0.08 | 0.1 | | |
| min | | 0.05 | 0.85 | | 0.17 | 0.1 | 12.4 | 6.0 | | 7.9 | | 0.4 | 0.35 | | | | 0.4 | 0° |

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot362-1_po

| Outline version | References | | | | European projection | Issue date |
|-----------------|------------|--------|-------|--|---------------------|----------------------|
| | IEC | JEDEC | JEITA | | | |
| SOT362-1 | | MO-153 | | | | 03-02-19 13-08-05 |

Figure 10. Package outline SOT362-1 (TSSOP48)

12 Abbreviations

Table 10. Abbreviations

| Acronym | Description |
|---------|---|
| CDM | Charged Device Model |
| CMOS | Complementary Metal-Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| TTL | Transistor-Transistor Logic |

13 Revision history

Table 11. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|----------------------------------|--|---------------------------|---------------|--|
| 74ALVC_ALVCH16245 v.4 | 20171121 | Product data sheet | - | 74ALVC_ALVCH16245 v.3 |
| Modifications: | <ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. | | | |
| 74ALVC_ALVCH16245 v.3 | 20040512 | Product data sheet | - | 74ALVCH16245 v.2 74ALVC16245_ 74ALVCH16245 v.1 |
| Modifications: | <ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the current presentation and information standard of Philips Semiconductors. Section 1: General description updated. | | | |
| 74ALVCH16245 v.2 | 19980629 | Product specification | - | 74ALVCH16245 v.1 |
| 74ALVC16245_ 74ALVCH16245 v.1 | 19980325 | Product specification | - | - |
| 74ALVCH16245 v.1 | 19950102 | Preliminary specification | - | - |

14 Legal information

14.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
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[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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