Power management integrated circuit (PMIC) for i.MX 7 & i.MX 6SL/SX/UL

PF3000

POWER MANAGEMENT

EP SUFFIX
98ASA00719D
48 QFN 7.0 X 7.0

ES SUFFIX
98ASA00933D
48 QFN 7.0 X 7.0

The PF3000 is a power management integrated circuit (PMIC) designed specifically for use with the NXP i.MX 7 and i.MX 6SL/SX/UL application processors. With up to four buck converters, six linear regulators, RTC supply, and coin-cell charger, the PF3000 can provide power for a complete system, including applications processors, memory, and system peripherals. This device is powered by SMARTMOS technology.

Features:

- Four adjustable high efficiency buck regulators: 1.75 A, 1.5 A, 1.25 A, 1.0 A
  - Selectable modes: PWM, PFM, APS
- 5.0 V, 600 mA boost regulator with PFM or auto mode
- Six adjustable general purpose linear regulators
- Input voltage range: 2.8 V to 4.5 V or 3.7 V to 5.5 V
- OTP (One Time Programmable) memory for device configuration
  - Programmable start-up sequence and timing
  - Selectable output voltage, frequency, soft start
- I^2C control
- Coin cell charger and always ON RTC supply
- DDR reference voltage
- -40 °C to +125 °C operating junction temperature

Applications:

- Tablets
- eReaders
- Wearables
- POS terminals
- Industrial control
- Medical monitoring
- Home automation
- Home security/energy management

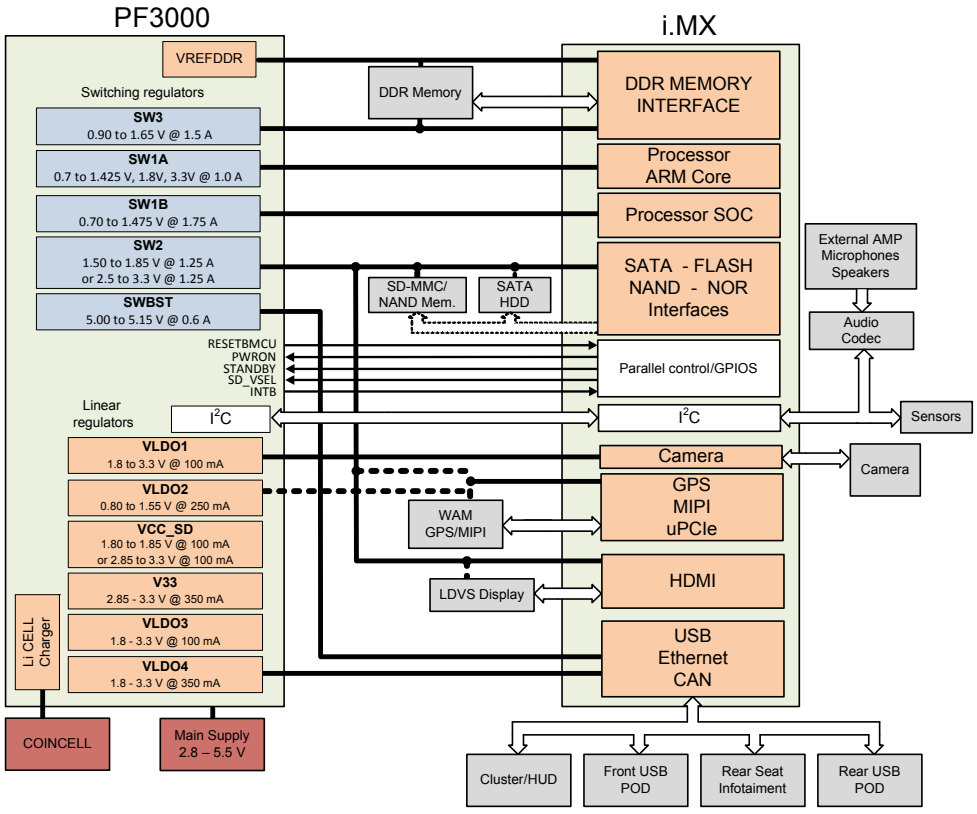

Figure 1. PF3000 Simplified Application Diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

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1 Orderable parts

The PF3000 is available with pre-programmed OTP memory configurations. The devices are identified using the program codes from Table 1. Details of the OTP programming for each device can be found in Table 42.

Table 1. Orderable part variations

Part number	Temperature (T_A)	Package	Programming options	Notes
MC32PF3000A0EP	-40 °C to 85 °C (For use in Consumer applications)	98ASA00719D, 48 QFN 7.0 mm x 7.0 mm with exposed pad	0 - Not programmed	(1), (2)
MC32PF3000A1EP			1 (i.MX 7 with DDR3L)	
MC32PF3000A2EP			2 (i.MX 7 with LPDDR3)	
MC32PF3000A3EP			3 (i.MX 6SX with DDR3L)	
MC32PF3000A4EP			4 (i.MX 6SX with DDR3)	
MC32PF3000A5EP			5 (i.MX 6SL with LPDDR2)	
MC32PF3000A6EP			6 (i.MX 6UL with LPDDR2)	
MC32PF3000A7EP			7 (i.MX 6UL with DDR3L)	
MC32PF3000A8EP			8 (i.MX 6UL with DDR3)	
MC33PF3000A0ES	-40 °C to 105 °C (For use in Automotive applications)	98ASA00933D, 48 QFN 7.0 mm x 7.0 mm WF-type (wettable flank)	0 - Not programmed	(1), (2)
MC33PF3000A3ES			3 (i.MX 6SX with DDR3L)	
MC33PF3000A4ES			4 (i.MX 6SX with DDR3)	
MC33PF3000A5ES			5 (i.MX 6SL with LPDDR2)	
MC33PF3000A6ES			6 (i.MX 6UL with LPDDR2)	
MC33PF3000A7ES			7 (i.MX 6UL with DDR3L)	
MC34PF3000A0EP	-40 °C to 105 °C (For use in Industrial applications)	98ASA00719D, 48 QFN 7.0 mm x 7.0 mm with exposed pad	0 - Not programmed	(1), (2)
MC34PF3000A1EP			1 (i.MX 7 with DDR3L)	
MC34PF3000A2EP			2 (i.MX 7 with LPDDR3)	
MC34PF3000A3EP			3 (i.MX 6SX with DDR3L)	
MC34PF3000A4EP			4 (i.MX 6SX with DDR3)	
MC34PF3000A5EP			5 (i.MX 6SL with LPDDR2)	
MC34PF3000A6EP			6 (i.MX 6UL with LPDDR2)	
MC34PF3000A7EP			7 (i.MX 6UL with DDR3L)	
MC34PF3000A8EP			8 (i.MX 6UL with DDR3)	

Notes
1. For tape and reel, add an R2 suffix to the part number.
2. The programming options specified in this table are reference for customer application. The part number selection should match the board power tree design. Table 42 provides details of the OTP programming for each device.

2 General description

The PF3000 is the power management integrated circuit (PMIC) designed primarily for use with NXP's i.MX 7 series of multi-media application processors. It is also capable of providing full power solution to i.MX 6SL/SX/UL processors.

2.1 Features

This section summarizes the PF3000 features.

- Input voltage range to PMIC: 2.8 V to 4.5 V, or 3.7 V to 5.5 V [(3)]
  - Buck regulators
    - Configurable three to four channels
    - SW1A/B, 2.75 A (single); 0.7 V to 1.425 V, 1.8 V, 3.3 V
    - SW1A, 1.0 A (independent); 0.7 V to 1.425 V, 1.8 V, 3.3 V
    - SW1B 1.75 A (independent); 0.7 V to 1.475 V
    - SW2, 1.25 A; 1.50 V to 1.85 V or 2.50 V to 3.30 V
    - SW3, 1.5 A; 0.90 V to 1.65 V
    - Dynamic voltage scaling
    - Modes: PWM, PFM, APS
    - Programmable output voltage
    - Programmable current limit
    - Programmable soft start sequence
    - Programmable PWM switching frequency
  - Boost regulator
    - SWBST, 5.0 to 5.15 V, 0.6 A, OTG support
    - Modes: PFM and Auto
    - OCP fault interrupt
  - LDOs
    - VCC_SD, 1.8 V to 1.85 V or 2.85 V to 3.30 V, 100 mA based on SD_VSEL
    - V33, 2.85 V to 3.30 V, 350 mA
    - VLDO1, 1.8 V to 3.3 V, 100 mA
    - VLDO2, 0.80 V to 1.55 V, 250 mA
    - VLDO3, 1.8 V to 3.3 V, 100 mA
    - VLDO4, 1.8 V to 3.3 V, 350 mA
- Always ON RTC Regulator/Switch VSNVS 3.0 V, 1.0 mA
- DDR memory reference voltage, VREFDDR, 0.5 V to 0.9 V, 10 mA
- OTP (One time programmable) memory for device configuration, user-programmable start-up sequence and timing
- Battery backed memory including coin cell charger
- I^2C interface
- User programmable standby, sleep/LPSR, and Off modes

Notes

3. 2.8 V to 4.5 V when VIN is used at input. 3.7 V to 5.5 V when VPWR is used as input.

2.2 Functional block diagram

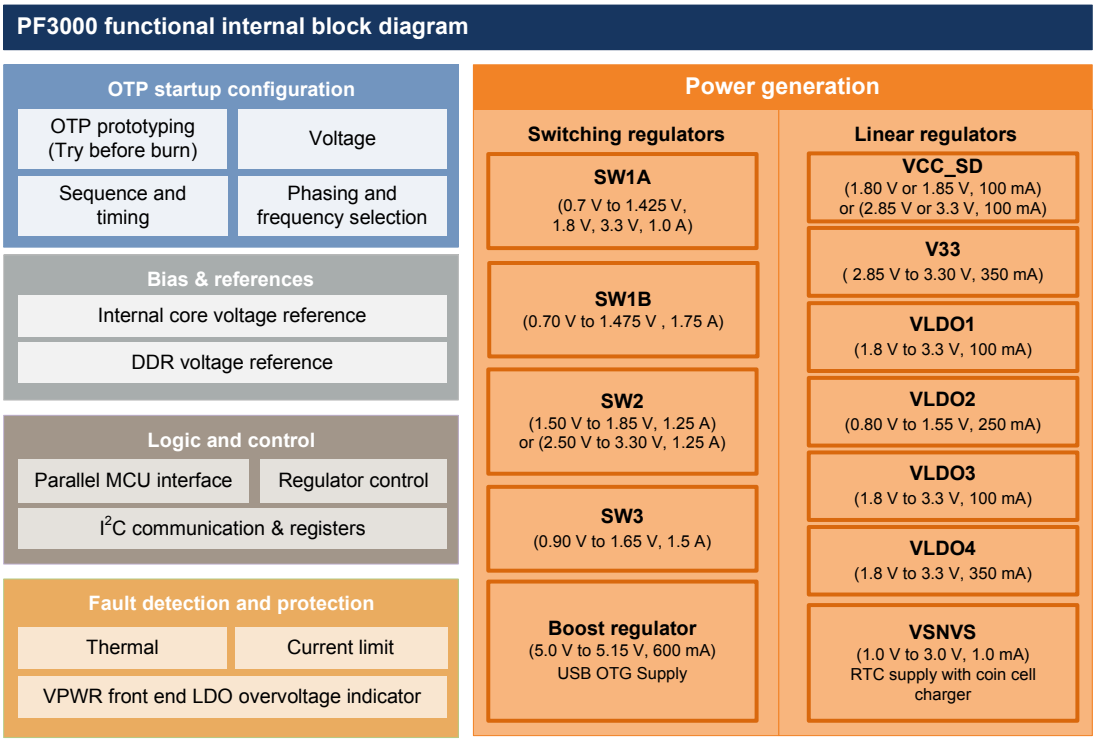


Figure 2. Functional block diagram

3 Internal block diagram

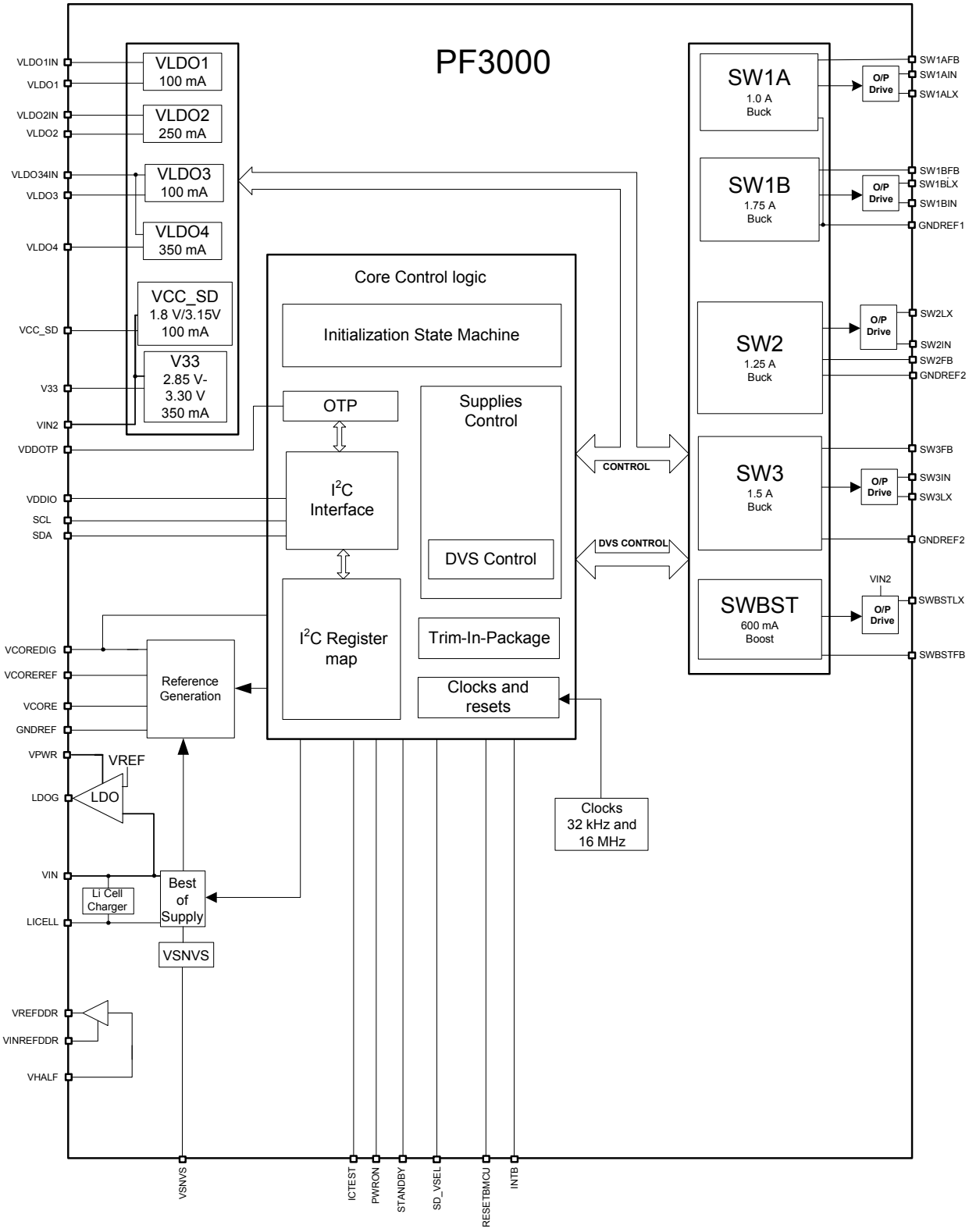


Figure 3. PF3000 simplified internal block diagram

4 Pin connections

4.1 Pinout diagram

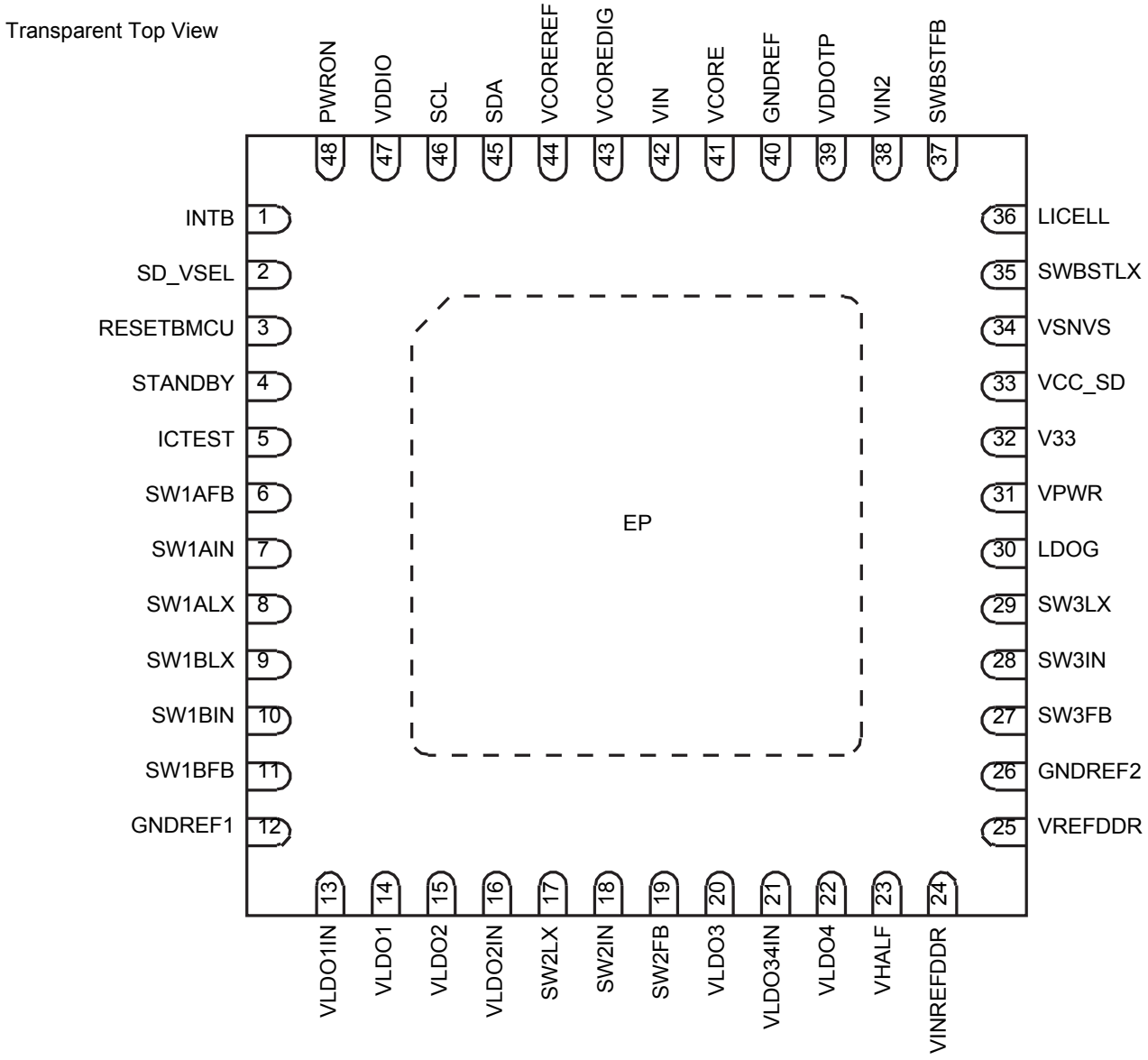


Figure 4. Pinout diagram

4.2 Pin definitions

Table 2. Pin definitions

Pin number	Pin name	Pin function	Type	Definition
1	INTB	O	Digital	Open drain interrupt signal to processor
2	SD_VSEL	I/O	Digital	Input from i.MX processor to select VCC_SD regulator voltage • SD_VSEL=0, VCC_SD = 2.85 V to 3.3 V • SD_VSEL= 1, VCC_SD = 1.8 V to 1.85 V
3	RESETBMCU	O	Digital	Open drain reset output to processor
4	STANDBY	I	Digital	Standby input signal from processor
5	ICTEST	I	Digital and Analog	Reserved pin. Connect to GND in application
6	SW1AFB (4)	I	Analog	SW1A output voltage feedback pin. Route this trace separately from the high current path and terminate at the output capacitance or near the load, if possible for best regulation
7	SW1AIN (4)	I	Analog	Input to SW1A regulator. Bypass with at least a 4.7 µF ceramic capacitor and a 0.1 µF decoupling capacitor as close to the pin as possible
8	SW1ALX (4)	O	Analog	Switcher 1A switch node connection. Connect to SW1A inductor when used in SW1A independent mode. Connect to SW1BLX and connect to SW1AB inductor when using SW1A/B as a single regulator
9	SW1BLX (4)	O	Analog	Switcher 1B switch node connection. Connect to SW1B inductor when used in SW1B independent mode. Connect to SW1ALX and connect to SW1AB inductor when using SW1A/B as a single regulator
10	SW1BIN (4)	I	Analog	Input to SW1B regulator. Bypass with at least a 4.7 µF ceramic capacitor and a 0.1 µF decoupling capacitor as close to the pin as possible
11	SW1BFB (4)	I	Analog	SW1B output voltage feedback pin. Route this trace separately from the high current path and terminate at the output capacitor or near the load, if possible for best regulation
12	GNDREF1	GND	GND	Ground reference for SW1A/B. Connect to GND. Keep away from high current ground return paths
13	VLDO1IN	I	Analog	VLDO1 input supply. Bypass with a 1.0 µF decoupling capacitor as close to the pin as possible
14	VLDO1	O	Analog	VLDO1 regulator output. Bypass with a 2.2 µF ceramic output capacitor
15	VLDO2	O	Analog	VLDO2 regulator output. Bypass with a 4.7 µF ceramic output capacitor
16	VLDO2IN	I	Analog	VLDO2 input supply. Bypass with a 1.0 µF decoupling capacitor as close to the pin as possible
17	SW2LX (4)	O	Analog	Switcher 2 switch node connection.Connect to SW2 inductor
18	SW2IN (4)	I	Analog	Input to SW2 regulator. Bypass with at least a 4.7 µF ceramic capacitor and a 0.1 µF decoupling capacitor as close to the pin as possible
19	SW2FB (4)	I	Analog	SW2 output voltage feedback pin. Route this trace separately from the high current path and terminate at the output capacitor or near the load, if possible for best regulation
20	VLDO3	O	Analog	VLDO3 regulator output. Bypass with a 2.2 µF ceramic output capacitor
21	VLDO34IN	I	Analog	VLDO3 and VLDO4 input supply. Bypass with a 1.0 µF decoupling capacitor as close to the pin as possible
22	VLDO4	O	Analog	VLDO4 regulator output. Bypass with a 2.2 µF ceramic output capacitor
23	VHALF	I	Analog	Half supply reference for VREFDDR. Bypass with 0.1 µF to ground.
24	VINREFDDR	I	Analog	VREFDDR regulator input. Connect a 0.1 µF capacitor between VINREFDDR and VHALF pin. Ensure there is at least 1.0 µF net capacitance from VINREFDDR to ground
25	VREFDDR	O	Analog	VREFDDR regulator output.Bypass with 1.0 µF to ground

Table 2. Pin definitions (continued)

26	GNDREF2	GND	GND	Reference ground for SW2 and SW3 regulators. Connect to GND. Keep away from high current ground return paths
27	SW3FB (4)	I	Analog	SW3 output voltage feedback pin. Route this trace separately from the high current path and terminate at the output capacitor or near the load, if possible for best regulation
28	SW3IN (4)	I	Analog	Input to SW3 regulator. Bypass with at least a 4.7 µF ceramic capacitor and a 0.1 µF decoupling capacitor as close to the pin as possible
29	SW3LX (4)	O	Analog	Switcher 3 switch node connection. Connect the SW3 inductor
30	LDOG	O	Analog	Connect to gate of front-end LDO external pass P-MOSFET. Leave floating if VPWR LDO is not used
31	VPWR	I	Analog	Input to optional front-end VPWR LDO for systems with input voltage > 4.5 V
32	V33	O	Analog	V33 regulator output. Bypass with a 4.7 µF ceramic output capacitor
33	VCC_SD	O	Analog	Output of VCC_SD regulator. Bypass with a 2.2 µF ceramic output capacitor.
34	VSNVS	O	Analog	VSNVS regulator/switch output. Bypass with 0.47 µF capacitor to ground.
35	SWBSTLX (4)	I/O	Analog	SWBST switch node connection. Connect to SWBST inductor and anode of Schottky diode
36	LICELL	I/O	Analog	Coin cell supply input/output. Bypass with 0.1 µF capacitor. Connect to optional coin cell.
37	SWBSTFB (4)	I	Analog	SWBST output voltage feedback pin. Route this trace separately from the high current path and terminate at the output capacitor
38	VIN2	I	Analog	Input to VCC_SD, V33 regulators and SWBST control circuitry. Connect to VIN rail and bypass with 10 µF capacitor
39	VDDOTP	I	Digital & Analog	Supply to program OTP fuses. Connect VDDOTP to GND during normal application
40	GNDREF	GND	GND	Ground reference for IC core circuitry. Connect to ground. Keep away from high current ground return paths
41	VCORE	O	Analog	Internal analog core supply. Bypass with 1 µF capacitor to ground
42	VIN	I	Analog	Main IC supply. Bypass with 1.0 µF capacitor to ground. Connect to system input supply if voltage ≤ 4.5 V. Connect to drain of external PFET when VPWR LDO is used for systems with input voltage > 4.5 V
43	VCOREDIG	O	Analog	Internal digital core supply. Bypass with 1.0 µF capacitor to ground
44	VCOREREF	O	Analog	Main band gap reference. Bypass with 220 nF capacitor to ground
45	SDA	I/O	Digital	I^2C data line (open drain). Pull up to VDDIO with a 4.7 kΩ resistor
46	SCL	I	Digital	I^2C clock. Pull up to VDDIO with a 4.7 kΩ resistor
47	VDDIO	I	Analog	Supply for I^2C bus. Bypass with 0.1 µF ceramic capacitor. Connect to 1.7 to 3.6 V supply. Ensure that VDDIO is always lesser than or equal to VIN
48	PWRON	I	Digital	Power ON/OFF input from processor
-	EP	GND	GND	Expose pad. Functions as ground return for buck and boost regulators. Tie this pad to the inner and external ground planes through vias to allow effective thermal dissipation

Notes

4. Unused switching regulators should be connected as follows: Pins SWxLX and SWxFB should be unconnected and Pin SWxIN should be connected to VIN with a 0.1 µF bypass capacitor.

5 General product characteristics

5.1 Absolute maximum ratings

Table 3. Absolute maximum voltage ratings

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause malfunction or permanent damage to the device. The detailed maximum voltage rating per pin can be found in the pin list section.

Symbol	Description	Value	Unit	Notes
Electrical ratings				
VPWR, ICTEST, LDOG, SWBSTLX	–	-0.3 to 7.5	V	
VIN, VIN2, VLDO1IN, SW1AIN, SW1BIN, SW2IN, SW3IN, SW1ALX, SW1BLX, SW2LX, SW3LX	–	-0.3 to 4.8	V	
VDDOTP	OTP programming input supply voltage	-0.3 to 10.0	V	(5)
SWBSTFB	Boost switcher feedback	-0.3 to 5.5	V	
INTB, SD_VSEL, RESETBMCU, STANDBY, SW1AFB, SW1BFB, SW2FB, SW3FB, VLDO1, VLDO2IN, VLDO3, VLDO34IN, VLDO4, VHALF, VINREFDDR, VREFDDR, V33, VCC_SD, VSNVS, LICELL, VCORE, SDA, SCL, VDDIO, PWRON	–	-0.3 to 3.6	V	
VLDO2	VLDO2 linear regulator output	-0.3 to 2.5	V	
VCOREDIG	Digital core supply voltage output	-0.3 to 1.65	V	
VCOREREF	Bandgap reference voltage output	-0.3 to 1.5	V	
V_{ESD}	ESD ratings • Human body model • Charge device model	 ±2000 ±500	V	(6)

Notes

5. 10 V maximum voltage rating during OTP fuse programming. 7.5 V maximum DC voltage rated otherwise.
6. ESD testing is performed in accordance with the human body model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), and the charge device model (CDM), robotic (C_{ZAP} = 4.0 pF).

5.2 Thermal Characteristics

Table 4. Thermal ratings

Symbol	Description (rating)	Min.	Max.	Unit	Notes
Thermal Ratings					
T_A	Ambient operating temperature range • Industrial version • Consumer version	 -40 -40	 105 85	°C	
T_J	Operating junction temperature range	-40	125	°C	(7)
T_{ST}	Storage temperature range	-65	150	°C	
T_{PPRT}	Peak package reflow temperature	–	(9)	°C	(8) (9)
QFN48 thermal resistance and package dissipation ratings					
$R_{\theta JA}$	Junction to ambient, natural convection • Four layer board (2s2p) • Eight layer board (2s6p)	 – –	 24 15	°C/W	(10) (11) (12)
$R_{\theta JB}$	Junction to board	–	11	°C/W	(13)
$R_{\Theta JCBOTTOM}$	Junction to case bottom	–	1.4	°C/W	(14)
ΨJT	Junction to package top • Natural convection	–	1.3	°C/W	(15)

Notes

7. Do not operate beyond 125 °C for extended periods of time. Operation above 150 °C may cause permanent damage to the IC. See Thermal Protection Thresholds for thermal protection features.
8. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause a malfunction or permanent damage to the device.
9. NXP's package reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For peak package reflow temperature and moisture sensitivity levels (MSL), go to www.nxp.com, search by part number (remove prefixes/suffixes) and enter the core ID to view all orderable parts, and review parametrics.
10. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
11. The Board uses the JEDEC specifications for thermal testing (and simulation) JESD51-7 and JESD51-5.
12. Per JEDEC JESD51-6 with the board horizontal.
13. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
14. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
15. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters (Ψ) are not available, the thermal characterization parameter is written as Psi-JT.

5.3 Current consumption

The current consumption of the individual blocks is described in detail in the following table.

Table 5. Current consumption summary

T_A= -40 °C to 105 °C, V_{PWR}= 0 V (External pass FET is not populated), V_{IN} = 3.6 V, V_{DDIO} = 1.7 V to 3.6 V, L_{ICELL} = 1.8 V to 3.3 V, V_{SNVS} = 3.0 V, typical external component values, unless otherwise noted. Typical values are characterized at VIN = 3.6 V, V_{PWR} = 0 V, V_{DDIO} = 3.3 V, L_{ICELL} = 3.0 V, V_{SNVS} = 3.0 V and 25 °C, unless otherwise noted.

Mode	PF3000 conditions	System conditions	Typ.	Max.	Unit	Notes
Coin cell	VSNVS from LICELL, All other blocks off, V_{IN} = 0.0 V	No load on VSNVS	4.0	7.0	µA	(16) (17)
Off	VSNVS from VIN or LICELL Wake-up from PWRON active 32 kHz RC on All other blocks off VIN ≥ UVDET	No load on VSNVS, PMIC able to wake-up	16	25	µA	(16) (17)
Sleep LPSR	VSNVS from VIN Wake-up from PWRON active Trimmed reference active SW3 PFM. All other regulators off. Trimmed 16 MHz RC off 32 kHz RC on VREFDDR disabled	No load on any of the regulators.	130 (16) 200 (19)	220 (16)	µA	(18)
	LDO1 & LDO3 activated in addition to SW3	No load on any of the regulators.	170 (16) 260 (19)	248 (16)	µA	(18)
Standby	VSNVS from either VIN or LICELL SW1A in PFM SW1B in PFM SW2 in PFM SW3 in PFM SWBST off Trimmed 16 MHz RC enabled Trimmed reference active VLDO1-4 enabled V33 enabled VCC_SD enabled VREFDDR enabled	No load on any of the regulators.	297	450	µA	(18)
ON	VSNVS from VIN SW1A in APS SW1B in APS SW2 in APS SW3 in APS SWBST off Trimmed 16 MHz RC enabled Trimmed reference active VLDO1-4 enabled V33 enabled VCC_SD enabled VREFDDR enabled	No load on any of the regulators.	1.2		mA	

Notes

16. At 25 °C only.
17. When V_{IN} is below the UVDET threshold, in the range of 1.8 V ≤ V_{IN} < 2.65 V, the quiescent current increases by 50 µA, typically.
18. For PFM operation, headroom should be 300 mV or greater.
19. At 105 °C only.

5.4 Electrical characteristics

Table 6. Electrical characteristics – front-end input LDO

All parameters are specified at T_A = -40 °C to 105 °C, V_{PWR} = 5.0 V, V_{IN} = 4.4 V, I_{VIN} = 300 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{PWR} = 5.0 V, V_{IN} = 4.4 V, I_{VIN} = 300 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Front end input LDO (VPWR LDO)						
V_{PWR}	Operating input voltage • In regulation • In dropout operation	 4.6 3.7	 – –	 5.5 4.6	V	(20)
V_{IN}	On mode output voltage, 4.6 V < V_{PWR} < 5.5 V, 0.0 mA < I_{VIN} < 3000 mA	4.3	4.4	4.55	V	
I_{VIN}	Operating load current at VIN, 3.7 V < V_{PWR} < 5.5 V	0.0	–	3.0	A	
I_{LDOGQ}	ON mode quiescent current, no load,	–	5.0	10	mA	
V_{IN}	Low-power mode output voltage, 4.6 V < V_{PWR} < 5.5 V 0.0 mA < I_{VIN} < 1.0 mA	3.7		4.5	V	
V_{IN_OFF}	Off mode output voltage, (CL = 100 µF) 4.6 V < V_{PWR} < 5.5 V, 0.0 mA < I_{VIN} < 35 µA	3.2		4.8	V	
I_{LDOQLP}	Low-power mode quiescent current, no load (Standby/Sleep/LPSR states)	–	150	300	µA	
V_{PWRUV}	VPWR undervoltage threshold (upon undervoltage condition the external pass FET is turned off)	3.1	–	3.7	V	
V_{PWROV}	VPWR overvoltage threshold (upon overvoltage condition interrupt is asserted at INTB)	5.5	–	6.5	V	
$I_{VINUVILIMIT}$	VPWR LDO current limit under VIN short-circuit (V_{IN} < UVDET)	–	–	300	mA	
$I_{VINLEAKAGE}$	Reverse leakage current from VIN to VPWR, No external pass FET, VPWR is grounded, device is in OFF state	–	–	1.0	µA	
$I_{VPWROFF}$	VPWR LDO Off mode quiescent current	–	–	75	µA	(21)

Notes

20. While the front end LDO can handle spikes up to 7.5 V at VPWR for as long as 200 µs, the circuit is not expected to be continuously operated when VPWR is above 5.5 V.
21. This specification gives the leakage current in the VPWR LDO block. Total OFF mode current includes the quiescent current from the other blocks as specified in Table 5.

Table 7. Static electrical characteristics – SW1

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = V_{SW1xIN} = 3.6 V, V_{SW1x} = 1.2 V, I_{SW1x} = 100 mA, typical external component values, f_{SW1x} = 2.0 MHz, unless otherwise noted. Typical values are characterized at V_{IN} = V_{SW1xIN} = 3.6 V, V_{SW1x} = 1.2 V, I_{SW1x} = 100 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Switch mode supply SW1A/B (single phase)						
V_{SW1AIN} V_{SW1BIN}	Operating input voltage	2.8	–	4.5	V	(22), (23)
V_{SW1AB}	Nominal output voltage	–	Table 53	–	V	
$V_{SW1ABACC}$	Output voltage accuracy • PWM, APS, 2.8 V < V_{SW1xIN} < 4.5 V, 0 < I_{SW1AB} < 2.75 A 0.7 V ≤ V_{SW1AB} ≤ 1.2 V • PFM, APS, 2.8 V < V_{SW1xIN} < 4.5 V, 0 < I_{SW1AB} < 2.75A 1.225 V < V_{SW1AB} < 1.425 V • PFM, steady state, 2.8 V < V_{SW1xIN} < 4.5 V, 0 < I_{SW1AB} < 150 mA 1.8 V ≤ V_{SW1AB} ≤ 1.425 V • PWM, APS, 2.8 V < V_{SW1xIN} < 4.5 V, 0 < I_{SW1AB} < 2.75A 1.8 V < V_{SW1AB} < 3.3 V • PFM, steady state, 2.8 V < V_{SW1xIN} < 4.5 V, 0 < I_{SW1AB} < 150 mA 1.8 V ≤ V_{SW1AB} ≤ 3.3 V	 -25 -25 -45 -6.0 -6.0	 – 	 25 35 45 6.0 6.0	 mV mV mV % %	
I_{SW1AB}	Rated output load current, • 2.8 V ≤ V_{SW1xIN} ≤ 4.5 V, 0.7 V < V_{SW1AB} < 1.425 V, 1.8V, 3.3V	2750	–	–	mA	
I_{SW1ABQ}	Quiescent current • PFM mode • APS mode	 – –	 22 300	 – –	 µA	
$I_{SW1ABLIM}$	Current limiter peak current detection , current through inductor • SW1xILIM = 0 • SW1xILIM = 1	 3.5 2.6	 5.5 4.0	 7.5 5.4	 A	
ΔV_{SW1AB}	Output ripple	–	5.0	–	mV	
$R_{SW1ABDIS}$	Discharge resistance	–	600	–	Ω	
Switch mode supply SW1A (independent)						
V_{SW1AIN}	Operating input voltage	2.8	–	4.5	V	(22), (23)
V_{SW1A}	Nominal output voltage	–	Table 53	–	V	
$V_{SW1AACC}$	Output voltage accuracy • PWM, APS, 2.8 V < V_{SW1AIN} < 4.5 V, 0 < I_{SW1A} < 1.0 A 0.7 V ≤ V_{SW1A} ≤ 1.2 V • APS, 3.0 V ≤ V_{SW1AIN} ≤ 3.6 V, 0.01 A < I_{SW1A} < 0.75 A V_{SW1A} = 1.225 V, T_A = 0 °C to 85 °C • PWM, APS, 2.8 V < V_{SW1AIN} < 4.5 V, 0 < I_{SW1A} < 1.0 A 1.225 V < V_{SW1A} ≤ 1.425 V • PFM, steady state, 2.8 V < V_{SW1AIN} < 4.5 V, 0 < I_{SW1A} < 50 mA 0.7 V ≤ V_{SW1A} ≤ 1.425V • PWM, APS, 2.8 V < V_{SW1AIN} < 4.5 V, 0 < I_{SW1A} < 1.0 A 1.8 V ≤ V_{SW1A} ≤ 3.3 V • PFM, steady state, 2.8 V < V_{SW1AIN} < 4.5 V, 0 < I_{SW1A} < 50 mA 1.8 V ≤ V_{SW1A} ≤ 3.3 V	 -25 -25 -25 -45 -6.0 -6.0	 – 	 25 25 35 45 6.0 6.0	 mV mV mV mV % %	
I_{SW1A}	Rated output load current 2.8 V < V_{SW1AIN} < 4.5 V, 0.7 V < V_{SW1A} < 1.425 V, 1.8V, 3.3V	1000	–	–	mA	
Switch mode supply SW1a (independent) (Continued)						
I_{SW1AQ}	Quiescent current • PFM mode • APS mode	 – –	 50 250	 – –	 µA	

Table 7. Static electrical characteristics – SW1 (continued)

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = V_{SW1xIN} = 3.6 V, V_{SW1x} = 1.2 V, I_{SW1x} = 100 mA, typical external component values, f_{SW1x} = 2.0 MHz, unless otherwise noted. Typical values are characterized at V_{IN} = V_{SW1xIN} = 3.6 V, V_{SW1x} = 1.2 V, I_{SW1x} = 100 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
$I_{SW1ALIM}$	Current limiter peak current detection, current through inductor • SW1AILIM = 0 • SW1AILIM = 1	 1.78 1.3	 2.75 2.0	 3.7 2.7	A	
ΔV_{SW1A}	Output Ripple	–	5.0	–	mV	
$R_{ONSW1AP}$	SW1A P-MOSFET R_{DSON}, at V_{SW1AIN} = 3.3 V	–	265	295	mΩ	
$R_{ONSW1AN}$	SW1A N-MOSFET R_{DSON}, at V_{SW1AIN} = 3.3 V	–	300	370	mΩ	
I_{SW1APQ}	SW1A P-MOSFET leakage current, V_{SW1AIN} = 4.5 V	–	–	10.5	µA	
I_{SW1ANQ}	SW1A N-MOSFET leakage current, V_{SW1AIN} = 4.5 V	–	–	3.5	µA	
$R_{SW1ADIS}$	Discharge resistance	–	600	–	Ω	
Switch mode supply SW1B (independent)						
V_{SW1BIN}	Operating input voltage	2.8	–	4.5	V	(24), (25)
V_{SW1B}	Nominal output voltage	–	Table 53	–	V	
$V_{SW1BACC}$	Output voltage accuracy • PWM, APS, 2.8 V < V_{SW1BIN} < 4.5 V, 0 < I_{SW1B} < 1.75 A 0.7 V < V_{SW1B} < 1.2 V • PWM, APS, 2.8 V < V_{SW1BIN} < 4.5 V, 0 < I_{SW1B} < 1.75 A 1.225 V < V_{SW1B} < 1.475 V • PFM, steady state 2.8 V < V_{SW1BIN} < 4.5 V, 0 < I_{SW1B} < 50 mA 0.7 V < V_{SW1B} < 1.475 V	 -25 -25 -45	 – 	 25 35 45	mV	
I_{SW1B}	Rated output load current 2.8 V < V_{SW1BIN} < 4.5 V, 0.7 V < V_{SW1B} < 1.475 V	1750	–	–	mA	
I_{SW1BQ}	Quiescent current • PFM mode • APS mode	 – –	 50 150	 – –	µA	
$I_{SW1BLIM}$	Current limiter peak current detection, current through inductor • SW1BILIM = 0 • SW1BILIM = 1	 2.4 1.725	 3.50 2.65	 4.725 3.575	A	
ΔV_{SW1B}	Output ripple	–	5.0	–	mV	
$R_{ONSW1BP}$	SW1B P-MOSFET R_{DSON}, at V_{SW1BIN} = 3.3 V	–	195	225	mΩ	
$R_{ONSW1BN}$	SW1B N-MOSFET R_{DSON}, at V_{SW1BIN} = 3.3 V	–	228	295	mΩ	
I_{SW1BPQ}	SW1B P-MOSFET leakage current, V_{SW1BIN} = 4.5 V	–	–	12	µA	
I_{SW1BNQ}	SW1B N-MOSFET leakage current, V_{SW1BIN} = 4.5 V	–	–	4.0	µA	
$R_{SW1BDIS}$	Discharge resistance during OFF mode	–	600	–	Ω	

Notes

22. The maximum operating input voltage is 4.55 V when VPWR LDO is used.
23. Minimum operating voltage is 2.8 V with a valid LICELL voltage (1.8 V to 3.3 V). Minimum operating voltage is 3.1 V when no voltage is applied at the LICELL pin. If operation down to 2.8 V is required for systems without a coin cell, connect the LICELL pin to any system voltage between 1.8 V and 3.3 V. This voltage can be an output from any PF3000 regulator, or external system supply.
24. The maximum operating input voltage is 4.55 V when VPWR LDO is used.
25. Minimum operating voltage is 2.8 V with a valid LICELL voltage (1.8 V to 3.3 V). Minimum operating voltage is 3.1 V when no voltage is applied at the LICELL pin. If operation down to 2.8 V is required for systems without a coin cell, connect the LICELL pin to any system voltage between 1.8 V and 3.3 V. This voltage can be an output from any PF3000 regulator, or external system supply.

Table 8. Dynamic electrical characteristics - SW1

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = V_{SW1xIN} = 3.6 V, V_{SW1x} = 1.2 V, I_{SW1x} = 100 mA, typical external component values, f_{SW1x} = 2.0 MHz, unless otherwise noted. Typical values are characterized at V_{IN} = V_{SW1xIN} = 3.6 V, V_{SW1x} = 1.2 V, I_{SW1x} = 100 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Switch mode supply SW1A/B (single phase)						
$V_{SW1ABOSH}$	Start-up overshoot, I_{SW1AB} = 0 mA, DVS clk = 25 mV/4 µs, V_{IN} = V_{SW1xIN} = 4.5 V, V_{SW1AB} = 1.425 V	–	–	66	mV	
$t_{ONSW1AB}$	Turn-on time, enable to 90% of end value, I_{SW1AB} = 0 mA, DVS clk = 25 mV/4 µs, V_{IN} = V_{SW1xIN} = 4.5 V, V_{SW1AB} = 1.425 V	–	–	500	µs	
Switch mode supply SW1A (independent)						
$V_{SW1AOSH}$	Start-up overshoot, ISW1A = 0 mA, DVS clk = 25 mV/4.0 µs, V_{IN} = V_{SW1AIN} = 4.5 V, V_{SW1A} = 1.425 V	–	–	66	mV	
t_{ONSW1A}	Turn-on time, enable to 90% of end value, I_{SW1A} = 0 mA, DVS clk = 25 mV/4.0 µs, V_{IN} = V_{SW1AIN} = 4.5 V, V_{SW1A} = 1.425 V	–	–	500	µs	
Switch mode supply SW1B (independent)						
$V_{SW1BOSH}$	Start-up overshoot, I_{SW1B} = 0 mA, DVS clk = 25 mV/4.0 µs, V_{IN} = V_{SW1BIN} = 4.5 V, V_{SW1B} = 1.475 V	–	–	66	mV	
t_{ONSW1B}	Turn-on time, enable to 90% of end value, I_{SW1B} = 0 mA, DVS clk = 25 mV/4 µs, V_{IN} = V_{SW1BIN} = 4.5 V, V_{SW1B} = 1.475 V	–	–	500	µs	

Table 9. Static electrical characteristics – SW2

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = V_{SW2IN} = 3.6 V, V_{SW2} = 3.15 V, I_{SW2} = 100 mA, typical external component values, f_{SW2} = 2.0 MHz, unless otherwise noted. Typical values are characterized at V_{IN} = V_{SW2IN} = 3.6 V, V_{SW2} = 3.15 V, I_{SW2} = 100 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Switch mode supply SW2						
V_{SW2IN}	Operating input voltage	2.8	–	4.5	V	(26), (27)
V_{SW2}	Nominal output voltage	–	Table 55	–	V	
V_{SW2ACC}	Output voltage accuracy • PWM, APS, 2.8 V ≤ V_{SW2IN} ≤ 4.5 V, 0 ≤ I_{SW2} ≤ 1.25 A • 1.50 V ≤ V_{SW2} ≤ 1.85 V • 2.5 V ≤ V_{SW2} ≤ 3.3 V • PFM, 2.8 V ≤ V_{SW2IN} ≤ 4.5 V, 0 ≤ I_{SW2} ≤ 50 mA • 1.50 V ≤ V_{SW2} ≤ 1.85 V • 2.5 V ≤ V_{SW2} ≤ 3.3 V	 -3.0% -6.0% -6.0% -6.0%	 – – – –	 3.0% 6.0% 6.0% 6.0%	%	
I_{SW2}	Rated output load current, 2.8 V < V_{SW2IN} < 4.5 V, 1.50 V < V_{SW2} < 1.85 V, 2.5 V < V_{SW2} < 3.3 V	1250	–	–	mA	(28)
I_{SW2Q}	Quiescent current • PFM mode • APS mode (low output voltage settings) • APS mode (high output voltage settings, SW2_HI=1)	 – – –	 23 145 305	 – – –	µA	

Notes

26. The maximum operating input voltage is 4.55 V when VPWR LDO is used.
27. Minimum operating voltage is 2.8 V with a valid LICELL voltage (1.8 V to 3.3 V). Minimum operating voltage is 3.1 V when no voltage is applied at the LICELL pin. If operation down to 2.8 V is required for systems without a coin cell, connect the LICELL pin to any system voltage between 1.8 V and 3.3 V. This voltage can be an output from any PF3000 regulator, or external system supply.
28. The higher output voltages available depend on the voltage drop in the conduction path as given by the following equation: (V_{SW2IN} - V_{SW2}) = I_{SW2}* (DCR of Inductor +R_{ONSW2P} + PCB trace resistance).

Table 9. Static electrical characteristics – SW2 (continued)

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = V_{SW2IN} = 3.6 V, V_{SW2} = 3.15 V, I_{SW2} = 100 mA, typical external component values, f_{SW2} = 2.0 MHz, unless otherwise noted. Typical values are characterized at V_{IN} = V_{SW2IN} = 3.6 V, V_{SW2} = 3.15 V, I_{SW2} = 100 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Switch mode supply SW2 (continued)						
I_{SW2LIM}	Current limiter peak current detection, current through inductor • SW2ILIM = 0 • SW2ILIM = 1	 1.625 1.235	 2.5 1.9	 3.375 2.565	A	
ΔV_{SW2}	Output ripple	–	5.0	–	mV	
R_{ONSW2P}	SW2 P-MOSFET R_{DSON} at V_{IN} = V_{SW2IN} = 3.3 V	–	215	245	mΩ	
R_{ONSW2N}	SW2 N-MOSFET R_{DSON} at V_{SW2IN} = V_{SW2IN} = 3.3 V	–	258	326	mΩ	
I_{SW2PQ}	SW2 P-MOSFET leakage current, V_{IN} = V_{SW2IN} = 4.5 V	–	–	10.5	µA	
I_{SW2NQ}	SW2 N-MOSFET leakage current, V_{IN} = V_{SW2IN} = 4.5 V	–	–	3.0	µA	
R_{SW2DIS}	Discharge resistance during OFF mode	–	600	–	Ω	

Table 10. Dynamic electrical characteristics - SW2

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = V_{SW2IN} = 3.6 V, V_{SW2} = 3.15 V, ISW2 = 100 mA, typical external component values, f_{SW2} = 2.0 MHz, unless otherwise noted. Typical values are characterized at V_{IN} = V_{SW2IN} = 3.6 V, V_{SW2} = 3.15 V, I_{SW2} = 100 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Switch mode supply SW2						
V_{SW2OSH}	Start-up overshoot, I_{SW2} = 0.0 mA, DVS clk = 25 mV/4 µs, V_{IN} = V_{SW2IN} = 4.5 V	–	–	66	mV	
t_{ONSW2}	Turn-on time, enable to 90% of end value, I_{SW2} = 0.0 mA, DVS clk = 25 mV/4 µs, V_{IN} = V_{SW2IN} = 4.5 V	–	–	500	µs	

Table 11. Static electrical characteristics – SW3

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = V_{SW3IN} = 3.6 V, V_{SW3} = 1.5 V, I_{SW3} = 100 mA, typical external component values, f_{SW3} = 2.0 MHz. Typical values are characterized at V_{IN} = V_{SW3IN} = 3.6 V, V_{SW3} = 1.5 V, I_{SW3} = 100 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Switch mode supply SW3						
V_{SW3IN}	Operating input voltage	2.8	–	4.5	V	(29), (30)
V_{SW3}	Nominal output voltage	–	Table 57	–	V	
V_{SW3ACC}	Output voltage accuracy • PWM, APS, 2.8 V < V_{SW3IN} < 4.5 V, 0 < I_{SW3} < 1.5 A, 0.9 V < V_{SW3} < 1.65 V • PFM, steady state (2.8 V < V_{SW3IN} < 4.5 V, 0 < I_{SW3} < 50 mA), 0.9 V < V_{SW3} < 1.65 V	 -3.0% -6.0%	 – –	 3.0% 6.0%	%	
I_{SW3}	Rated output load current, 2.8 V < V_{SW3IN} < 4.5 V, 0.9 V < V_{SW3} < 1.65 V, PWM, APS mode	1500	–	–	mA	(31)

Notes

29. The maximum operating input voltage is 4.55 V when VPWR LDO is used.
30. Minimum operating voltage is 2.8 V with a valid LICELL voltage (1.8 V to 3.3 V). Minimum operating voltage is 3.1 V when no voltage is applied at the LICELL pin. If operation down to 2.8 V is required for systems without a coin cell, connect the LICELL pin to any system voltage between 1.8 V and 3.3 V. This voltage can be an output from any PF3000 regulator, or external system supply.
31. The higher output voltages available depend on the voltage drop in the conduction path as given by the following equation: (V_{SW3IN} - V_{SW3}) = I_{SW3}* (DCR of Inductor +R_{ONSW3P} + PCB trace resistance).

Table 11. Static electrical characteristics – SW3 (continued)

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = V_{SW3IN} = 3.6 V, V_{SW3} = 1.5 V, I_{SW3} = 100 mA, typical external component values, f_{SW3} = 2.0 MHz. Typical values are characterized at V_{IN} = V_{SW3IN} = 3.6 V, V_{SW3} = 1.5 V, I_{SW3} = 100 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Switch mode supply SW3 (continued)						
I_{SW3Q}	Quiescent current • PFM mode • APS mode	 – –	 50 150	 – –	µA	
I_{SW3LIM}	Current limiter peak current detection, current through inductor • SW3ILIM = 0 • SW3ILIM = 1	 1.95 1.45	 3.0 2.25	 4.05 3.05	A	
ΔV_{SW3}	Output ripple	–	5.0	–	mV	
R_{ONSW3P}	SW3 P-MOSFET R_{DSON} at V_{IN} = V_{SW3IN} = 3.3 V	–	205	235	mΩ	
R_{ONSW3N}	SW3 N-MOSFET R_{DSON} at V_{IN} = V_{SW3IN} = 3.3 V	–	250	315	mΩ	
I_{SW3PQ}	SW3 P-MOSFET leakage current, V_{IN} = V_{SW3IN} = 4.5 V	–	–	12	µA	
I_{SW3NQ}	SW3 N-MOSFET leakage current, V_{IN} = V_{SW3IN} = 4.5 V	–	–	4.0	µA	
R_{SW3DIS}	Discharge resistance during Off mode	–	600	–	Ω	

Table 12. Dynamic electrical characteristics - SW3

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = V_{SW3IN} = 3.6 V, V_{SW3} = 1.5 V, I_{SW3} = 100 mA, typical external component values, f_{SW3} = 2.0 MHz. Typical values are characterized at V_{IN} = V_{SW3IN} = 3.6 V, V_{SW3} = 1.5 V, I_{SW3} = 100 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
V_{SW3OSH}	Start-up overshoot, I_{SW3} = 0.0 mA, DVS clk = 25 mV/4 µs, V_{IN} = V_{SW3IN} = 4.5 V	–	–	66	mV	
t_{ONSW3}	Turn-on time, enable to 90% of end value, I_{SW3} = 0 mA, DVS clk = 25 mV/4 µs, V_{IN} = V_{SW3IN} = 4.5 V	–	–	500	µs	

Table 13. Static electrical characteristics - SWBST

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = $V_{SWBSTIN}$ = 3.6 V, V_{SWBST} = 5.0 V, I_{SWBST} = 100 mA, typical external component values, f_{SWBST} = 2.0 MHz, otherwise noted. Typical values are characterized at V_{IN} = $V_{SWBSTIN}$ = 3.6 V, V_{SWBST} = 5.0 V, I_{SWBST} = 100 mA, and 25 °C, unless otherwise noted.

Symbol	Parameters	Min.	Typ.	Max.	Unit	Notes
Switch mode supply SWBST						
$V_{SWBSTIN}$	Input voltage range	2.8	–	4.5	V	(32), (33)
V_{SWBST}	Nominal output voltage	–	Table 59	–	V	
I_{SWBST}	Continuous load current • 2.8 V ≤ V_{IN} ≤ 3.0 V • 3.0 V ≤ V_{IN} ≤ 4.5 V	 500 600	 – –	 – –	mA	
$V_{SWBSTACC}$	Output voltage accuracy, 2.8 V ≤ V_{IN} ≤ 4.5 V, 0 < I_{SWBST} < $I_{SWBSTMAX}$	-4.0	–	3.0	%	
I_{SWBSTQ}	Quiescent current (auto mode)	–	222	289	µA	

Notes

32. The maximum operating input voltage is 4.55 V when VPWR LDO is used.
33. Minimum operating voltage is 2.8 V with a valid LICELL voltage (1.8 V to 3.3 V). Minimum operating voltage is 3.1 V when no voltage is applied at the LICELL pin. If operation down to 2.8 V is required for systems without a coin cell, connect the LICELL pin to any system voltage between 1.8 V and 3.3 V. This voltage can be an output from any PF3000 regulator, or external system supply.

Table 13. Static electrical characteristics - SWBST (continued)

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = $V_{SWBSTIN}$ = 3.6 V, V_{SWBST} = 5.0 V, I_{SWBST} = 100 mA, typical external component values, f_{SWBST} = 2.0 MHz, otherwise noted. Typical values are characterized at V_{IN} = $V_{SWBSTIN}$ = 3.6 V, V_{SWBST} = 5.0 V, I_{SWBST} = 100 mA, and 25 °C, unless otherwise noted.

Symbol	Parameters	Min.	Typ.	Max.	Unit	Notes
Switch mode supply SWBST (continued)						
ΔV_{SWBST}	Output ripple, 2.8 V ≤ V_{IN} ≤ 4.5 V, 0 < I_{SWBST} < $I_{SWBSTMAX}$, excluding reverse recovery of Schottky diode	–	–	120	mVp-p	
$I_{SWBSTLIM}$	Peak Current Limit	1400	2200	3200	mA	(34)
$R_{DS(on)BST}$	MOSFET on resistance	–	206	306	mΩ	
$I_{SWBSTHSQ}$	NMOS Off leakage, V_{SWBST} = 4.5 V, SWBSTMODE [1:0] = 00	–	1.0	5.0	µA	

Notes

34. Only in Auto and APS modes.

Table 14. Dynamic electrical characteristics - SWBST

All parameters are specified at T_A = -40 °C to 105 °C, VIN = $V_{SWBSTIN}$ = 3.6 V, V_{SWBST} = 5.0 V, I_{SWBST} = 100 mA, typical external component values, f_{SWBST} = 2.0 MHz, otherwise noted. Typical values are characterized at V_{IN} = $V_{SWBSTIN}$ = 3.6 V, V_{SWBST} = 5.0 V, I_{SWBST} = 100 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Switch mode supply SWBST						
$V_{SWBSTOSH}$	Start-up overshoot, I_{SWBST} = 0.0 mA	–	–	500	mV	
$t_{ONSWBST}$	Turn-on time, enable to 90% of VSWBST, ISWBST = 0.0 mA	–	–	2.0	ms	

Table 15. Static electrical characteristics - VSNVS

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, V_{SNVS} = 3.0 V, I_{SNVS} = 5.0 µA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V_{SNVS} = 3.0 V, I_{SNVS} = 5.0 µA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VSNVS						
V_{IN}	Operating input voltage • Valid coin cell range • Valid V_{IN}	 1.8 2.25	 – –	 3.3 4.5	V	(35)
I_{SNVS}	Operating load current, V_{INMIN} < V_{IN} < V_{INMAX}	1.0	–	1000	µA	
V_{SNVS}	Output voltage • 5.0 µA < I_{SNVS} < 1000 µA (OFF), 3.20 V < V_{IN} < 4.5 V • 5.0 µA < I_{SNVS} < 1000 µA (ON), 3.20 V < V_{IN} < 4.5 V • 5.0 µA < I_{SNVS} < 1000µA (Coin cell mode), 2.84 V < V_{COIN} < 3.3 V	 -5.0% -5.0% V_{COIN}-0.10	 3.0 3.0 –	 7.0% 5.0% V_{COIN}	V	
$V_{SNVSDROP}$	Dropout voltage, 2.85 V < V_{IN} < 2.9 V, 1.0 µA < I_{SNVS} < 1000 µA	–	–	110	mV	
$I_{SNVSLIM}$	Current limit, V_{IN} > V_{TH1}	1100	–	6750	µA	
VSNVS DC, SWITCH						
V_{LiCell}	Operating input voltage, valid coin cell range	1.8	–	3.3	V	
I_{SNVS}	Operating load current	1.0	–	1000	µA	
$R_{DS(on)SNVS}$	Internal switch $R_{DS(on)}$, V_{COIN} = 2.6 V	–	–	100	Ω	

Notes

35. The maximum operating input voltage is 4.55 V when VPWR LDO is used

Table 16. Dynamic electrical characteristics - VSNVS

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, V_{SNVS} = 3.0 V, I_{SNVS} = 5.0 µA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V_{SNVS} = 3.0 V, I_{SNVS} = 5.0 µA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VSNVS						
$V_{SNVSTON}$	Turn-on time (load capacitor, 0.47 µF), from V_{IN} = V_{TH1} to 90% of V_{SNVS}, V_{COIN} = 0.0 V, I_{SNVS} = 5.0 µA	–	–	24	ms	(36),(37)
$V_{SNVSOSH}$	Start-up overshoot, I_{SNVS} = 5.0 µA	–	40	70	mV	
$V_{SNVSLOTR}$	Transient load response, 3.2 < V_{IN} ≤ 4.5 V, I_{SNVS} = 100 to 1000 µA	2.8	–	–	V	
V_{TL1}	V_{IN} falling threshold (V_{IN} powered to coin cell powered)	2.45	2.70	3.05	V	
V_{TH1}	V_{IN} rising threshold (coin cell powered to V_{IN} powered)	2.50	2.75	3.10	V	
V_{HYST1}	V_{IN} threshold hysteresis for V_{TH1}-V_{TL1}	5.0	–	–	mV	
$V_{SNVSCROSS}$	Output voltage during crossover, V_{COIN} > 2.9 V, Switch to LDO: V_{IN} > V_{TH1}, I_{SNVS} = 100 µA, LDO to Switch: V_{IN} < V_{TL1}, I_{SNVS} = 100 µA	2.45	–	–	V	

Notes

36. The start-up of V_{SNVS} is not monotonic. It first rises to 1.0 V and then settles to 3.0 V.
37. From coin cell insertion to V_{SNVS} = 1.0 V, the delay time is typically 400 ms.

Table 17. Static electrical characteristics - VLDO1

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, V_{LDO1IN} = 3.6 V, V_{LDO1} = 3.3 V, I_{LDO1} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V_{LDO1IN} = 3.6 V, V_{LDO1} = 3.3 V, I_{LDO1} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VLDO1 linear regulator						
V_{LDO1IN}	Operating input voltage • 1.8 V ≤ $V_{LDO1NOM}$ ≤ 2.5 V • 2.6 V ≤ $V_{LDO1NOM}$ ≤ 3.3 V	2.8 $V_{LDO1NOM}$ +0.250	– –	4.5 4.5	V	(38), (39)
$V_{LDO1NOM}$	Nominal output voltage	–	Table 62	–	V	
I_{LDO1}	Rated output load current	100	–	–	mA	
$V_{LDO1TOL}$	Output voltage tolerance, $V_{LDO1INMIN}$ < V_{LDO1IN} < 4.5 V, 0.0 mA < I_{LDO1} < 100 mA, VLDO1 = 1.8 V to 3.3 V	-3.0	–	3.0	%	
I_{LDO1Q}	Quiescent current, no load, change in $I_{VIN,}$ when VLDO1 enabled	–	13	–	µA	
$I_{LDO1LIM}$	Current limit, I_{LDO1} when V_{LDO1} is forced to $V_{LDO1NOM}$/2	122	167	280	mA	

Notes

38. The maximum operating input voltage is 4.55 V when VPWR LDO is used.
39. Minimum operating voltage is 2.8 V with a valid LICELL voltage (1.8 V to 3.3 V). Minimum operating voltage is 3.1 V when no voltage is applied at the LICELL pin. If operation down to 2.8 V is required for systems without a coin cell, connect the LICELL pin to any system voltage between 1.8 V and 3.3 V. This voltage can be an output from any PF3000 regulator, or external system supply.

Table 18. Dynamic electrical characteristics - VLDO1

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, V_{LDO1IN} = 3.6 V, V_{LDO1} = 3.3 V, I_{LDO1} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V_{LDO1IN} = 3.6 V, V_{LDO1} = 3.3 V, I_{LDO1} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VLDO1 linear regulator						
$PSRR_{VLDO1}$	PSRR, I_{LDO1} = 75 mA, 20 Hz to 20 kHz • VLDO1 = 1.8 V to 3.3 V, V_{LDO1IN} = $V_{LDO1INMIN}$ + 100 mV • VLDO1 = 1.8 V to 3.3 V, V_{LDO1IN} = $V_{LDO1NOM}$ + 1.0 V	 35 52	 40 60	 – –	dB	
$NOISE_{VLDO1}$	Output noise density, V_{LDO1IN} = $V_{LDO1INMIN}$, I_{LDO1} = 75 mA • 100 Hz to <1.0 kHz • 1.0 kHz to <10 kHz • 10 kHz to 1.0 MHz	 – – –	 -114 -129 -135	 -102 -123 -130	dBV/ √Hz	
t_{ONLDO1}	Turn-on time, enable to 90% of end value, V_{LDO1IN} = $V_{LDO1INMIN}$ to 4.5 V, I_{LDO1} = 0.0 mA, all output voltage settings	60	–	500	µs	
$t_{OFFLDO1}$	Turn-off time, disable to 10% of initial value, V_{LDO1IN} = $V_{LDO1INMIN}$, I_{LDO1} = 0.0 mA	–	–	10	ms	
$LDO1_{OSHT}$	Start-up overshoot, V_{LDO1IN} = $V_{LDO1INMIN}$ to 4.5 V, I_{LDO1} = 0.0 mA	–	1.0	2.0	%	

Table 19. Static electrical characteristics - VLDO2

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, V_{LDO2IN} = 3.0 V, V_{LDO2} = 1.55 V, I_{LDO2} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V_{LDO2IN} = 3.0 V, V_{LDO2} = 1.55 V, I_{LDO2} = 10 mA and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VLDO2 linear regulator						
V_{LDO2IN}	Operating input voltage	1.75	–	3.40	V	
$V_{LDO2NOM}$	Nominal output voltage	–	Table 63	–	V	
I_{LDO2}	Rated output load current	250	–	–	mA	
$V_{LDO2TOL}$	Output voltage tolerance, 1.75 V < V_{LDOIN1} < 3.40 V, 0.0 mA < I_{LDO2} < 250 mA, VLDO2 = 0.8 V to 1.55 V	-3.0	–	3.0	%	
I_{LDO2Q}	Quiescent current, no load, change in I_{VIN} and $I_{VLDO2IN}$, when V_{LDO2} enabled	–	16	–	µA	
$I_{LDO2LIM}$	Current limit, I_{LDO2} when V_{LDO2} is forced to $V_{LDO2NOM}$/2	333	417	612	mA	

Table 20. Dynamic electrical characteristics - VLDO2

All parameters are specified at TA = -40 °C to 105 °C, VIN = 3.6 V, V_{LDO2IN} = 3.0 V, V_{LDO2} = 1.55 V, I_{LDO2} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V_{LDO2IN} = 3.0 V, V_{LDO2} = 1.55 V, I_{LDO2} = 10 mA and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VLDO2 linear regulator						
$PSRR_{VLDO2}$	PSRR, I_{LDO2} = 187.5 mA, 20 Hz to 20 kHz • VLDO2 = 0.8 V to 1.55 V • VLDO2 = 1.1 V to 1.55 V	 50 37	 60 45	 – –	dB	
$NOISE_{VLDO2}$	Output noise density, V_{LDO2IN} = 1.75 V, I_{LDO2} = 187.5 mA • 100 Hz to <1.0 kHz • 1.0 kHz to <10 kHz • 10 kHz to 1.0 MHz	 – – –	 -108 -118 -124	 -100 -108 -112	dBV/√Hz	

Table 20. Dynamic electrical characteristics - VLDO2 (continued)

All parameters are specified at TA = -40 °C to 105 °C, VIN = 3.6 V, V_{LDO2IN} = 3.0 V, V_{LDO2} = 1.55 V, I_{LDO2} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V_{LDO2IN} = 3.0 V, V_{LDO2} = 1.55 V, I_{LDO2} = 10 mA and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VLDO2 linear regulator (continue)						
t_{ONLDO2}	Turn-on time, enable to 90% of end value, V_{LDO2IN} = 1.75 V to 3.4 V, I_{LDO2} = 0.0 mA	60	–	500	µs	
$t_{OFFLDO2}$	Turn-off time, disable to 10% of initial value, V_{LDO2IN} = 1.75 V, I_{LDO2} = 0.0 mA	–	–	10	ms	
$LDO2_{OSHT}$	Start-up overshoot, V_{LDO2IN} = 1.75 V to 3.4 V, I_{LDO2} = 0.0 mA	–	1.0	2.0	%	

Table 21. Static electrical characteristics – VCC_SD

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, VCC_SD = 1.85 V, I_{VCC_SD} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, VCC_SD = 1.85 V, I_{VCC_SD} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VCC_SD linear regulator						
V_{IN}	Operating input voltage	2.8	–	4.5	V	(40), (41), (41)
V_{CC_SDNOM}	Nominal output voltage	–	Table 65	–	V	
I_{VCC_SD}	Rated output load current	100	–	–	mA	
V_{CC_SDTOL}	Output voltage accuracy, 2.8 V < V_{IN} < 4.5 V, 0.0 mA < I_{VCC_SD} < 100 mA, VCC_SD[1:0] = 00 to 11	-3.0	–	3.0	%	
I_{VCC_SDQ}	Quiescent current, no load, change in I_{VIN} and I_{VIN2}, when V_{CC_SD} enabled	–	13	–	µA	
I_{VCC_SDLIM}	Current limit, I_{VCC_SD} when V_{CC_SD} is forced to V_{CC_SDNOM}/2	122	167	280	mA	

Notes

40. When the LDO output voltage is set above 2.6 V, the minimum allowed input voltage needs to be at least the output voltage plus 0.25 V.
41. The maximum operating input voltage is 4.55 V when VPWR LDO is used.
42. Minimum operating voltage is 2.8 V with a valid LICELL voltage (1.8 V to 3.3 V). Minimum operating voltage is 3.1 V when no voltage is applied at the LICELL pin. If operation down to 2.8 V is required for systems without a coin cell, connect the LICELL pin to any system voltage between 1.8 V and 3.3 V. This voltage can be an output from any PF3000 regulator, or external system supply.

Table 22. Dynamic electrical characteristics - VCC_SD

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, VCC_SD = 1.85 V, IVCC_SD = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, VCC_SD = 1.85 V, IVCC_SD = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VCC_SD linear regulator						
$PSRR_{VCC_SD}$	PSRR, I_{VCC_SD} = 75 mA, 20 Hz to 20 kHz • VCC_SD[1:0] = 00 - 10, V_{IN} = 2.8 V + 100 mV • VCC_SD[1:0] = 10 - 11, V_{IN} = V_{CC_SDNOM} + 1.0 V	 35 52	 40 60	 – –	dB	
$NOISE_{VCC_SD}$	Output noise density, V_{IN} = 2.8V, I_{VCC_SD} = 75 mA • 100 Hz – <1.0 kHz • 1.0 kHz – <10 kHz • 10 kHz – 1.0 MHz	 – – –	 -114 -129 -135	 -102 -123 -130	dBV/√Hz	
t_{ONVCC_SD}	Turn-on time, enable to 90% of end value, V_{IN} = 2.8 V to 4.5 V, I_{VCC_SD} = 0.0 mA	60	–	500	µs	

Table 22. Dynamic electrical characteristics - VCC_SD (continued)

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, VCC_SD = 1.85 V, IVCC_SD = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, VCC_SD = 1.85 V, IVCC_SD = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VCC_SD linear regulator (continued)						
t_{OFFVCC_SD}	Turn-off time, disable to 10% of initial value, V_{IN} = 2.8 V, I_{VCC_SD} = 0.0 mA	–	–	10	ms	
VCC_SD_{OSHT}	Start-up overshoot, V_{IN} = 2.8 V to 4.5 V, I_{VCC_SD} = 0.0 mA	–	1.0	2.0	%	

Table 23. Static electrical characteristics – V33

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, V_{33} = 3.3 V, I_{V33} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V_{33} = 3.3 V, I_{V33} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
V33 linear regulator						
V_{IN}	Operating input voltage, 2.9 V ≤ V_{33NOM} ≤ 3.6 V	2.8	–	4.5	V	(43), (44), (45)
V_{33NOM}	Nominal output voltage	–	Table 64	–	V	
I_{V33}	Rated output load current	350	–	–	mA	
V_{33TOL}	Output voltage tolerance, 2.8 V < V_{IN} < 4.5 V, 0.0 mA < I_{V33} < 350 mA, V_{33}[1:0] = 00 to 11	-3.0	–	3.0	%	
I_{V33Q}	Quiescent current, no load, change in I_{VIN}, when V_{33} enabled	–	13	–	µA	
I_{V33LIM}	Current limit, I_{V33} when V_{33} is forced to V_{33NOM}/2	435	584.5	950	mA	

Notes

43. When the LDO output voltage is set above 2.6 V the minimum allowed input voltage need to be at least the output voltage plus 0.25 V for proper regulation due to the dropout voltage generated through the internal LDO transistor.
44. The maximum operating input voltage is 4.55 V when VPWR LDO is used.
45. Minimum operating voltage is 2.8 V with a valid LICELL voltage (1.8 V to 3.3 V). Minimum operating voltage is 3.1 V when no voltage is applied at the LICELL pin. If operation down to 2.8 V is required for systems without a coin cell, connect the LICELL pin to any system voltage between 1.8 V and 3.3 V. This voltage can be an output from any PF3000 regulator, or external system supply.

Table 24. Dynamic electrical characteristics – V33

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, V_{33} = 3.3 V, I_{V33} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V_{33} = 3.3 V, I_{V33} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
V33 linear regulator						
$PSRR_{V33}$	PSRR, I_{V33} = 262.5 mA, 20 Hz to 20 kHz, V_{33}[1:0] = 00 - 11, V_{IN} = V_{33NOM} + 1.0 V	52	60	–	dB	(46)
$NOISE_{V33}$	Output noise density, V_{IN} = 2.8 V, I_{V33} = 262.5 mA • 100 Hz to <1.0 kHz • 1.0 kHz to <10 kHz • 10 kHz to 1.0 MHz	 – – –	 -114 -129 -135	 -102 -123 -130	dBV/√Hz	
t_{ONV33}	Turn-on time, enable to 90% of end value, V_{IN} = 2.8 V, to 4.5 V, I_{V33} = 0.0 mA	60	–	500	µs	

Table 24. Dynamic electrical characteristics – V33 (continued)

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, V_{33} = 3.3 V, I_{V33} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, V_{33} = 3.3 V, I_{V33} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
V33 linear regulator (continued)						
t_{OFFV33}	Turn-off time, disable to 10% of initial value, V_{IN} = 2.8 V, I_{V33} = 0.0 mA	–	–	10	ms	
V_{33OSHT}	Start-up overshoot, V_{IN} = 2.8 V to 4.5 V, I_{V33} = 0.0 mA	–	1.0	2.0	%	

Notes

46. When the LDO Output voltage is set above 2.6 V the minimum allowed input voltage need to be at least the output voltage plus 0.25 V for proper regulation due to the dropout voltage generated through the internal LDO transistor.

Table 25. Static electrical characteristics – VLDO3

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, $V_{LDO34IN}$ = 3.6 V, V_{LDO3} = 3.3 V, I_{LDO3} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, $V_{LDO34IN}$ = 3.6 V, V_{LDO3} = 3.3 V, I_{LDO3} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VLDO3 linear regulator						
$V_{LDO34IN}$	Operating input voltage • 1.8 V ≤ $V_{LDO3NOM}$ ≤ 2.5 V • 2.6 V ≤ $V_{LDO3NOM}$ ≤ 3.3 V	2.8 $V_{LDO3NOM}$ +0.250	– –	3.6 3.6	V	(47), (48)
$V_{LDO3NOM}$	Nominal output voltage	–	Table 63	–	V	
I_{LDO3}	Rated output load current	100	–	–	mA	
$V_{LDO3TOL}$	Output voltage tolerance, $V_{LDO34INMIN}$ < $V_{LDO34IN}$ < 4.5 V, 0.0 mA < I_{LDO3} < 100 mA, VLDO3 = 1.8 V to 3.3 V	-3.0	–	3.0	%	
I_{LDO3Q}	Quiescent current, no load, change in I_{VIN} and $I_{VLDO34IN}$, when V_{LDO3} enabled	–	13	–	µA	
$I_{LDO3LIM}$	Current limit, I_{LDO3} when V_{LDO3} is forced to $V_{LDO3NOM}$/2	122	167	280	mA	

Notes

47. Beyond VLDO34IN rating, the ESD protection can be sensitive to voltage transients.
48. Minimum operating voltage is 2.8 V with a valid LICELL voltage (1.8 V to 3.3 V). Minimum operating voltage is 3.1 V when no voltage is applied at the LICELL pin. If operation down to 2.8 V is required for systems without a coin cell, connect the LICELL pin to any system voltage between 1.8 V and 3.3 V. This voltage can be an output from any PF3000 regulator, or external system supply.

Table 26. Dynamic electrical characteristics – VLDO3

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, $V_{LDO34IN}$ = 3.6 V, V_{LDO3} = 3.3 V, I_{LDO3} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, $V_{LDO34IN}$ = 3.6 V, V_{LDO3} = 3.3 V, I_{LDO3} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VLDO3 linear regulator						
$PSRR_{VLDO3}$	PSRR, I_{LDO3} = 75 mA, 20 Hz to 20 kHz • VLDO3 = 1.8 V to 3.3 V, $V_{LDO34IN}$ = $V_{LDO34INMIN}$ + 100 mV • VLDO3 = 1.8 V to 3.3 V, $V_{LDO34IN}$ = $V_{LDO3NOM}$ + 1.0 V	35 52	40 60	– –	dB	
$NOISE_{VLDO3}$	Output noise density, $V_{LDO34IN}$ = $V_{LDO34INMIN}$, I_{LDO3} = 75 mA • 100 Hz to <1.0 kHz • 1.0 kHz to <10 kHz • 10 kHz to 1.0 MHz	– – –	-114 -129 -135	-102 -123 -130	dBV/√Hz	

Table 26. Dynamic electrical characteristics – VLDO3 (continued)

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, $V_{LDO34IN}$ = 3.6 V, V_{LDO3} = 3.3 V, I_{LDO3} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, $V_{LDO34IN}$ = 3.6 V, V_{LDO3} = 3.3 V, I_{LDO3} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VLDO3 linear regulator (continued)						
t_{ONLDO3}	Turn-on time, enable to 90% of end value, $V_{LDO34IN}$ = $V_{LDO34INMIN}$ to 4.5 V, I_{LDO3} = 0.0 mA	60	–	500	µs	
$t_{OFFLDO3}$	Turn-off time, disable to 10% of initial value, $V_{LDO34IN}$ = $V_{LDO34INMIN}$, I_{LDO3} = 0.0 mA	–	–	10	ms	
$LDO3_{OSHT}$	Start-up overshoot, $V_{LDO34IN}$ = $V_{LDO34IN2MIN}$ to 4.5 V, I_{LDO3} = 0.0 mA	–	1.0	2.0	%	

Table 27. Static electrical characteristics - VLDO4

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, $V_{LDO34IN}$ = 3.6 V, V_{LDO4} = 3.3 V, I_{LDO4} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, $V_{LDO34IN}$ = 3.6 V, VLDO4 = 3.3 V, I_{LDO4} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VLDO4 linear regulator						
$V_{LDO34IN}$	Operating input voltage • 1.8 V ≤ $V_{LDO4NOM}$ ≤ 2.5 V • 2.6 V ≤ $V_{LDO4NOM}$ ≤ 3.3 V	2.8 $V_{LDO4NOM}$ +0.250	– –	3.6 3.6	V	(49), (50)
$V_{LDO4NOM}$	Nominal output voltage	–	Table 63	–	V	
I_{LDO4}	Rated output load current	350	–	–	mA	
$V_{LDO4TOL}$	Output voltage tolerance, $V_{LDO34INMIN}$ < $V_{LDO34IN}$ < 4.5 V, 0.0 mA < I_{LDO3} < 100 mA, V_{LDO4} = 1.9 V to 3.3 V	-3.0	–	3.0	%	
I_{LDO4Q}	Quiescent current, no load, change in I_{VIN} and $I_{VLDO34IN}$, when V_{LDO4} enabled	–	13	–	µA	
$I_{LDO4LIM}$	Current limit, I_{LDO4} when V_{LDO4} is forced to $V_{LDO4NOM}$/2	435	584.5	950	mA	
$PSRR_{VLDO4}$	PSRR, I_{LDO4} = 262.5 mA, 20 Hz to 20 kHz • VLDO4 = 1.9 V to 3.3 V, $V_{LDO34IN}$ = $V_{LDO34INMIN}$ + 100 mV • VLDO4 = 1.9 V to 3.3 V, $V_{LDO34IN}$ = $V_{LDO4NOM}$ + 1.0 V	 35 52	 40 60	 – –	dB	

Notes

49. Beyond VLDO34IN rating, the ESD protection can be sensitive to voltage transients.
50. Minimum operating voltage is 2.8 V with a valid LICELL voltage (1.8 V to 3.3 V). Minimum operating voltage is 3.1 V when no voltage is applied at the LICELL pin. If operation down to 2.8 V is required for systems without a coin cell, connect the LICELL pin to any system voltage between 1.8 V and 3.3 V. This voltage can be an output from any PF3000 regulator, or external system supply.

Table 28. Dynamic electrical characteristics - VLDO4

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, $V_{LDO34IN}$ = 3.6 V, V_{LDO4} = 3.3 V, I_{LDO4} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, $V_{LDO34IN}$ = 3.6 V, VLDO4 = 3.3 V, I_{LDO4} = 10 mA, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VLDO4 linear regulator						
$NOISE_{VLDO4}$	Output noise density, $V_{LDO34IN2}$ = $V_{LDO34INMIN}$, I_{LDO4} = 262.5 mA • 100 Hz to <1.0 kHz • 1.0 kHz to <10 kHz • 10 kHz to 1.0 MHz	 – – –	 -114 -129 -135	 -102 -123 -130	dBV/√Hz	
t_{ONLDO4}	Turn-on time, enable to 90% of end value, $V_{LDO34IN}$ = $V_{LDO34INMIN}$, 4.5 V, I_{LDO4} = 0.0 mA	60	–	500	µs	
$t_{OFFLDO4}$	Turn-off time, disable to 10% of initial value, $V_{LDO34IN}$ = $V_{LDO34INMIN}$, I_{LDO4} = 0.0 mA	–	–	10	ms	
$LDO4_{OSHT}$	Start-up overshoot, $V_{LDO34IN}$ = $V_{LDO34INMIN}$, 4.5 V, I_{LDO4} = 0.0 mA	–	1.0	2.0	%	

Table 29. Static electrical characteristics - coin cell

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, typical external component values, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit	Notes
Coin cell						
$V_{COINACC}$	Charge voltage accuracy	-100	–	-100	mV	
$I_{COINACC}$	Charge current accuracy	-30	–	30	%	
I_{COIN}	Coin cell charge current • I_{COINHI} (in on mode) • I_{COINLO} (in on mode)	 – –	 60 10	 – –	µA	

Table 30. Static electrical characteristics - VREFDDR

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, I_{REFDDR} = 0.0 mA, $V_{INREFDDR}$ = 1.5 V, and typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, I_{REFDDR} = 0.0 mA, $V_{INREFDDR}$ = 1.5 V, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VREFDDR linear regulator						
$V_{INREFDDR}$	Operating input voltage range	1.2	–	1.65	V	(51)
V_{REFDDR}	Output voltage, 1.2 V < $V_{INREFDDR}$ < 1.65 V, 0.0 mA < I_{REFDDR} < 10 mA	–	$V_{INREFDDR}$/2	–	V	
$V_{REFDDRTOL}$	Output voltage tolerance, as a percentage of $V_{INREFDDR}$, 1.2 V < $V_{INREFDDR}$ < 1.65 V, 0.6 mA < I_{REFDDR} < 10 mA	49.5	50	50.5	%	
I_{REFDDR}	Rated output load current	10	–	–	mA	
$I_{REFDDRQ}$	Quiescent current	–	12	–	µA	(52)
$I_{REFDDRLM}$	Current limit, I_{REFDDR} when V_{REFDDR} is forced to $V_{INREFDDR}$/4	10.5	15	25	mA	

Notes

51. When using SW3 as input, the VINREFDDR input voltage range specification refers to the voltage set point of SW3 and not the absolute value
52. When VREFDDR is off there is a quiescent current of a typical 2.0 µA.

Table 31. Dynamic electrical characteristics - VREFDDR

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 3.6 V, I_{REFDDR} = 0.0 mA, $V_{INREFDDR}$ = 1.5 V, and typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, I_{REFDDR} = 0.0 mA, $V_{INREFDDR}$ = 1.5 V, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VREFDDR linear regulator						
$t_{ONREFDDR}$	Turn-on time, enable to 90% of end value, $V_{INREFDDR}$ = 1.2 V to 1.65 V, I_{REFDDR} = 0.0 mA	–	–	100	µs	
$t_{OFFREFDDR}$	Turn-off time, disable to 10% of initial value, $V_{INREFDDR}$ = 1.2 V to 1.65 V, I_{REFDDR} = 0.0 mA	–	–	10	ms	
$V_{REFDDROSH}$	Start-up overshoot, $V_{INREFDDR}$ = 1.2 V to 1.65 V, I_{REFDDR} = 0.0 mA	–	1.0	6.0	%	

Table 32. Static electrical characteristics - Digital I/O

All parameters are specified at T_A = -40 °C to 105 °C, V_{DDIO} = 1.7 V to 3.6 V, V_{PWR} = 0 V (external FET not populated), and typical external component values and full load current range, unless otherwise noted.

Pin name	Parameter	Load condition	Min	Max	Unit	Notes
PWRON	• V_L • V_H	– –	0.0 0.8 * V_{SNVS}	0.2 * V_{SNVS} 3.6	V	
RESETBMCU	• V_{OL} • V_{OH}	-2.0 mA Open drain	0.0 0.7 * V_{DDIO}	0.4 * V_{DDIO} V_{DDIO}	V	
SCL	• V_L • V_H	– –	0.0 0.8 * V_{DDIO}	0.2 * V_{DDIO} 3.6	V	
SDA	• V_L • V_H • V_{OL} • V_{OH}	– – -2.0 mA Open drain	0.0 0.8 * V_{DDIO} 0.0 0.7 * V_{DDIO}	0.2 * V_{DDIO} 3.6 0.4 * V_{DDIO} V_{DDIO}	V	
INTB	• V_{OL} • V_{OH}	-2.0 mA Open drain	0.0 0.7 * V_{DDIO}	0.4 * V_{DDIO} V_{DDIO}	V	
STANDBY	• V_L • V_H	– –	0.0 0.8 * V_{SNVS}	0.2 * V_{SNVS} 3.6	V	
SD_VSEL	• V_L • V_H	– –	0.0 0.8 * V_{DDIO}	0.2 * V_{DDIO} 3.6	V	
VDDOTP	• V_L • V_H	– –	0.0 1.1	0.3 1.7	V	

Table 33. Static electrical characteristics - internal supplies

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 2.8 V to 4.5 V, LICELL = 1.8 V to 3.3 V, and typical external component values. Typical values are characterized at V_{IN} = 3.6 V, LICELL = 3.0 V, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VCOREDIG (digital core supply)						
$V_{COREDIG}$	Output voltage • ON mode • Coin cell mode and OFF mode	 – –	 1.5 1.3	 – –	V	(53)
VCORE (analog core supply)						
V_{CORE}	Output voltage • ON mode and charging • Coin cell mode and OFF mode	 – –	 2.775 0.0	 – –	V	(53)
VCOREREF (bandgap regulator reference)						
$V_{COREREF}$	Output voltage at 25 °C	–	1.2	–	V	(53)
$V_{COREREFACC}$	Absolute trim accuracy	–	0.5	–	%	
$V_{COREREFTACC}$	Temperature Drift	–	0.25	–	%	

Notes

53. 3.1 V < V_{IN} < 4.5 V, no external loading on VCOREDIG, VCORE, or VCOREREF.

Table 34. Static electrical characteristics - UVDET threshold

All parameters are specified at T_A = -40 °C to 105 °C, V_{IN} = 2.8 V to 4.5 V, LICELL = 1.8 V to 3.3 V, and typical external component values. Typical values are characterized at V_{IN} = 3.6 V, LICELL = 3.0 V, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
V_{IN} UVDET threshold						
V_{UVDET}	• Rising • Falling	– 2.5	– –	3.1 –	V	

6 Functional description and application information

6.1 Introduction

The PF3000 is a highly integrated, low quiescent current power management IC featuring four buck regulators, one boost regulator, seven LDO regulators, and a DDR voltage reference. The PF3000 provides all the necessary rails to power a complete system including the application processor, memory and peripherals. The PF3000 operates from an input voltage of up to 5.5 V. Output voltage, startup sequence, and other functions are set using integrated one-time-programmable (OTP) memory, thus providing flexibility and reducing external component count.

6.2 Power generation

The buck regulators in the PF3000 provide supply to the processor cores and to other voltage domains, such as I/O and memory. Dynamic voltage scaling is provided to allow controlled supply rail adjustments for the processor cores and other circuitry. The SW1A and SW1B buck regulators can either be used as independent 1.0 A and 1.75 A regulators, or can be combined as a single 2.75 A regulator.

The linear regulators in the PF3000 can be used as general purpose regulators to power peripherals and lower power processor rails. The VCC_SD LDO regulator supports the dual voltage requirement by high speed SD card readers. Depending on the system power path configuration, the LDO regulators can be directly supplied from the main input supply or from the switching regulators to power peripherals, such as audio, camera, Bluetooth, and Wireless LAN, etc.

A specific V_{REFDDR} voltage reference is included to provide accurate reference voltage for DDR memories. The VSNVS block behaves as an LDO, or as a bypass switch to supply the SNVS/SRTC circuitry on the i.MX processors; V_{SNVS} may be powered from V_{IN}, or from a coin cell.

To accommodate applications that are powered by main supplies of voltages higher than 4.5 V and up to 5.5 V, the PF3000 incorporates a front-end LDO regulator using an external pass FET to keep the maximum regulator input voltage of the regulators at 4.5 V. Applications with an input voltage lower than 4.5 V can directly power the regulators without using the front-end LDO.

PF3000 shows a summary of the voltage regulators in the PF3000.

Table 35. PF3000 power tree

Supply	Output voltage (V)	Programming Step size (mV)	Maximum load current (mA)
SW1A	0.70 to 1.425 1.8 to 3.3	25 (N/A)	1000
SW1B	0.70 to 1.475	25	1750
SW2	1.50 to 1.85 2.50 to 3.30	50 variable	1250
SW3	0.90 to 1.65	50	1500
SWBST	5.00 to 5.15	50	600
VLDO1	1.8 to 3.3	50	100
VLDO2	0.80 to 1.55	50	250
VCC_SD	2.85 to 3.30 1.80 to 1.85	150 50	100
V33	2.85 to 3.30	150	350
VLDO3	1.8 to 3.3	100	100
VLDO4	1.8 to 3.3	100	350
VSNVS	3.0	NA	1.0
VREFDDR	0.5*SW3_OUT	NA	10

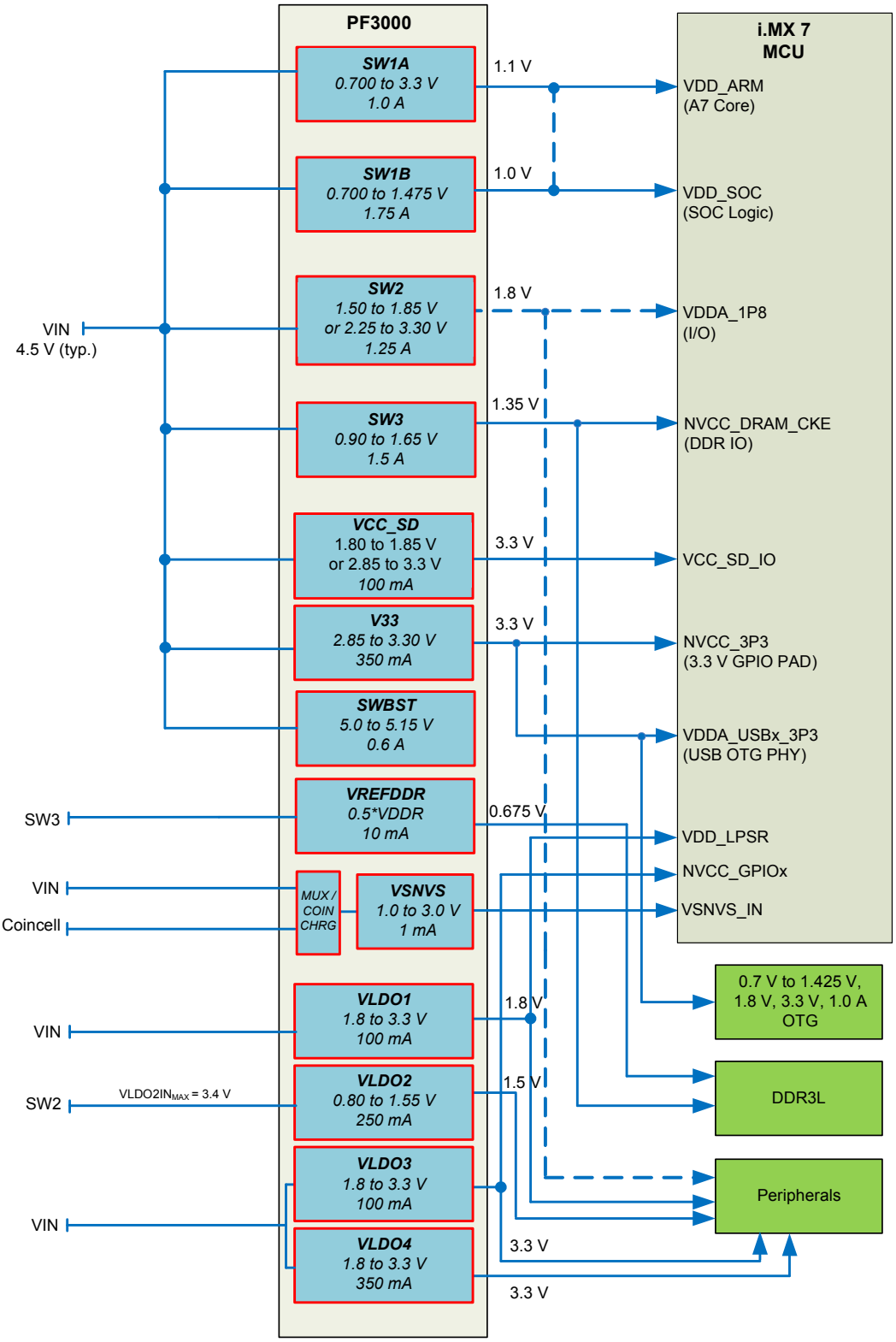


Figure 5. PF3000 typical power map

Figure 5 shows a simplified power map with various recommended options to supply the different block within the PF3000, as well as the typical application voltage domain on the i.MX 7 processors. Note that each application power tree is dependent upon the system's voltage and current requirements, therefore a proper input voltage should be selected for the regulators.

6.3 Functional description

6.3.1 Control logic and interface signals

The PF3000 is fully programmable via the I^2C interface. Additional communication is provided by direct logic interfacing including INTB, RESETBMCU, STANDBY, PWRON, and SD_VSEL. Refer to Table 30 for logic levels for these pins.

6.3.1.1 PWRON

PWRON is an input signal to the IC that generates a turn-on event. A turn-on event brings the PF3000 out of OFF and sleep modes and into the ON mode. Refer to Modes of operation for the various modes (states) of operation of the IC. The PWRON pin can be configured using OTP to detect a level, or an edge using the PWRON_CFG bit.

- If PWRON_CFG = 0, the PWRON signal is high and VIN > UVDET, the PMIC turns on; the interrupt and sense bits, PWRONI and PWRONS respectively, is set.
- If PWRON_CFG = 1, VIN > UVDET and PWRON transitions from high to low, the PMIC turns on; the interrupt and sense bits, PWRONI and PWRONS respectively, is set.

Any regulator enabled in the sleep mode remains enabled when transitioning from Sleep to ON, i.e., the regulator is not turned off and then on again to match the start-up sequence.

When PWRON_CFG = 1, the PWRON input can be a mechanical switch debounced through a programmable debouncer PWRONDBNC[1:0], to avoid a response to a very short key press. The interrupt is generated for both the falling and the rising edge of the PWRON pin. By default, a 31.25 ms interrupt debounce is applied to both falling and rising edges. The falling edge debounce timing can be extended with PWRONDBNC[1:0] as defined in the table below. The interrupt is cleared by software, or when cycling through the OFF mode.

Table 36. PWRON hardware debounce bit settings (54)

Bits	State	Turn on debounce (ms)	Falling edge INT debounce (ms)	Rising edge INT debounce (ms)
PWRONDBNC[1:0]	00	0.0	31.25	31.25
	01	31.25	31.25	31.25
	10	125	125	31.25
	11	750	750	31.25

Notes

54. The sense bit, PWRONS, is not debounced and follows the state of the PWRON pin.

6.3.1.2 STANDBY

STANDBY is an input signal to the IC. When it is asserted the part enters standby mode and when de-asserted, the part exits standby mode. STANDBY can be configured as active high or active low using the STANDBYINV bit. See Standby mode for more details.

Note: When operating the PMIC at VIN ≤ 2.85 V a coin cell must be present to provide V_{SNVS}, or the PMIC does not reliably enter and exit the STANDBY mode.

6.3.1.3 RESETBMCU

RESETBMCU is an open-drain, active low output OTP configurable for two modes of operation. In its default mode, it is de-asserted 2.0 ms after the last regulator in the start-up sequence is enabled. In this mode, the signal can be used to bring the processor out of reset (POR), or as an indicator that all supplies have been enabled; it is only asserted during a turn-off event. In the default mode, the RESETBMCU signal is internal timer based and does not monitor the regulators. When configured for its fault mode, RESETBMCU is de-asserted after the start-up sequence is completed only if no faults occurred during start-up. At any time, if a fault occurs and persists for 1.8 ms, RESETBMCU is asserted LOW. The PF3000 is turned off if the fault persists for more than 100 ms. The PWRON signal can be used to restart the part, though if the fault persists, the sequence described above is repeated. To enter the fault mode, set bit OTP_PG_EN of register OTP PWRGD EN to “1” during OTP programming.

6.3.1.4 INTB

INTB is an open drain, active low output. It is asserted when any fault occurs, provided that the fault interrupt is unmasked. INTB is de-asserted after the fault interrupt is cleared by software, which requires writing a “1” to the fault interrupt bit.

6.3.1.5 SD_VSEL

SD_VSEL is an input pin that sets the output voltage range of the VCC_SD regulator. When SD_VSEL = HIGH, the VCC_SD regulator operates in the lower output voltage range. When SD_VSEL = LOW, the VCC_SD regulator operates in the higher output voltage range. The SD_VSEL input buffer is powered by the VDDIO supply. When a valid VDDIO voltage is not present, the output of the SD_VSEL buffer defaults to a logic high thus keeping the VCC_SD regulator output in the lower voltage range.

6.3.2 One-time-programmable memory

One-time-programmable memory is used to store key startup parameters and regulators’ configuration information. This eliminates the need to set regulator voltage and sequence using external components. The following parameters are programmable in the PF3000.

General: I^2C slave address, PWRON pin configuration, RESETBMCU configuration

Buck regulators: Output voltage, single phase or independent mode configuration for SW1A and SW1B regulators, switching frequency, regulator start-up sequence and timing

Boost regulator and LDOs: Output voltage, regulator start-up sequence and timing

The PF3000 starts up based on the contents of the TBBOTP registers. During power up, contents of the OTP memory are loaded on to the TBBOTP registers. There is an optional Try-before-buy mode of operation available which bypasses loading of the OTP memory onto the TBBOTP registers. Instead, regulators directly start up based on the current contents of the TBBOTP registers during this mode of operation. This mode is useful when trying to determine a suitable OTP configuration for the system. TBB mode can also be used in lieu of OTP programming provided a microcontroller can initiate the TBB sequence is available in the system.

6.3.2.1 Register naming convention

Register and bit names for the TBBOTP registers are prefixed with “OTP”. This is to differentiate them from “functional registers” which are responsible for real-time control of regulator settings. For example, “OTP_SW1A_VOLT” refers to the TBBOTP register associated with the voltage setting for SW1A regulator. “SW1AVOLT” refers to the functional register which is fed into the SW1A regulator block. During power up, contents of the OTP fuses are copied onto the “OTP_SW1A_VOLT” register which is further copied on to the “SW1AVOLT” register. During normal operation, writes to the “OTP_SW1A_VOLT” register has no effect on the output voltage of the SW1A regulator. Writes to the “SW1AVOLT” register do have an effect.

6.3.2.2 Regulator startup sequence programming

Each regulator has 3-bits or 4-bits allocated to program its start-up time slot from a turn-on event; therefore, each can be placed from position one to seven or one to fifteen in the start-up sequence as shown in Table 37. When the sequence is code is set to 0, the regulator remains off during the startup sequence. It can be enabled using I^2C after the start up sequence is completed. The delay between each position can be programmed to be 0.5 ms or 2.0 ms as shown in Table 38. The start-up sequence terminates at the last programmed regulator. RESETBMCU pin is de-asserted HIGH 2.0 ms after the last utilized startup slot.

Table 37. Start-up sequence

OTP_SWx_SEQ[2:0]/ OTP_V33_SEQ[2:0]/ OTP_VCC_SD_SEQ[2:0]	OTP_VLDOx_SEQ[3:0]/	Sequence
000	0000	Off
001	0001	SEQ_CLK_SPEED * 1
010	0010	SEQ_CLK_SPEED * 2
011	0011	SEQ_CLK_SPEED * 3
100	0100	SEQ_CLK_SPEED * 4
101	0101	SEQ_CLK_SPEED * 5
110	0110	SEQ_CLK_SPEED * 6

Table 37. Start-up sequence (continued)

OTP_SWx_SEQ[2:0]/ OTP_V33_SEQ[2:0]/ OTP_VCC_SD_SEQ[2:0]	OTP_VLDOx_SEQ[3:0]/	Sequence
111	0111	SEQ_CLK_SPEED * 7
–	1000	SEQ_CLK_SPEED * 8
–	1001	SEQ_CLK_SPEED * 9
–	1010	SEQ_CLK_SPEED * 10
–	1011	SEQ_CLK_SPEED * 11
–	1100	SEQ_CLK_SPEED * 12
–	1101	SEQ_CLK_SPEED * 13
–	1110	SEQ_CLK_SPEED * 14
–	1111	SEQ_CLK_SPEED * 15

Table 38. Start-up sequence clock speed

SEQ_CLK_SPEED	Time (µs)
0	500
1	2000

6.3.2.3 PWRON pin configuration

The PWRON pin can be configured as either a level sensitive input (PWRON_CFG = 0), or as an edge sensitive input (PWRON_CFG = 1). As a level sensitive input, an active high signal turns on the part and an active low signal turns off the part, or puts it into sleep mode. As an edge sensitive input, such as when connected to a mechanical switch, a falling edge turns on the part and if the switch is held low for greater than or equal to 4.0 seconds, the part turns off or enters sleep mode.

Table 39. PWRON configuration

PWRON_CFG	Mode
0	PWRON pin HIGH = ON PWRON pin LOW = OFF or sleep mode
1	PWRON pin pulled LOW momentarily = ON PWRON pin LOW for 4.0 seconds = OFF or sleep mode

6.3.2.4 I^2C address configuration

The I^2C device address can be programmed from 0x08 to 0x0F. This allows flexibility to change the I^2C address to avoid bus conflicts. Address bit, I2C_SLV_ADDR[3] in OTP_I2C_ADDR register is hard coded to “1” while the lower three LSBs of the I^2C address (I2C_SLV_ADDR[2:0]) are programmable as shown in Table 40. The I^2C address of the PF3000 immediately changes after write instructions to the OTP_I2C_ADDR register are complete. To continue using the default address of 0x08, set bit 7 (USE_DEFAULT_ADD) of the OTP_I2C_ADDR register.

Table 40. I^2C address configuration

I2C_SLV_ADDR[3] Hard Coded	I2C_SLV_ADDR[2:0]	I^2C Device Address (Hex)
1	000	0x08
1	001	0x09
1	010	0x0A
1	011	0x0B
1	100	0x0C

Table 40. I^2C address configuration (continued)

I2C_SLV_ADDR[3] Hard Coded	I2C_SLV_ADDR[2:0]	I^2C Device Address (Hex)
1	101	0x0D
1	110	0x0E
1	111	0x0F

6.3.2.5 Buck regulator soft start ramp rate

The start-up ramp rate ramp rate or soft start ramp rate of buck regulators can be chosen by using the SWDVS_CLK bit during OTP. Table 41 shows the startup ramp rate options for the buck regulators in the PF3000.

Table 41. DVS speed selection for SWx

SWDVS_CLK	Function
0	25 mV step each 2.0 µs
1	25 mV step each 4.0 µs

6.3.3 Start-up

Regulators in the PF3000 start up based on the contents of the TBBOTP registers. During cold start, contents from the OTP memory are loaded into the TBBOTP registers when VIN > UVDET irrespective of whether the PMIC is powered using the VIN or the VPWR path. Contents of the TBBOTP registers are reloaded from the fuses during a turn-on event.

The PF3000 is available in a number of pre-programmed flavors to suit a wide variety of system configurations. Refer to Table 42 for programming details of the different flavors. Refer to Section 6.3.2 for a detailed explanation of the OTP block.

Table 42. Start-up configuration (55)

OTP registers	Default configuration	Non-programmed	Pre-programmed OTP configuration							
	All Devices	A0	A1	A2	A3	A4	A5	A6	A7	A8
Default I2C Address	0x08	0x08	0x08	0x08	0x08	0x08	0x08	0x08	0x08	0x08
OTP_VSNVS_VOLT	3.0 V	1.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V
OTP_SW1A_VOLT	1.15 V	0.7 V	1.10 V	1.10 V	1.375 V	1.375 V	1.375 V	3.3 V	3.3 V	3.3 V
OTP_SW1A_SEQ	1	OFF	1	1	2	1	1	3	3	3
OTP_SW1B_VOT	1.15 V	0.7 V	1.0 V	1.0 V	1.375 V	1.375 V	1.375 V	1.4 V	1.4 V	1.4 V
OTP_SW1B_SEQ	1	OFF	1	1	2	1	1	3	3	3
OTP_SW2_VOLT	1.8 V	1.5 V	1.8 V	1.8 V	3.3 V	3.3 V	3.15 V	3.3 V	3.3 V	3.3 V
OTP_SW2_SEQ	2	OFF	2	2	4	2	2	3	3	3
OTP_SW3_VOLT	1.2 V	0.9 V	1.35 V	1.2 V	1.35 V	1.5 V	1.2 V	1.2 V	1.35 V	1.5 V
OTP_SW3_SEQ	3	OFF	5	5	3	3	4	3	3	3
OTP_SWBST_VOLT	5.0 V	5.0 V	5.0 V	5.0 V	5.0 V	5.0 V	5.0 V	5.0 V	5.0 V	5.0 V
OTP_SWBST_SEQ	OFF	OFF	OFF	OFF	OFF	OFF	6	OFF	OFF	OFF
OTP_VLDO1_VOLT	1.8 V	1.8 V	1.8 V	1.8 V	3.3 V	1.8 V	1.8 V	3.3 V	3.3 V	3.3 V
OTP_VLDO1_SEQ	2	OFF	4	4	OFF	OFF	3	3	3	3
OTP_VLDO2_VOLT	1.2 V	0.8 V	1.5 V	1.5 V	1.5 V	1.2 V	1.5 V	1.5 V	1.5 V	1.5 V
OTP_VLDO2_SEQ	OFF	OFF	4	4	OFF	3	OFF	OFF	OFF	OFF
OTP_VLDO3_VOLT	1.8 V	1.8 V	3.3 V	3.3 V	2.5 V	1.8 V	3.1 V	1.8 V	1.8 V	1.8 V
OTP_VLDO3_SEQ	2	OFF	3	3	OFF	OFF	2	3	3	3
OTP_VLDO4_VOLT	1.8 V	1.8 V	3.3 V	3.3 V	1.8 V	1.8 V	1.8 V	1.8 V	1.8 V	1.8 V
OTP_VLDO4_SEQ	OFF	OFF	3	3	4	3	3	3	3	3
OTP_V33_VOLT	3.15 V	2.85 V	3.3 V	3.3 V	3.0 V	3.3 V	2.85 V	3.3 V	3.3 V	3.3 V
OTP_V33_SEQ	2	OFF	3	3	1	2	OFF	2	2	2
OTP_VCC_SD_VOLT	3.15 V/1.80 V	2.85 V/1.80 V	3.3 V/1.85 V	3.3 V/1.85 V	3.3 V/1.85 V	3.0 V/1.80 V	3.15 V/1.80 V	3.3 V/1.85 V	3.3 V/1.85 V	3.3 V/1.85 V
OTP_VCC_SD_SEQ	3	OFF	4	4	5	3	2	3	3	3
OTP_SEQ_CLK_SPEED	500 µs	500 µs	2000 µs	2000 µs	500 µs	2000 µs	2000 µs	2000 µs	2000 µs	2000 µs
OTP_SWDVS_CLK	6.25 mV/µs	12.5 mV/µs	12.5 mV/µs	12.5 mV/µs	6.25 mV/µs	12.5 mV/µs	12.5 mV/µs	12.5 mV/µs	12.5 mV/µs	12.5 mV/µs
OTP_PWRON_CFG	Level sensitive	Level sensitive	Level sensitive	Level sensitive	Level sensitive	Level sensitive	Level sensitive	Level sensitive	Level sensitive	Level sensitive
OTP_SW1_CONFIG	SW1A, SW1B Independent Mode, 2.0 MHz	SW1A, SW1B Independent Mode, 1.0 MHz	SW1A, SW1B Independent Mode, 2.0 MHz	SW1A, SW1B Independent Mode, 2.0 MHz	SW1A, SW1B Independent Mode, 2.0 MHz	SW1A, SW1B Independent Mode, 2.0 MHz	SW1A, SW1B Independent Mode, 2.0 MHz	SW1A, SW1B Independent Mode, 2.0 MHz	SW1A, SW1B Independent Mode, 2.0 MHz	SW1A, SW1B Independent Mode, 2.0 MHz
OTP_SW2_FREQ	2.0 MHz	1.0 MHz	2.0 MHz	2.0 MHz	2.0 MHz	2.0 MHz	2.0 MHz	2.0 MHz	2.0 MHz	2.0 MHz
OTP_SW3_FREQ	2.0 MHz	1.0 MHz	2.0 MHz	2.0 MHz	2.0 MHz	2.0 MHz	2.0 MHz	2.0 MHz	2.0 MHz	2.0 MHz
OTP_PG_EN	RESETBMCU in Default Mode	RESETBMCU in Default Mode	RESETBMCU in Default Mode	RESETBMCU in Default Mode	RESETBMCU in Default Mode	RESETBMCU in Default Mode	RESETBMCU in Default Mode	RESETBMCU in Default Mode	RESETBMCU in Default Mode	RESETBMCU in Default Mode

Notes

55. This table specifies the default output voltage of the LDOs and SWx after start-up and/or when the LDOs and SWx are enabled. VREFDDR_SEQ is internally fixed to be same as SW3_SEQ. VCC_SD voltage depends on the state of the SD_VSEL pin.

6.3.3.1 Start-up timing diagram

The startup timing of the regulators is programmable through OTP and seq_clk_speed. Figure 6 shows the startup timing of the regulators as determined by their OTP sequence. The trimmed 32 kHz clock controls all the start up timing.

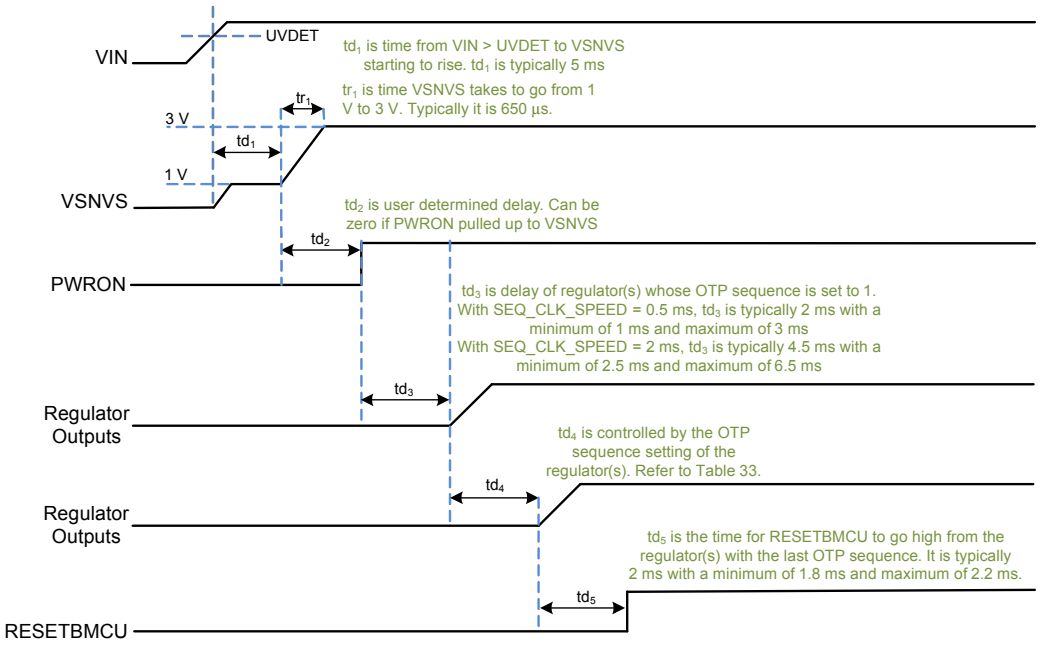


Figure 6. Startup timing diagram

6.3.4 16 MHz and 32 kHz clocks

The PF3000 incorporates two clocks: a trimmed 16 MHz RC oscillator and an untrimmed 32 kHz RC oscillator. The 32 kHz untrimmed clock is only used in the following conditions:

- V_{IN} < UVDET
- All regulators are in sleep mode
- All regulators are in PFM switching mode

A 32 kHz clock, derived from the 16 MHz trimmed clock, is used when accurate timing is needed under the following conditions:

- During start-up, V_{IN} > UVDET
- PWRON_CFG = 1, for power button debounce timing

When the 16 MHz is active in the ON mode, the debounce times are referenced to the 32 kHz derived from the 16 MHz clock. The exceptions are the LOWVINI and PWRONI interrupts, which are referenced to the 32 kHz untrimmed clock. Switching frequency of the switching regulators is derived from the trimmed 16 MHz clock.

The 16 MHz clock and hence the switching frequency of the regulators, can be adjusted to improve the noise integrity of the system. By changing the factory trim values of the 16 MHz clock, the user may add an offset as small as ±3.0% of the nominal frequency. Contact your NXP representative for detailed information on this feature.

6.3.5 Optional front-end input LDO regulator

6.3.5.1 LDO regulator description

This section describes the optional front-end LDO regulator provided by the PF3000 in order to facilitate the operation with supply voltages higher than 4.5 V and up to 5.5 V.

For non-battery operated applications, when the input supply voltage exceeds 4.5 V, the front-end LDO can be activated by populating the external PMOS pass FET MP1 in Figure 7 and connecting the VPWR pin to the main supply. Under this condition, the LDO control block self-starts with a local bandgap reference. When the VIN pin reaches UVDET rising threshold, the reference is switched to the main trimmed bandgap reference to maintain the required VIN accuracy. In applications using an input supply voltage of 4.5 V or lower, the PMOS pass FET should not be populated, VPWR pin should be grounded externally and the VIN pin should be used instead as the main supply input pin. The input pins of the switching regulators should always be connected to the VIN net.

The main components of the LDO regulator are an external power P-channel MOSFET and an internal differential error amplifier. One input of the amplifier monitors a fraction of the output voltage at VIN determined by the resistor ratio of R1 and R2 as shown in Figure 7. The second input to the differential amplifier is from a stable bandgap voltage reference. If the output voltage rises too high relative to the reference voltage, the gate voltage of the power FET is changed to maintain a constant output voltage.

In order to maintain the power consumption at reasonable levels during PF3000 standby and sleep modes, the LDO circuit enters low-power mode of operation using an embedded pass FET while the external pass FET is kept off. When the STBY_LOWPOWER_B bit in register LDOGCTL is set the activation of the low-power mode during IC standby mode is disabled; however the LDO low-power mode is always activated during the IC sleep mode. Moreover, during IC Off mode, an even simpler internal circuit is used to further reduce the power consumption. Refer to Modes of operation for different modes of operation of the IC.

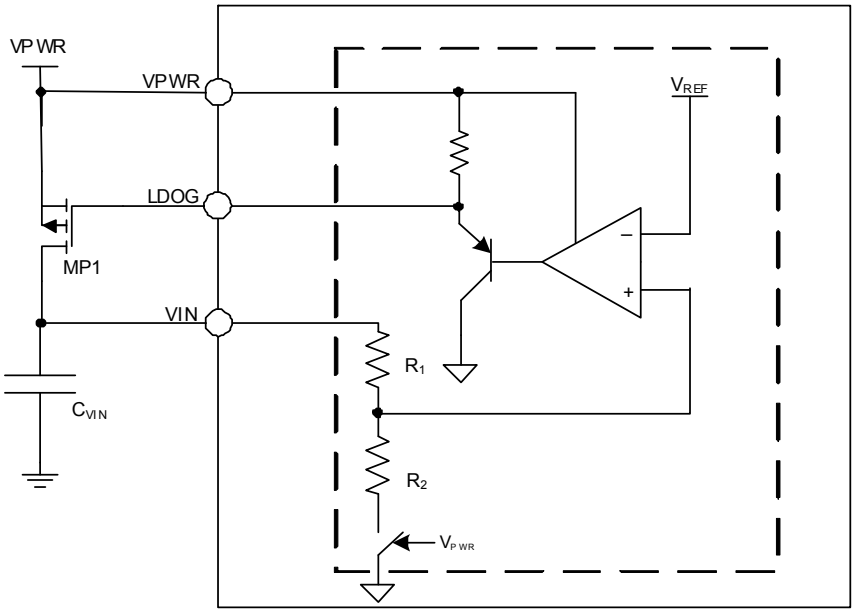


Figure 7. Front-end LDO block diagram

6.3.5.2 Undervoltage/short-circuit and overvoltage detection

Short-circuit to GND at VIN is detected using an under voltage monitor at VIN that would sense excessive droop on the VIN line and consequently turn off (disable) the external PMOS pass FET. Overvoltage at VPWR is detected if VPWR exceeds the V_{PWROV} threshold (typically 6.0 V). Upon the detection of an overvoltage event an interrupt is generated and bit 2 is set in INTSTAT3 register. The INTB pin is pulled low if the VPWROVM mask bit is cleared. The interrupt is filtered using a 122 µs debouncing circuit. The VPWROV interrupt is not asserted if the overvoltage event occurs during start up. The VPWROVS bit can be read using I^2C to detect an overvoltage condition.

6.3.5.3 External components

Table 43 lists the typical component values for the general purpose LDO regulators.

Table 43. Input LDO external components

Component	Value
Minimum output capacitor on VIN rail	100 µF [56]
MP1	Fairchild FDMA908PZ, Vishay SiA447DJ, or comparable

Notes

56. Use X5R/X7R ceramic capacitors with a voltage rating at least two times the nominal voltage. The 100 µF capacitance is the total capacitance on the VIN rail including the capacitance at the various regulator inputs. For example, 2 x 22 µF capacitors can be used along with 10 µF capacitors at all the SWx and LDOx inputs to achieve a total of 100 µF capacitance.

6.3.6 Internal core voltages

All regulators use the main bandgap as the reference. The main bandgap is bypassed with a capacitor at VCOREREF. VCOREDIG is a 1.5 V regulator that powers all the digital logic in the PF3000. VCOREDIG is regulated at 1.28 V in Off and coin cell modes. The VCORE supply is used to bias internal analog rails and the OTP fuses. No external DC loading is allowed on VCORE, VCOREDIG, or VCOREREF. VCOREDIG is kept powered as long as there is a valid supply and/or valid coin cell.

6.3.7 VREFDDR voltage reference

VREFDDR is an internal PMOS half supply voltage follower capable of supplying up to 10 mA. The output voltage is at one half the input voltage. It is typically used as the reference voltage for DDR memories. A filtered resistor divider is utilized to create a low frequency pole. This divider then uses a voltage follower to drive the load.

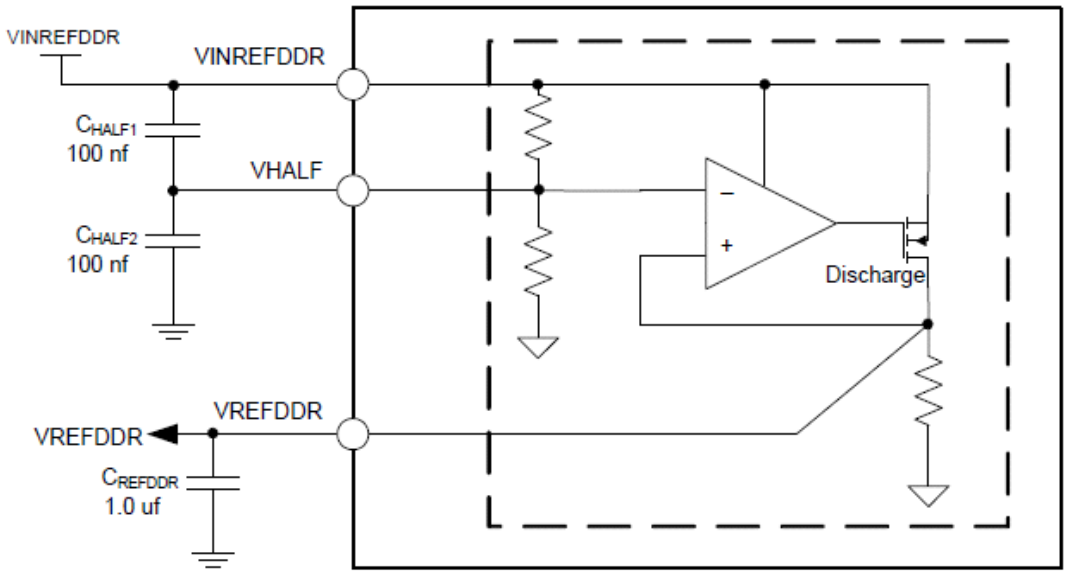


Figure 8. VREFDDR block diagram

6.3.7.1 VREFDDR external components

Table 44. VREFDDR external components [57]

Capacitor	Capacitance (µF)
VINREFDDR [58] to VHALF	0.1
VHALF to GND	0.1
VREFDDR	1.0

Notes
57. Use X5R or X7R capacitors.
58. VINREFDDR to GND, 1.0 µF minimum capacitance is provided by buck regulator output.

6.3.8 Buck regulators

The PF3000 integrates four independent buck regulators: SW1A, SW1B, SW2, and SW3. Regulators SW1A and SW1B regulators can be configured as a single regulator through OTP. Output of the buck regulators during start up is programmable through OTP. Each regulator has associated registers that control its output voltage during On, standby, and sleep modes. During start-up, contents of the OTP_SWx_VOLT register is copied onto the SWxVOLT[4:0], SWxSTBY[4:0] and SWxOFF[4:0]. After boot up, contents of the SWxVOLT, SWxSTBY and SWxOFF registers can be set through I^2C to set the output voltage during On, standby, and sleep modes respectively.

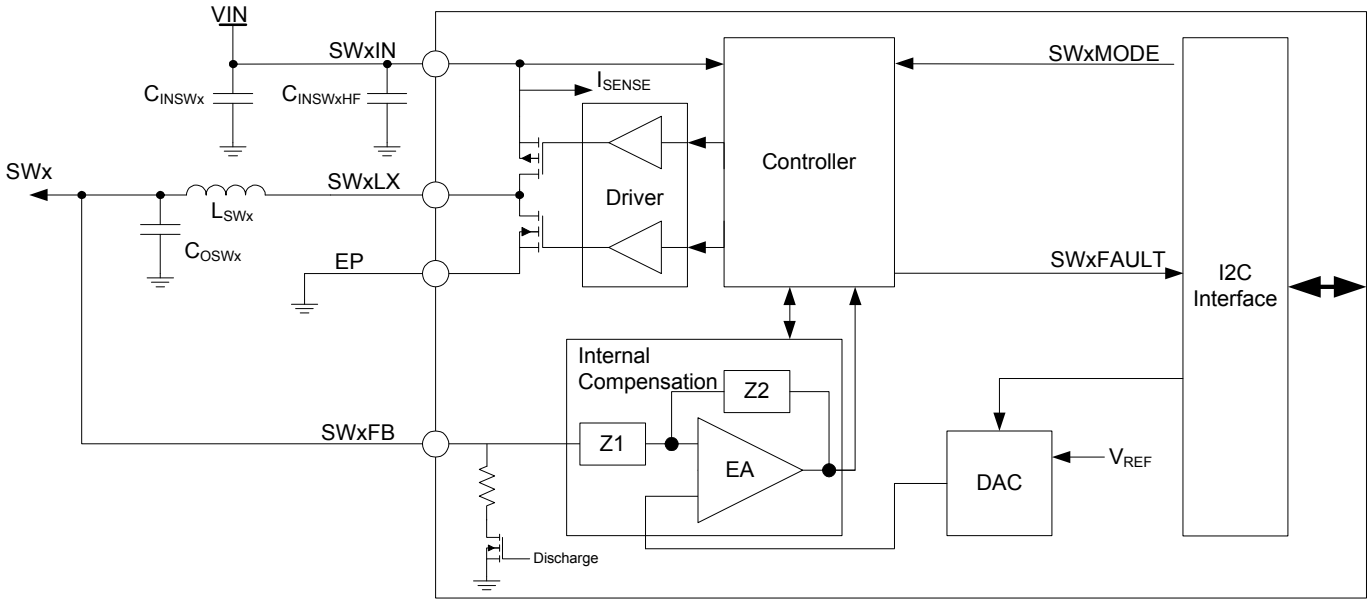


Figure 9. Generic SWx block diagram

Table 45. SWx regulators external components

Components	Description	Values
CINSWx	SWx input capacitor	4.7 µF
CINSWxHF	SWx decoupling input capacitor	0.1 µF
COSWx	SWx output capacitor	2 x 22 µF (10 V or higher voltage rated capacitors) or 3 x 22 µF (6.3 V rated capacitors)
LSWx	SWx inductor	1.5 µH

Use X5R or X7R capacitors with voltage rating at least two times the nominal voltage.

6.3.8.1 Switching modes

To improve system efficiency the buck regulators can operate in different switching modes. Changing between switching modes can occur by any of the following means: I^2C programming, exiting/entering the standby mode, exiting/entering sleep mode, and load current variation. Available switching modes for buck regulators are presented in Table 45.

Table 46. Switching mode description

Mode	Description
OFF	The regulator is switched off and the output voltage is discharged using an internal resistor
PFM	In this mode, the regulator operates in forced PFM mode. The main error amplifier is turned off and a hysteretic comparator is used to regulate output voltage. Use this mode for load currents less than 50 mA.
PWM	In this mode, the regulator operates in forced PWM mode.
APS	In this mode, the regulator operates in pulse skipping mode at light loads and switches over to PWM modes for heavier load conditions. This is the default mode in which the regulators power up during a turn-on event.

During soft-start of the buck regulators, the controller transitions through the PFM, APS, and PWM switching modes. 3.0 ms after the output voltage reaches regulation, the controller transitions to the selected switching mode. Depending on the particular switching mode selected, additional ripple may be observed on the output voltage rail as the controller transitions between switching modes. The operating mode of the regulator in On and standby modes is controlled using the SWxMODE[3:0] bits associated with each regulator. Table 46 summarizes the buck regulator programmability for normal and standby modes.

Table 47. Regulator mode control

SWxMODE[3:0]	Normal mode	Standby mode
0000	Off	Off
0001	PWM	Off
0010	Reserved	Reserved
0011	PFM	Off
0100	APS	Off
0101	PWM	PWM
0110	PWM	APS
0111	Reserved	Reserved
1000 (default)	APS	APS
1001	Reserved	Reserved
1010	Reserved	Reserved
1011	Reserved	Reserved
1100	APS	PFM
1101	PWM	PFM
1110	Reserved	Reserved
1111	Reserved	Reserved

Transitioning between normal and standby modes can affect a change in switching modes as well as output voltage. When in standby mode, the regulator outputs the voltage programmed in its standby voltage register and operates in the mode selected by the SWxMODE[3:0] bits. Upon exiting standby mode, the regulator returns to its normal switching mode and its output voltage programmed in its voltage register.

Any regulators whose SWxOMODE bit is set to “1” enters sleep mode if a PWRON turn-off event occurs, and any regulator whose SWxOMODE bit is set to “0” is turned off. In sleep mode, the regulator outputs the voltage programmed in SWxOFF registers and operates in the PFM mode. The regulator exits the sleep mode when a turn-on event occurs. Any regulator whose SWxOMODE bit is set to “1” remains on and changes to its normal configuration settings when exiting the Sleep state to the ON state. Any regulator whose SWxOMODE bit is set to “0” is powered up with the same delay in the start-up sequence as when powering ON from Off. At this point, the regulator returns to its default ON state output voltage and switch mode settings.

When sleep mode is activated by the SWxOMODE bit, the regulator uses the set point as programmed by SW1xOFF[4:0] for SW1A/B and by SW2OFF[2:0] for SW2, and SW3OFF[3:0] for SW3.

6.3.8.2 Dynamic voltage scaling

To reduce overall power consumption, processor core voltages can be varied depending on the mode or activity level of the processor.

1. Normal operation: The output voltage is selected by I^2C bits SW1x[4:0] for SW1A/B and SW2[2:0] for SW2, and SW3[3:0] for SW3. A voltage transition initiated by I^2C is governed by the DVS stepping rates shown in Table 48.

2. Standby mode: The output voltage can be selected by I^2C bits SW1xSTBY[4:0] for SW1A/B and by bits SW2STBY[2:0] for SW2, and SW3STBY[3:0] for SW3. Voltage transitions initiated by a Standby event are governed by the DVS stepping rates shown in Table 48.

3. Sleep mode: The output voltage can be higher or lower than in normal operation, but is typically selected to be the lowest state retention voltage of a given processor; it is selected by I^2C bits SW1xOFF[4:0] for SW1A/B and by bits SW2OFF[2:0] for SW2, and SW3OFF[3:0] for SW3. Voltage transitions initiated by a turn-off event are governed by the DVS stepping rates shown in Table 48.

Table 48. DVS speed selection for SWx

SWxDVSSPEED	Function
0	25 mV step each 2.0 µs
1	25 mV step each 4.0 µs

The regulators have a strong sourcing capability and sinking capability in PWM mode, therefore the fastest rising and falling slopes are determined by the regulator in PWM mode. However, if the regulators are programmed in PFM or APS mode during a DVS transition, the falling slope can be influenced by the load. Additionally, as the current capability in PFM mode is reduced, controlled DVS transitions in PFM mode could be affected. Critically timed DVS transitions are best assured with PWM mode operation.

Figure 10 shows the general behavior for the regulators when initiated with I^2C programming, or standby control. During the DVS period the overcurrent condition on the regulator should be masked.

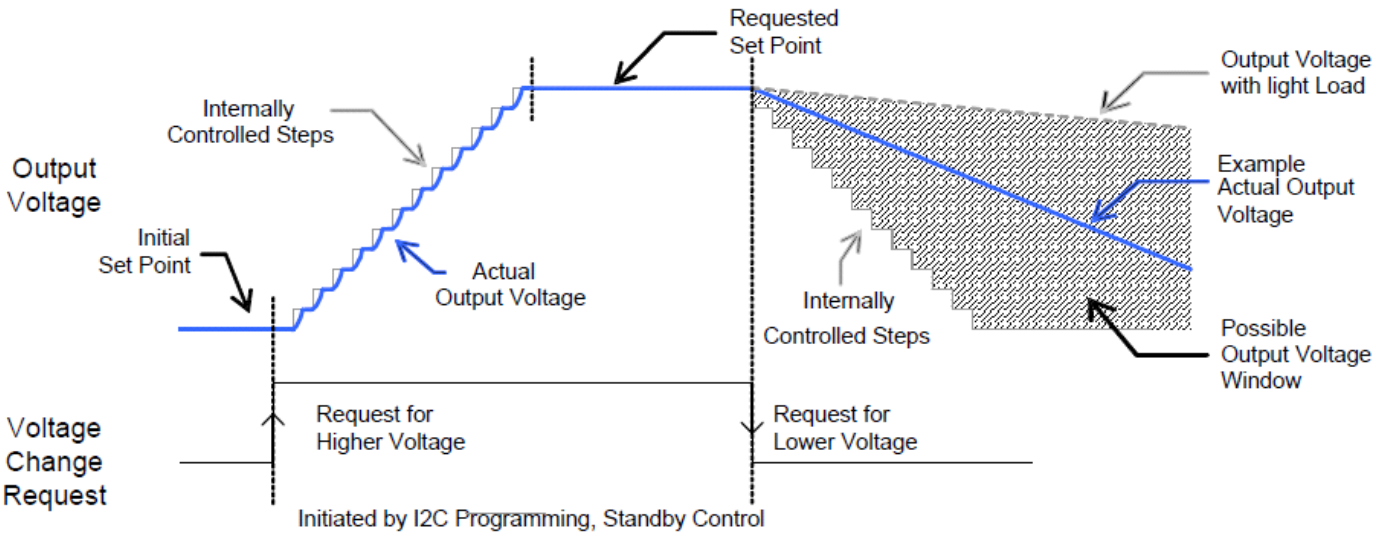


Figure 10. Voltage stepping with DVS

Note: In SW1A independent and SW1AB single phase modes, DVS to and from the 1.8 V and 3.3 V output voltage settings is not allowed.

6.3.8.3 Regulator phase clock

The SWxPHASE[1:0] bits select the phase of the regulator clock as shown in Table 49. By default, each regulator is initialized at 90 ° out of phase with respect to each other. For example, SW1x is set to 0 °, SW2 is set to 90 °, and SW3 is set to 180 ° by default at power up.

Table 49. Regulator phase clock selection

SWxPHASE[1:0]	Phase of clock sent to regulator (degrees)
00	0
01	90
10	90
11	270

The SWxFREQ[1:0] register is used to set the desired switching frequency for each one of the buck regulators. Table 51 shows the selectable options for SWxFREQ[1:0]. For each frequency, all phases are available, this allows regulators operating at different frequencies to have different relative switching phases. However, not all combinations are practical. For example, 2.0 MHz, 90 ° and 4.0 MHz, 180 ° are the same in terms of phasing. Table 50 shows the optimum phasing when using more than one switching frequency.

Table 50. Optimum phasing

Frequencies	Optimum Phasing
1.0 MHz 2.0 MHz	0° 180°
1.0 MHz 4.0 MHz	0° 180°
2.0 MHz 4.0 MHz	0° 180°
1.0 MHz 2.0 MHz 4.0 MHz	0° 90° 90°

Table 51. Regulator frequency configuration

SWxFREQ[1:0]	Frequency
00	1.0 MHz
01	2.0 MHz (default)
10	4.0 MHz
11	Reserved

6.3.8.4 SW1A/B

SW1A/B are 1 to 2.75 A buck regulators that can be configured in various phasing schemes, depending on the desired cost/performance trade-offs. The following configurations are available:

- SW1A/B single phase with one inductor
- SW1A in independent with one inductor and SW1B in independent mode with a second inductor

The desired configuration is programmed by OTP by using OTP_SW1_CONFIG[1:0] bits in the register map, as shown below in Table 52.

Table 52. SW1 configuration

OTP_SW1_CONFIG[1:0]	Description
00	Unused
01	A/B Single Phase
10	Unused
11	A Independent mode B Independent mode

6.3.8.5 SW1A/B single phase

In this configuration, the phases SW1ALX, and SW1BLX, are connected together to a single inductor, thus, providing up to 2.75 A current capability for high current applications. The feedback and all other controls are accomplished by use of pin SW1AFB and SW1A control registers, respectively. However, the same configuration settings for frequency, phase, and DVS speed setting on SW1B registers should be used. The SW1BFB pin should be left floating in this configuration.

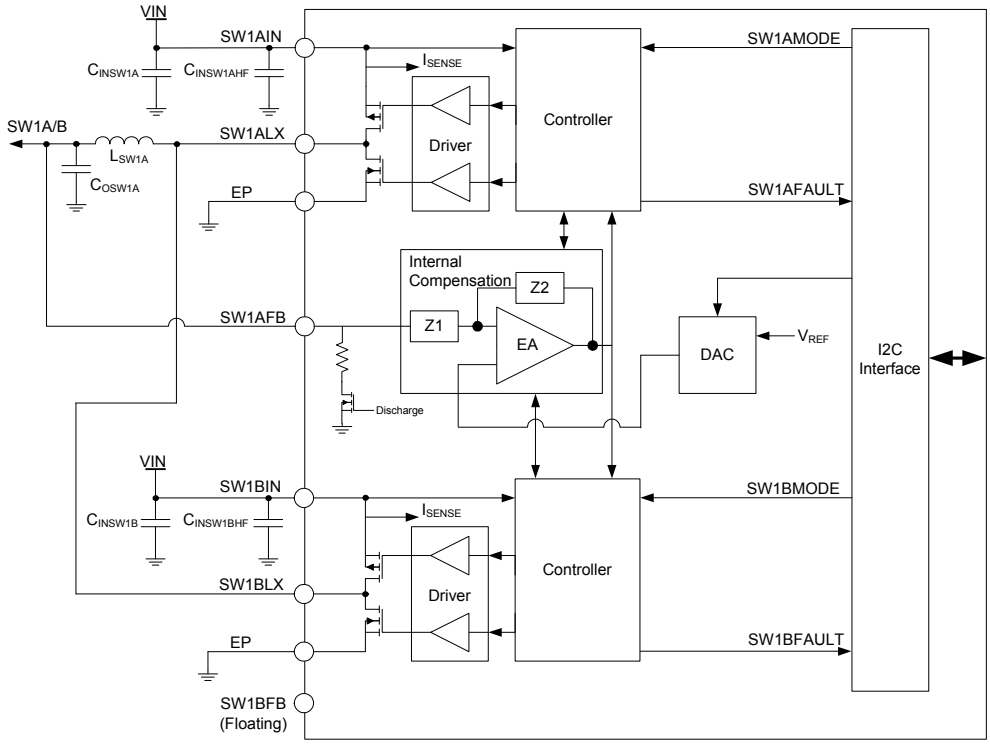


Figure 11. SW1A/B single phase diagram

6.3.8.6 SW1A - SW1B

Independent mode In this configuration, SW1A is connected as an independent output with a single inductor, while SW1B is used as another independent output, using another inductor and configuration parameters. They can be operated with a different voltage set point for normal, standby, and sleep modes, as well as switching mode selection and on/off control.

6.3.8.7 SW1A/B setup and control registers

SW1A and SW1AB output voltages are programmable from 0.700 V to 1.425 V in steps of 25 mV. They can additionally be programmed at 1.8 V or 3.3 V. SW1B output voltage is programmable from 0.700 V to 1.475 V in steps of 25 mV. The output voltage set point is independently programmed for normal, standby, and sleep mode by setting the SW1x[4:0], SW1xSTBY[4:0], and SW1xOFF[4:0] bits respectively. Table 53 shows the output voltage coding for SW1A, SW1B or SW1A/B. Values shown in Table 53 are also to be used during OTP programming by setting the OTP_SW1A_VOLT and OTP_SW1B_VOLT registers appropriately.

Table 53. SW1A/B output voltage configuration

Set point	SW1x[4:0] SW1xSTBY[4:0] SW1xOFF[4:0]	SW1x output (V)	Set point	SW1x[4:0] SW1xSTBY[4:0] SW1xOFF[4:0]	SW1x output (V)
0	00000	0.700	16	10000	1.100
1	00001	0.725	17	10001	1.125
2	00010	0.750	18	10010	1.150
3	00011	0.775	19	10011	1.175
4	00100	0.800	20	10100	1.200
5	00101	0.825	21	10101	1.225
6	00110	0.850	22	10110	1.250
7	00111	0.875	23	10111	1.275
8	01000	0.900	24	11000	1.300
9	01001	0.925	25	11001	1.325
10	01010	0.950	26	11010	1.350
11	01011	0.975	27	11011	1.375
12	01100	1.000	28	11100	1.400
13	01101	1.025	29	11101	1.425
14	01110	1.050	30	11110	1.450 (SW1B), 1.8 (SW1A/SW1AB)
15	01111	1.075	31	11111	1.475 (SW1B), 3.3 (SW1A/SW1AB)

Table 54 provides a list of registers used to configure and operate SW1A/B regulator(s).

Table 54. SW1A/B register summary

Register	Address	Output
SW1AVOLT	0x20	SW1A output voltage set point in normal operation
SW1ASTBY	0x21	SW1A output voltage set point on standby
SW1AOFF	0x22	SW1A output voltage set point on sleep
SW1AMODE	0x23	SW1A switching mode selector register
SW1ACONF	0x24	SW1A DVS, phase, and frequency configuration
SW1BVOLT	0x2E	SW1B output voltage set point in normal operation
SW1BSTBY	0x2F	SW1B output voltage set point in standby
SW1BOFF	0x30	SW1B output voltage set point in sleep
SW1BMODE	0x31	SW1B switching mode selector register
SW1BCONF	0x32	SW1B DVS, phase, and frequency configuration

6.3.8.8 SW2 setup and control registers

SW2 is a single phase, 1.25 A rated buck regulator. SW2 output voltage is programmable from 1.500 V to 1.850 V in 50 mV steps if the OTP_SW2_HI bit is low or from 2.500 V to 3.300 V in 150 mV steps if the bit OTP_SW2_HI is set high. During normal operation, output voltage of the SW2 regulator can be changed through I^2C only within the range set by the OTP_SW2_HI bit. The output voltage set point is independently programmed for normal, standby, and sleep mode by setting the SW2[2:0], SW2STBY[2:0] and SW2OFF[2:0] bits, respectively. Table 55 shows the output voltage coding valid for SW2.

Table 55. SW2 output voltage configuration

Low output voltage range (OTP_SW2_HI= 0)		High output voltage range (OTP_SW2_HI=1)	
SW2[2:0] SW2STBY[2:0] SW2OFF[2:0]	SW2 output	SW2[2:0] SW2STBY[2:0] SW2OFF[2:0]	SW2 output
000	1.500	000	2.500
001	1.550	001	2.800
010	1.600	010	2.850
011	1.650	011	3.000
100	1.700	100	3.100
101	1.750	101	3.150
110	1.800	110	3.200
111	1.850	111	3.300

Setup and control of SW2 is done through the I^2C registers listed in Table 56.

Table 56. SW2 register summary

Register	Address	Description
SW2VOLT	0x35	Output voltage set point on normal operation
SW2STBY	0x36	Output voltage set point on Standby
SW2OFF	0x37	Output voltage set point on Sleep
SW2MODE	0x38	Switching mode selector register
SW2CONF	0x39	DVS, phase, frequency, and ILIM configuration

6.3.8.9 SW3 setup and control registers

SW3 output voltage is programmable from 0.90 V to 1.65 V in 50 mV steps to support different types of DDR memory as listed in Table 57.

Table 57. SW3 output voltage configuration

SW3[3:0]	SW3 Output (V)	SW3[3:0]	SW3 Output (V)
0000	0.90	1000	1.30
0001	0.95	1001	1.35
0010	1.00	1010	1.40
0011	1.05	1011	1.45
0100	1.10	1100	1.50
0101	1.15	1101	1.55
0110	1.20	1110	1.60
0111	1.25	1111	1.65

Table 58 provides a list of registers used to configure and operate SW3.

Table 58. SW3 register summary

Register	Address	Output
SW3VOLT	0x3C	SW3 output voltage set point on normal operation
SW3STBY	0x3D	SW3 output voltage set point on Standby
SW3OFF	0x3E	SW3 output voltage set point on Sleep
SW3MODE	0x3F	SW3 switching mode selector register
SW3CONF	0x40	SW3 DVS, phase, frequency and ILIM configuration

6.3.9 Boost regulator

SWBST is a boost regulator with a programmable output from 5.0 V to 5.15 V. SWBST can supply the VUSB regulator for the USB PHY in OTG mode, as well as the VBUS voltage. Note that the parasitic leakage path for a boost regulator causes the SWBSTOUT and SWBSTFB voltage to be a Schottky drop below the input voltage whenever SWBST is disabled. A load switch is recommended on the output path to isolate the output for applications where this is not desired. The switching NMOS transistor is integrated on-chip. Figure 12 shows the block diagram and component connection for the boost regulator.

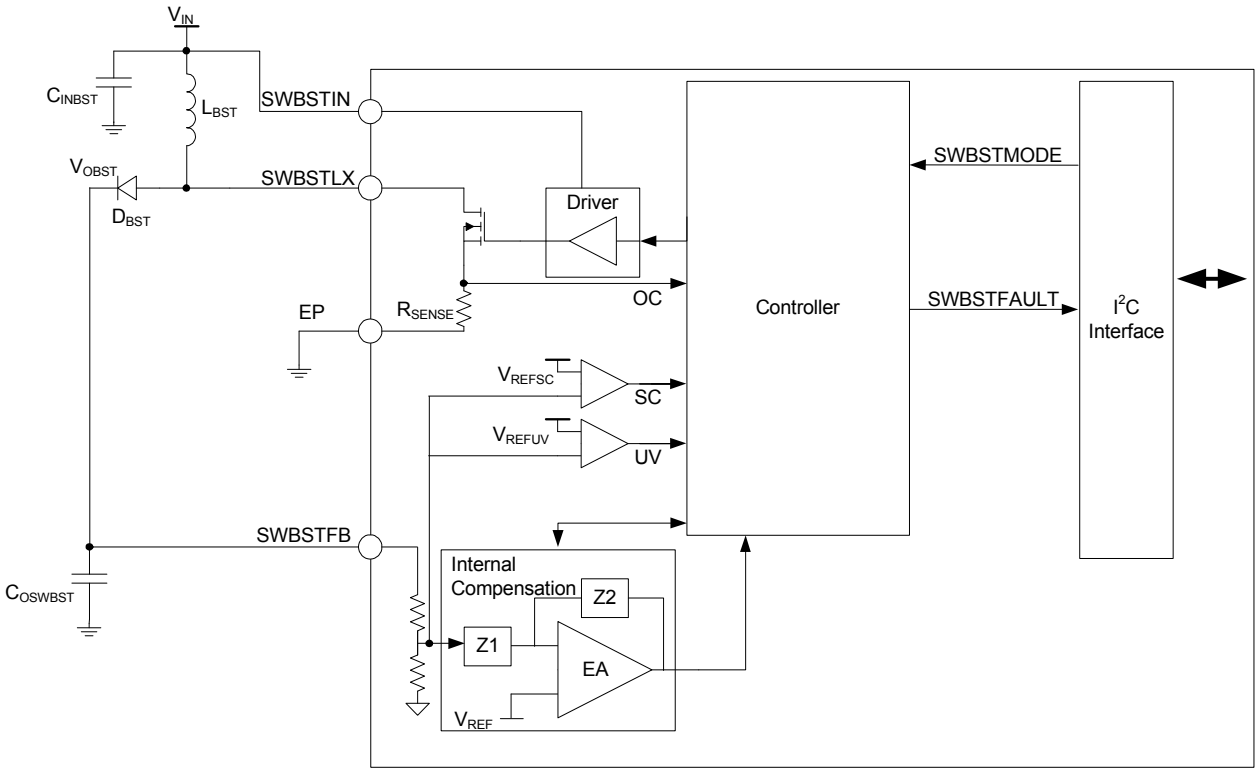


Figure 12. Boost regulator architecture

6.3.9.1 SWBST setup and control

Boost regulator control is done through a single register SWBSTCTL described in Table 59. SWBST is included in the power-up sequence if its OTP power-up timing bits, OTP_SWBST_SEQ[2:0], are not all zeros.

Table 59. Register SWBSTCTL - ADDR 0x66

Name	Bit #	R/W	Default	Description
SWBST1VOLT	1:0	R/W	0b00	Set the output voltage for SWBST 00 = 5.000 V 01 = 5.050 V 10 = 5.100 V 11 = 5.150 V
SWBST1MODE	3:2	R	0b10	Set the switching mode on normal operation 00 = OFF 01 = PFM 10 = Auto (Default) (59) 11 = APS
Unused	4	–	0b0	Unused
SWBST1STBYMODE	6:5	R/W	0b10	Set the switching mode on standby 00 = OFF 01 = PFM 10 = Auto (Default) (59) 11 = APS
Unused	7	–	0b0	Unused

Notes
59. In auto mode, the controller automatically switches between PFM and APS modes depending on the load current. Regulator switches in auto mode if enabled in the startup sequence.

6.3.9.2 SWBST external components

Table 60. SWBST external component requirements

Components	Description	Values
C_{INBST} (60)	SWBST input capacitor	10 µF
$C_{INBSTHF}$ (60)	SWBST decoupling input capacitor	0.1 µF
C_{OSWBST} (60)	SWBST output capacitor	2 x 22 µF
L_{SBST}	SWBST inductor	2.2 µH
D_{BST}	SWBST boost diode	1.0 A, 20 V Schottky

Notes
60. Use X5R or X7R capacitors.

6.3.10 LDO Regulators Description

This section describes the LDO regulators provided by the PF3000. All regulators use the main bandgap as reference. When a regulator is disabled, the output is discharged by an internal pull-down resistor.

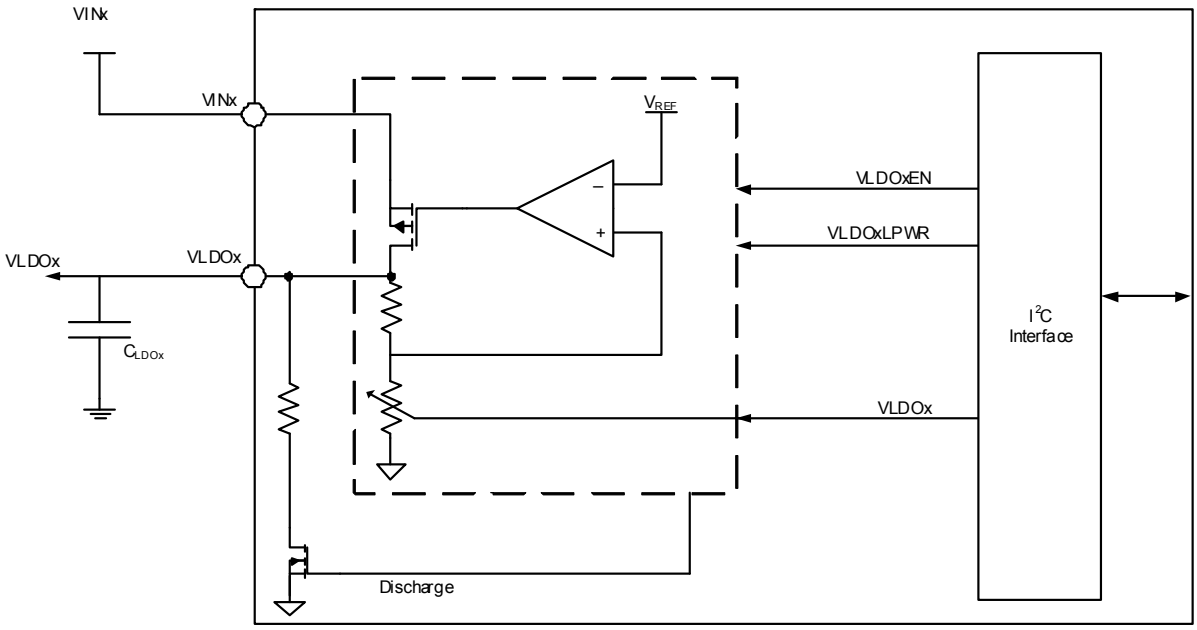


Figure 13. General LDO block diagram

6.3.10.1 External components

Table 61 lists the typical component values for the general purpose LDO regulators.

Table 61. LDO External Components

Regulator	Output capacitor (µF)[61]
VLDO1	2.2
VLDO2	4.7
VLDO3	2.2
VLDO4	4.7
V33	4.7
VCC_SD	2.2

Notes
61. Use X5R/X7R ceramic capacitors.

6.3.10.2 Current limit protection

All the LDO regulators in the PF3000 have current limit protection. In the event of an overload condition, the regulators transitions from a voltage regulator to a current regulator that regulates output current per the current limit threshold.

Additionally, if the REGSCPEN bit in Table 124 is set, the LDO is turned off if the current limit event lasts for more than 8.0 ms. The LDO is disabled by resetting its VLDOxEN bit, while at the same time, an interrupt VLDOxFAULTI is generated to flag the fault to the system processor. The VLDOxFAULTI interrupt is maskable through the VLDOxFAULTM mask bit. By default, the REGSCPEN is not set; therefore, at start-up none of the regulators is disabled if an overloaded condition occurs. A fault interrupt, VLDOxFAULTI, is generated in an overload condition regardless of the state of the REGSCPEN bit.

6.3.10.3 LDO voltage control

Each LDO is fully controlled through its respective VLDOxCTL register. This register enables the user to set the LDO output voltage according toTable 62 for VLDO1 and VLDO2; and uses the voltage set point on Table 63 for VLDO3 and VLDO4. Table 64 lists the voltage set points for the V33 LDO and Table 65 provides the output voltage set points for the VCC_SD LDO based on SD_VSEL control signal. During power-up, contents of the OTP_VLDO_VOLT register is copied to the VLDOxCTL registers.

Table 62. VLDO1, VLDO2 output voltage configuration

VLDO1[3:0] VLDO2[3:0]	VLDO1 Output (V)	VLDO2 Output (V)
0000	1.80	0.80
0001	1.90	0.85
0010	2.00	0.90
0011	2.10	0.95
0100	2.20	1.00
0101	2.30	1.05
0110	2.40	1.10
0111	2.50	1.15
1000	2.60	1.20
1001	2.70	1.25
1010	2.80	1.30
1011	2.90	1.35
1100	3.00	1.40
1101	3.10	1.45
1110	3.20	1.50
1111	3.30	1.55

Table 63. VLDO3, VLDO4 output voltage configuration

VLDO3[3:0] VLDO4[3:0]	VLDO3 or VLDO4 output (V)
0000	1.80
0001	1.90
0010	2.00
0011	2.10
0100	2.20
0101	2.30
0110	2.40
0111	2.50
1000	2.60
1001	2.70
1010	2.80
1011	2.90
1100	3.00
1101	3.10
1110	3.20
1111	3.30

Table 64. V33 output voltage configuration

V33[1:0]	V33 Output (V)
00	2.85
01	3.00
10	3.15
11	3.30

Table 65. VCC_SD output voltage configuration

VCC_SD[1:0]	VCC_SD output (V) VSD_VSEL= 0	VCC_SD output (V) VSD_VSEL= 1
00	2.85	1.80
01	3.00	1.80
10	3.15	1.80
11	3.30	1.85

Along with the output voltage configuration, the LDOs can be enabled or disabled at anytime during normal mode operation, as well as programmed to stay “ON” or be disabled when the PMIC enters standby mode. Each regulator has associated I^2C bits for this. Table 66 presents a summary of all valid combinations of the control bits on VLDOxCTL register and the expected behavior of the LDO output.

Table 66. LDO control

VLDOxEN/ V33EN/ VCC_SDEN	VLDOxLPWR/ V33LPWR/ VCC_SDLPWR	VLDOxSTBY/ V33STBY/ VCC_SDSTBY	STANDBY (62)	VLDOxOUT
0	X	X	X	Off
1	0	0	X	On
1	1	0	X	Low Power
1	X	1	0	On
1	0	1	1	Off
1	1	1	1	Low Power

Notes
62. STANDBY refers to a standby event as described earlier.

6.3.11 VSNVS LDO/switch

VSNVS powers the low-power, SNVS/RTC domain on the processor. It derives its power from either VIN, or coin cell, and cannot be disabled. When powered by both, V_{IN} takes precedence when above the appropriate comparator threshold. When powered by V_{IN}, VSNVS is an LDO capable of supplying 3.0 V. When powered by coin cell, the VSNVS output tracks the coin cell voltage by means of a switch, whose maximum resistance is 100 Ω. In this case, the V_{SNVS} voltage is simply the coin cell voltage minus the voltage drop across the switch, which is 100 mV at a rated maximum load current of 1000 μA.

When the coin cell is applied for the very first time, VSNVS outputs 1.0 V. Only when V_{IN} is applied thereafter does V_{SNVS} transition to its default value. Upon subsequent removal of V_{IN}, with the coin cell attached, V_{SNVS} changes configuration from an LDO to a switch, provided certain conditions are met as described in Table 67.

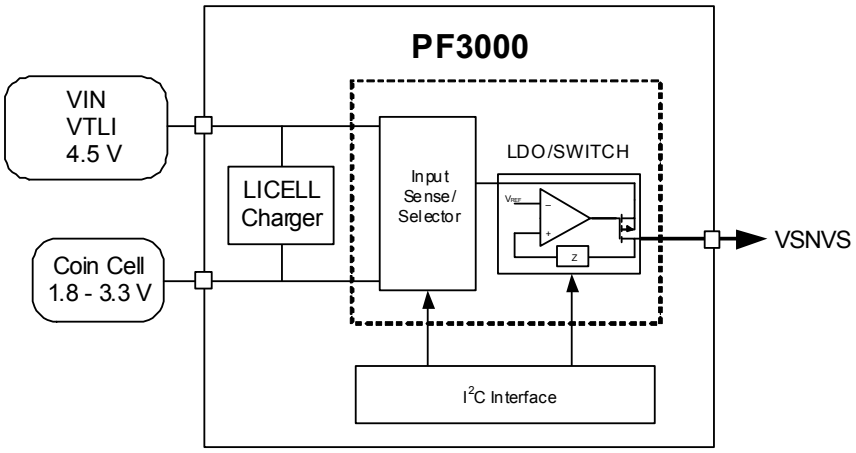


Figure 14. VSNVS supply switch architecture

Table 67 provides a summary of the V_{SNVS} operation at different input voltage V_{IN} and with or without coin cell connected to the system.

Table 67. SNVS modes of operation

VSNVSVOLT[2:0]	VIN	MODE
110	> VTH1	VIN LDO 3.0 V
110	< VTL1	Coin cell switch

6.3.11.1 VSNVS control

The V_{SNVS} output level is configured through the VSNVSVOLT[2:0] bits on VSNVSCTL register as shown in table Table 68.

Table 68. Register VSNVSCTL - ADDR 0x6B

Name	Bit #	R/W	Default	Description
VSNVSVOLT	2:0	R/W	0b000	Configures VSNVS output voltage.(63) 000 = RSVD 001 = RSVD 010 = RSVD 011 = RSVD 100 = RSVD 101 = RSVD 110 = 3.0 V (default) 111 = RSVD
Unused	7:3	–	0b00000	Unused

Notes
63. Only valid when a valid input voltage is present.

6.3.11.2 VSNVS external components

Table 69. VSNVS external components

Capacitor	Value (µF)
VSNVS	0.47

6.3.11.3 Coin cell battery backup

The LICELL pin provides for a connection of a coin cell backup battery or a “super” capacitor. If the voltage at VIN goes below the V_{IN} threshold (VTL1), contact-bounced, or removed, the coin cell maintained logic is powered by the voltage applied to LICELL. The supply for internal logic and the VSNVS rail switches over to the LICELL pin when V_{IN} goes below VTL1, even in the absence of a voltage at the LICELL pin, resulting in clearing of memory and turning off VSNVS. Applications concerned about this behavior can tie the LICELL pin to any system voltage between 1.8 V and 3.0 V. A 0.47 μF capacitor should be placed from LICELL to ground under all circumstances.

6.3.11.4 Coin cell charger control

The coin cell charger circuit functions as a current-limited voltage source, resulting in the CC/CV taper characteristic typically used for rechargeable Lithium-Ion batteries. The coin cell charger is enabled via the COINCHEN bit while the coin cell voltage is programmable through the VCOIN[2:0] bits on register COINCTL on Table 70. The coin cell charger voltage is programmable. In the ON state, the charger current is fixed at ICOINHI. In sleep and standby modes, the charger current is reduced to a typical 10 μA. In the OFF state, coin cell charging is not available as the main battery could be depleted unnecessarily. The coin cell charging is stopped when V_{IN} is below UVDET.

Table 70. Coin cell charger voltage

VCOIN[2:0]	V_{COIN} (V) [64]
000	2.50
001	2.70
010	2.80
011	2.90
100	3.00
101	3.10
110	3.20
111	3.30

Notes
64. Coin cell voltages selected based on the type of LICELL used on the system.

Table 71. Register COINCTL - ADDR 0x1A

Name	Bit #	R/W	Default	Description
VCOIN	2:0	R/W	0x00	Coin cell charger output voltage selection. See Table 70 for all options selectable through these bits.
COINCHEN	3	R/W	0x00	Enable or disable the coin cell charger
Unused	7:4	–	0x00	Unused

6.3.11.5 External components

Table 72. Coin cell charger external components

Component	Value	Units
LICELL bypass capacitor	100	nF

6.4 Power dissipation

During operation, the temperature of the die should not exceed the operating junction temperature noted in Table 4. To optimize the thermal management and to avoid overheating, the PF3000 provides thermal protection. An internal comparator monitors the die temperature. Interrupts THERM110, THERM120, THERM125, and THERM130 is generated when the respective thresholds specified in Table 73 are crossed in either direction. The temperature range can be determined by reading the THERMxxxS bits in register INTSENSE0.

In the event of excessive power dissipation, thermal protection circuitry shuts down the PF3000. This thermal protection acts above the thermal protection threshold listed in Table 73. To avoid any unwanted power downs resulting from internal noise, the protection is debounced for 8.0 ms. This protection should be considered as a fail-safe mechanism and therefore the system should be configured such that this protection is not tripped under normal conditions.

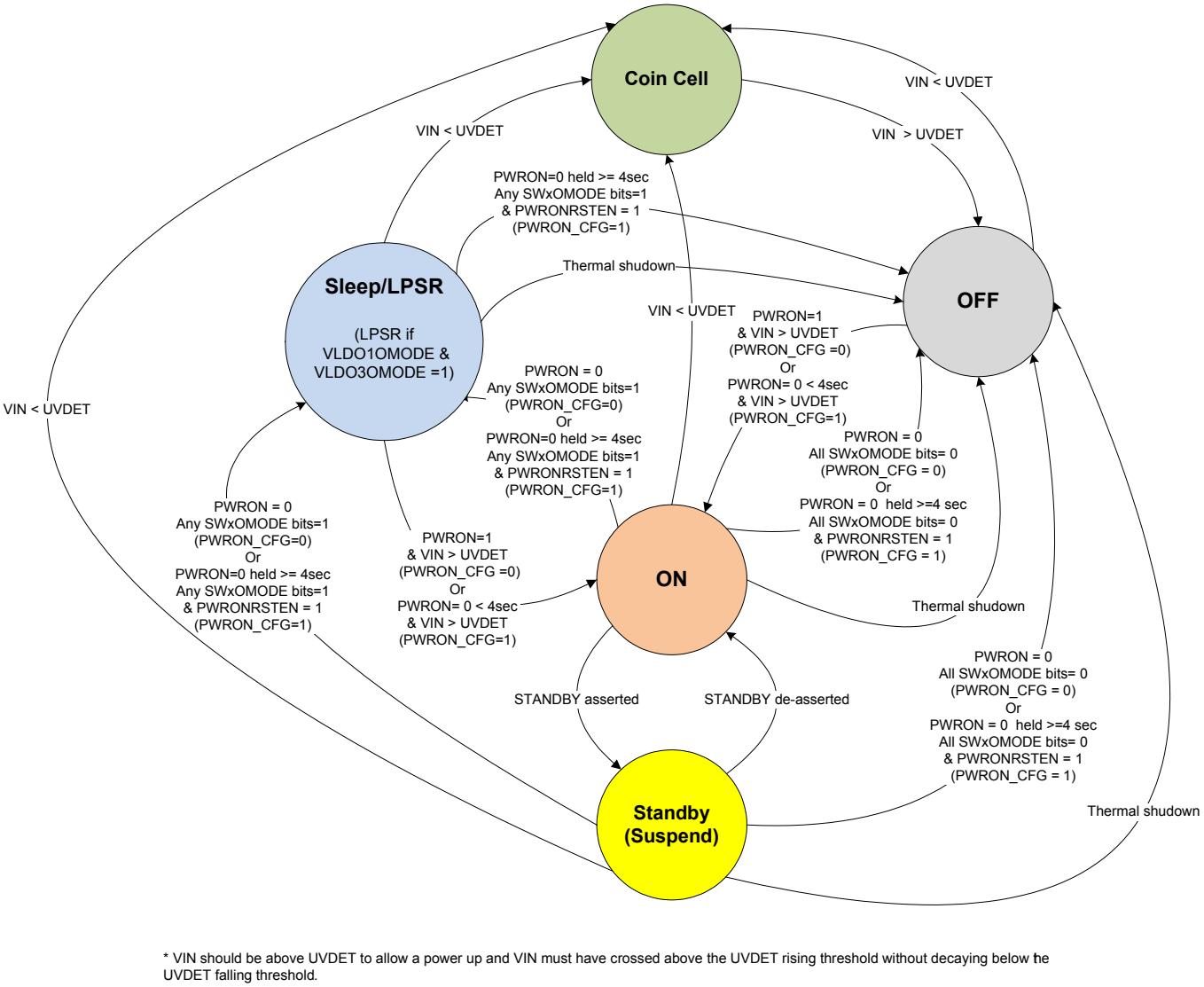
Table 73. Thermal protection thresholds

Parameter	Min.	Typ.	Max.	Units
Thermal 110 °C threshold (THERM110)	100	110	120	°C
Thermal 120 °C threshold (THERM120)	110	120	130	°C
Thermal 125 °C threshold (THERM125)	115	125	135	°C
Thermal 130 °C threshold (THERM130)	120	130	140	°C
Thermal warning hysteresis	2.0	–	4.0	°C
Thermal protection threshold	130	140	150	°C

6.5 Modes of operation

6.5.1 State diagram

The operation of the PF3000 can be reduced to five states, or modes: ON, OFF, Sleep, Standby, and Coin Cell. Figure 15 shows the state diagram of the PF3000, along with the conditions to enter and exit from each state.



* VIN should be above UVDET to allow a power up and VIN must have crossed above the UVDET rising threshold without decaying below the UVDET falling threshold.

Figure 15. State diagram

To complement the state diagram in Figure 15, a description of the states is provided in following sections. Note that V_{IN} must exceed the rising UVDET threshold to allow a power up. Refer to Table 32 for the UVDET thresholds. Additionally, I^2C control is not possible in the coin cell mode and the interrupt signal, INTB, is only active in sleep, standby, and ON states.

6.5.1.1 ON mode

The PF3000 enters the On mode after a turn-on event. RESETBMCU is de-asserted, and pulled high via an external pull-up resistor, in this mode of operation. To enter the On mode, V_{IN} voltage must surpass the rising UVDET threshold and PWRON must be asserted. From the On mode, when the voltage at V_{IN} drops below the undervoltage falling threshold, UVDET, the state machine transitions to the coin cell mode.

6.5.1.2 OFF mode

The PF3000 enters the Off mode after a turn-off event. Only VCOREDIG and VSNVS are powered in the mode of operation. To exit the Off mode, a valid turn-on event is required. RESETBMCU is asserted, LOW, in this mode. Turn off events can be achieved using the PWRON pin, thermal protection, as described below.

6.5.1.3 PWRON pin

The PWRON pin is used to power off the PF3000. The PWRON pin can be configured with OTP to power off the PMIC under the following two conditions:

1. PWRON_CFG bit = 0, SWxOMODE bit = 0 and PWRON pin is low.
2. PWRON_CFG bit = 1, SWxOMODE bit = 0, PWRONRSTEN = 1 and PWRON is held low for longer than 4.0 seconds. Alternatively, the system can be configured to restart automatically by setting the RESTARTEN bit.

6.5.1.4 Thermal protection

If the die temperature surpasses a given threshold, the thermal protection circuit powers off the PMIC to avoid damage. A turn-on event does not power on the PMIC while it is in thermal protection. The part remains in Off mode until the die temperature decreases below a given threshold. See Power dissipation section for more detailed information.

6.5.1.5 Standby mode

- Depending on STANDBY pin configuration, Standby is entered when the STANDBY pin is asserted. This is typically used for low-power mode of operation.
- When STANDBY is de-asserted, standby mode is exited.

A product may be designed to go into a low-power mode after periods of inactivity. The STANDBY pin is provided for board level control of going in and out of such deep sleep modes (DSM). When a product is in DSM, it may be able to reduce the overall platform current by lowering the regulator output voltage, changing the operating mode of the regulators or disabling some regulators. The configuration of the regulators in standby is pre-programmed through the I^2C interface. Note that the STANDBY pin is programmable for Active High or Active Low polarity, and that decoding of a standby event takes into account the programmed input polarity as shown in Table 74. When the PF3000 is powered up first, regulator settings for the standby mode are mirrored from the regulator settings for the ON mode. To change the STANDBY pin polarity to Active Low, set the STANDBYINV bit via software first, and then change the regulator settings for standby mode as required. For simplicity, STANDBY is generally be referred to as active high throughout this document.

Table 74. Standby pin and polarity control

STANDBY (Pin) (66)	STANDBYINV (I^2C bit) (67)	STANDBY Control (65)
0	0	0
0	1	1
1	0	1
1	1	0

Notes
65. STANDBY = 0: System is not in standby, STANDBY = 1: system is in standby
66. The state of the STANDBY pin only has influence in On mode.
67. Bit 6 in Power Control register (ADDR - 0x1B)

Since STANDBY pin activity is driven asynchronously to the system, a finite time is required for the internal logic to qualify and respond to the pin level changes. A programmable delay is provided to hold off the system response to a standby event. This allows the processor and peripherals some time after a standby instruction has been received to terminate processes to facilitate seamless entering into standby mode.

When enabled (STBYDLY = 01, 10, or 11) per Table 75, STBYDLY delays the standby initiated response for the entire IC, until the STBYDLY counter expires. An allowance should be made for three additional 32 kHz cycles required to synchronize the standby event.

Table 75. STANDBY delay - initiated response

STBYDLY[1:0] (68)	Function
00	No delay
01	One 32 kHz period (default)
10	Two 32 kHz periods
11	Three 32 kHz periods

Notes
68. Bits [5:4] in Power Control register (ADDR - 0x1B)

6.5.1.6 Sleep/LPSR mode

- Depending on PWRON pin configuration, sleep mode is entered when PWRON is de-asserted and SWxOMODE bit is set.
- To exit sleep mode, assert the PWRON pin.

In the sleep mode, the regulator uses the set point as programmed by SW1xOFF[3:0] for SW1A/B and by SWxOFF[2:0] for SW2 and SW3. The activated regulators maintains settings for this mode and voltage until the next turn-on event. Table 76 shows the control bits in sleep mode. During sleep mode, interrupts are active and the INTB pin reports any unmasked fault event. If LPSR is activated by requesting VDD_LPSR and VCC_GPIO to stay ON, LDO1 and LDO3 enables in low-power mode.

Table 76. Regulator mode control

SWxOMODE	Off operational mode (sleep) (69)
0	Off
1	PFM

Notes
69. For sleep mode, activated switching regulators, should use the Off mode set point as programmed by SW1xOFF[4:0] for SW1A/B and SW2OFF[2:0] for SW2, and SW3OFF[3:0] for SW3.

6.5.1.7 Coin cell mode

In the Coin Cell state, the coin cell is the only valid power source to the PMIC. No turn-on event is accepted in the Coin Cell state. Transition to the OFF state requires that V_{IN} surpasses UVDET threshold. RESETBMCU is held low in this mode. If the coin cell is depleted, a complete system reset occurs. At the next application of power and the detection of a turn-on event, the system re-initializes with all I^2C bits including, those that reset on COINPORB are restored to their default states.

6.5.2 State machine flow summary

Table 77 provides a summary matrix of the PF3000 flow diagram to show the conditions needed to transition from one state to another.

Table 77. State machine flow summary

STATE		Next state				
		OFF	**Coin cell**	**Sleep**	**Standby**	**ON**
Initial state	**OFF**	X	V_{IN} < UVDET	X	X	PWRON_CFG = 0 PWRON = 1 & V_{IN} > UVDET or PWRON_CFG = 1 PWRON = 0 < 4.0 s & V_{IN} > UNDET
	Coin cell	V_{IN} > UVDET	X	X	X	X
	Sleep/ LPSR	Thermal shutdown	V_{IN} < UVDET	X	X	PWRON_CFG = 0 PWRON = 1 & V_{IN} > UVDET or PWRON_CFG = 1 PWRON = 0 < 4.0 s & V_{IN} > UNDET
		PWRON_CFG = 1 PWRON = 0 ≥ 4.0 s Any SWxOMODE = 1 & PWRONRSTEN = 1		LPSR (LDO1 & LDO3 or V33 Enabled) if VLDO1OMODE =1 & VLDO3OMODE=1 or V33OMODE=1		
	Standby	Thermal shutdown	V_{IN} < UVDET	PWRON_CFG = 0 PWRON = 0 Any SWxOMODE = 1 or PWRON_CFG = 1 PWRON = 0 ≥ 4.0 s Any SWxOMODE = 1 & PWRONRSTEN = 1	X	Standby de-asserted
		PWRON_CFG = 0 PWRON = 0 All SWxOMODE = 0 or PWRON_CFG = 1 PWRON = 0 ≥ 4.0 s All SWxOMODE = 0 & PWRONRSTEN = 1				
	ON	Thermal shutdown	V_{IN} < UVDET	PWRON_CFG = 0 PWRON = 0 Any SWxOMODE = 1 or PWRON_CFG = 1 PWRON = 0 ≥ 4.0 s Any SWxOMODE = 1 & PWRONRSTEN = 1	Standby asserted	X
		PWRON_CFG = 0 PWRON = 0 All SWxOMODE = 0 or PWRON_CFG = 1 PWRON = 0 ≥ 4.0 s All SWxOMODE = 0 & PWRONRSTEN = 1				

6.5.3 Performance characteristics curves

(V_{IN} = 3.6 V, $SW1A_{OUT}$ = 1.0 V; $SW1B_{OUT}$ = 1.0 V, $SW2_{OUT}$ = 1.8 V, $SW3_{OUT}$ = 1 V, $SWBST_{OUT}$ = 5.0 V Switching frequency = 2.0 MHz, Mode = APS; $LDO1_{OUT}$ = 1.8 V, $LDO2_{OUT}$ = 1.0 V, $LDO3_{OUT}$ = 1.8 V, $LDO4_{OUT}$ = 1.8 V, $V33_{OUT}$ = 3.3 V, VCC_SD_{OUT} = 3.3 V, unless otherwise noted)

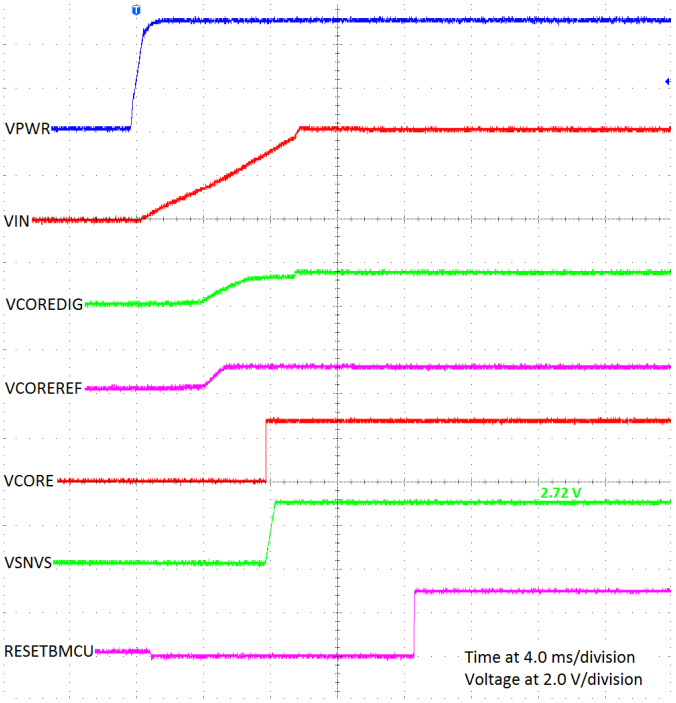


Figure 16. Typical startup waveforms

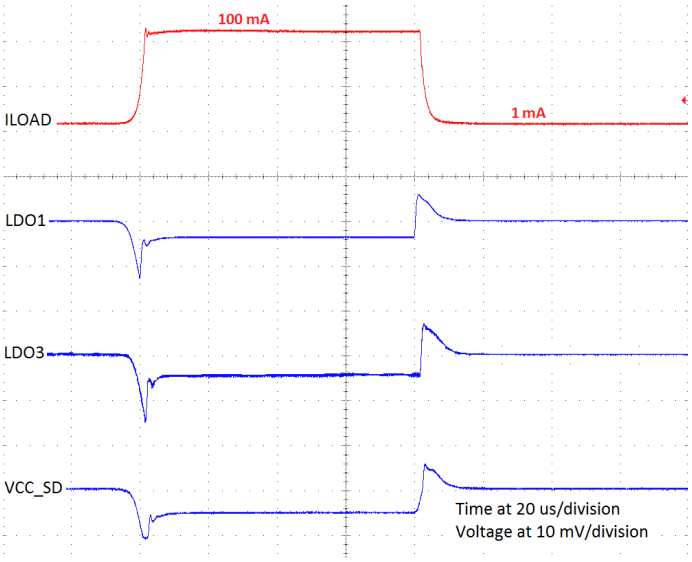


Figure 17. Load transient response - LDO1, LDO3 and VCC_SD

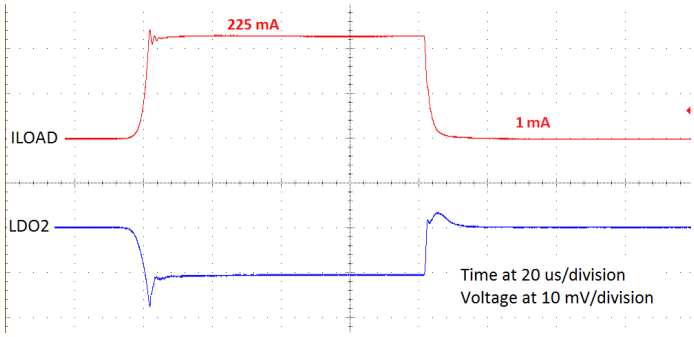


Figure 18. Load transient response - LDO2

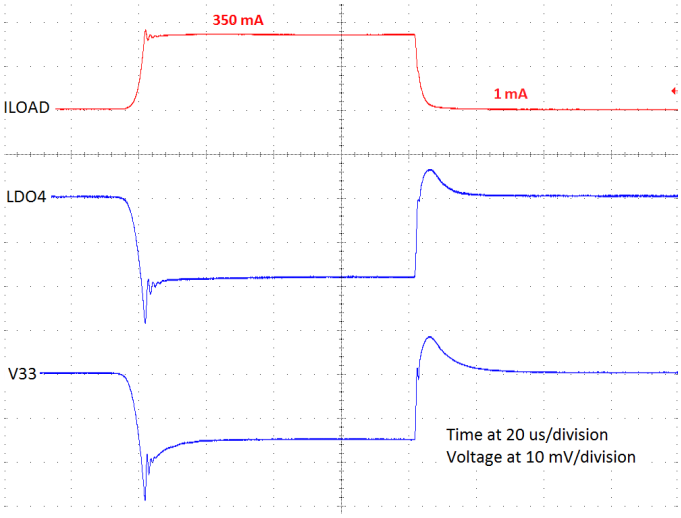


Figure 19. Load transient response - LDO4 and V33

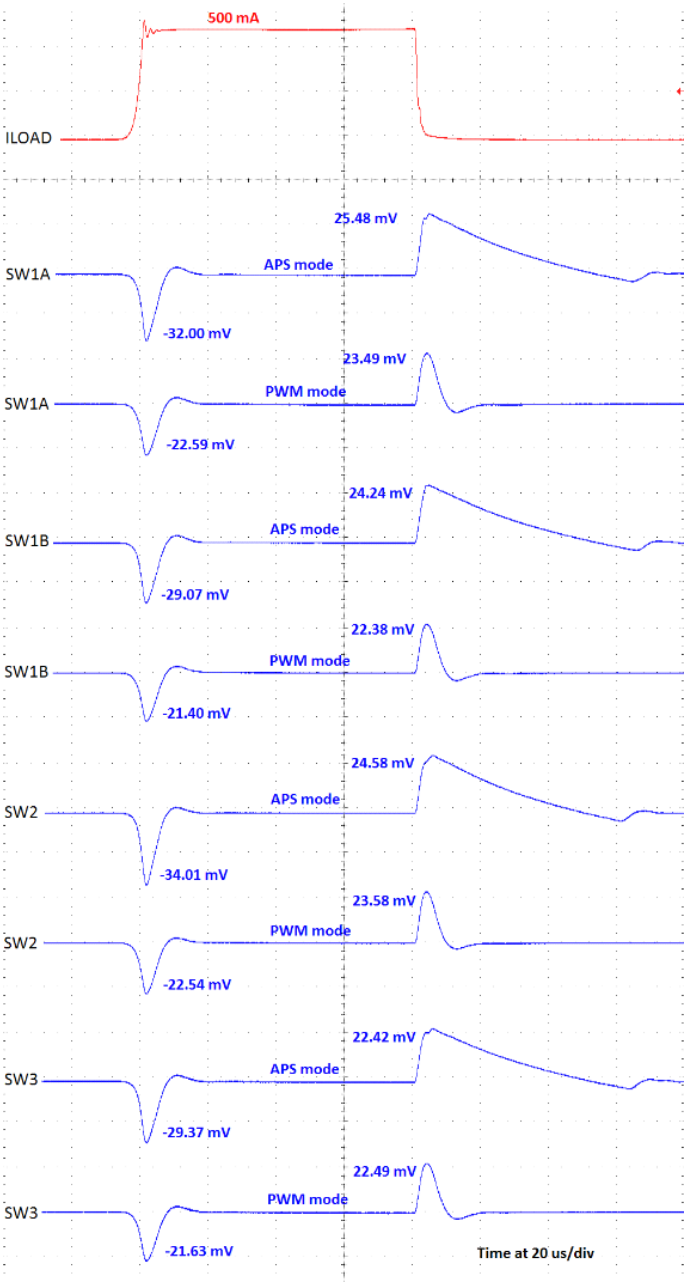


Figure 20. Load transient response - buck regulators

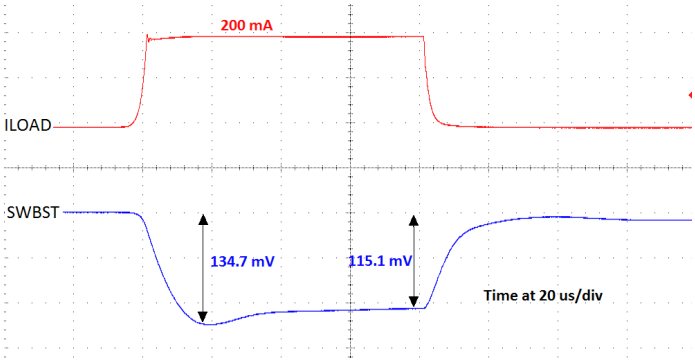


Figure 21. Load transient response - SWBST

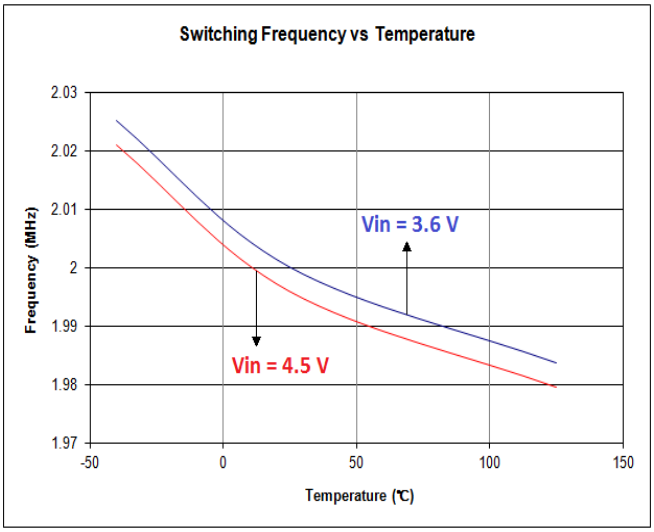


Figure 22. Switching frequency vs. temperature

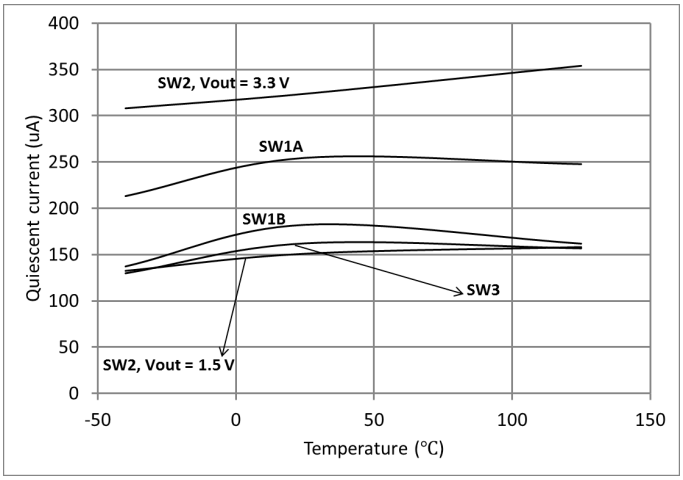


Figure 23. Quiescent current - buck regulators in APS mode

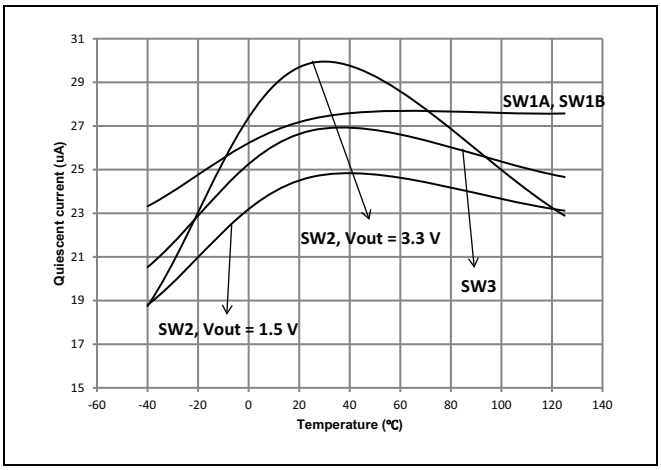


Figure 24. Quiescent current - buck regulators in PFM mode

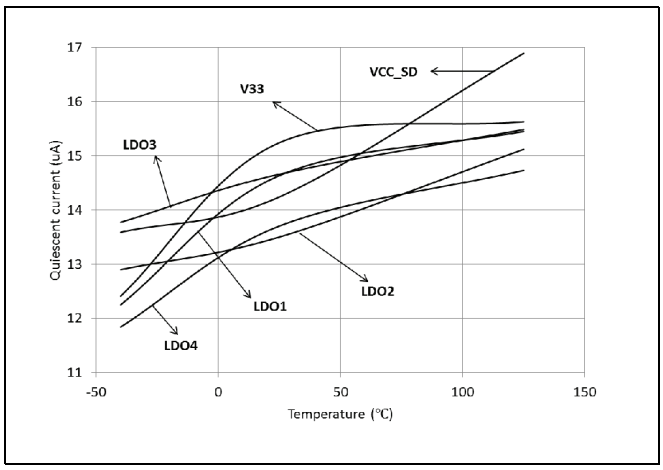


Figure 25. Quiescent current - LDOs

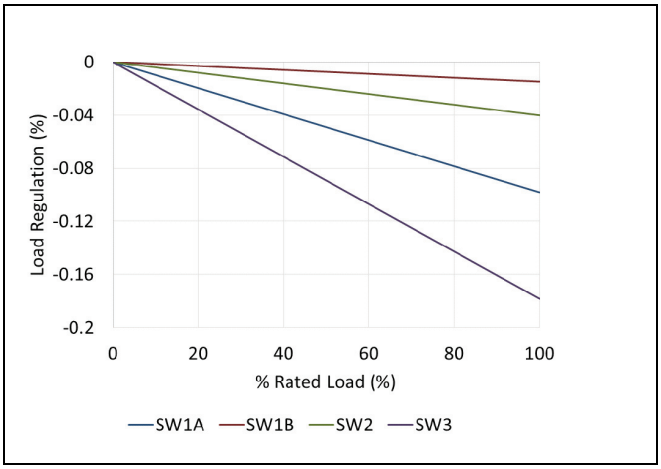


Figure 26. Load regulation - buck regulators

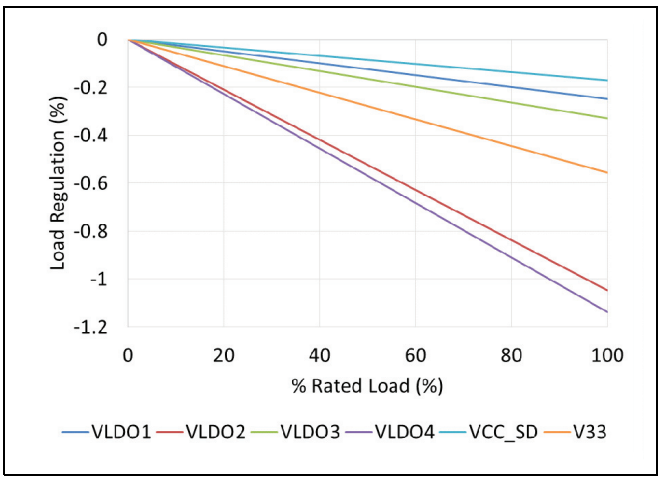


Figure 27. Load regulation - LDOs

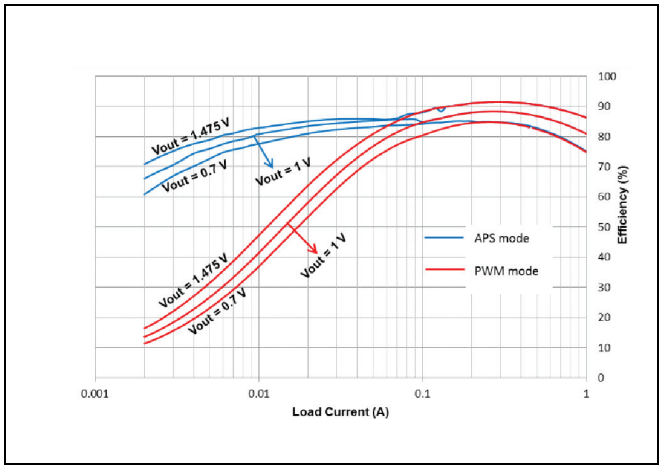


Figure 28. SW1A efficiency - APS and PWM modes

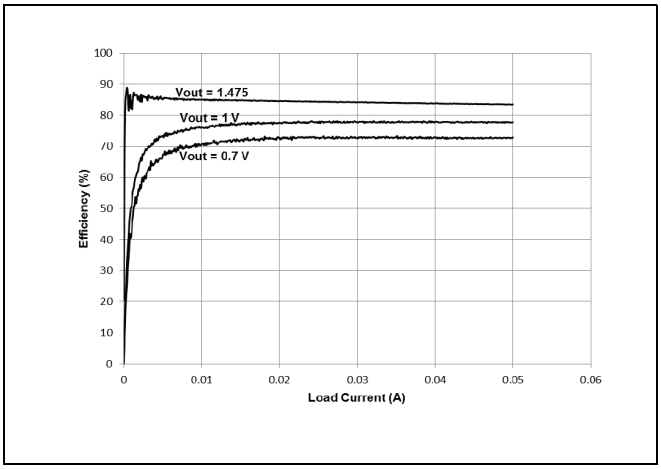


Figure 29. SW1A efficiency - PFM mode

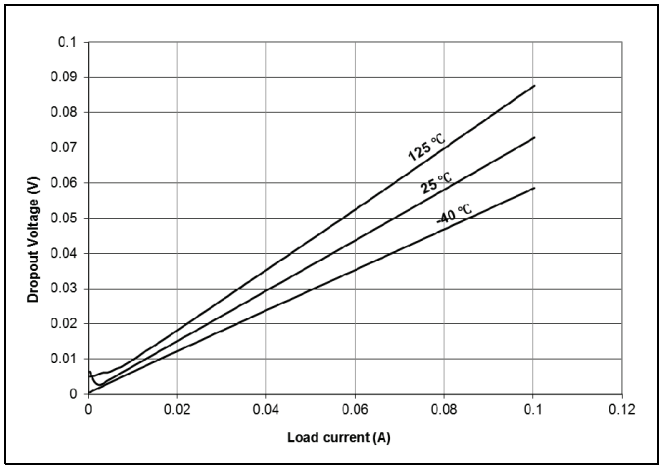


Figure 30. Dropout voltage - VLDO1, VLDO3, VCC_SD - V_{OUT} = 3.3 V

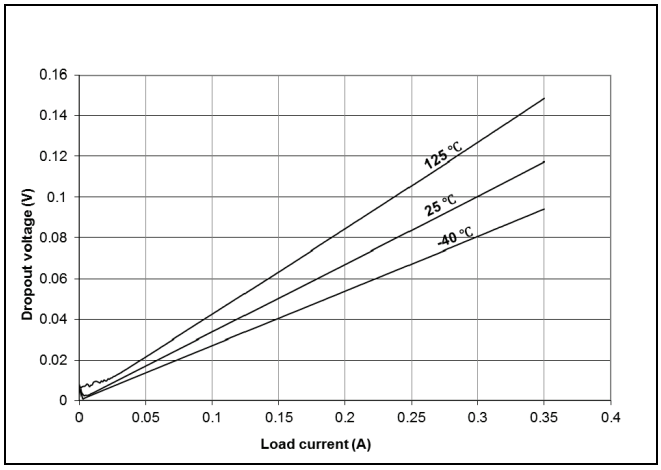


Figure 32. Dropout voltage - VLDO4, V33 - V_{OUT} = 3.3 V

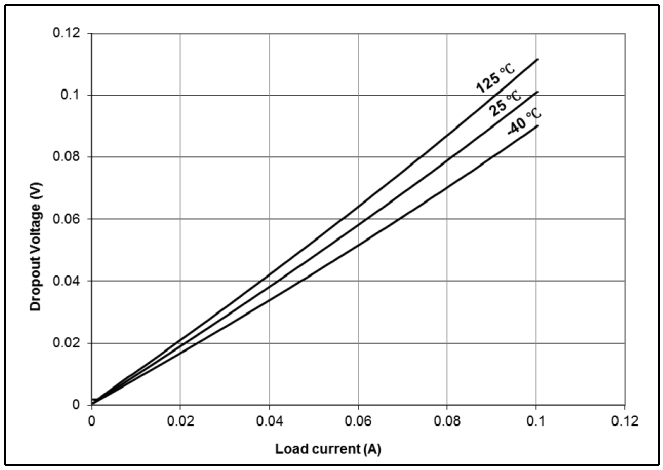


Figure 31. Dropout voltage - VLDO1, VLDO3, VCC_SD - V_{OUT} = 1.8 V

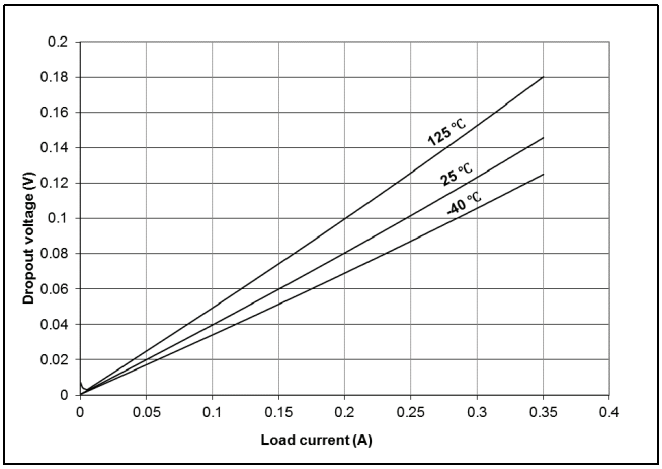


Figure 33. Dropout voltage - VLDO4 - V_{OUT} = 1.8 V

6.6 Control Interface I^2C block description

The PF3000 contains an I^2C interface port which allows access by a processor, or any I^2C master, to the register set. Via these registers the resources of the IC can be controlled. The registers also provide status information about how the IC is operating.

The SCL and SDA lines should be routed away from noisy signals and planes to minimize noise pick up. To prevent reflections in the SCL and SDA traces from creating false pulses, the rise and fall times of the SCL and SDA signals must be greater than 20 ns. This can be accomplished by reducing the drive strength of the I^2C master via software. It is recommended to use a drive strength of 80 Ω or higher to increase the edge times. Alternatively, this can be accomplished by using small capacitors from SCL and SDA to ground. For example, use 5.1 pF capacitors from SCL and SDA to ground for bus pull-up resistors of 4.8 kΩ.

6.6.1 I^2C device ID

I^2C interface protocol requires a device ID for addressing the target IC on a multi-device bus. The I^2C address is set to 0x08.

6.6.2 I²C operation

The I²C mode of the interface is implemented generally following the fast mode definition which supports up to 400 kbits/s operation (exceptions to the standard are noted to be 7-bit only addressing and no support for general call addressing.)

The I²C interface is configured as “Slave”.

Timing diagrams, electrical specifications, and further details can be found in the I²C specification, which is available for download at:

http://www.nxp.com/acrobat_download/literature/9398/39340011.pdf

I²C read operations are also performed in byte increments separated by an ACK. Read operations also begin with the MSB and each byte is sent out unless a STOP command or NACK is received prior to completion.

PF3000 only supports single-byte I²C transactions for read and write. The host initiates and terminates all communication. The host sends a master command packet after driving the start condition. The device responds to the host if the master command packet contains the corresponding slave address. In the following examples, the device is shown always responding with an ACK to transmissions from the host. If at any time a NACK is received, the host should terminate the current transaction and retry the transaction.

PF3000 uses the “repeated start” operation for reads as shown in Figure 35

.

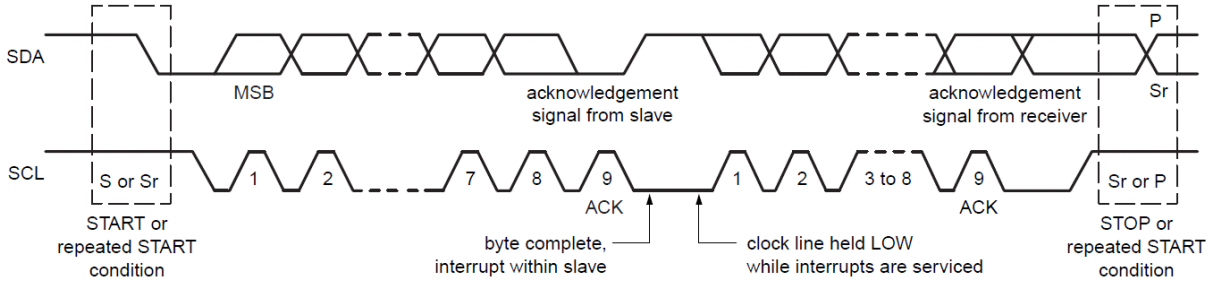


Figure 34. Data transfer on the I²C bus

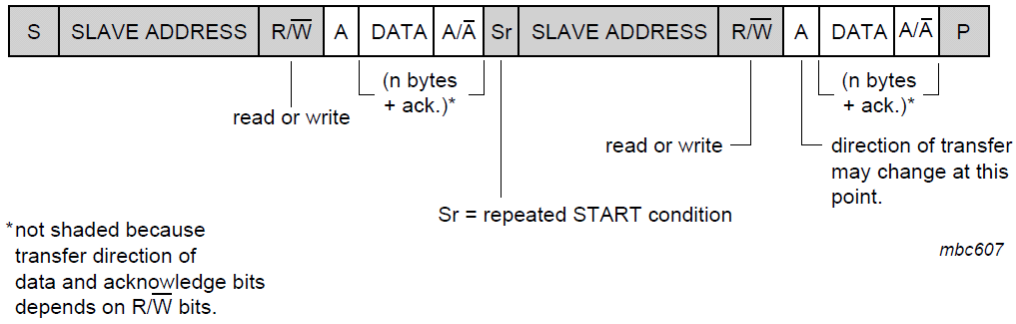


Figure 35. Read operation

6.6.3 Interrupt handling

The system is informed about important events based on interrupts. Unmasked interrupt events are signaled to the processor by driving the INTB pin low. Each interrupt is latched so that even if the interrupt source becomes inactive, the interrupt remains set until cleared. Each interrupt can be cleared by writing a “1” to the appropriate bit in the Interrupt Status register; this causes the INTB pin to go high. If there are multiple interrupt bits set the INTB pin remains low until all are either masked or cleared. If a new interrupt occurs while the processor clears an existing interrupt bit, the INTB pin remains low.

Each interrupt can be masked by setting the corresponding mask bit to a 1. As a result, when a masked interrupt bit goes high, the INTB pin does not go low. A masked interrupt can still be read from the Interrupt Status register. This gives the processor the option of polling for status from the IC. The IC powers up with all interrupts masked, so the processor must initially poll the device to determine if any interrupts are active. Alternatively, the processor can unmask the interrupt bits of interest. If a masked interrupt bit was already high, the INTB pin goes low after unmasking.

The sense registers contain status and input sense bits so the system processor can poll the current state of interrupt sources. They are read only, and not latched or clearable. Interrupts generated by external events are debounced; therefore, the event needs to be stable throughout the debounce period before an interrupt is generated. Nominal debounce periods for each event are documented in the INT summary Table 78. Due to the asynchronous nature of the debounce timer, the effective debounce time can vary slightly.

6.6.4 Interrupt bit summary

Table 78 summarizes all interrupt, mask, and sense bits associated with INTB control. For more detailed behavioral descriptions, refer to the related chapters.

Table 78. Interrupt, mask, and sense bits

Interrupt	Mask	Sense	Purpose	Trigger	Debounce time (ms)
LOWVINI	LOWVINM	LOWVINS	Low input voltage detect Sense is 1 if below 2.70 V threshold	H to L	3.9 (70)
PWRONI	PWRONM	PWRONS	Power on button event	H to L	31.25 (70)
			Sense is 1 if PWRON is high.	L to H	31.25
THERM110	THERM110M	THERM110S	Thermal 110 °C threshold Sense is 1 if above threshold	Dual	3.9
THERM120	THERM120M	THERM120S	Thermal 120 °C threshold Sense is 1 if above threshold	Dual	3.9
THERM125	THERM125M	THERM125S	Thermal 125 °C threshold Sense is 1 if above threshold	Dual	3.9
THERM130	THERM130M	THERM130S	Thermal 130 °C threshold Sense is 1 if above threshold	Dual	3.9
SW1AFAULTI	SW1AFAULTM	SW1AFAULTS	Regulator 1A overcurrent limit Sense is 1 if above current limit	L to H	8.0
SW1BFAULTI	SW1BFAULTM	SW1BFAULTS	Regulator 1C overcurrent limit Sense is 1 if above current limit	L to H	8.0
SW2FAULTI	SW2FAULTM	SW2FAULTS	Regulator 2 overcurrent limit Sense is 1 if above current limit	L to H	8.0
SW3FAULTI	SW3FAULTM	SW3FAULTS	Regulator 3 overcurrent limit Sense is 1 if above current limit	L to H	8.0
SWBSTFAULTI	SWBSTFAULTM	SWBSTFAULTS	SWBST overcurrent limit Sense is 1 if above current limit	L to H	8.0
VLDO1FAULTI	VLDO1FAULTM	VLDO1FAULTS	VLDO1 overcurrent limit Sense is 1 if above current limit	L to H	8.0
VLDO2FAULTI	VLDO2FAULTM	VLDO2FAULTS	VLDO2 overcurrent limit Sense is 1 if above current limit	L to H	8.0
VCC_SDFAULTI	VCC_SDFAULTM	VCC_SDFAULTS	VCC_SD overcurrent limit Sense is 1 if above current limit	L to H	8.0

Table 78. Interrupt, mask, and sense bits (continued)

Interrupt	Mask	Sense	Purpose	Trigger	Debounce time (ms)
V33FAULTI	V33FAULTM	V33FAULTS	V33 overcurrent limit Sense is 1 if above current limit	L to H	8.0
VLDO3FAULTI	VLDO3FAULTM	VLDO1FAULTS	VLDO3 overcurrent limit Sense is 1 if above current limit	L to H	8.0
VLDO4FAULTI	VLDO4FAULTM	VLDO4FAULTS	VLDO4 overcurrent limit Sense is 1 if above current limit	L to H	8.0
OTP_ECCI	OTP_ECCM	OTP_ECCS	1 or 2 bit error detected in OTP registers Sense is 1 if error detected	L to H	-
OTP_AUTO_BLOW	OTP_AUTO_BLOWM	OTP_AUTO_BLOWS	Interrupt to indicate completion of fuse auto blow	L to H	-
VPWROVI	VPWROVM	VPWROVS	VPWR pin overvoltage interrupt	L to H	0.122

Notes
70. Debounce timing for the falling edge can be extended with PWRONDBNC[1:0].

A full description of all interrupt, mask, and sense registers is provided in Table 79 to Table 90.

Table 79. Register INTSTAT0 - ADDR 0x05

Name	Bit #	R/W	Default	Description
PWRONI	0	R/W1C	0	Power on interrupt bit
LOWVINI	1	R/W1C	0	Low-voltage interrupt bit
THERM110I	2	R/W1C	0	110 °C Thermal interrupt bit
THERM120I	3	R/W1C	0	120 °C Thermal interrupt bit
THERM125I	4	R/W1C	0	125 °C Thermal interrupt bit
THERM130I	5	R/W1C	0	130 °C Thermal interrupt bit
Unused	7:6	–	0b00	Unused

Table 80. Register INTMASK0 - ADDR 0x06

Name	Bit #	R/W	Default	Description
PWRONM	0	R/W1C	1	Power on interrupt mask bit
LOWVINM	1	R/W1C	1	Low-voltage interrupt mask bit
THERM110M	2	R/W1C	1	110 °C thermal interrupt mask bit
THERM120M	3	R/W1C	1	120 °C thermal interrupt mask bit
THERM125M	4	R/W1C	1	125 °C thermal interrupt mask bit
THERM130M	5	R/W1C	1	130 °C thermal interrupt mask bit
Unused	7:6	–	0b00	Unused

Table 81. Register INTSENSE0 - ADDR 0x07

Name	Bit #	R/W	Default	Description
PWRONS	0	R	0	Power on sense bit 0 = PWRON low 1 = PWRON high
LOWVINS	1	R	0	Low-voltage sense bit 0 = VIN > 2.7 V 1 = VIN ≤ 2.7 V
THERM110S	2	R	0	110 °C thermal sense bit 0 = Below threshold 1 = Above threshold
THERM120S	3	R	0	120 °C thermal sense bit 0 = Below threshold 1 = Above threshold
THERM125S	4	R	0	125 °C thermal sense bit 0 = Below threshold 1 = Above threshold
THERM130S	5	R	0	130 °C thermal sense bit 0 = Below threshold 1 = Above threshold
ICTESTS	6	R	0	0 = ICTEST pin is grounded 1 = ICTEST to VCOREDIG or greater
VDDOTPS	7	R	0	Additional VDDOTP voltage sense pin 0 = VDDOTP grounded 1 = VDDOTP to VCOREDIG or greater

Table 82. Register INTSTAT1 - ADDR 0x08

Name	Bit #	R/W	Default	Description
SW1AFAULTI	0	R/W1C	0	SW1A overcurrent interrupt bit
SW1BFAULTI	1	R/W1C	0	SW1B overcurrent interrupt bit
Unused	2	R/W1C	0	Unused
SW2FAULTI	3	R/W1C	0	SW2 Overcurrent interrupt bit
SW3FAULTI	4	R/W1C	0	SW3 Overcurrent interrupt bit
Unused	5	R/W1C	0	Unused
Unused	6	R/W1C	0	Unused
Unused	7	–	0	Unused

Table 83. Register INTMASK1 - ADDR 0x09

Name	Bit #	R/W	Default	Description
SW1AFAULTM	0	R/W	1	SW1A overcurrent interrupt mask bit
SW1BFAULTM	1	R/W	1	SW1B overcurrent interrupt mask bit
Unused	2	R/W	1	Unused
SW2FAULTM	3	R/W	1	SW2 overcurrent interrupt mask bit
SW3FAULTM	4	R/W	1	SW3 overcurrent interrupt mask bit
Unused	5	R/W	1	Unused
Unused	6	R/W	1	Unused
Unused	7	–	0	Unused

Table 84. Register INTSENSE1 - ADDR 0x0A

Name	Bit #	R/W	Default	Description
SW1AFAULTS	0	R	0	SW1A overcurrent sense bit 0 = Normal operation 1 = Above current limit
Unused	1	R	0	Unused
SW1BFAULTS	2	R	0	SW1B overcurrent sense bit 0 = Normal operation 1 = Above current limit
SW2FAULTS	3	R	0	SW2 overcurrent sense bit 0 = Normal operation 1 = Above current limit
SW3FAULTS	4	R	0	SW3 overcurrent sense bit 0 = Normal operation 1 = Above current limit
Unused	5	R	0	Unused
Unused	6	R	0	Unused
Unused	7	–	0	Unused

Table 85. Register INTSTAT3 - ADDR 0x0E

Name	Bit #	R/W	Default	Description
SWBSTFAULTI	0	R/W1C	0	SWBST overcurrent limit interrupt bit
Unused	1	–	0b0	Unused
VPWROVI	2	R/W1C	0b0	High when overvoltage event is detected in the front-end LDO circuit. This bit defaults to 0b1 when VPWR is grounded and the VIN path is used to power the PF3000.
Unused	5:3	–	0b0	Unused
OTP AUTO BLOW	6	R/W1C	0b0	High after auto fuse blow sequence is completed
OTP_ECCI	7	R/W1C	0	OTP error interrupt bit

Table 86. Register INTMASK3 - ADDR 0x0F

Name	Bit #	R/W	Default	Description
SWBSTFAULTM	0	R/W	1	SWBST overcurrent limit interrupt mask bit
Unused	1	–	0	Unused
VPWROVM	2	R/W	1	VPWR overvoltage interrupt mask bit
Unused	5:3	–	0b000	Unused
OTP_AUTO_BLOW_DONE_M	6	R/W	1	OTP auto blow mask bit
OTP_ECCM	7	R/W	1	OTP error interrupt mask bit

Table 87. Register INTSENSE3 - ADDR 0x10

Name	Bit #	R/W	Default	Description
SWBSTFAULTS	0	R	0	SWBST overcurrent limit sense bit 0 = Normal operation 1 = Above current limit
Unused	1	–	0b0	Unused
VPWROVS	2	R	0	VPWR overvoltage interrupt sense bit
Unused	5:3	–	0b000	Unused
OTP_AUTO_BLOW_DONE_S	6	R	0	OTP auto blow sense bit. This bit is high while the auto blow sequence is running. Do not read/write the OTP TBB registers while this bit is 1.
OTP_ECCS	7	R	0	OTP error sense bit 0 = No error detected 1 = OTP error detected

Table 88. Register INTSTAT4 - ADDR 0x11

Name	Bit #	R/W	Default	Description
VLDO1FAULTI	0	R/W1C	0	VLDO1 overcurrent interrupt bit
VLDO2FAULTI	1	R/W1C	0	VLDO2 overcurrent interrupt bit
VCC_SDFAULTI	2	R/W1C	0	VCC_SD overcurrent interrupt bit
V33FAULTI	3	R/W1C	0	V33 overcurrent interrupt bit
VLDO3FAULTI	4	R/W1C	0	VLDO3 overcurrent interrupt bit
VLDO4FAULTI	5	R/W1C	0	VLDO4 overcurrent interrupt bit
Unused	7:6	–	0b00	Unused

Table 89. Register INTMASK4 - ADDR 0x12

Name	Bit #	R/W	Default	Description
VLDO1FAULTM	0	R/W	1	VLDO1 overcurrent interrupt mask bit
VLDO2FAULTM	1	R/W	1	VLDO2 overcurrent interrupt mask bit
VCC_SDFAULTM	2	R/W	1	VCC_SD overcurrent interrupt mask bit
V33FAULTM	3	R/W	1	V33 overcurrent interrupt mask bit
VLDO3FAULTM	4	R/W	1	VLDO3 overcurrent interrupt mask bit
VLDO4FAULTM	5	R/W	1	VLDO4 overcurrent interrupt mask bit
Unused	7:6	–	0b00	Unused

Table 90. Register INTSENSE4 - ADDR 0x13

Name	Bit #	R/W	Default	Description
VLDO1FAULTS	0	R	0	VLDO1 overcurrent sense bit 0 = Normal operation 1 = Above current limit
VLDO2FAULTS	1	R	0	VLDO2 overcurrent sense bit 0 = Normal operation 1 = Above current limit
VCC_SDFAULTS	2	R	0	VCC_SD overcurrent sense bit 0 = Normal operation 1 = Above current limit

Table 90. Register INTSENSE4 - ADDR 0x13 (continued)

Name	Bit #	R/W	Default	Description
V33FAULTS	3	R	0	V33 overcurrent sense bit 0 = Normal operation 1 = Above current limit
VLDO3FAULTS	4	R	0	VLDO3 overcurrent sense bit 0 = Normal operation 1 = Above current limit
VLDO4FAULTS	5	R	0	VLDO4 overcurrent sense bit 0 = Normal operation 1 = Above current limit
Unused	7:6	–	0b00	Unused

6.6.5 Specific registers

6.6.5.1 IC and version identification

The IC and other version details can be read via identification bits. These are hard-wired on the chip and described in Table 91 to Table 93.

Table 91. Register DEVICEID - ADDR 0x00

Name	Bit #	R/W	Default	Description
DEVICEID	3:0	R	0x0	0000 = PF3000
FAMILY	7:4	R	0x3	0011 = PF3000

Table 92. Register SILICON REV- ADDR 0x03

Name	Bit #	R/W	Default	Description
METAL_LAYER_REV	3:0	R	0x0	Represents the metal mask revision Pass 0.0 = 0000 … Pass 0.15 = 1111
FULL_LAYER_REV	7:4	R	0x1	Represents the full mask revision Pass 1.0 = 0001 … Pass 15.0 = 1111

Table 93. Register FABID - ADDR 0x04

Name	Bit #	R/W	Default	Description
FIN	1:0	R	0b00	Allows for characterizing different options within the same reticule
FAB	3:2	R	0b00	Represents the wafer manufacturing facility
Unused	7:4	R	0b0000	Unused

6.6.5.2 Embedded memory

There are four register banks of general purpose embedded memory to store critical data. The data written to MEMA[7:0], MEMB[7:0], MEMC[7:0], and MEMD[7:0] is maintained by the coin cell when the main battery is deeply discharged, removed, or contact-bounced. The contents of the embedded memory are reset by COINPORB. The banks can be used for any system need for bit retention with coin cell backup.

Table 94. Register MEMA ADDR 0x1C

Name	Bit #	R/W	Default	Description
MEMA	7:0	R/W	0x00	Memory bank A

Table 95. Register MEMB ADDR 0x1D

Name	Bit #	R/W	Default	Description
MEMB	7:0	R/W	0x00	Memory bank B

Table 96. Register MEMC ADDR 0x1E

Name	Bit #	R/W	Default	Description
MEMC	7:0	R/W	0x00	Memory bank C

Table 97. Register MEMD ADDR 0x1F

Name	Bit #	R/W	Default	Description
MEMD	7:0	R/W	0x00	Memory bank D

6.6.5.3 Register descriptions

This section describes all the PF3000 registers and their individual bits. Address order is as listed in Register map.

6.6.5.3.1 Interrupt status register 0 (INTSTAT0)

INSTAT0 is one of the four status interrupt registers. This register contains six status flags. Write a logic 1 to clear a flag.

Table 98. Status interrupt register 0 (INTSTAT0)

Address: 0x05 functional page **Access: User read/write [71]**

	7	6	5	4	3	2	1	0
R W			THERM130I	THERM125I	THERM120I	THERM110I	LOWVINI	PWRONI
Default	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Notes
71. Read: Anytime
Write: Anytime

Table 99. INTSTAT0 field descriptions

Field	Description
5 THERM130I	**130 °C Thermal interrupt bit** — THERM130I is set to 1 when the THERM130 threshold specified in is crossed in either direction (bi-directional). This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 Die temperature has not crossed THERM130 threshold. 1 Die temperature has crossed THERM130 threshold.
4 THERM125I	**125 °C Thermal interrupt bit** — THERM125I is set to 1 when the THERM125 threshold specified in is crossed in either direction (bi-directional). This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 Die temperature has not crossed THERM125 threshold. 1 Die temperature has crossed THERM125 threshold.
3 THERM120I	**120 °C Thermal interrupt bit** — THERM120I is set to 1 when the THERM120 threshold specified in is crossed in either direction (bi-directional). This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 Die temperature has not crossed THERM120 threshold. 1 Die temperature has crossed THERM120 threshold.
2 THERM110I	**110 °C Thermal interrupt bit** — THERM110I is set to 1 when the THERM110 threshold specified in is crossed in either direction (bi-directional). This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 Die temperature has not crossed THERM110 threshold. 1 Die temperature has crossed THERM110 threshold.
1 LOWVINI	**Low-voltage interrupt bit** — LOWVINI is set to 1 when a low-voltage event occurs on VIN. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 V_{IN} > 2.7 V (typical) 1 V_{IN} < 2.7 V (typical)
0 PWRONI	**Power on interrupt bit** —PWRONI is set to 1 when the turn on event occurs. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 Power on has not occurred. 1 Power on has occurred.

6.6.5.3.2 Interrupt status mask register 0 (INTMASK0)

INTMASK0 is the mask register for the status interrupt register INTSTAT0. Write a logic 0 to a bit to unmask the corresponding interrupt. When unmasked, the corresponding interrupt state is reflected on the INTB pin.

Table 100. Interrupt status mask register 0 (INTMASK0)

Address: 0x06 functional page — **Access: User read/write** (72)

	7	6	5	4	3	2	1	0
R W			THERM130M	THERM125M	THERM120M	THERM110M	LOWVINM	PWRONM
Default	0	0	1	1	1	1	1	1

= Unimplemented or Reserved

Notes

72. Read: Anytime
Write: Anytime

Table 101. INTMASK0 field descriptions

Field	Description
5 THERM130M	130 °C Thermal interrupt mask bit 0 THERM130I Unmasked 1 THERM130I Masked
4 THERM125M	125 °C Thermal interrupt mask bit 0 THERM125I Unmasked 1 THERM125I Masked
3 THERM120M	120 °C Thermal interrupt mask bit 0 THERM120I Unmasked 1 THERM120I Masked
2 THERM110M	110 °C Thermal interrupt mask bit 0 THERM110I Unmasked 1 THERM110I Masked
1 LOWVINM	Low-voltage interrupt mask bit 0 LOWVINI Unmasked 1 LOWVINI Masked
0 PWRONM	Power on interrupt mask bit 0 PWRONI Unmasked 1 PWRONI Masked

6.6.5.3.3 Interrupt sense register 0 (INTSENSE0)

This register has seven read-only sense bits. These sense bits reflects the actual state of the corresponding function.

Table 102. Interrupt sense register 0 (INTSENSE0)

Address: 0x07 functional page — **Access: User read-only** (73)

	7	6	5	4	3	2	1	0
R	VDDOTPS		THERM130S	THERM125S	THERM120S	THERM110S	LOWVINS	PWRONS
W								
Default	X (77)	0	X (76)	X (76)	X (76)	X (76)	X (75)	X (74)

= Unimplemented or Reserved

Notes
73. Read: Anytime
74. Default value depends on the initial PWRON pin state.
75. Default value depends on the initial VIN voltage.
76. Default value depends on the initial temperature of the die.
77. Default value depends on the initial VDDOTP pin state.

Table 103. INTSENSE0 field descriptions

Field	Description
7 VDDOTPS	**VDDOTP voltage sense bit** 0 VDDOTP grounded. 1 VDDOTP to VCOREDIG or greater.
5 THERM130S	**130 °C thermal interrupt sense bit** 0 Die temperature below THERM130 threshold. 1 Die temperature above THERM130 threshold.
4 THERM125S	125 °C thermal interrupt sense bit 0 Die temperature below THERM125 threshold. 1 Die temperature has crossed THERM125 threshold.

Table 103. INTSENSE0 field descriptions (continued)

Field	Description
3 THERM120S	120 °C thermal interrupt sense bit 0 Die temperature below THERM120 threshold. 1 Die temperature has crossed THERM120 threshold.
2 THERM110S	110 °C thermal interrupt sense bit 0 Die temperature below THERM110 threshold. 1 Die temperature has crossed THERM110 threshold.
1 LOWVINS	Low-voltage interrupt sense bit 0 V_{IN} > 2.7 V (typical) 1 V_{IN} < 2.7 V (typical)
0 PWRONS	Power on interrupt sense bit 0 PWRON low. 1 PWRON high.

6.6.5.3.4 Interrupt status register 1 (INTSTAT1)

INSTAT1 is one of the four status interrupt registers. This register contains four status flags. Write a logic 1 to clear a flag.

Table 104. Status interrupt register 1 (INTSTAT1)

Address: 0x08 functional page **Access: User read/write** (78)

	7	6	5	4	3	2	1	0
R W				SW3FAULTI	SW2FAULTI		SW1BFAULTI	SW1AFAULTI
Default	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Notes
78. Read: Anytime
Write: Anytime

Table 105. INTSTAT1 field descriptions

Field	Description
4 SW3FAULTI	**SW3 overcurrent interrupt bit** — SW3FAULTI is set to 1 when the SW3 regulator is in current limit protection. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 SW3 in normal operation 1 SW3 above current limit
3 SW2FAULTI	**SW2 overcurrent interrupt bit** — SW2FAULTI is set to 1 when the SW2 regulator is in current limit protection. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 SW2 in normal operation 1 SW2 above current limit
1 SW1BFAULTI	**SW1B overcurrent interrupt bit** — SW1BFAULTI is set to 1 when the SW1B regulator is in current limit protection. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 SW1B in normal operation 1 SW1B above current limit
0 SW1AFAULTI	**SW1A overcurrent interrupt bit** — SW1AFAULTI is set to 1 when the SW1A regulator is in current limit protection. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 SW1A in normal operation 1 SW1A above current limit

6.6.5.3.5 Interrupt status mask register 1 (INTMASK1)

INTMASK1 is the mask register for the status interrupt register INTSTAT1. Write a logic 0 to a bit to unmask the corresponding interrupt. When unmasked, the corresponding interrupt state is reflected on the INTB pin.

Table 106. Interrupt status mask register 1 (INTMASK1)

Address: 0x09 functional page							Access: User read/write (79)	
	7	6	5	4	3	2	1	0
R W				SW3FAULTM	SW2FAULTM		SW1BFAULTM	SW1AFAULTM
Default	0	0	0	1	1	0	1	1

= Unimplemented or Reserved

Notes
79. Read: Anytime
Write: Anytime

Table 107. INTMASK1 field descriptions

Field	Description
4 SW3FAULTM	SW3 overcurrent interrupt mask bit 0 SW3FAULTI Unmasked 1 SW3FAULTI Masked
3 SW2FAULTM	SW2 overcurrent interrupt mask bit 0 SW2FAULTI Unmasked 1 SW2FAULTI Masked
1 SW1BFAULTM	SW1B overcurrent interrupt mask bit 0 SW1BFAULTI Unmasked 1 SW1BFAULTI Masked
0 SW1AFAULTM	SW1A overcurrent interrupt mask bit 0 SW1AFAULTI Unmasked 1 SW1AFAULTI Masked

6.6.5.3.6 Interrupt sense register 1 (INTSENSE1)

This register has four read-only sense bits. These sense bits reflect the actual state of the corresponding function.

Table 108. Interrupt sense register 1 (INTSENSE1)

Address: 0x0A functional page							Access: User read-only (80)	
	7	6	5	4	3	2	1	0
R				SW3FAULTS	SW2FAULTS		SW1BFAULTS	SW1AFAULTS
W								
Default	0	0	0	X (81)	X (81)	0	X (81)	X (81)

= Unimplemented or Reserved

Notes
80. Read: Anytime
81. Default value depends on the regulator initial state

Table 109. INTSENSE1 field descriptions

Field	Description
4 SW3FAULTS	SW3 overcurrent sense bit 0 SW3 in normal operation 1 SW3 above current limit
3 SW2FAULTS	SW2 overcurrent sense bit 0 SW2 in normal operation 1 SW2 above current limit
1 SW1BFAULTS	SW1B overcurrent sense bit 0 SW1B in normal operation 1 SW1B above current limit
0 SW1AFAULTS	SW1A overcurrent sense bit 0 SW1A in normal operation 1 SW1A above current limit

6.6.5.3.7 Interrupt status register 3 (INTSTAT3)

INSTAT3 is one of the four status interrupt registers. This register contains four status flags. Write a logic 1 to clear a flag.

Table 110. Status Interrupt Register 3 (INTSTAT3)

Address: 0x0E functional page **Access: User read/write (82)**

	7	6	5	4	3	2	1	0
R W	OTP_ECCI	OTP_AUTO_BLOW_DONEI				VPWROVI		SWBSTFAULTI
Default	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Notes
82. Read: Anytime
Write: Anytime

Table 111. INTSTAT3 field descriptions

Field	Description
7 OTP_ECCI	**OTP error interrupt bit** — OTP_ECCI is set to 1 when an error is detected in OTP registers. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 No error detected 1 OTP error detected
6 OTP_AUTO_BLOW_DONEI	**OTP auto fuse blow interrupt bit** — OTP_AUTO_BLOW_DONEI is set to 1 after the auto fuse blow sequence is completed. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 OTP auto fuse blow sequence not completed 1 OTP auto fuse blow sequence completed
2 VPWROVI	**VPWR overvoltage interrupt bit** — High when an overvoltage event is detected in the front-end LDO circuit. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 VPWR in normal operation range. 1 VPWR in overvoltage range.
0 SWBSTFAULTI	**SWBST overcurrent limit interrupt bit** — SWBSTFAULTI is set to 1 when the SWBST regulator is in current limit protection. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 SWBST in normal operation 1 SWBST above current limit

6.6.5.3.8 Interrupt status mask register 3 (INTMASK3)

INTMASK3 is the mask register for the status interrupt register INTSTAT3. Write a logic 0 to a bit to unmask the corresponding interrupt. When unmasked, the corresponding interrupt state is reflected on the INTB pin.

Table 112. Interrupt status mask register 3 (INTMASK3)

Address: 0x0F functional page							Access: User read/write (83)	
	7	6	5	4	3	2	1	0
R W	OTP_ECCM	OTP_AUTO_BLOW_DONEM				VPWROVM		SWBSTFAULTM
Default	1	1	0	0	0	1	0	1

= Unimplemented or Reserved

Notes
83. Read: Anytime
Write: Anytime

Table 113. INTMASK3 field descriptions

Field	Description
7 OTP_ECCM	OTP error interrupt mask bit 0 OTP_ECCI Unmasked 1 OTP_ECCI Masked
6 OTP_AUTO_BLOW_DONEM	OTP auto blow mask bit 0 OTP_AUTO_BLOW_DONEI Unmasked 1 OTP_AUTO_BLOW_DONEI Masked
2 VPWROVM	VPWR overvoltage interrupt mask bit 0 VPWROVI Unmasked 1 VPWROVI Masked
0 SWBSTFAULTM	SWBST overcurrent limit interrupt mask bit 0 SWBSTFAULTI Unmasked 1 SWBSTFAULTI Masked

6.6.5.3.9 Interrupt sense register 3 (INTSENSE3)

This register has four read-only sense bits. These sense bits reflect the actual state of the corresponding function.

Table 114. Interrupt sense register 3 (INTSENSE3)

Address: 0x10 functional page							Access: User read-only (84)	
	7	6	5	4	3	2	1	0
R	OTP_ECCS	OTP_AUTO_BLOW_DONES				VPWROVS		SWBSTFAULTS
W								
Default	0	0	0	0	0	0	0	X (85)

= Unimplemented or Reserved

Notes
84. Read: Anytime
85. Default value depends on the regulator initial state

Table 115. INTSENSE3 field descriptions

Field	Description
7 OTP_ECCS	OTP error sense bit 0 No error detected 1 OTP error detected
6 OTP_AUTO_BLOW_DONES	**OTP auto blow sense bit** — This bit is high while the auto blow sequence is running. Do not read/write the OTP TBB registers while this bit is 1. 0 SW2 in normal operation 1 SW2 at current limit
2 VPWROVS	VPWR overvoltage interrupt sense bit 0 VPWR in normal operation range. 1 VPWR in overvoltage range.
0 SWBSTFAULTS	SWBST overcurrent limit sense bit 0 SWBST in normal operation 1 SWBST above current limit

6.6.5.3.10 Interrupt status register 4 (INTSTAT4)

INSTAT4 is one of the four status interrupt registers. This register contains six status flags. Write a logic 1 to clear a flag.

Table 116. Status interrupt register 4 (INTSTAT4)

Address: 0x11 functional page **Access: User read/write (86)**

	7	6	5	4	3	2	1	0
R W			VLDO4FAULTI	VLDO3FAULTI	V33FAULTI	VCC_SDFAULTI	VLDO2FAULTI	VLDO1FAULTI
Default	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Notes
86. Read: Anytime
Write: Anytime

Table 117. INTSTAT4 field descriptions

Field	Description
5 VLDO4FAULTI	**VLDO4 overcurrent interrupt bit** — VLDO4FAULTI is set to 1 when the VLDO4 regulator is in current limit protection. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 VLDO4 in normal operation 1 VLDO4 above current limit
4 VLDO3FAULTI	**VLDO3 overcurrent interrupt bit** — VLDO3FAULTI is set to 1 when the VLDO3 regulator is in current limit protection. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 VLDO3 in normal operation 1 VLDO3 above current limit
3 V33FAULTI	**V33 overcurrent interrupt bit** — V33FAULTI is set to 1 when the V33 regulator is in current limit protection. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 V33 in normal operation 1 V33 above current limit

Table 117. INTSTAT4 field descriptions (continued)

Field	Description
2 VCC_SDFAULTI	**VCC_SD overcurrent interrupt bit** — VCC_SDFAULTI is set to 1 when the VCC_SD regulator is in current limit protection. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 VCC_SD in normal operation 1 VCC_SD above current limit
1 VLDO2FAULTI	**VLDO2 overcurrent interrupt bit** — VLDO2FAULTI is set to 1 when the VLDO2 regulator is in current limit protection. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 VLDO2 in normal operation range. 1 VLDO2 above current limit
0 VLDO1FAULTI	**VLDO1 overcurrent interrupt bit** — SWBSTFAULTI is set to 1 when the SWBST regulator is in current limit protection. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 VLDO1 in normal operation range. 1 VLDO1 above current limit

6.6.5.3.11 Interrupt status mask register 4 (INTMASK4)

INTMASK4 is the mask register for the status interrupt register INTSTAT4. Write a logic 0 to a bit to unmask the corresponding interrupt. When unmasked, the corresponding interrupt state is reflected on the INTB pin.

Table 118. Interrupt status mask register 4 (INTMASK4)

Address: 0x12 functional page **Access: User read/write (87)**

	7	6	5	4	3	2	1	0
R W			VLDO4FAULTM	VLDO3FAULTM	V33FAULTM	VCC_SDFAULTM	VLDO2FAULTM	VLDO1FAULTM
Default	0	0	1	1	1	1	1	1

= Unimplemented or Reserved

Notes
87. Read: Anytime
Write: Anytime

Table 119. INTMASK4 field descriptions

Field	Description
5 VLDO4FAULTM	VLDO4 overcurrent interrupt mask bit 0 VLDO4FAULTI Unmasked 1 VLDO4FAULTI Masked
4 VLDO3FAULTM	VLDO3 overcurrent interrupt mask bit 0 VLDO3FAULTI Unmasked 1 VLDO3FAULTI Masked
3 V33FAULTM	V33 overcurrent interrupt mask bit 0 V33FAULTI Unmasked 1 V33FAULTI Masked
2 VCC_SDFAULTM	VCC_SD overcurrent interrupt mask bit 0 VCC_SDFAULTI Unmasked 1 VCC_SDFAULTI Masked
1 VLDO2FAULTM	VLDO2 Overcurrent interrupt mask bit 0 VLDO2FAULTI Unmasked 1 VLDO2FAULTI Masked
0 VLDO1FAULTM	VLDO1 overcurrent interrupt mask bit 0 VLDO1FAULTI Unmasked 1 VLDO1FAULTI Masked

6.6.5.3.12 Interrupt sense register 4 (INTSENSE4)

This register has four read-only sense bits. These sense bits reflect the actual state of the corresponding function.

Address: 0x13 functional page **Access: User read-only (88)**

	7	6	5	4	3	2	1	0
R			VLDO4FAULTS	VLDO3FAULTS	V33FAULTS	VCC_SDFAULTS	VLDO2FAULTS	VLDO1FAULTS
W								
Default	0	0	X (89)	X (89)	X (89)	X (89)	X (89)	X (89)

= Unimplemented or Reserved

Notes
88. Read: Anytime
89. Default value depends on the regulator initial state

Table 120. INTSENSE4 Field Descriptions

Field	Description
5 VLDO4FAULTS	VLDO4 overcurrent sense bit 0 VLDO4 in normal operation 1 VLDO4 above current limit
4 VLDO3FAULTS	VLDO3 overcurrent sense bit 0 VLDO3 in normal operation 1 VLDO3 above current limit
3 V33FAULTS	V33 overcurrent sense bit 0 V33 in normal operation 1 V33 above current limit
2 VCC_SDFAULTS	VCC_SD overcurrent sense bit 0 VCC_SD in normal operation 1 VCC_SD above current limit
1 VLDO2FAULTS	VLDO2 overcurrent sense bit 0 VLDO2 in normal operation 1 VLDO2 above current limit
0 VLDO1FAULTS	VLDO1 overcurrent sense bit 0 VLDO1 in normal operation 1 VLDO1 above current limit

6.6.5.3.13 Coin cell control register (COINCTL)

This register is used to control the coin cell charger.

Table 121. Coin cell control register (COINCTL)

Address: 0x1A functional page							Access: User read/write (90)	
	7	6	5	4	3	2	1	0
R W					COINCHEN	VCOIN		
Default	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Notes
90. Read: Anytime
Write: Anytime

Table 122. COINCTL field descriptions

Field	Description
3 COINCHEN	Coin cell charger enable bit 0 Coin cell charger disabled. 1 Coin cell charger enabled.
2:0 VCOIN	**Coin cell charger output voltage selection** — This field is used to set the coin cell charging voltage from 2.50 V to 3.30 V. See Table 70 for all options selectable through these bits.

6.6.5.3.14 Power control register (PWRCTL)

Table 123. Power control register (PWRCTL)

Address: 0x1B functional page							Access: User read/write (91)	
	7	6	5	4	3	2	1	0
R W	REGSCPEN	STANDBYINV	STBYDLY		PWRONBDBNC		PWRONRSTEN	RESTARTEN
Default	0	0	0	1	0	0	0	0

= Unimplemented or Reserved

Notes
91. Read: Anytime
Write: Anytime

Table 124. PWRCTL field descriptions

Field	Description
7 REGSCPEN	**Short-circuit protection enable bit** — When REGSCPEN is set to 1, whenever a current limit event occurs on a LDO regulator, this regulator is shutdown. 0 Short-circuit protection disabled 1 Short-circuit protection enabled
6 STANDBYINV	**STANDBY inversion bit** —STANDBYINV is used to control the polarity of the STANDBY pin. 0 STANDBY pin is active high 1 STANDBY pin is active low
4:3 STBYDLY	**STANDBY delay bits** — STBYDLY is used to set the delay between a standby request from the STANDBY pin and the entering in standby mode. 00 No delay 01 One 32 kHz period (default) 10 Two 32 kHz periods 11 Three 32 kHz periods
3:2 PWRONDBNC	**PWRON programmable debouncer bits** — PWRONDBNC is used to set the debounce time for the PWRON input pin. For configuration, see Table 36.
1 PWRONRSTEN	**PWRON reset enable bit** — When set to 1, the PF3000 can enter OFF mode when the PWRON pin is held low for 4 seconds or longer. See PWRON Pin section for details. 0 Disallow OFF mode after PWRON held low 1 Allow OFF mode after PWRON held low
0 RESTARTEN	**Restart enable bit** — When set to 1, the PF3000 restarts automatically after a power off event generated by the PWRON (held low for 4 seconds or longer) when PWR_CFG bit = 1. 0 Automatic restart disabled. 1 Automatic restart enabled.

6.6.5.3.15 Embedded memory register A (MEMA)

Table 125. Embedded memory register A (MEMA)

Address: 0x1C functional page — **Access: User read/write (92)**

	7	6	5	4	3	2	1	0
R W	MEMA							
Default	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Notes
92. Read: Anytime
Write: Anytime

Table 126. MEMA field descriptions

Field	Description
7:0 MEMA	**Memory bank A** — This register is maintained in case of a main battery loss as long as the coin cell is present. The contents of the embedded memory are reset by COINPORB.

6.6.5.3.16 Embedded memory register B (MEMB)

Table 127. Embedded memory register B (MEMB)

Address: 0x1D functional page							Access: User read/write	
	7	6	5	4	3	2	1	0
R W	MEMB							
Default	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Notes

93. Read: Anytime
Write: Anytime

Table 128. MEMB field descriptions

Field	Description
7:0 MEMB	**Memory bank B** — This register is maintained in case of a main battery loss as long as the coin cell is present. The contents of the embedded memory are reset by COINPORB.

6.6.5.3.17 Embedded memory register C (MEMC)

Table 129. Embedded Memory Register C (MEMC)

Address: 0x1E functional page							Access: User read/write (94)	
	7	6	5	4	3	2	1	0
R W	MEMC							
Default	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Notes

94. Read: Anytime
Write: Anytime

Table 130. MEMC field descriptions

Field	Description
7:0 MEMC	**Memory bank C** — This register is maintained in case of a main battery loss as long as the coin cell is present. The contents of the embedded memory are reset by COINPORB.

6.6.5.3.18 Embedded memory register D (MEMD)

Table 131. Embedded memory register D (MEMD)

Address: 0x1F functional page							Access: User read/write [95]
	7	6	5	4	3	2	1	0
R W	MEMD							
Default	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Notes
95. Read: Anytime
Write: Anytime

Table 132. MEMD field descriptions

Field	Description
7:0 MEMD	**Memory bank D** — This register is maintained in case of a main battery loss as long as the coin cell is present. The contents of the embedded memory are reset by COINPORB.

6.6.5.3.19 SW1A voltage control register (SW1AVOLT)

This register is used to set the output voltage of the SW1A regulator in normal operation.

Table 133. SW1A voltage control register (SW1AVOLT)

Address: 0x20 functional page							Access: User read/write [96]
	7	6	5	4	3	2	1	0
R W				SW1A				
Default	0	0	0	X [97]	X [97]	X [97]	X [97]	X [97]

= Unimplemented or Reserved

Notes
96. Read: Anytime
Write: Anytime
97. Default value depends on OTP content.

Table 134. SW1AVOLT field descriptions

Field	Description
4:0 SW1A	**SW1A output voltage** — Refer to Table 53

6.6.5.3.20 SW1A standby voltage control register (SW1ASTBY)

This register is used to set the output voltage of the SW1A regulator in standby operation.

Table 135. SW1A standby voltage control register (SW1ASTBY)

Address: 0x21 functional page							Access: User read/write [98]
	7	6	5	4	3	2	1	0
R W				SW1ASTBY				
Default	0	0	0	X [99]	X [99]	X [99]	X [99]	X [99]

= Unimplemented or Reserved

Notes
98. Read: Anytime
Write: Anytime
99. Default value depends on OTP content.

Table 136. SW1ASTBY field descriptions

Field	Description
4:0 SW1ASTBY	**SW1A standby output voltage** — Refer to Table 53

6.6.5.3.21 SW1A sleep mode voltage control register (SW1AOFF)

This register is used to set the output voltage of the SW1A regulator in sleep mode operation.

Table 137. SW1A sleep mode voltage control register (SW1AOFF)

Address: 0x22 functional page							Access: User read/write [100]
	7	6	5	4	3	2	1	0
R W				SW1AOFF				
Default	0	0	0	X [101]	X [101]	X [101]	X [101]	X [101]

= Unimplemented or Reserved

Notes
100. Read: Anytime
Write: Anytime
101. Default value depends on OTP content.

Table 138. SW1AOFF field descriptions

Field	Description
4:0 SW1ASTBY	**SW1A sleep mode output voltage** — Refer to Table 53

6.6.5.3.22 SW1A switching mode selector register (SW1AMODE)

This register is used to set the switching mode of the SW1A regulator.

Table 139. SW1A switching mode selector register (SW1AMODE)

Address: 0x23 functional page							Access: User read/write [102]	
	7	6	5	4	3	2	1	0
R W			SW1AOMODE		SW1AMODE			
Default	0	0	0	0	X [103]	X [103]	X [103]	X [103]

= Unimplemented or Reserved

Notes
102. Read: Anytime
Write: Anytime
103. Default value depends on OTP content.

Table 140. SW1AMODE field descriptions

Field	Description
5 SW1AOMODE	**SW1A Off mode bit**— This bit configures the mode entered by SW1A after a turn-off event 0 OFF mode entered after a turn-off event. 1 Sleep mode entered after a turn-off event.
3:0 SW1AMODE	**SW1A switching mode selector** — Refer to Table 47

6.6.5.3.23 SW1A configuration register (SW1ACONF)

This register is used to configure DVS, switching frequency, phase and current limit settings of the SW1A regulator.

Table 141. SW1A configuration register (SW1ACONF)

Address: 0x24 functional page							Access: User read/write [104]	
	7	6	5	4	3	2	1	0
R W		SW1ADVSSPEED	SW1APHASE		SW1AFREQ			SW1AILIM
Default	0	X [105]	0	0	X [105]	X [105]	0	X [105]

= Unimplemented or Reserved

Notes
104. Read: Anytime
Write: Anytime
105. Default value depends on OTP content.

Table 142. SW1ACONF field descriptions

Field	Description
6 SW1ADVSSPEED	**SW1A DVS speed bit**— This bit configures the DVS stepping rates speed for SW1A. Refer to the Table 48. 0 25 mV step each 2.0 µs. 1 25 mV step each 4.0 µs.
5:4 SW1APHASE	**SW1A phase clock bit**— SW1APHASE is used to set the phase clock for SW1A. Refer to Table 49.
3:2 SW1AFREQ	**SW1A switching frequency**— SW1APHASE is used to set the desired switching frequency for SW1A. Refer to Table 51.
0 SW1AILIM	**SW1A current limiter bit**— This bit configures the current limit for SW1A. 0 2.75 A (typ). 1 2.0 A (typ).

6.6.5.3.24 SW1B voltage control register (SW1BVOLT)

This register is used to set the output voltage of the SW1B regulator in normal operation.

Table 143. SW1B voltage control register (SW1BVOLT)

Address: 0x2E functional page **Access: User read/write (106)**

	7	6	5	4	3	2	1	0
R W				SW1B				
Default	0	0	0	X (107)	X (107)	X (107)	X (107)	X (107)

= Unimplemented or Reserved

Notes
106. Read: Anytime
Write: Anytime
107. Default value depends on OTP content.

Table 144. SW1BVOLT field descriptions

Field	Description
4:0 SW1B	**SW1B output voltage** — Refer to Table 53.

6.6.5.3.25 SW1B standby voltage control register (SW1BSTBY)

This register is used to set the output voltage of the SW1B regulator in standby operation.

Table 145. SW1B standby voltage control register (SW1BSTBY)

Address: 0x2F functional page							Access: User read/write (108)
7	6	5	4	3	2	1	0
R W				SW1BSTBY			
Default	0	0	0	X (109)	X (109)	X (109)	X (109)	X (109)

= Unimplemented or Reserved

Notes
108. Read: Anytime
Write: Anytime
109. Default value depends on OTP content.

Table 146. SW1BSTBY field descriptions

Field	Description
4:0 SW1BSTBY	**SW1B standby output voltage** — Refer to Table 53.

6.6.5.3.26 SW1B sleep mode voltage control register (SW1BOFF)

This register is used to set the output voltage of the SW1B regulator in sleep mode operation.

Table 147. SW1B sleep mode voltage control register (SW1BOFF)

Address: 0x30 functional page							Access: User read/write (110)
7	6	5	4	3	2	1	0
R W				SW1BOFF			
Default	0	0	0	X (111)	X (111)	X (111)	X (111)	X (111)

= Unimplemented or Reserved

Notes
110. Read: Anytime
Write: Anytime
111. Default value depends on OTP content.

Table 148. SW1BOFF field descriptions

Field	Description
4:0 SW1BSTBY	**SW1B sleep mode output voltage** — Refer to Table 53.

6.6.5.3.27 SW1B switching mode selector register (SW1BMODE)

This register is used to set the switching mode of the SW1B regulator.

Table 149. SW1B switching mode selector register (SW1BMODE)

Address: 0x31 functional page					Access: User read/write (112)			
	7	6	5	4	3	2	1	0
R W			SW1BOMODE		SW1BMODE			
Default	0	0	0	0	X (113)	X (113)	X (113)	X (113)

= Unimplemented or Reserved

Notes
112. Read: Anytime
Write: Anytime
113. Default value depends on OTP content.

Table 150. SW1BMODE field descriptions

Field	Description
5 SW1BOMODE	**SW1B Off mode bit**— This bit configures the mode entered by SW1B after a turn-off event 0 OFF mode entered after a turn-off event. 1 Sleep mode entered after a turn-off event.
3:0 SW1BMODE	**SW1B switching mode selector** — Refer to Table 47.

6.6.5.3.28 SW1B configuration register (SW1BCONF)

This register is used to configure DVS, switching frequency, phase and current limit settings of the SW1B regulator.

Table 151. SW1B configuration register (SW1BCONF)

Address: 0x32 functional page					Access: User read/write X (114)			
	7	6	5	4	3	2	1	0
R W	SW1BDVSSPEED		SW1BPHASE		SW1BFREQ			SW1BILIM
Default	0	X (115)	0	0	X (115)	X (115)	0	X (115)

= Unimplemented or Reserved

Notes
114. Read: Anytime
Write: Anytime
115. Default value depends on OTP content.

Table 152. SW1BCONF field descriptions

Field	Description
6 SW1BDVSSPEED	**SW1B DVS speed bit**— This bit configures the DVS stepping rates speed for SW1B. Refer to the Table 48. 0 25 mV step each 2.0 µs. 1 25 mV step each 4.0 µs.
5:4 SW1BPHASE	**SW1B phase clock bit**— SW1BPHASE is used to set the phase clock for SW1B. Refer to Table 49.
3:2 SW1BFREQ	**SW1B switching frequency**— SW1BPHASE is used to set the desired switching frequency for SW1B. Refer to Table 51.
0 SW1BILIM	**SW1B current limiter bit**— This bit configures the current limit for SW1B. 0 2.75 A (typ). 1 2.0 A (typ).

6.6.5.3.29 SW2 voltage control register (SW2VOLT)

This register is used to set the output voltage of the SW2 regulator in normal operation.

Table 153. SW2 voltage control register (SW2VOLT)

Address: 0x35 functional page **Access: User read/write (116)**

	7	6	5	4	3	2	1	0
R W			SW2_HI	SW2				
Default	0	0	X (117)	X (117)	X (117)	X (117)	X (117)	X (117)

= Unimplemented or Reserved

Notes
116. Read: Anytime
Write: Anytime
117. Default value depends on OTP content.

Table 154. SW2VOLT field descriptions

Field	Description
4:0 SW2	**SW2 output voltage** — Refer to Table 55.
5 SW2_HI	**SW2 Output voltage range** —This bit configures the range of SW2 Output voltage. Refer to Table 55. 0 Low output voltage settings 1 High output voltage settings

6.6.5.3.30 SW2 standby voltage control register (SW2STBY)

This register is used to set the output voltage of the SW2 regulator in standby operation.

Table 155. SW2 standby voltage control register (SW2STBY)

Address: 0x36 functional page							Access: User read/write [118]	
	7	6	5	4	3	2	1	0
R W			SW2_HI	SW2STBY				
Default	0	0	X [119]	X [119]	X [119]	X [119]	X [119]	X [119]

= Unimplemented or Reserved

Notes
118. Read: Anytime
Write: Anytime
119. Default value depends on OTP content.

Table 156. SW2STBY field descriptions

Field	Description
4:0 SW2STBY	**SW2 standby output voltage** — Refer to Table 55.
5 SW2_HI	**SW2 output voltage range** —This bit configures the range of SW2 Output voltage. Refer to Table 55. 0 Low output voltage settings 1 High output voltage settings

6.6.5.3.31 SW2 sleep mode voltage control register (SW2OFF)

This register is used to set the output voltage of the SW2 regulator in sleep mode operation.

Table 157. SW2 sleep mode voltage control register (SW2OFF)

Address: 0x37 functional page							Access: User read/write [120]	
	7	6	5	4	3	2	1	0
R W			SW2_HI	SW2OFF				
Default	0	0	X [121]	X [121]	X [121]	X [121]	X [121]	X [121]

= Unimplemented or Reserved

Notes
120. Read: Anytime
Write: Anytime
121. Default value depends on OTP content.

Table 158. SW2OFF field descriptions

Field	Description
4:0 SW2STBY	**SW2 sleep mode output voltage** — Refer to Table 55.
5 SW2_HI	**SW2 output voltage range** —This bit configures the range of SW2 Output voltage. Refer to Table 55. 0 Low output voltage settings 1 High output voltage settings

6.6.5.3.32 SW2 switching mode selector register (SW2MODE)

This register is used to set the switching mode of the SW2 regulator.

Table 159. SW2 switching mode selector register (SW2MODE)

Address: 0x38 functional page **Access: User read/write (122)**

	7	6	5	4	3	2	1	0
R W			SW2OMODE		SW2MODE			
Default	0	0	0	0	X (123)	X (123)	X (123)	X (123)

= Unimplemented or Reserved

Notes
122. Read: Anytime
Write: Anytime
123. Default value depends on OTP content.

Table 160. SW2MODE field descriptions

Field	Description
5 SW2OMODE	**SW2 Off mode bit**— This bit configures the mode entered by SW2 after a turn-off event 0 OFF mode entered after a turn-off event. 1 Sleep mode entered after a turn-off event.
3:0 SW2MODE	**SW2 switching mode selector** — Refer to Table 47.

6.6.5.3.33 SW2 configuration register (SW2CONF)

This register is used to configure DVS, switching frequency, phase and current limit settings of the SW2 regulator.

Table 161. SW2 configuration register (SW2CONF)

Address: 0x39 functional page						Access: User read/write (124)		
	7	6	5	4	3	2	1	0
R W		SW2DVSSPEED	SW2PHASE		SW2FREQ			SW2ILIM
Default	0	X (125)	0	0	X (125)	X (125)	0	X (125)

= Unimplemented or Reserved

Notes
124. Read: Anytime
Write: Anytime
125. Default value depends on OTP content.

Table 162. SW2CONF field descriptions

Field	Description
6 SW2DVSSPEED	SW2 DVS speed bit- This bit configures the DVS stepping rates speed for SW2. Refer to the Table 48. 0 25 mV step each 2.0 µs. 1 25 mV step each 4.0 µs.
5:4 SW2PHASE	**SW2 phase clock bit**— SW2PHASE is used to set the phase clock for SW2. Refer to Table 49.
3:2 SW2FREQ	**SW2 switching frequency**— SW2PHASE is used to set the desired switching frequency for SW2. Refer to Table 51.
0 SW2ILIM	**SW2 current limiter bit**— This bit configures the current limit for SW2. 0 2.75 A (typ). 1 2.0 A (typ).

6.6.5.3.34 SW3 voltage control register (SW3VOLT)

This register is used to set the output voltage of the SW3 regulator in normal operation.

Table 163. SW3 voltage control register (SW3VOLT)

Address: 0x3C functional page						Access: User read/write (126)		
	7	6	5	4	3	2	1	0
R W				SW3				
Default	0	0	0	X (127)	X (127)	X (127)	X (127)	X (127)

= Unimplemented or Reserved

Notes
126. Read: Anytime
Write: Anytime
127. Default value depends on OTP content.

Table 164. SW3VOLT field descriptions

Field	Description
4:0 SW3	**SW3 output voltage** — Refer to Table 57.

6.6.5.3.35 SW3 standby voltage control register (SW3STBY)

This register is used to set the output voltage of the SW3 regulator in standby operation.

Table 165. SW3 standby voltage control register (SW3STBY)

Address: 0x3D functional page **Access: User read/write (128)**

	7	6	5	4	3	2	1	0
R W				SW3STBY				
Default	0	0	0	X (129)	X (129)	X (129)	X (129)	X (129)

= Unimplemented or Reserved

Notes
128. Read: Anytime
Write: Anytime
129. Default value depends on OTP content.

Table 166. SW3STBY field descriptions

Field	Description
4:0 SW3STBY	**SW3 standby output voltage** — Refer to Table 57.

6.6.5.3.36 SW3 sleep mode voltage control register (SW3OFF)

This register is used to set the output voltage of the SW3 regulator in sleep mode operation.

Table 167. SW3 sleep mode voltage control register (SW3OFF)

Address: 0x3E functional page **Access: User read/write (130)**

	7	6	5	4	3	2	1	0
R W				SW3OFF				
Default	0	0	0	X (131)	X (131)	X (131)	X (131)	X (131)

= Unimplemented or Reserved

Notes
130. Read: Anytime
Write: Anytime
131. Default value depends on OTP content.

Table 168. SW3OFF field descriptions

Field	Description
4:0 SW3STBY	**SW3 sleep mode output voltage** — Refer to Refer to Table 57.

6.6.5.3.37 SW3 switching mode selector register (SW3MODE)

This register is used to set the switching mode of the SW3 regulator.

Table 169. SW3 switching mode selector register (SW3MODE)

	Address: 0x3F functional page				Access: User read/write (132)			
	7	6	5	4	3	2	1	0
R W			SW3OMODE		SW3MODE			
Default	0	0	0	0	X (133)	X (133)	X (133)	X (133)

= Unimplemented or Reserved

Notes
132. Read: Anytime
Write: Anytime
133. Default value depends on OTP content.

Table 170. SW3MODE field descriptions

Field	Description
5 SW3OMODE	**SW3 Off mode bit**— This bit configures the mode entered by SW3 after a turn-off event 0 OFF mode entered after a turn-off event. 1 Sleep mode entered after a turn-off event.
3:0 SW3MODE	**SW3 switching mode selector** — Refer to Table 47.

6.6.5.3.38 SW3 configuration register (SW3CONF)

This register is used to configure DVS, switching frequency, phase and current limit settings of the SW3 regulator.

Table 171. SW3 configuration register (SW3CONF)

	Address: 0x40 functional page				Access: User read/write (134)			
	7	6	5	4	3	2	1	0
R W		SW3DVSSPEED	SW3PHASE		SW3FREQ			SW3ILIM
Default	0	X (135)	0	0	X (135)	X (135)	0	X (135)

= Unimplemented or Reserved

Notes
134. Read: Anytime
Write: Anytime
135. Default value depends on OTP content.

Table 172. SW3CONF field descriptions

Field	Description
6 SW3DVSSPEED	**SW3 DVS speed bit**— This bit configures the DVS stepping rates speed for SW3. Refer to the Table 48. 0 25 mV step each 2.0 µs. 1 25 mV step each 4.0 µs.
5:4 SW3PHASE	**SW3 phase clock bit**— SW3PHASE is used to set the phase clock for SW3. Refer to Table 49.
3:2 SW3FREQ	**SW3 switching frequency**— SW3PHASE is used to set the desired switching frequency for SW3. Refer to Table 51.
0 SW3ILIM	**SW3 current limiter bit**— This bit configures the current limit for SW3. 0 2.75 A (typ). 1 2.0 A (typ).

6.6.5.3.39 SWBST setup and control register (SWBSTCTL)

This register is used to configure both the output voltage and switching modes of the SWBST regulator.

Table 173. SWBST configuration register (SWBSTCTL)

Address: 0x66 functional page — **Access: User read/write (136)**

	7	6	5	4	3	2	1	0
R W		SWBST1STBYMODE			SWBST1MODE		SWBST1VOLT	
Default	0	X (137)	X (137)	0	X (137)	X (137)	X (137)	X (137)

= Unimplemented or Reserved

Notes

136. Read: Anytime
Write: Anytime

137. Default value depends on OTP content.

Table 174. SWBSTCTL field descriptions

Field	Description
6:5 SWBST1STBYMODE	**SWBST switching mode in standby**— SWBST1MODE is used to set the switching mode in standby mode. 00 OFF 01 PFM 10 Auto (138) 11 APS
3:2 SWBST1MODE	**SWBST switching mode in normal operation**— SWBST1MODE is used to set the switching mode on normal operation. 00 OFF 01 PFM 10 Auto (138) 11 APS
1:0 SWBST1VOLT	**SWBST output voltage**— SWBST1VOLT is used to set the output voltage for SWBST. 00 5.000 V (typ.) 01 5.050 V (typ.) 10 5.100 V (typ.) 11 5.150 V (typ.)

Notes

138. In auto mode, the controller automatically switches between PFM and APS modes depending on the load current. Regulator switches in auto mode if enabled in the startup sequence.

6.6.5.3.40 Front-end LDO control register (LDOGCTL)

This register is used to configure the front-end LDO standby mode operation.

Table 175. Front-end LDO control register (LDOGCTL)

Address: 0x69 functional page							Access: User read/write (139)
	7	6	5	4	3	2	1	0
R W								STBY_LOWPOWER_B
Default	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Notes
139. Read: Anytime
Write: Anytime

Table 176. LDOGCTL field descriptions

Field	Description
0 STBY_LOWPOWER_B	**Front-end LDO standby mode operation bit**— When STBY_LOWPOWER_B bit is set to 1, the front-end LDO does not enter in low-power mode during IC standby mode. 0 Low-power mode enabled during IC standby mode. 1 Low-power mode disabled during IC standby mode.

6.6.5.3.41 VREFDDR control register (VREFDDRCTL)

This register is used to control the VREFDDR supply operation.

Table 177. VREFDDR control register (VREFDDRCTL)

Address: 0x6A functional page							Access: User read/write (140)
	7	6	5	4	3	2	1	0
R W								VREFDDREN
Default	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Notes
140. Read: Anytime
Write: Anytime

Table 178. VREFDDR field descriptions

Field	Description
0 VREFDDREN	**VREFDDR supply enable bit**— VREFDDREN is used to enable or disable the VREFDDR supply. 0 VREFDDR supply disabled 1 VREFDDR supply enabled

6.6.5.3.42 VSNVS control register (VSNVSCTL)

This register is used to control the VSNVS supply operation.

Table 179. VSNVS control register (VSNVSCTL)

Address: 0x6B functional page							Access: User read/write (141)	
	7	6	5	4	3	2	1	0
R W						VSNVSVOLT		
Default	0	0	0	0	0	X (142)	X (142)	X (142)

= Unimplemented or Reserved

Notes
141. Read: Anytime
Write: Anytime
142. Default value depends on OTP content.

Table 180. VSNVSCTL field descriptions

Field	Description
2:0 VSNVSVOLT	**VSNVS output voltage configuration**— VSNVSVOLT is used to configure the VSNVS output voltage. Values below are typical voltages. 000 = RSVD 001 = RSVD 010 = RSVD 011 = RSVD 100 = RSVD 101 = RSVD 110 = 3.0 V (default) 111 = RSVD

6.6.5.3.43 VLDO1 control register (VLDO1CTL)

This register is used to configure output voltage, normal and standby mode operation of the VLDO1 regulator.

Table 181. VLDO1 control register (VLDO1CTL)

Address: 0x6C functional page							Access: User read/write (143)	
	7	6	5	4	3	2	1	0
R W	LDO1OMODE	VLDO1LPWR	VLDO1STBY	VLDO1EN	VLDO1			
Default	0	0	0	X (144)	X (144)	X (144)	X (144)	X (144)

= Unimplemented or Reserved

Notes
143. Read: Anytime
Write: Anytime
144. Default value depends on OTP content.

Table 182. VLDO1CTL field descriptions

Field	Description
7 LDO1OMODE	**VLDO1 OFF mode bit**—LDO1OMODE is used to configure VLDO1 operating mode when a PWRON turn-off event occurs. 0 VLDO1 in OFF mode if a PWRON turn off event occurs 1 VLDO1 in sleep mode if a PWRON turn off event occurs
6 VLDO1LPWR	**VLDO1 Low-power mode enable bit**— When VLDO1LPWR is set to 1, VLDO1 can enter Low-power mode per the conditions in the Table 66. 0 Low-power mode disabled 1 Low-power mode enabled
5 VLDO1STBY	**VLDO1 standby enable bit**— When VLDO1STBY is set to 1, VLDO1 is turned off during standby mode. Refer to Table 66. 0 VLDO1 is ON during standby mode. 1 VLDO1 is OFF during standby mode.
4 VLDO1EN	**VLDO1 enable bit** — VLDO1EN is used to enable or disable the VLDO1 regulator. 0 VLDO1 disabled 1 VLDO1 enabled
3:0 VLDO1	**VLDO1 output voltage configuration**— Refer to Table 62.

6.6.5.3.44 VLDO2 control register (VLDO2CTL)

This register is used to configure output voltage, normal, and standby mode operation of the VLDO2 regulator.

Table 183. VLDO2 control register (VLDO2CTL)

Address: 0x6D functional page **Access: User read/write (145)**

	7	6	5	4	3	2	1	0
R W	LDO2OMODE	VLDO2LPWR	VLDO2STBY	VLDO2EN	VLDO2			
Default	0	0	0	X (146)	X (146)	X (146)	X (146)	X (146)

= Unimplemented or Reserved

Notes
145. Read: Anytime
Write: Anytime
146. Default value depends on OTP content.

Table 184. VLDO2CTL field descriptions

Field	Description
7 LDO2OMODE	**VLDO2 OFF mode bit**—LDO2OMODE is used to configure VLDO2 operating mode when a PWRON turn-off event occurs. 0 VLDO2 in OFF mode if a PWRON turn off event occurs 1 VLDO2 in Sleep mode if a PWRON turn off event occurs
6 VLDO2LPWR	**VLDO2 low-power mode enable bit**— When VLDO2LPWR is set to 1, VLDO2 can enter low-power mode per the conditions in the LDO control table. 0 Low-power mode disabled 1 Low-power mode enabled
5 VLDO2STBY	**VLDO2 standby enable bit**— When VLDO2STBY is set to 1, VLDO2 is turned off during standby mode. Refer to Table 66. 0 VLDO2 is ON during standby mode. 1 VLDO2 is OFF during standby mode.
4 VLDO2EN	**VLDO2 enable bit** — VLDO2EN is used to enable or disable the VLDO2 regulator. 0 VLDO2 disabled 1 VLDO2 enabled
3:0 VLDO2	**VLDO2 output voltage configuration**— Refer to Table 62.

6.6.5.3.45 VCC_SD control register (VCC_SDCTL)

This register is used to configure output voltage, normal and standby mode operation of the VCC_SD regulator.

Table 185. CC_SD control register (VCC_SDCTL)

Address: 0x6E functional page **Access: User read/write** (147)

	7	6	5	4	3	2	1	0
R W	VCC_SDOMODE	VCC_SDLPWR	VCC_SDSTBY	VCC_SDEN			VCC_SD	
Default	0	0	0	X (148)	0	0	X (148)	X (148)

= Unimplemented or Reserved

Notes
147. Read: Anytime
Write: Anytime
148. Default value depends on OTP content.

Table 186. VCC_SDCTL field descriptions

Field	Description
7 VCC_SDOMODE	**VCC_SD OFF mode bit**— VCC_SDOMODE is used to configure VCC_SD operating mode when a PWRON turn-off event occurs. 0 VCC_SD in OFF mode if a PWRON turn off event occurs 1 VCC_SD in Sleep mode if a PWRON turn off event occurs
6 VCC_SDLPWR	**VCC_SD low-power mode enable bit**— When VCC_SDLPWR is set to 1, VCC_SD can enter low-power mode per the conditions in the Table 66. 0 Low-power mode disabled 1 Low-power mode enabled
5 VCC_SDSTBY	**VCC_SD standby enable bit**— When VCC_SDSTBY is set to 1, VCC_SD is turned off during standby mode. Refer to Table 66. 0 VCC_SD is ON during standby mode. 1 VCC_SD is OFF during standby mode.
4 VCC_SDEN	**VCC_SD enable bit** — VCC_SDEN is used to enable or disable the VCC_SD regulator. 0 VCC_SD disabled 1 VCC_SD enabled
1:0 VCC_SD	**VCC_SD output voltage configuration**— Refer to Table 65.

6.6.5.3.46 V33 control register (V33CTL)

This register is used to configure output voltage, normal, and standby mode operation of the V33 regulator.

Table 187. V33 control register (V33CTL)

Address: 0x6F functional page						Access: User read/write (149)		
	7	6	5	4	3	2	1	0
R W	V33OMODE	V33LPWR	V33STBY	V33EN			V33	
Default	0	0	0	X (150)	0	0	X (150)	X (150)

= Unimplemented or Reserved

Notes
149. Read: Anytime
Write: Anytime
150. Default value depends on OTP content.

Table 188. V33CTL field descriptions

Field	Description
7 V33OMODE	**V33 OFF mode bit**— V33OMODE is used to configure V33 operating mode when a PWRON turn-off event occurs. 0 V33 in OFF mode if a PWRON turn off event occurs 1 V33 in sleep mode if a PWRON turn off event occurs
6 V33LPWR	**V33 low-power mode enable bit**— When V33LPWR is set to 1, V33 can enter low-power mode per the conditions in the Table 66. 0 Low-power mode disabled 1 Low-power mode enabled
5 V33STBY	**V33 standby enable bit**— When V33STBY is set to 1, V33 is turned off during standby mode. Refer to Table 66. 0 V33 is ON during standby mode. 1 V33 is OFF during standby mode.
4 V33EN	**V33 Enable bit** — V33EN is used to enable or disable the VLDO2 regulator. 0 V33 disabled 1 V33 enabled
1:0 V33	**V33 output voltage configuration**— Refer to Table 64.

6.6.5.3.47 VLDO3 control register (VLDO3CTL)

This register is used to configure output voltage, normal, and standby mode operation of the VLDO3 regulator.

Table 189. VLDO3 control register (VLDO3CTL)

	Address: 0x70 functional page							Access: User read/write (151)
	7	6	5	4	3	2	1	0
R W	LDO3OMODE	VLDO3LPWR	VLDO3STBY	VLDO3EN	VLDO3			
Default	0	0	0	X (152)	X (152)	X (152)	X (152)	X (152)

= Unimplemented or Reserved

Notes
151. Read: Anytime
Write: Anytime
152. Default value depends on OTP content.

Table 190. VLDO3CTL field descriptions

Field	Description
7 LDO3OMODE	**VLDO3 OFF mode bit**—LDO3OMODE is used to configure VLDO3 operating mode when a PWRON turn-off event occurs. 0 VLDO3 in OFF mode if a PWRON turn off event occurs 1 VLDO3 in sleep mode if a PWRON turn off event occurs
6 VLDO3LPWR	**VLDO3 low-power mode enable bit**— When VLDO3LPWR is set to 1, VLDO3 can enter low-power mode per the conditions in the Table 66. 0 Low-power mode disabled 1 Low-power mode enabled
5 VLDO3STBY	**VLDO3 standby enable bit**— When VLDO3STBY is set to 1, VLDO3 is turned off during standby mode. Refer to Table 66. 0 VLDO3 is ON during standby mode. 1 VLDO3 is OFF during standby mode.
4 VLDO3EN	**VLDO3 enable bit** — VLDO3EN is used to enable or disable the VLDO3 regulator. 0 VLDO3 disabled 1 VLDO3 enabled
3:0 VLDO3	**VLDO3 output voltage configuration**— Refer to Table 63.

6.6.5.3.48 VLDO4 control register (VLDO4CTL)

This register is used to configure output voltage, normal, and standby mode operation of the VLDO4 regulator.

Table 191. VLDO4 control register (VLDO4CTL)

	Address: 0x71 functional page							Access: User read/write (153)
	7	6	5	4	3	2	1	0
R W	LDO4OMODE	VLDO4LPWR	VLDO4STBY	VLDO4EN	VLDO4			
Default	0	0	0	X (154)	X (154)	X (154)	X (154)	X (154)

= Unimplemented or Reserved

Notes
153. Read: Anytime
Write: Anytime
154. Default value depends on OTP content.

Table 192. VLDO4CTL field descriptions

Field	Description
7 LDO4OMODE	**VLDO4 OFF mode bit**—LDO4OMODE is used to configure VLDO4 operating mode when a PWRON turn-off event occurs. 0 VLDO4 in OFF mode if a PWRON turn off event occurs 1 VLDO4 in sleep mode if a PWRON turn off event occurs
6 VLDO4LPWR	**VLDO4 low-power mode enable bit**— When VLDO4LPWR is set to 1, VLDO4 can enter low-power mode per the conditions in the Table 66. 0 Low-power mode disabled 1 Low-power mode enabled
5 VLDO4STBY	**VLDO4 standby enable bit**— When VLDO4STBY is set to 1, VLDO4 is turned off during standby mode. Refer to Table 66. 0 VLDO4 is ON during standby mode. 1 VLDO4 is OFF during standby mode.
4 VLDO4EN	**VLDO4 enable bit** — VLDO4EN is used to enable or disable the VLDO4 regulator. 0 VLDO4 disabled 1 VLDO4 enabled
3:0 VLDO4	**VLDO4 output voltage configuration**— Refer to Table 63.

6.6.5.3.49 Page selection register

This register is used to access the extended register pages.

Table 193. Page selection register

	Address: 0x7F functional page							Access: User read/write (155)
	7	6	5	4	3	2	1	0
R W					PAGE			
Default	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Notes
155. Read: Anytime
Write: Anytime

Table 194. Page register field descriptions

Field	Description
3:0 PAGE	**Register page selection** — The PAGE field is used to select one of the three available register pages. 0000 Functional page selected 0001 Extended page 1 selected 0010 Extended page 2 selected

6.6.6 Register map

The register map is comprised of thirty-two pages, and its address and data fields are each eight bits wide. Only the first two pages can be accessed. On each page, registers 0 to 0x7F are referred to as 'functional', and registers 0x80 to 0xFF as 'extended'. On each page, the functional registers are the same, but the extended registers are different. To access registers in Extended page 1, one must first write 0x01 to the page register at address 0x7F, and to access registers Extended page 2, one must first write 0x02 to the page register at address 0x7F. To access the Functional page from one of the extended pages, no write to the page register is necessary.

Registers that are missing in the sequence are reserved; reading from them returns a value 0x00, and writing to them has no effect. The contents of all registers are given in the tables defined in this chapter; each table is structure as follows:

Name: Name of the bit

Bit #: The bit location in the register (7-0)

R/W: Read / Write access and control

- R is read-only access
- R/W is read and write access
- RW1C is read and write access with write 1 to clear

Reset: Reset signals are color coded based on the following legend.

Bits reset by SC and VCOREDIG_PORB
Bits reset by PWRON or loaded default or OTP configuration
Bits reset by DIGRESETB
Bits reset by PORB or RESETBMCU
Bits reset by VCOREDIG_PORB
Bits reset by POR or OFFB

Default: The value after reset, as noted in the default column of the memory map.

- Fixed defaults are explicitly declared as 0 or 1.
- “X” corresponds to Read/Write bits that are initialized at start-up, based on the OTP fuse settings or default if V_{DDOTP} = 1.5 V. Bits are subsequently I^2C modifiable, when their reset has been released. “X” may also refer to bits that may have other dependencies. For example, some bits may depend on the version of the IC, or a value from an analog block, for instance the sense bits for the interrupts.

6.6.6.1 Register map

Table 195. Functional page

				BITS[7:0]							
Add	**Register name**	**R/W**	**Default**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
00	DeviceID	R	8'b0011_0000	–	–	–	–	DEVICE ID [3:0]			
				0	0	1	1	0	0	0	0
03	SILICONREVID	R	8'b0001_0000	FULL_LAYER_REV[3:0]				METAL_LAYER_REV[3:0]			
				0	0	0	1	0	0	0	0
04	FABID	R	8'b0000_0000	–	–	–	–	FAB[1:0]		FIN[1:0]	
				0	0	0	0	0	0	0	0
05	INTSTAT0	RW1C	8'b0000_0000	–	–	THERM130I	THERM125I	THERM120I	THERM110I	LOWVINI	PWRONI
				0	0	0	0	0	0	0	0
06	INTMASK0	R/W	8'b0011_1111	–	–	THERM130M	THERM125M	THERM120M	THERM110M	LOWVINM	PWRONM
				0	0	1	1	1	1	1	1
07	INTSENSE0	R	8'b00xx_xxxx	VDDOTPS	ICTESTS	THERM130S	THERM125S	THERM120S	THERM110S	LOWVINS	PWRONS
				0	0	x	x	x	x	x	x
08	INTSTAT1	RW1C	8'b0000_0000	–	–	–	SW3FAULTI	SW2FAULTI	–	SW1BFAULTI	SW1AFAULTI
				0	0	0	0	0	x	0	0
09	INTMASK1	R/W	8'b0111_1111	–	–	–	SW3FAULTM	SW2FAULTM	–	SW1BFAULTM	SW1AFAULTM
				0	1	1	1	1	1	1	1
0A	INTSENSE1	R	8'b0xxx_xxxx	–	–	–	SW3FAULTS	SW2FAULTS	–	SW1BFAULTS	SW1AFAULTS
				0	x	x	x	x	x	x	x
0E	INTSTAT3	RW1C	8'b0000_0000	OTP_ECCI	OTP AUTO BLOW DONE	–	–	–	VPWROVI	–	SWBSTFAULTI
				0	0	0	0	0	0	0	0
0F	INTMASK3	R/W	8'b1100_0101	OTP_ECCM	OTP_AUTO_BLOW_DONEM	–	–	–	VPWROVI	–	SWBSTFAULTM
				1	1	0	0	0	1	0	1
10	INTSENSE3	R	8'b0000_000x	OTP_ECCS	OTP_AUTO_BLOW_DONES	–	–	–	VPWROVS	–	SWBSTFAULTS
				0	0	0	0	0	0	0	0
11	INTSTAT4	RW1C	8'b0000_0000	–	–	VLDO4FAULTI	VLDO3FAULTI	V33FAULTI	VCC_SDFAULTI	VLDO2FAULTI	VLDO1FAULTI
				0	0	0	0	0	0	0	0
12	INTMASK4	R/W	8'b0011_1111	–	–	VLDO4 FAULTM	VLDO3 FAULTM	V33 FAULTM	VCC_SDFAULTM	VLDO2FAULTM	VLDO1FAULTM
				0	0	1	1	1	1	1	1
13	INTSENSE4	R	8'b00xx_xxxx	–	–	VLDO4 FAULTS	VLDO3 FAULTS	V33 FAULTS	VCC_SD FAULTS	VLDO2 FAULTS	VLDO1 FAULTS
				0	0	x	x	x	x	x	x
1A	COINCTL	R/W	8'b0000_0000	–	–	–	–	COINCHEN	VCOIN[2:0]		
				0	0	0	0	0	0	0	0

Table 195. Functional page (continued)

				BITS[7:0]							
Add	**Register name**	**R/W**	**Default**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
1B	PWRCTL	R/W	8'b0001_0000	REGSCPEN	STANDBYINV	STBYDLY[1:0]		PWRONBDBNC[1:0]		PWRONRSTEN	RESTARTEN
				0	0	0	1	0	0	0	0
1C	MEMA	R/W	8'b0000_0000	MEMA[7:0]							
				0	0	0	0	0	0	0	0
1D	MEMB	R/W	8'b0000_0000	MEMB[7:0]							
				0	0	0	0	0	0	0	0
1E	MEMC	R/W	8'b0000_0000	MEMC[7:0]							
				0	0	0	0	0	0	0	0
1F	MEMD	R/W	8'b0000_0000	MEMD[7:0]							
				0	0	0	0	0	0	0	0
20	SW1AVOLT	R/W	8'b000x_xxxx	–	–	–	SW1A[4:0]				
				0	0	0	–	–	–	–	–
21	SW1ASTBY	R/W	8'b000x_xxxx	–	–	–	SW1ASTBY[4:0]				
				0	0	0	–	–	–	–	–
22	SW1AOFF	R/W	8'b000x_xxxx	–	–	–	SW1AOFF[4:0]				
				0	0	0	–	–	–	–	–
23	SW1AMODE	R/W	8'b0000_xxxx	–	–	SW1AOMODE	–	SW1AMODE[3:0]			
				0	0	0	x	–	–	–	–
24	SW1ACONF	R/W	8'bxx00_0100	–	SW1ADVSSPEED	SW1APHASE[1:0]		SW1AFREQ[1:0]		–	SW1AILIM
				x	-1	0	0	–	–	0	0
2E	SW1BVOLT	R/W	8'b0xx1_0010	–	–	–	SW1B[4:0]				
				0	x	x	1	0	0	0	0
2F	SW1BSTBY	R/W	8'b0xx1_0010	–	–	–	SW1BSTBY[4:0]				
				0	x	x	1	0	0	1	0
30	SW1BOFF	R/W	8'b0xx1_0010	–	–	–	SW1BOFF[4:0]				
				0	x	x	1	0	0	1	0
31	SW1BMODE	R/W	8'b0001_1000	–	–	SW1BOMODE	–	SW1BMODE[3:0]			
				0	0	0	–	–	–	–	–
32	SW1BCONF	R/W	8'bx100_0100	–	SW1BDVSSPEED	SW1BPHASE[1:0]		SW1BFREQ[1:0]		–	SW1BILIM
				x	–	0	0	–	–	0	0
35	SW2VOLT	R/W	8'b0xxx_0110	–	–	–	–	SW2_HI	SW2[2:0]		
				0	x	x	x	–	–	–	—
36	SW2STBY	R/W	8'b0xxx_xxxx	–	–	–	–	SW2_HI	SW2STBY[2:0]		
				0	x	x	x	–	–	–	—
37	SW2OFF	R/W	8'b0xxx_xxxx	–	–	–	–	SW2_HI	SW2STBY[2:0]		
				0	x	x	x	–	–	–	—

Table 195. Functional page (continued)

				BITS[7:0]							
Add	**Register name**	**R/W**	**Default**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
38	SW2MODE	R/W	8'b0010_1000	–	–	SW2OMODE	–	SW2MODE[3:0]			
				0	0	1	0	1	0	0	0
39	SW2CONF	R/W	8'bxx01_0100	–	SW2DVS SPEED	SW2PHASE[1:0]		SW2FREQ[1:0]		–	SW2ILIM
				x	–	0	1	–	–	0	0
3C	SW3VOLT	R/W	8'b0xxx_1100	–	–	–	–	SW3[3:0]			
				0	x	x	x	–	–	–	–
3D	SW3STBY	R/W	8'b0xxx_1100	–	–	–	–	SW3STBY[3:0]			
				0	x	x	x	–	–	–	–
3E	SW3OFF	R/W	8'b0xxx_1100	–	–	–	–	SW3OFF[3:0]			
				0	x	x	x	–	–	–	–
3F	SW3MODE	R/W	8'b0011_1000	–	–	SW3OMODE	–	SW3MODE[3:0]			
				0	0	1	1	1	0	0	0
40	SW3CONF	R/W	8'bxx10_0100	–	SW3DVS SPEED	SW3PHASE[1:0]		SW3FREQ[1:0]		–	SW3ILIM
				x	–	1	0	–	–	0	0
66	SWBSTCTL	R/W	8'b0xx0_10xx	–	SWBST1STBYMODE[1:0]		–	SWBST1MODE[1:0] –		SWBST1VOLT[1:0]	
				0	–	–	0	–	–	–	–
69	LDOGCTL	R/W	8'b0xxx_xxx0	–	–	–	–	–	–	–	STBY_LP_B
				0	x	x	x	x	x	x	x
6A	VREFDDRCTL	R/W	8'b000x_0000	–	–	–	VREFDDREN	–	–	–	–
				0	0	0	–	0	0	0	0
6B	VSNVSCTL	R/W	8'b0000_0110	–	–	–	–	–	VSNVSVOLT[2:0]		
				0	0	0	0	0	1	1	0
6C	VLDO1CTL	R/W	8'b010x_1110	LDO1OMODE	VLDO1LPWR	VLDO1STBY	VLDO1EN	VLDO1[3:0]			
				0	0	0	–	–	–	–	—
6D	VLDO2CTL	R/W	8'b000x_1000	LDO2OMODE	VLDO2LPWR	VLDO2STBY	VLDO2EN	VLDO2[3:0]			
				0	0	0	–	–	–	–	—
6E	VCC_SDCTL	R/W	8'b000x_xx10	VCC_SDOMODE	VCC_SDLPWR	VCC_SDSTBY	VCC_SDEN	–	–	VCC_SD[1:0]	
				0	0	0	–	x	x	–	–
6F	V33CTL	R/W	8'b000x_xx10	V33OMODE	V33LPWR	V33STBY	V33EN	–	–	V33[1:0]	
				0	0	0	–	x	x	–	–
70	VLDO3CTL	R/W	8'b010x_0000	VLDO3OMODE	VLDO3LPWR	VLDO3STBY	VLDO3EN	VLDO3[3:0]			
				0	0	0	–	–	–	–	–
71	VLDO4CTL	R/W	8'b000x_xxxx	VLDO4OMODE	VLDO4LPWR	VLDO4STBY	VLDO4EN	VLDO4[3:0]			
				0	0	0	–	–	–	–	–
7F	Page Register	R/W	8'b0000_0000	–	–	–	PAGE[4:0]				
				0	0	0	0	0	0	0	0

Table 196. Extended page 1

Address	Register Name	TYPE	Default	BITS[7:0]							
				7	6	5	4	3	2	1	0
80	OTP FUSE READ EN	R/W	8'b000x_xxx0	–	–	–	–	–	–	–	OTP FUSE READ EN
				0	0	0	x	x	x	x	x
84	OTP LOAD MASK	R/W	8'b0000_0000	START	RL PWBRTN	FORCE PWRCTL	RL PWRCTL	RL OTP	RL OTP ECC	RL OTP FUSE	RL TRIM FUSE
				0	0	0	0	0	0	0	0
8A	OTP ECC SE1	R	8'bxxx0_0000	–	–	–	ECC5_SE	ECC4_SE	ECC3_SE	ECC2_SE	ECC1_SE
				x	x	x	0	0	0	0	0
8B	RSVD	R	8'bxxx0_0000								
8C	OTP ECC DE1	R	8'bxxx0_0000	–	–	–	ECC5_DE	ECC4_DE	ECC3_DE	ECC2_DE	ECC1_DE
				x	x	x	0	0	0	0	0
8D	RSVD	R	8'bxxx0_0000								
A0	OTP SW1A VOLT	R/W	8'b00xx_xxxx				OTP_SW1A_VOLT[4:0]				
				x	x	x	x	x	x	x	x
A1	OTP SW1A SEQ								OTP_SW1A_SEQ[2:0]		
A2	OTP SW1x CONFIG	R/W	8'b000x_xxXx	–	–	–	–	OTP_SW1_CONFIG[1:0]		OTP_SW1x_FREQ[1:0]	
				x	x	x	x	x	x	x	x
A8	OTP SW1B VOLT	R/W	8'b00xx_xxxx				OTP_SW1B_VOLT[4:0]				
				x	x	x	x	x	x	x	x
A9	OTP SW1B SEQ	R/W	8'b00xx_xxxx						OTP_SW1B_SEQ[2:0]		
				x	x	x	x	x	x	x	x
AA	RSVD	R/W	8'b00xx_xxxx								
				x	x	x	x	x	x	x	x
AC	OTP SW2 VOLT	R/W	8'b0xxx_xxxx					OTP_SW2_HI	OTP_SW2_VOLT[2:0]		
				x	x	x	x	x	x	x	x
AD	OTP SW2 SEQ	R/W	8'b0xxx_xxxx					–	OTP_SW2_SEQ[2:0]		
				x	x	x	x	x	x	x	x
AE	OTP SW2 CONFIG	R/W	8'b0000_00xx	–	–	–	–	–	–	OTP_SW2_FREQ[1:0]	
				0	0	0	x	x	0	x	x
B0	OTP SW3 VOLT	R/W	8'b0xxx_xxxx				–	OTP_SW3_VOLT[3:0]			
				x	x	x	x	x	x	x	x
B1	OTP SW3 SEQ	R/W	8'b0xxx_xxxx					–	OTP_SW3_SEQ[2:0]		
				x	x	x	x	x	x	x	x
B2	OTP SW3 CONFIG	R/W	8'b0xxx_xxxx				–			OTP_SW3_FREQ[1:0]	
				x	x	x	x	x	x	x	x
BC	OTP SWBST VOLT	R/W	8'b0000_00xx	–	–	–	–	–	–	OTP_SWBST_VOLT[1:0]	
				0	0	0	0	0	0	0	0

Table 196. Extended page 1 (continued)

Address	Register Name	TYPE	Default	BITS[7:0]							
				7	6	5	4	3	2	1	0
BD	OTP SWBST SEQ	R/W	8'b0000_xxxx	–	–	–	–	–	OTP_SWBST_SEQ[2:0]		
				0	0	0	0	0	0	0	0
C0	OTP VSNVS VOLT	R/W	8'b0000_0xxx	–	–	–	–	–	OTP_VSNVS_VOLT[2:0]		
				0	0	0	0	0	0	0	0
C4	RSVD	R/W	8'b000x_x0xx	–	–	–	–	–	–	–	–
				0	0	0	x	x	x	x	x
C8	OTP VLDO1 VOLT	R/W	8'b0000_xxxx					OTP_VLDO1_VOLT[3:0]			
				0	0	0	0	x	x	x	x
C9	OTP VLDO1 SEQ	R/W	8'b0000_xxxx					OTP_VLDO1_SEQ[3:0]			
				0	0	0	0	x	x	x	x
CC	OTP VLDO2 VOLT	R/W	8'b0000_xxxx					OTP_VLDO2_VOLT[3:0]			
				0	0	0	0	x	x	x	x
CD	OTP VLDO2 SEQ	R/W	8'b0000_xxxx					OTP_VLDO2_SEQ[3:0]			
				0	0	0	0	x	x	x	x
D0	OTP VCC_SD VOLT	R/W	8'b0000_xxxx					–		OTP_VCC_SD_VOLT[2:0]	
				0	0	0	0	x	x	x	x
D1	OTP VCC_SD SEQ	R/W	8'b0000_xxxx						OTP_VCC_SD_SEQ[2:0]		
				0	0	0	0	0	x	x	x
D4	OTP V33 VOLT	R/W	8'b0000_xxxx							OTP_V33_VOLT[2:0]	
				0	0	0	0	x	x	x	x
D5	OTP V33 SEQ	R/W	8'b0000_xxxx						OTP_V33_SEQ[3:0]		
				0	0	0	0	x	x	x	x
D8	OTP VLDO3 VOLT	R/W	8'b0000_xxxx					OTP_VLDO3_VOLT[3:0]			
				0	0	0	0	x	x	x	x
D9	OTP VLDO3 SEQ	R/W	8'b0000_xxxx					OTP_VLDO3_SEQ[3:0]			
				0	0	0	0	x	x	x	x
DC	OTP VLDO4 VOLT	R/W	8'b0000_xxxx					OTP_VLDO4_VOLT[3:0]			
				0	0	0	0	x	x	x	x
DD	OTP VLDO4 SEQ	R/W	8'b0000_xxxx					OTP_VLDO4_SEQ[3:0]			
				0	0	0	0	x	x	x	x
E0	OTP PU CONFIG1	R/W	8'b000x_xxxx				OTP_PWRON_CFG		OTP_SWDVS_CLK		OTP_SEQ_CLK_SPEED
				x	x	x	x	x	x	x	x
E4	OTP FUSE POR1	R/W	8'b0000_00x0	TBB_POR	–	–	–	–	–	–	–
				0	0	0	0	0	0	x	0
E5	RSVD	R/W	8'b0000_00x0	–	–	–	–	–	–		–
				0	0	0	0	0	0		0
E6	RSVD	R/W	8'b0000_00x0	–	–	–	–	–	–		–
				0	0	0	0	0	0		0

Table 196. Extended page 1 (continued)

Address	Register Name	TYPE	Default	BITS[7:0]							
				7	6	5	4	3	2	1	0
E7	RSVD	R	8'b0000_00x0	–	–	–	–	–	–		–
				0	0	0	0	0	0		0
E8	OTP PWRGD EN	R/W/M	8'b0000_000x	–	–	–	–	–	–	–	OTP_PG_EN
				0	0	0	0	0	0	x	0
F0	RSVD	R/W	8'b000x_xxxx	–	–	–					
				0	0	0	x	x	x	x	x
F1	RSVD	R/W	8'b000x_xxxx	–	–	–					
				0	0	0	x	x	x	x	x
F7	OTP BLOWN	R/W	8'b0000_000x	–	–	–	–	–	–	–	OTP_BLOWN
				0	0	0	0	0	0	0	x
FF	OTP I2C ADDR	R/W	8'b0000_1xxx	USE_DEFAULT_ADD		–		I2C_SLV ADDR[3]	OTP_I2C_SLV ADDR[2:0]		
				0	0	0	0	1	x	x	x

Table 197. Extended page 2

Address	Register Name	TYPE	Default	BITS[7:0]							
				7	6	5	4	3	2	1	0
81	SW1A PWRSTG	R/W	8'b1111_1111	RSVD	RSVD	RSVD	RSVD	RSVD	SW1A_PWRSTG[2:0]		
				1	1	1	1	1	1	1	1
83	SW1B PWRSTG	R	8'b1111_1111	RSVD	RSVD	RSVD	RSVD	RSVD	SW1B_PWRSTG[2:0] RSVD		
				1	1	1	1	1	1	1	1
84	SW2 PWRSTG	R	8'b1111_1111	RSVD	RSVD	RSVD	RSVD	RSVD	SW2_PWRSTG[2:0] RSVD		
				1	1	1	1	1	1	1	1
85	SW3 PWRSTG	R	8'b1111_1111	RSVD	RSVD	RSVD	RSVD	RSVD	SW3_PWRSTG[2:0] RSVD		
				1	1	1	1	1	1	1	1
88	PWRCTRL OTP CTRL	R	8'b0000_0001	–	–	–	–	–	–	OTP_PWRGD_EN	PG_SHDWN_EN
				0	0	0	0	0	0	0	1
8D	I2C WRITE ADDRESS TRAP	R/W	8'b0000_0000	I2C_WRITE_ADDRESS_TRAP[7:0]							
				0	0	0	0	0	0	0	0
8E	I2C TRAP PAGE	R/W	8'b0000_0000	LET_IT_ ROLL	RSVD	RSVD	I2C_TRAP_PAGE[4:0]				
				0	0	0	0	0	0	0	0
8F	I2C TRAP CNTR	R/W	8'b0000_0000	I2C_WRITE_ADDRESS_COUNTER[7:0]							
				0	0	0	0	0	0	0	0
90	IO DRV	R/W	8'b00xx_xxxx	SDA_DRV[1:0]		RSVD		INTB_DRV[1:0]		RESETBMCU_DRV[1:0]	
				0	0	x	x	x	x	x	x
D0	OTP AUTO ECC0	R/W	8'b0000_0000	–	–	–	AUTO_ECC_BANK5	AUTO_ECC_BANK4	AUTO_ECC_BANK3	AUTO_ECC_BANK2	AUTO_ECC_BANK1
				0	0	0	0	0	0	0	0
D8	Reserved	–	8'b0000_0000	AUTO_BLOW_TIME[7:0]							
				0	0	0	0	0	0	0	0
D9	Reserved	–	8'b0000_0000	START	RELOAD	EN_RW	AUTO_FUSE_BLOW5	AUTO_FUSE_BLOW4	AUTO_FUSE_BLOW3	AUTO_FUSE_BLOW2	AUTO_FUSE_BLOW1
				0	0	0	0	0	0	0	0

Table 197. Extended page 2 (continued)

Address	Register Name	TYPE	Default	BITS[7:0]							
				7	6	5	4	3	2	1	0
E1	OTP ECC CTRL1	R/W	8'b0000_0000	RSVD	ECC1_CALC_CIN	ECC1_CIN_TBB[5:0]					
				0	0	0	0	0	0	0	0
E2	OTP ECC CTRL2	R/W	8'b0000_0000	RSVD	ECC2_CALC_CIN	ECC2_CIN_TBB[5:0]					
				0	0	0	0	0	0	0	0
E3	OTP ECC CTRL3	R/W	8'b0000_0000	RSVD	ECC3_CALC_CIN	ECC3_CIN_TBB[5:0]					
				0	0	0	0	0	0	0	0
E4	OTP ECC CTRL4	R/W	8'b0000_0000	RSVD	ECC4_CALC_CIN	ECC4_CIN_TBB[5:0]					
				0	0	0	0	0	0	0	0
E5	OTP ECC CTRL5	R/W	8'b0000_0000	RSVD	ECC5_CALC_CIN	ECC5_CIN_TBB[5:0]					
				0	0	0	0	0	0	0	0
F1	OTP FUSE CTRL1	R/W	8'b0000_0000	–	–	–	–	ANTIFUSE1_EN	ANTIFUSE1_LOAD	ANTIFUSE1_RW	BYPASS1
				0	0	0	0	0	0	0	0
F2	OTP FUSE CTRL2	R/W	8'b0000_0000	–	–	–	–	ANTIFUSE2_EN	ANTIFUSE2_LOAD	ANTIFUSE2_RW	BYPASS2
				0	0	0	0	0	0	0	0
F3	OTP FUSE CTRL3	R/W	8'b0000_0000	–	–	–	–	ANTIFUSE3_EN	ANTIFUSE3_LOAD	ANTIFUSE3_RW	BYPASS3
				0	0	0	0	0	0	0	0
F4	OTP FUSE CTRL4	R/W	8'b0000_0000	–	–	–	–	ANTIFUSE4_EN	ANTIFUSE4_LOAD	ANTIFUSE4_RW	BYPASS4
				0	0	0	0	0	0	0	0
F5	OTP FUSE CTRL5	R/W	8'b0000_0000	–	–	–	–	ANTIFUSE5_EN	ANTIFUSE5_LOAD	ANTIFUSE5_RW	BYPASS5
				0	0	0	0	0	0	0	0

7 Typical applications

7.1 Application diagram

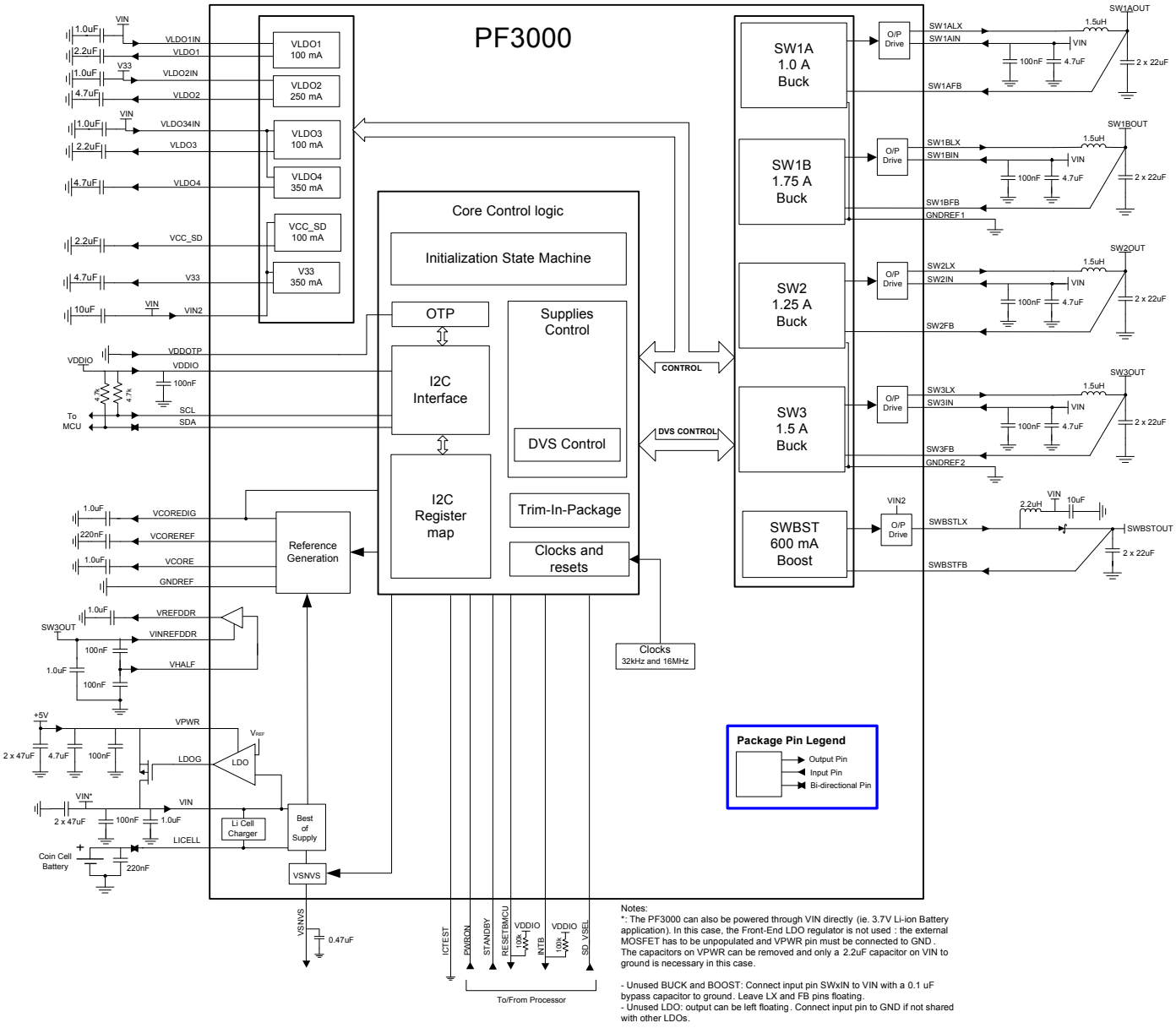


Figure 36. Typical application schematic

8 Bill of materials

The following table provides a complete list of the recommended components on a full featured system using the PF3000 Device for -40 °C to 85 °C applications. Components are provided with an example part number; equivalent components may be used.

Table 198. Bill of materials for -40 °C to 85 °C applications

Value	Qty	Description	Part#	Manufacturer	Component/Pin
PMIC					
N/A	1	Power management IC	PF3000	NXP	IC
Buck regulators					
1.5 µH	4	IND PWR 1.5 µH at 1.0 MHz 2.9 A 20% 2016	DFE201610E-1R5M	TOKO INC.	SW1A, SW1B, SW2, SW3 inductors
		IND PWR 1.5 µH at 1.0 MHz 2.2 A 20% 1210	BRL3225T1R5M	Taiyo Yuden	Alternate for low-power applications
4.7 µF	4	CAP CER 4.7 µF 10 V 20% X5R 0402	GRM155R61A475MEAA	Murata	SW1A, SW1B, SW2, SW3 input capacitors
0.1 µF	4	CAP CER 0.1 µF 10 V 20% X5R 0201	GRM033R61A104ME84	Murata	SW1A, SW1B, SW2, SW3 input capacitors (optional)
22 µF	8	CAP CER 22 µF 10 V 20% X5R 0603	GRM188R61A226ME15	Murata	SW1A, SW1B, SW2, SW3 output capacitors
Boost regulator					
2.2 µH	1	IND PWR 2.2 µH at 1.0 MHz 2.4 A 20% 2016	DFE201610E-2R2M	TOKO INC.	SWBST inductor
		IND PWR 2.2 µH at 1.0 MHz 1.85 A 20% 1210	BRL3225T2R2M	Taiyo Yuden	Alternate for low-power applications
10 µF	1	CAP CER 10 µF 10 V 20% X5R 0402	GRM155R61A106ME11	Murata	SWBST input capacitor
N/A	1	DIODE SCH PWR RECT 1.0 A 20 V SMT	MBR120LSFT3G	ON Semi	SWBST diode
22 µF	2	CAP CER 22 µF 10 V 20% X5R 0603	GRM188R61A226ME15D	Murata	SWBST output capacitors
Linear regulators					
1.0 µF	3	CAP CER 1.0 µF 10 V 20% X5R 0201	GRM033R61A105ME44	Murata	VLDO1, VLDO2, VLDO3 and VLDO4 input capacitors
2.2 µF	3	CAP CER 2.2 µF 10 V 20% X5R 0201	GRM033R61A225ME47	Murata	VLDO1, VLDO3, VCC_SD output capacitors
10 µF	1	CAP CER 10 µF 10 V 20% X5R 0402	GRM155R61A106ME11	Murata	V33 and VCC_SD input capacitor
4.7 µF	3	CAP CER 4.7 µF 10 V 20% X5R 0402	GRM155R61A475MEAA	Murata	VLDO2, VLDO4, V33 output capacitors
Miscellaneous					
1.0 µF	4	CAP CER 1.0 µF 10 V 20% X5R 0201	GRM033R61A105ME44	Murata	VCORE, VCOREDIG, VREFDDR, VINREFDDR capacitors
0.22 µF	2	CAP CER 0.22 µF 10 V 20% X5R 0201	GRM033R61A224ME90	Murata	VCOREREF and Coin Cell output capacitors
0.47 µF	1	CAP CER 0.47 µF 10 V 20% X5R 0201	GRM033R61A474ME90	Murata	VSNVS output capacitor
47 µF	4	CAP CER 47 µF 10 V 20% X5R 0805	GRM21BR61A476ME15	Murata	Front-end LDO capacitors for VIN and VPWR.

Table 198. Bill of materials for -40 °C to 85 °C applications (continued)

Value	Qty	Description	Part#	Manufacturer	Component/Pin
2.2 µF	1	CAP CER 2.2 µF 10 V 20% X5R 0201	GRM033R61A225ME47	Murata	VIN input capacitor when not using Front-end LDO
0.1 µF	5	CAP CER 0.1 µF 10 V 10% X5R 0201	GRM033R61A104KE84	Murata	VDDIO, VHALF, VPWR, VIN input capacitors (optional)
N/A	1	TRAN PMOS 11. A 12 V 12 SOT-1220	PMPB15XP	NXP	External MOSFET
100 k	2	RES MF 100 k 1/16 W 1% 0402	RC0402FR-07100KL	Yageo America	Pull-up resistors
4.7 k	2	RES MF 4.70 k 1/20 W 1% 0201	RC0201FR-074K7L	Yageo America	I²C pull-up resistors

The following table provides a complete list of the recommended components on a full featured system using the PF3000 Device for -40 °C to 105 °C applications. Components are provided with an example part number, equivalent components may be used.

Table 199. Bill of materials for -40 °C to 105 °C applications

Value	Qty	Description	Part#	Manufacturer	Component/Pin
PMIC					
N/A	1	Power management IC	PF3000	NXP	IC
Buck regulators					
1.5 µH	4	IND PWR 1.5 µH at 1.0 MHz 2.9 A 20% 2016	DFE201610E-1R5M	Toko Inc.	SW1A, SW1B, SW2, SW3 inductors
		IND PWR 1.5 µH at 1.0 MHz 2.2 A 20% 1210	BRL3225T1R5M	Taiyo Yuden	Alternate for low-power applications
4.7 µF	4	CAP CER 4.7 µF 10 V 10% X7S 0603	GRM188C71A475KE11	Murata	SW1A, SW1B, SW2, SW3 input capacitors
0.1 µF	4	CAP CER 0.1 µF 10 V 10% X7S 0201	GRM033C71A104KE14	Murata	SW1A, SW1B, SW2, SW3 input capacitors (optional)
22 µF	8	CAP CER 22 µF 10 V 20% X7T 0805	GRM21BD71A226ME44	Murata	SW1A, SW1B, SW2, SW3 output capacitors
Boost regulator					
2.2 µH	1	IND PWR 2.2 µH at 1.0 MHz 2.4 A 20% 2016	DFE201610E-2R2M	Toko Inc.	SWBST Inductor
		IND PWR 2.2 µH at 1.0 MHz 1.85 A 20% 1210	BRL3225T2R2M	Taiyo Yuden	Alternate for low-power applications
10 µF	1	CAP CER 10 µF 10 V 20% X7T 0603	GRM188D71A106MA73	Murata	SWBST input capacitor
N/A	1	DIODE SCH PWR RECT 1.0 A 20 V SMT	MBR120LSFT3G	ON Semi	SWBST diode
22 µF	2	CAP CER 22 µF 10 V 20% X5R 0603	GRM188R61A226ME15D	Murata	SWBST output capacitors
Linear regulators					
1.0 µF	3	CAP CER 1.0 µF 10 V 10% X7S 0402	GRM155C71A105KE11	Murata	VLDO1, VLDO2, VLDO3 and VLDO4 input capacitors
2.2 µF	3	CAP CER 2.2 µF 10 V 10% X7S 0402	GRM155C71A225KE11	Murata	VLDO1, VLDO3, VCC_SD output capacitors
10 µF	1	CAP CER 10 µF 10 V 20% X7T 0603	GRM188D71A106MA73	Murata	V33 and VCC_SD input capacitor

Table 199. Bill of materials for -40 °C to 105 °C applications (continued)

Value	Qty	Description	Part#	Manufacturer	Component/Pin
4.7 µF	3	CAP CER 4.7 µF 10 V 10% X7S 0603	GRM188C71A475KE11	Murata	VLDO2, VLDO4, V33 output capacitors
Miscellaneous					
1.0 µF	4	CAP CER 1.0 µF 10 V 10% X7R 0402	GRM155C71A105KE11	Murata	VCORE, VCOREDIG, VREFDDR, VINREFDDR capacitors
0.22 µF	2	CAP CER 0.22 µF 10 V 10% X7R 0402	GRM155R71A224KE01	Murata	VCOREREF and coin cell output capacitors
0.47 µF	1	CAP CER 0.47 µF 10 V 20% X5R 0201	GRM155R71A474KE01	Murata	VSNVS output capacitor
47 µF	4	CAP CER 47 µF 10 V 20% X7R 1210	GRM32ER71A476ME15	Murata	Front-end LDO capacitors for VIN and VPWR.
2.2 µF	1	CAP CER 2.2 µF 10 V 10% X7S 0402	GRM155C71A225KE11	Murata	VIN input capacitor when not using front-end LDO
0.1 µF	5	CAP CER 0.1 µF 10 V 10% X7S 0201	GRM033C71A104KE14	Murata	VDDIO, VHALF, VPWR, VIN input capacitors (optional)
N/A	1	TRAN PMOS 11. A 12 V 12 SOT-1220	PMPB15XP	NXP	External MOSFET
100 k	2	RES MF 100k 1/16 W 1% 0402	RC0402FR-07100KL	Yageo America	Pull-up resistors
4.7 k	2	RES MF 4.70k 1/20 W 1% 0201	RC0201FR-074K7L	Yageo America	I²C pull-up resistors

9 Thermal information

9.1 Rating data

The thermal rating data of the packages has been simulated with the results listed in Thermal ratings. Junction to ambient thermal resistance nomenclature: the JEDEC specification reserves the symbol $R_{\theta JA}$ or θJA (Theta-JA) strictly for junction-to-ambient thermal resistance on a 1s test board in natural convection environment. $R_{\theta JMA}$ or θJMA (Theta-JMA) is used for both junction-to-ambient on a 2s2p test board in natural convection and for junction-to-ambient with forced convection on both 1s and 2s2p test boards. It is anticipated that the generic name, Theta-JA, continues to be commonly used. The JEDEC standards can be consulted at http://www.jedec.org.

9.2 Estimation of junction temperature

An estimation of the chip junction temperature T_J can be obtained from the equation:

$T_J = T_A + (R_{\theta JA} \times P_D)$

with:

T_A = Ambient temperature for the package in °C

$R_{\theta JA}$ = Junction to ambient thermal resistance in °C/W

P_D = Power dissipation in the package in W

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board $R_{\theta JA}$ and the value obtained on a four layer board $R_{\theta JMA}$. Actual application PCBs show a performance close to the simulated four layer board value although this may be somewhat degraded in case of significant power dissipated by other components placed close to the device.

At a known board temperature, the junction temperature T_J is estimated using the following equation

$T_J = T_B + (R_{\theta JB} \times P_D)$ with

T_B = Board temperature at the package perimeter in °C

$R_{\theta JB}$ = Junction to board thermal resistance in °C/W

P_D = Power dissipation in the package in W

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made.

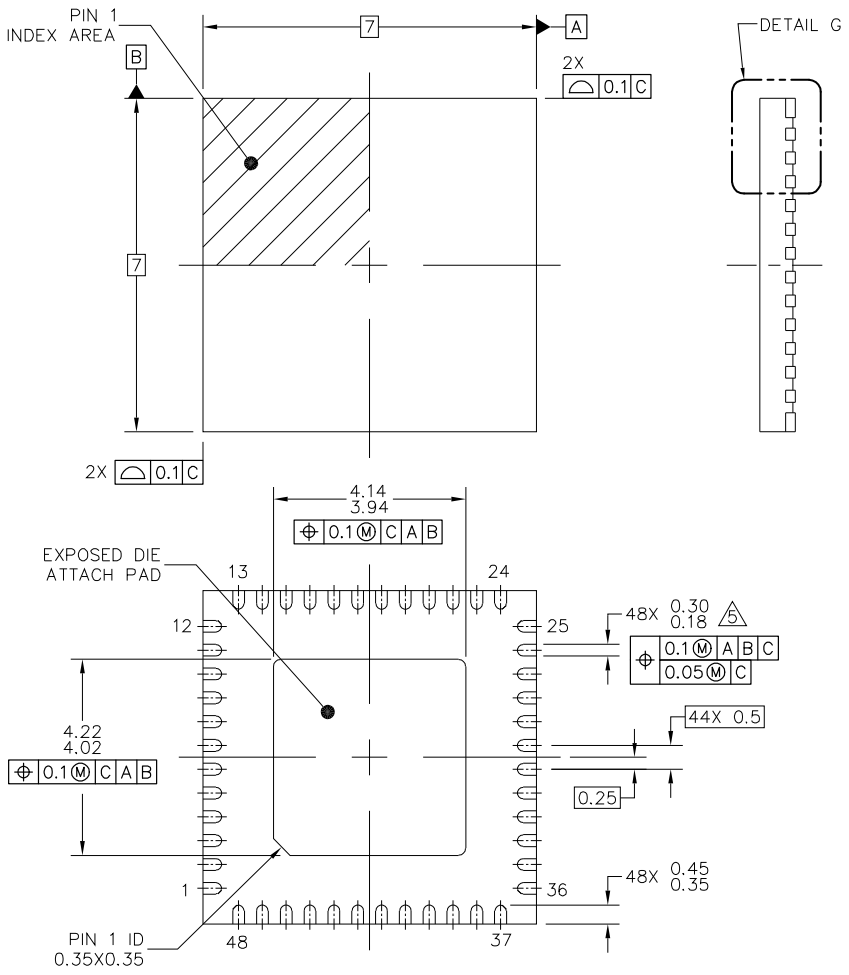
10 Packaging

10.1 Packaging dimensions

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.nxp.com and perform a keyword search for the drawing's document number. See the Thermal Characteristics section for specific thermal characteristics for each package.

Table 200. Package drawing information

Package	Suffix	Package outline drawing number
48-pin QFN 7X7 mm - 0.5mm pitch	EP	98ASA00719D
48 QFN 7.0 mm x 7.0 mm WF-type (wettable flank)	ES	98ASA00933D



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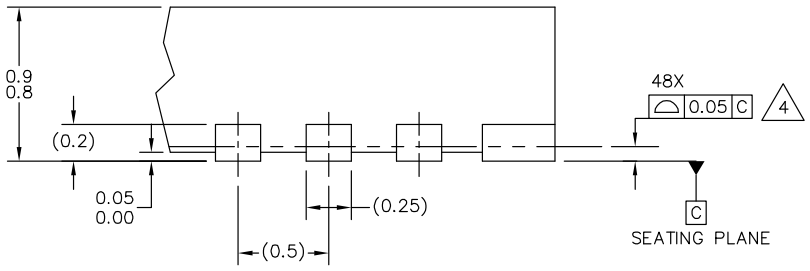
TITLE: QFN, THERMALLY ENHANCED, 7 X 7 X 0.85, 0.5 PITCH, 48 TERMINAL	DOCUMENT NO: 98ASA00719D	REV: B
	STANDARD: NON-JEDEC	
	27 JUN 2014	

PF3000



DETAIL G
VIEW ROTATED 90°CW

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TITLE: QFN, THERMALLY ENHANCED, 7 X 7 X 0.85, 0.5 PITCH, 48 TERMINAL	DOCUMENT NO: 98ASA00719D	REV: B
	STANDARD: NON-JEDEC	
	27 JUN 2014	

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. THIS IS A NON–JEDEC REGISTERED PACKAGE.
4. COPLANARITY APPLIES TO LEADS AND DIE ATTACH FLAG.
5. DIMENSION APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.3 MM FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION SHOULD NOT BE MEASURED IN THAT RADIUS AREA.

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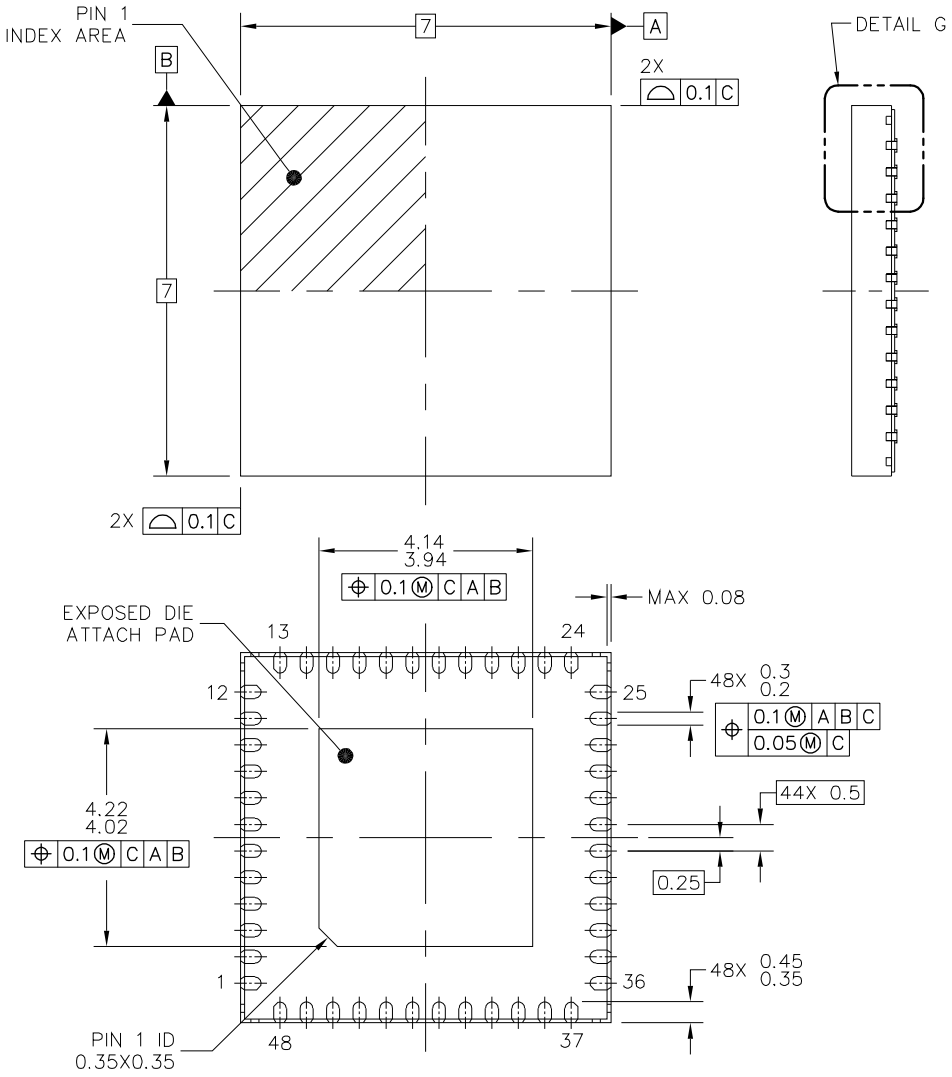
	STANDARD: NON–JEDEC	
	27 JUN 2014	



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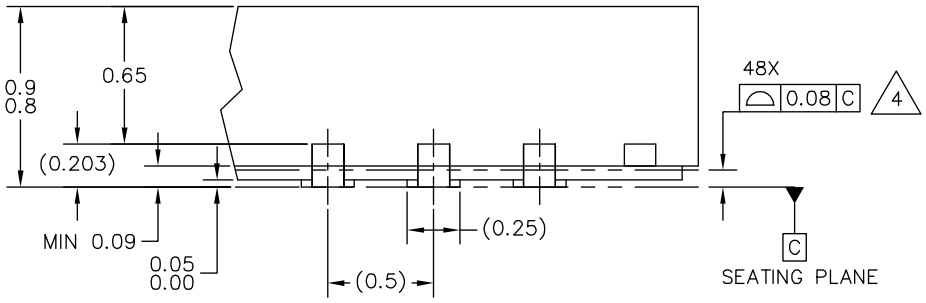
TITLE: QFN, THERMALLY ENHANCED, 7 X 7 X 0.85, 0.5 PITCH, 48 TERMINAL	DOCUMENT NO: 98ASA00933D	REV: O
	STANDARD: NON-JEDEC	
	23 SEP 2015	



DETAIL G
VIEW ROTATED 90°CW

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	STANDARD: NON-JEDEC	
	23 SEP 2015	

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. THIS IS A NON–JEDEC REGISTERED PACKAGE.
4. COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.
5. MIN METAL GAP SHOULD BE 0.2 MM.

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MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: QFN, THERMALLY ENHANCED, 7 X 7 X 0.85, 0.5 PITCH, 48 TERMINAL	DOCUMENT NO: 98ASA00933D REV: O
	STANDARD: NON–JEDEC
	23 SEP 2015

11 Revision history

Revision	Date	Description of changes
1.0	11/2014	• Initial release
2.0	2/2015	• VREFDDR output accuracy spec re-formatted • Added typical performance waveforms • Corrected OTP option 1 set points • LDO current limit specifications updated • VPWR LDO output voltage accuracy specification updated • Updated register names of Extended Page 1 registers to maintain consistency throughout document • Added typical bill of materials
3.0	2/2015	• Corrected Register INTSENSE0 - ADDR 0x07 • Added orderable part numbers PC32PF3000A5EP and PC34PF3000A5EP
4.0	6/2015	• Included i.MX Series processor • Redefined voltages for SW1A and SW1A/B • Corrected typographic errors • Improved bill of materials capacitors • Updated SW1A/B, SW1A, and SW1B Output Voltage Accuracy • Added note on LICELL for Operating Input Voltage • Improved temperature range to 105 °C • Updated ILIM max values for Linear regulators • VCOREDIG/VCOREREF tables updated • Updated LSL of ISW1BLIM to 2.4 A
5.0	6/2015	• Replaced i.MX Series by i.MX 7 • Added i.MX 6UL processor • Updated Bill of Materials Table 199
6.0	8/2015	• Added MC32PF3000A6EP, MC34PF3000A6EP, MC32PF3000A7EP, and MC34PF3000A7EP parts to the Orderable Part Variations Table • Updated Table 42 • Removed i.MX 6 DL note on Power Virus • Updated the definition of rated current for switchers and linear regulators
7.0	3/2016	• Added 98ASA00933D and the page 1 package image for wettable flank • Changed Table 2, pins 7, 10, 18, and 28, from Bypass with at least a 10 µF to Bypass with at least a 4.7 µF • Added PC33PF3000A0ES, PC33PF3000A3ES, PC33PF3000A4ES, PC33PF3000A5ES, PC33PF3000A6ES, and PC33PF3000A7ES to Table 1
	8/2016	• Changed PC33PF3000A0ES, PC33PF3000A3ES, PC33PF3000A4ES, PC33PF3000A5ES, PC33PF3000A6ES, and PC33PF3000A7ES to MC parts in Table 1
	9/2016	• Updated Table 66 LDO Control to accurately describe all modes
8.0	3/2017	• Added MC32PF3000A8EP and MC34PF3000A8EP parts to Table 1 • Added new note (2) to Table 1 • Updated $V_{SW1AACC}$ parameter in Table 7 • Added OTP configuration for A8 to Table 42 • Updated Table 80 (changed default value to 1)
9.0	8/2017	• Updated notes (47) and (49) as per 201707041I

RoHS

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