

HEF4001B

Quad 2-input NOR gate

Rev. 10 — 10 December 2015

Product data sheet

1. General description

The HEF4001B is a quad 2-input NOR gate. The outputs are fully buffered for the highest noise immunity and pattern insensitivity to output impedance.

It operates over a recommended V_{DD} power supply range of 3 V to 15 V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD} , V_{SS} , or another input.

2. Features and benefits

- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from -40°C to $+125^{\circ}\text{C}$
- Complies with JEDEC standard JESD 13-B
- Inputs and outputs are protected against electrostatic effects

3. Ordering information

Table 1. Ordering information

All types operate from -40°C to $+125^{\circ}\text{C}$

Type number	Package		Version
	Name	Description	
HEF4001BT	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1

4. Functional diagram

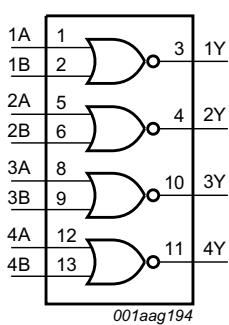


Fig 1. Functional diagram

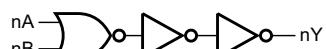


Fig 2. Logic diagram (one gate)

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5. Pinning information

5.1 Pinning

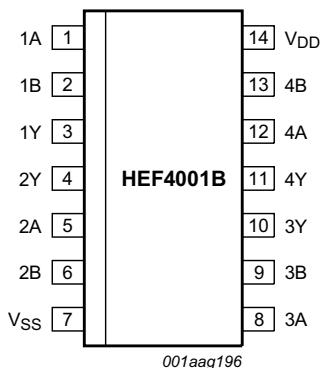


Fig 3. Pin configuration

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
nA	1, 5, 8, 12	input
nB	2, 6, 9, 13	input
nY	3, 4, 10, 11	output
V _{SS}	7	ground (0 V)
V _{DD}	14	supply voltage

6. Functional description

Table 3. Function table^[1]

Input		Output
nA	nB	nY
L	L	H
L	H	L
H	L	L
H	H	L

[1] H = HIGH voltage level; L = LOW voltage level.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to $V_{SS} = 0$ V (ground).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		-0.5	+18	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{DD} + 0.5$ V	-	± 10	mA
V_I	input voltage		-0.5	$V_{DD} + 0.5$	V
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{DD} + 0.5$ V	-	± 10	mA
$I_{I/O}$	input/output current		-	± 10	mA
I_{DD}	supply current		-	50	mA
T_{stg}	storage temperature		-65	+150	°C
T_{amb}	ambient temperature		-40	+125	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to + 125 °C			
		SO14	[1]	-	500 mW
P	power dissipation	per output	-	100	mW

[1] For SO14 packages: above $T_{amb} = 70$ °C, P_{tot} derates linearly with 8 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		3	-	15	V
V_I	input voltage		0	-	V_{DD}	V
T_{amb}	ambient temperature	in free air	-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{DD} = 5$ V	-	-	3.75	μs/V
		$V_{DD} = 10$ V	-	-	0.5	μs/V
		$V_{DD} = 15$ V	-	-	0.08	μs/V

9. Static characteristics

Table 6. Static characteristics

$V_{SS} = 0$ V; $V_I = V_{SS}$ or V_{DD} ; unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	$T_{amb} = -40$ °C		$T_{amb} = +25$ °C		$T_{amb} = +85$ °C		$T_{amb} = +125$ °C		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$ I_O < 1$ μA	5 V	3.5	-	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	11.0	-	V
V_{IL}	LOW-level input voltage	$ I_O < 1$ μA	5 V	-	1.5	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	-	4.0	V
V_{OH}	HIGH-level output voltage	$ I_O < 1$ μA	5 V	4.95	-	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	14.95	-	V
V_{OL}	LOW-level output voltage	$ I_O < 1$ μA	5 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	-	0.05	V
I_{OH}	HIGH-level output current	$V_O = 2.5$ V	5 V	-	-1.7	-	-1.4	-	-1.1	-	-1.1	mA
		$V_O = 4.6$ V	5 V	-	-0.64	-	-0.5	-	-0.36	-	-0.36	mA
		$V_O = 9.5$ V	10 V	-	-1.6	-	-1.3	-	-0.9	-	-0.9	mA
		$V_O = 13.5$ V	15 V	-	-4.2	-	-3.4	-	-2.4	-	-2.4	mA
I_{OL}	LOW-level output current	$V_O = 0.4$ V	5 V	0.64	-	0.5	-	0.36	-	0.36	-	mA
		$V_O = 0.5$ V	10 V	1.6	-	1.3	-	0.9	-	0.9	-	mA
		$V_O = 1.5$ V	15 V	4.2	-	3.4	-	2.4	-	2.4	-	mA
I_I	input leakage current		15 V	-	± 0.1	-	± 0.1	-	± 1.0	-	± 1.0	μA
I_{DD}	supply current	all valid input combinations; $I_O = 0$ A	5 V	-	0.25	-	0.25	-	7.5	-	7.5	μA
			10 V	-	0.5	-	0.5	-	15.0	-	15.0	μA
			15 V	-	1.0	-	1.0	-	30.0	-	30.0	μA
C_I	input capacitance			-	-	-	7.5	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

$T_{amb} = 25^\circ C$; for waveforms see [Figure 4](#); for test circuit see [Figure 5](#); unless otherwise specified.

Symbol	Parameter	Extrapolation formula ^[1]	V _{DD}	Min	Typ	Max	Unit
t _{PHL}	HIGH to LOW propagation delay	33 + 0.55 × C _L	5 V	-	60	120	ns
		14 + 0.23 × C _L	10 V	-	25	50	ns
		12 + 0.16 × C _L	15 V	-	20	40	ns
t _{PLH}	LOW to HIGH propagation delay	23 + 0.55 × C _L	5 V	-	50	100	ns
		14 + 0.23 × C _L	10 V	-	25	45	ns
		12 + 0.16 × C _L	15 V	-	20	35	ns
t _{THL}	HIGH to LOW output transition time	10 + 1.00 × C _L	5 V	-	60	120	ns
		9 + 0.42 × C _L	10 V	-	30	60	ns
		6 + 0.28 × C _L	15 V	-	20	40	ns
t _{TLH}	LOW to HIGH output transition time	10 + 1.00 × C _L	5 V	-	60	120	ns
		9 + 0.42 × C _L	10 V	-	30	60	ns
		6 + 0.28 × C _L	15 V	-	20	40	ns

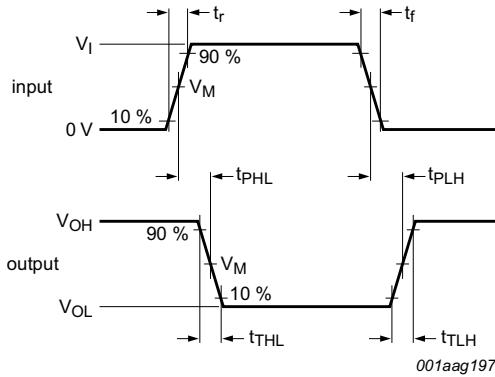
[1] The typical value of the propagation delay and output transition time can be calculated with the extrapolation formula (C_L in pF).

Table 8. Dynamic power dissipation

$V_{SS} = 0 V$; $t_f = t_f \leq 20 \text{ ns}$; $T_{amb} = 25^\circ C$.

Symbol	Parameter	V _{DD}	Typical formula	Where
P _D	dynamic power dissipation	5 V	$P_D = 1100 \times f_i + \sum(f_o \times C_L) \times V_{DD}^2 \text{ (} \mu\text{W)}$	$f_i = \text{input frequency in MHz};$ $f_o = \text{output frequency in MHz};$ $C_L = \text{output load capacitance in pF};$ $\sum(f_o \times C_L) = \text{sum of the outputs};$ $V_{DD} = \text{supply voltage in V}.$
		10 V	$P_D = 5000 \times f_i + \sum(f_o \times C_L) \times V_{DD}^2 \text{ (} \mu\text{W)}$	
		15 V	$P_D = 14200 \times f_i + \sum(f_o \times C_L) \times V_{DD}^2 \text{ (} \mu\text{W)}$	

11. Waveforms



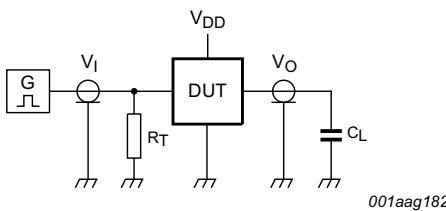
Measurement points are given in [Table 9](#).

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 4. Propagation delay, output transition time

Table 9. Measurement points

Supply voltage	Input	Output
V_{DD}	V_M	V_M
5 V to 15 V	$0.5V_{DD}$	$0.5V_{DD}$



Test data is given in [Table 10](#).

Definitions for test circuit:

DUT = Device Under Test.

C_L = load capacitance including jig and probe capacitance.

R_T = termination resistance should be equal to the output impedance Z_0 of the pulse generator.

Fig 5. Test circuit for measuring switching times

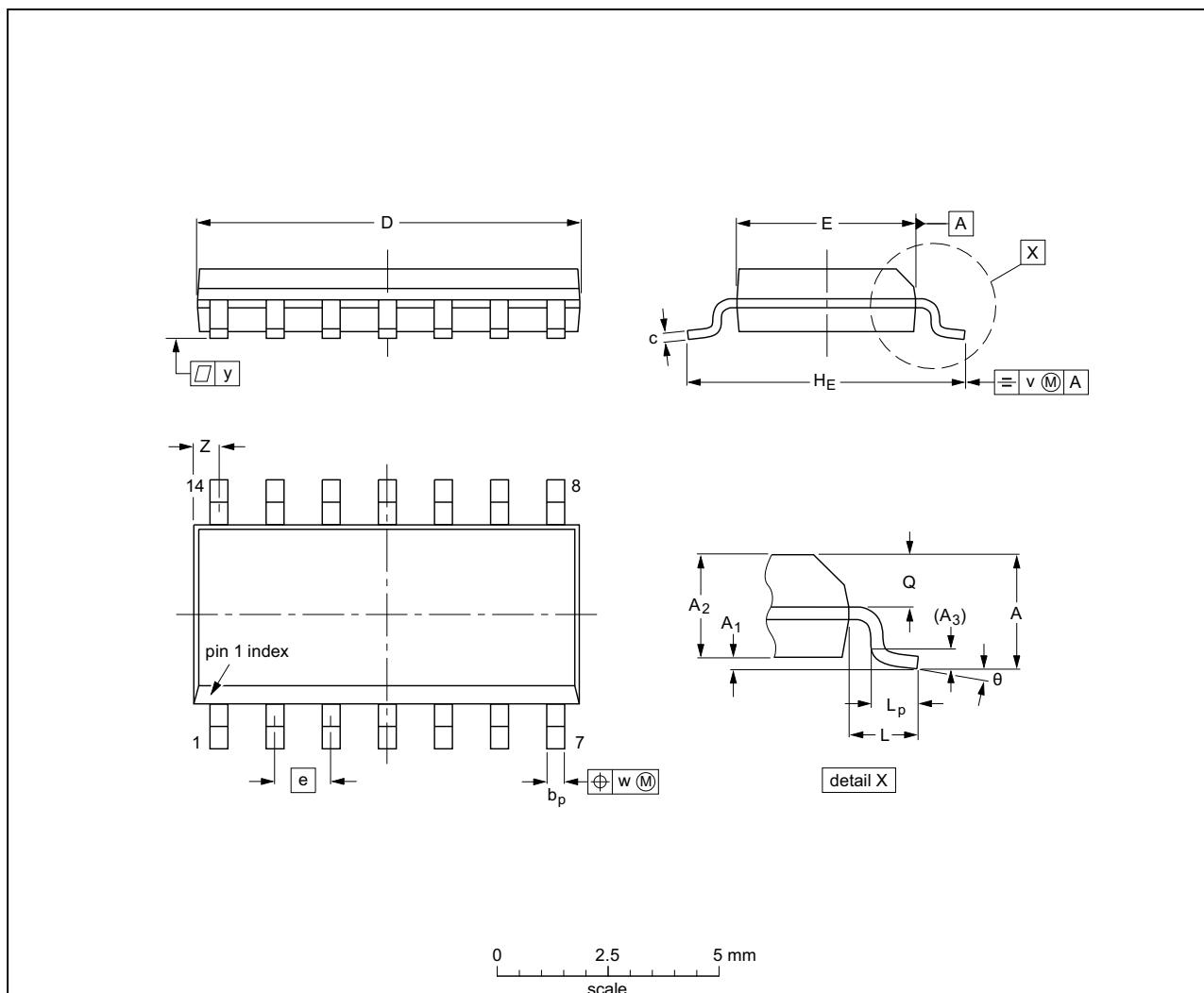
Table 10. Test data

Supply voltage	Input	Load
V_{DD}	V_I	t_r, t_f
5 V to 15 V	V_{SS} or V_{DD}	≤ 20 ns
		50 pF

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75 0.10	0.25 1.25	1.45	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069 0.004	0.010 0.049	0.057	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	0° 0°

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				99-12-27 03-02-19

Fig 6. Package outline SOT108-1 (SO14)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
DUT	Device Under Test

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4001B v.10	20151210	Product data sheet	-	HEF4001B v.9
Modifications:	<ul style="list-style-type: none">• Type number HEF4001BP (SOT27-1) removed.			
HEF4001B v.9	20111121	Product data sheet	-	HEF4001B v.8
Modifications:	<ul style="list-style-type: none">• Legal pages updated.• Changes in “General description” and “Features and benefits”.• Section “Applications” removed.			
HEF4001B v.8	20110913	Product data sheet	-	HEF4001B v.7
HEF4001B v.7	20091027	Product data sheet	-	HEF4001B v.6
HEF4001B v.6	20090618	Product data sheet	-	HEF4001B v.5
HEF4001B v.5	20080327	Product data sheet	-	HEF4001B v.4
HEF4001B v.4	20070731	Product data sheet	-	HEF4001B_CNV v.3
HEF4001B_CNV v.3	19950101	Product specification	-	HEF4001B_CNV v.2
HEF4001B_CNV v.2	19950101	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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17. Contents

1	General description	1
2	Features and benefits	1
3	Ordering information	1
4	Functional diagram	1
5	Pinning information	2
5.1	Pinning	2
5.2	Pin description	2
6	Functional description	2
7	Limiting values	3
8	Recommended operating conditions	3
9	Static characteristics	4
10	Dynamic characteristics	5
11	Waveforms	6
12	Package outline	7
13	Abbreviations	8
14	Revision history	8
15	Legal information	9
15.1	Data sheet status	9
15.2	Definitions.....	9
15.3	Disclaimers.....	9
15.4	Trademarks.....	10
16	Contact information	10
17	Contents	11