LTC1864
16-Bit 250ksps ADC

DESCRIPTION

Demonstration circuit 416 features the LTC1864 16-bit 250ksps analog-to-digital converter.

This board provides a means to evaluate the performance of the LTC1864 with either the Linear Technology PScope™ data acquisition system, or with other parallel or serial data acquisition systems.

The board also demonstrates proper layout techniques in the circuitry surrounding the ADC and in the segmentation of the planes required to achieve full performance with the ADC.

These techniques include proper grounding of the device and associated bypass capacitors, placement of the device relative to interconnection of analog and digital subsystems and signal routing in proximity to the ADC.

This board performs serial to parallel conversion in a manner that is unlikely to be used in an actual implementation, but is representative of what could be implemented in an FPGA. It is expected that with this ADC, the interface will be performed serially with either programmable logic, a general-purpose processor, a DSP, or across an isolated link of one of many types. The complexity of the circuitry is hence much greater than what would be required in almost any practical application.

The LTC1864 and its demo board are intended to be used with the PScope data acquisition system for characterization of the ADC in AC applications extending from Hz to MHz. The full power bandwidth of the LTC1864 is high enough to produce good performance in under-sampling applications, as well as applications where the signal content is below Nyquist.

The board contains a bandwidth-limiting filter at the input of the ADC (C7, C8, C9, R1 and R2), as well as provision for an amplifier (U2). This bandwidth-limiting filter (–3dB at 1.5MHz) is typical of what may be required for many applications, but it is not necessarily the best for all applications.

The board also incorporates an LTC1799 resistor programmable oscillator as an optional clock source.

Design files for this circuit board are available at http://www.linear.com/demo/DC416

QUICK START PROCEDURE

Demonstration circuit 416 is easy to set up to evaluate the performance of the LTC1864. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

NOTE: The demo board is shipped with jumpers in place to allow the use of an external oscillator at 80× the sample rate. Figure 1 shows the default jumper positions.

1. Connect the parallel output J4 to either the DC718 data collection board, or to a suitable acquisition system. Pin 3 of J4 is the data strobe.
2. Observe correct polarity; Connect +8V to +15V to terminal E1. Note that –15V is only required if U2 is installed. There are two on board regulators. Both are 5V, although U1 the reference can be substituted with a lower voltage.

QUICK START PROCEDURE

3. If the intent is to do an evaluation of AC performance, connect a sinusoidal (or other) input signal to J1, or J1 and J2, with a nominal DC bias of 2.5V. If only J1 is used (single-ended operation), JP3 should be installed. This converter converts unipolar differential inputs from 0 – V_{REF}.

NOTE: The A_{IN} inputs do not have 50Ω termination. Most generators will produce the correct signal level only if the cable is terminated at 50Ω. If you are driving this from a generator, you should use 50Ω through terminators. Take care not to overdrive the inputs if you do not use terminators.

4. Connect a 20MHz digital clock to CLKIN. With default jumpers in place, this will result in a 250ksps conversion rate.

5. Collect data via PScope for a Fourier transform into the frequency domain, or to allow data to be collected and saved to a file for subsequent import and analysis in Excel, Matlab or other analysis packages.

Duplication of the FFT results shown in the data sheet requires the use of a low jitter clock and waveform generators synchronized such that the input waveform must be within a few ppm of an exact multiple of the conversion clock divided by the FFT size (termed coherent). For 250kHz sample rate and a 4096 point FFT, input frequencies should be an exact multiple of 61.035156Hz, and preferably a prime number multiple or at least an odd number multiple. The use of an even number multiple will exercise a minimal number of codes, producing poor results.

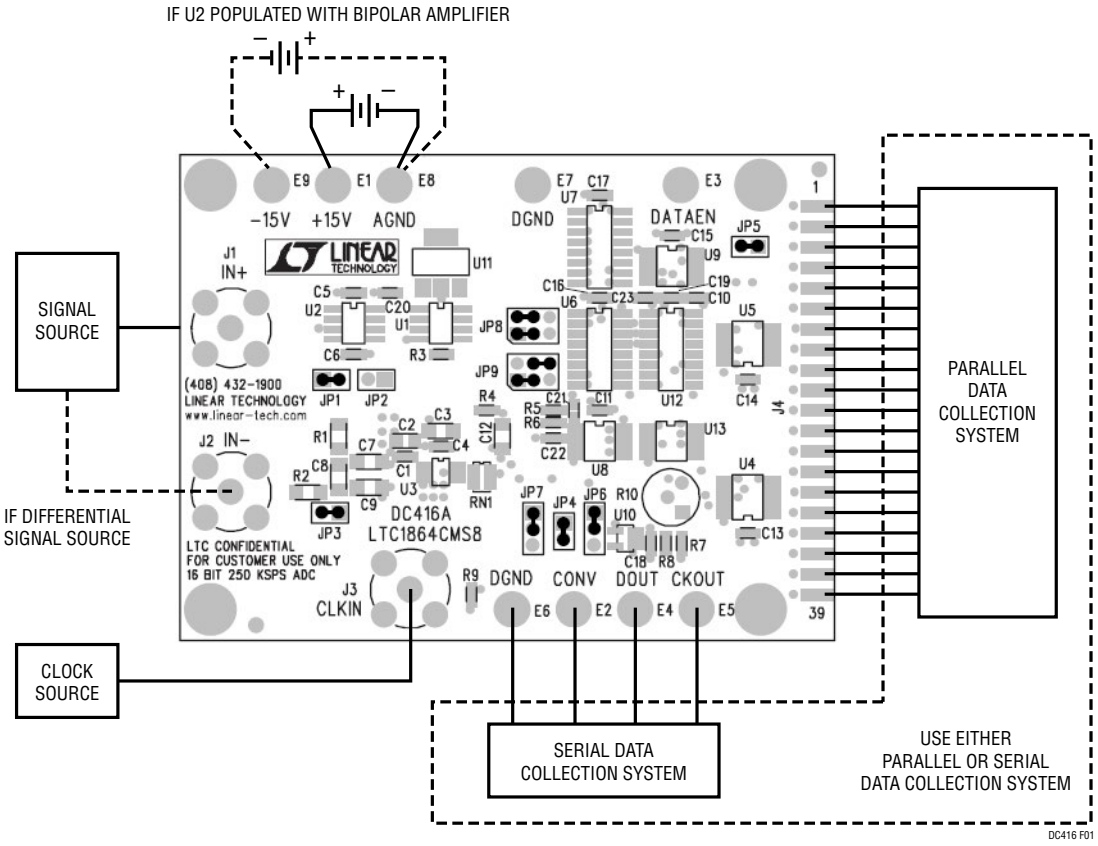


Figure 1. Proper Measurement Equipment Setup

OPERATION

The conversion clock (CONV) is derived from the CLKIN connector (J3) via a programmable divider.

The board is shipped with this divider set to divide by 80 (JP8 and JP9). In order for this converter to achieve its maximum throughput of 250ksps, the data transfer time must be completed in $1/f_{SAMPLE} – T_{CONV}$, which requires that the SCLK be at 20MHz.

The programmable divider can be strapped for different divide ratios if the required sample rate is less than 250ksps, allowing a greater percentage of the time available doing data transfer (divide ratio of less than 80), or if a comparable SCLK rate is used, with a lower sample rate (divide ratio greater than 80).

JP8 and JP9 are set to code 16–(divide ratio/16) or 11 in the case of a divide ratio of 80.

The counter circuitry gates a sequence of 16 clock pulses during CONV = 0. These can be observed on CLKOUT, or if CONV is introduced externally, (remove JP4) the clock pulses can be introduced via CLKIN (JP6 to pin 1, JP7 to pin 1 if no inversion is required).

JP6 (pin 2–3) allows the use of the onboard LTC1799 oscillator. Note that this oscillator will not produce data sheet performance unless the input frequency is quite low, as the phase jitter of this oscillator will be transformed in the presence of high slew rate signals into random noise. If the amplitude of the signal falls off with increasing frequency as many natural phenomena do, this oscillator may produce acceptable results.

If you are under-sampling, or operating the converter near Nyquist, it is important to have a low jitter clock source.

The data output DOUT is shifted into a pair of 74HC595 serial to parallel shift registers that have output holding registers, and tri-stateable outputs. If you intend to incorporate the demo board into a prototype of a system, ENABLEDATA can be used to gate the outputs onto a 16-bit bus. Alternatively, all of the signals can be produced externally, and data can be read into a DSP via DOUT.

If you elect to use the on-board timing to clock data into a slaved serial input port, you can use DOUT, CKOUT, along with CONV as a busy signal or as a means of producing a frame sync.

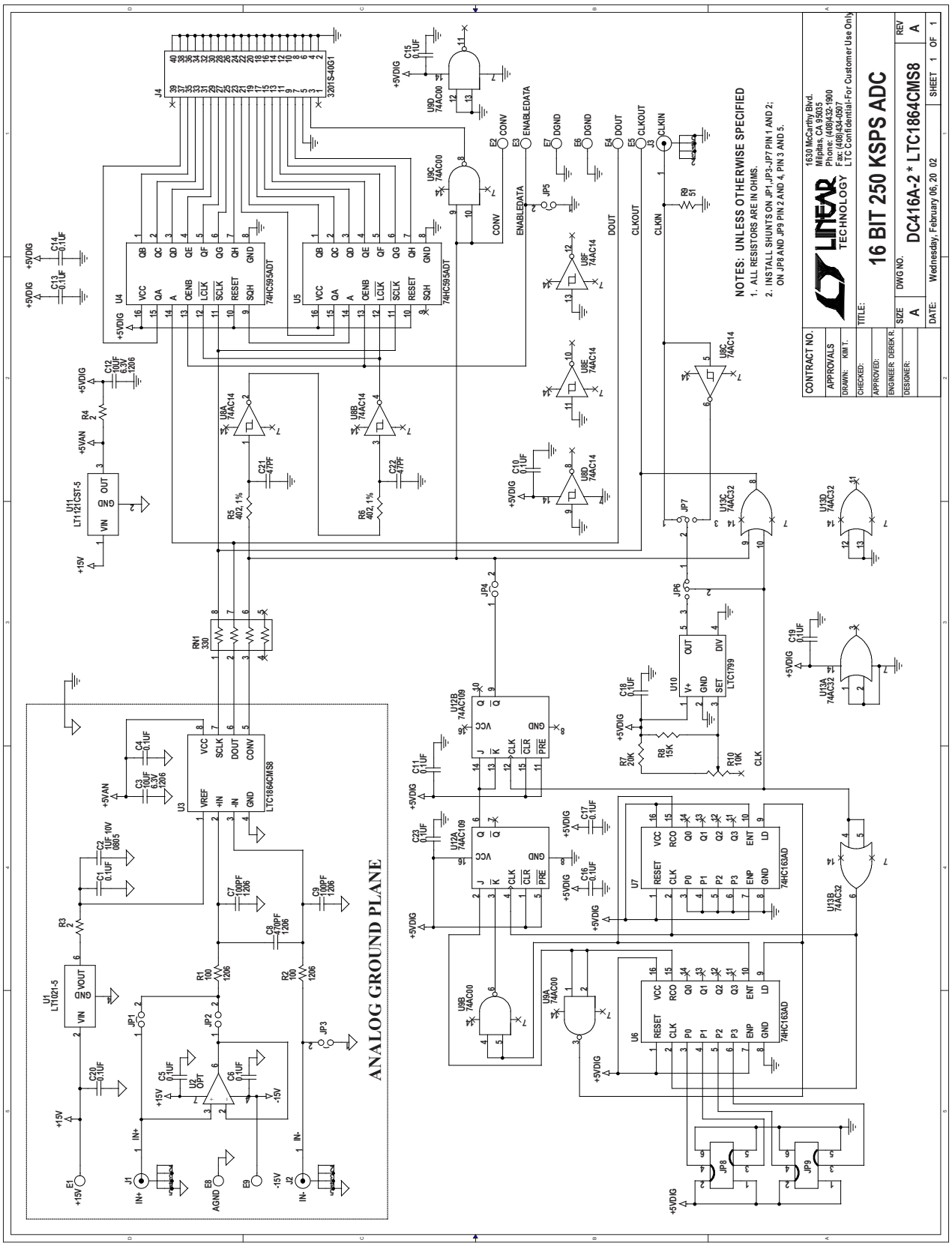
In the event that you do not have “coherent” signal sources as described above, you can use windowing functions to reduce the “leakage” effect that occurs in the Fourier transform and get a reasonably accurate figure for SNR, THD, SINAD and the levels of the various harmonics.

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
1	15	C1, C4-C6, C10, C11, C13-C20, C23	CAP., X7R, 0.1µF, 16V	AVX, 0603YC104MAT1A
2	1	C2	CAP., X7R, 1µF, 10V, 20%	AVX, 0805ZC105MAT1T
3	2	C3, C12	CAP., X5R, 10µF, 6.3V, 20%, 1206	TAIYO YUDEN JMK316BJ106MLT
4	2	C7,C9	CAP., NPO, 100PF, 50V, 1206	VITRAMON, VJ1206A101JXB
5	1	C8	CAP., NPO, 470PF, 100V,1206	AVX, 12061A471JAT
6	2	C21, C22	CAP., NPO, 47PF, 50V	AVX, 06035A470MAT1A
7	9	E1-E9	TP, TURRET, .094"	MILL-MAX, 2501-2
8	5	JP1, JP2, JP3, JP4, JP5	JMP, 1 × 2 .079CC	COMM-CON, 2802S-02-G1
9	2	JP6, JP7	JMP, 1 × 3 .079CC	COMM-CON, 2802S-03-G1
10	2	JP8, JP9	JMP, 2 × 3 .079CC	COMM-CON, 2202S-06-G2
11	9	SHUNTS FOR JP1-JP9	SHUNT, .079" CENTER	COMM-CON, CCIJ2MM-138G
12	3	J1-J3	CONN, BNC 50Ω, PCB-VERTICADTL	CONNEX, 112404
13	1	J4	CON, HDR, .1 × .1 CNTRS, 40PIN	COMMCON, 3201S-40G1
14	1	RN1	RES 2 × 4 ARRAY, CHIP, 330Ω, ISO	CTS, 742-C083-331JTR-ND
15	2	R1, R2	RES, CHIP 100, 1/16W, 5%, 1206	AAC, CR18-101JM
16	2	R3, R4	RES, CHIP 2, 1/16W, 5%, 0603	AAC, CR16-2R0JM
17	2	R5, R6	RES, CHIP 402, 1/16W, 1%,0603	AAC, CR16-4020FM
18	1	R7	RES, CHIP 20k, 1/16W, 5%,0603	AAC, CR16-203JM
19	1	R8	RES, CHIP 15k, 1/16W, 5%,0603	AAC, CR16-153JM
20	1	R9	RES, CHIP 51, 1/16W, 5%,0603	AAC, CR16-510JM
21	1	R10	RES POT3321H, POT-3321H-MURATA	MURATA, POT3321H-1-103
22	1	U1	IC, LT1021DCS8-5, SO8	LINEAR TECH., LT1021DCS8-5
23	0	U2	IC, OP AMP, SO8	TBD
24	1	U3	IC, LTC1864AIMS8, MSOP8	LINEAR TECH., LTC1864AIMS8
25	2	U4, U5	IC, MC74HC595ADT, TSSOP16	MOTOROLA, MC74HC595ADT
26	2	U6, U7	IC, MC74HC163AD, SO16	MOTOROLA, MC74HC163AD
27	1	U8	IC, MC74AC14DTR2, TSSOP14	ON SEMI., MC74AC14DTR2
28	1	U9	IC, MC74AC00DTR2, TSSOP14	ON SEMI., MC74AC00DTR2
29	1	U10	IC, LTC1799, SOT23-5	LINEAR TECH., LTC1799
30	1	U11	IC, LT1121CST-5, SOT223	LINEAR TECH., LT1121CST-5
31	1	U12	IC, MC74AC109DR2, SO16	ON SEMI., MC74AC109DR2
32	1	U13	IC, MC74AC32DTR2, TSSOP14	ON SEMI., MC74AC32DTR2
33	4	MTGS AT 4 CORNERS	SCREW, #4-40, 1/4"	ANY
34	4	MTGS AT 4 CORNERS	STANDOFF, NYLON HEX #4-40 1/2"	MICRO PLASTICS 14HTSP003

NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE IN OHMS.
2. INSTALL SHUNTS ON JP1, JP3-JP7 PIN 1 AND 2;
   ON JP8 AND JP9 PIN 2 AND 4, PIN 3 AND 5.

SCHEMATIC DIAGRAM



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This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact a LTC application engineer.

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