MCP39F511A

AC/DC Dual-Mode Power-Monitoring IC with Calculation and Energy Accumulation

Features

- Real-Time Measurement of Input Power for AC or DC Supplies
- AC/DC Dual-Mode Power Monitoring Accuracy Capable of 0.1% Error Across 4000:1 Dynamic Range
- Automatic Sensing and Switching Between AC and DC Modes
- Built-In Calculations on Fast 16-Bit Processing Core
  - Active and Reactive Energy Accumulation
  - Active, Reactive, Apparent Power
  - True RMS Current, RMS Voltage
  - Line Frequency, Power Factor
- 64-bit Wide Import and Export Active Energy Accumulation Registers
- 64-bit Four Quadrant Reactive Energy Accumulation Registers
- Automatic Saving the Energy Accumulation Registers into EEPROM at Power Off
- Automatic Loading the Energy Accumulation Registers from EEPROM at Power On
- Signed Active and Reactive Power Outputs
- Dedicated Zero Crossing Detection (ZCD) Pin Output with Less than 200 µs Latency
- Dedicated PWM Output Pin with Programmable Frequency and Duty Cycle
- Automatic Event Pin Control through Fast Voltage Sag/Surge Detection
- Two Wire Serial Protocol with Selectable Baud Rate Up to 115.2 kbps using Universal Asynchronous Receiver/Transmitter (UART)
- Four Independent Registers for Minimum and Maximum Output Quantity Tracking
- Fast Calibration Routines and Simplified Command Protocol
- 512 Bytes User-Accessible EEPROM through Page Read/Write Commands
- Low-Drift Internal Voltage Reference, 7 ppm/°C Typical
- 28-lead 5x5 QFN Package
- Extended Temperature Range -40°C to +125°C

Applications

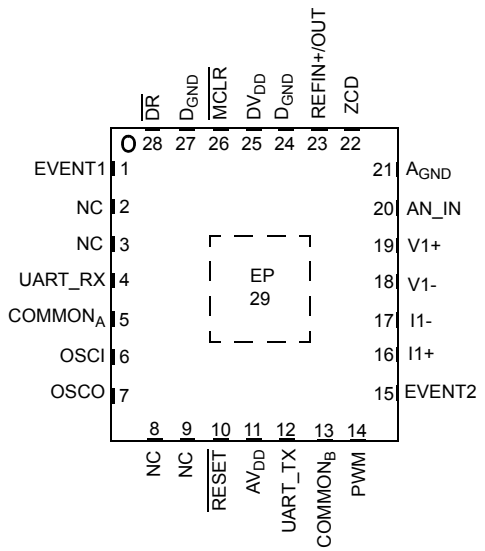
- Power Monitoring and Management for Smart Home/City
- Industrial Lighting Power Monitoring
- Power Measurement for Renewable Energy System
- Intelligent Power Distribution Units
- Server Power Monitor

Description

The MCP39F511A device is a highly-integrated, complete single-phase power-monitoring IC designed for real-time measurement of input power for AC or DC power supplies, making it suitable for a wide range of consumer and industrial applications. It is capable of detecting the input voltage in order to work as DC or AC mode. It includes dual-channel Delta-Sigma ADCs, a 16-bit calculation engine, EEPROM and a flexible 2-wire interface. Separate AC and DC calibration registers are provided, to ensure high-accuracy measurements in both modes. An integrated low-drift voltage reference with 7 ppm/°C in addition to 94.5 dB of SINAD performance on each measurement channel allows for better than 0.1% accurate designs across a 4000:1 dynamic range.

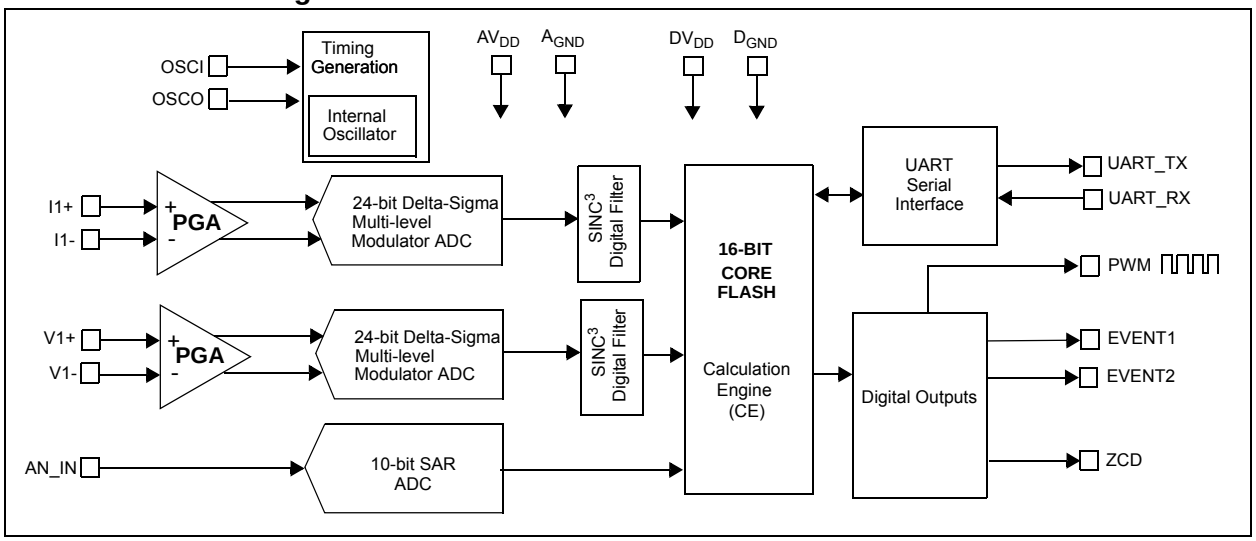
Package Types

MCP39F511A
5x5 QFN*

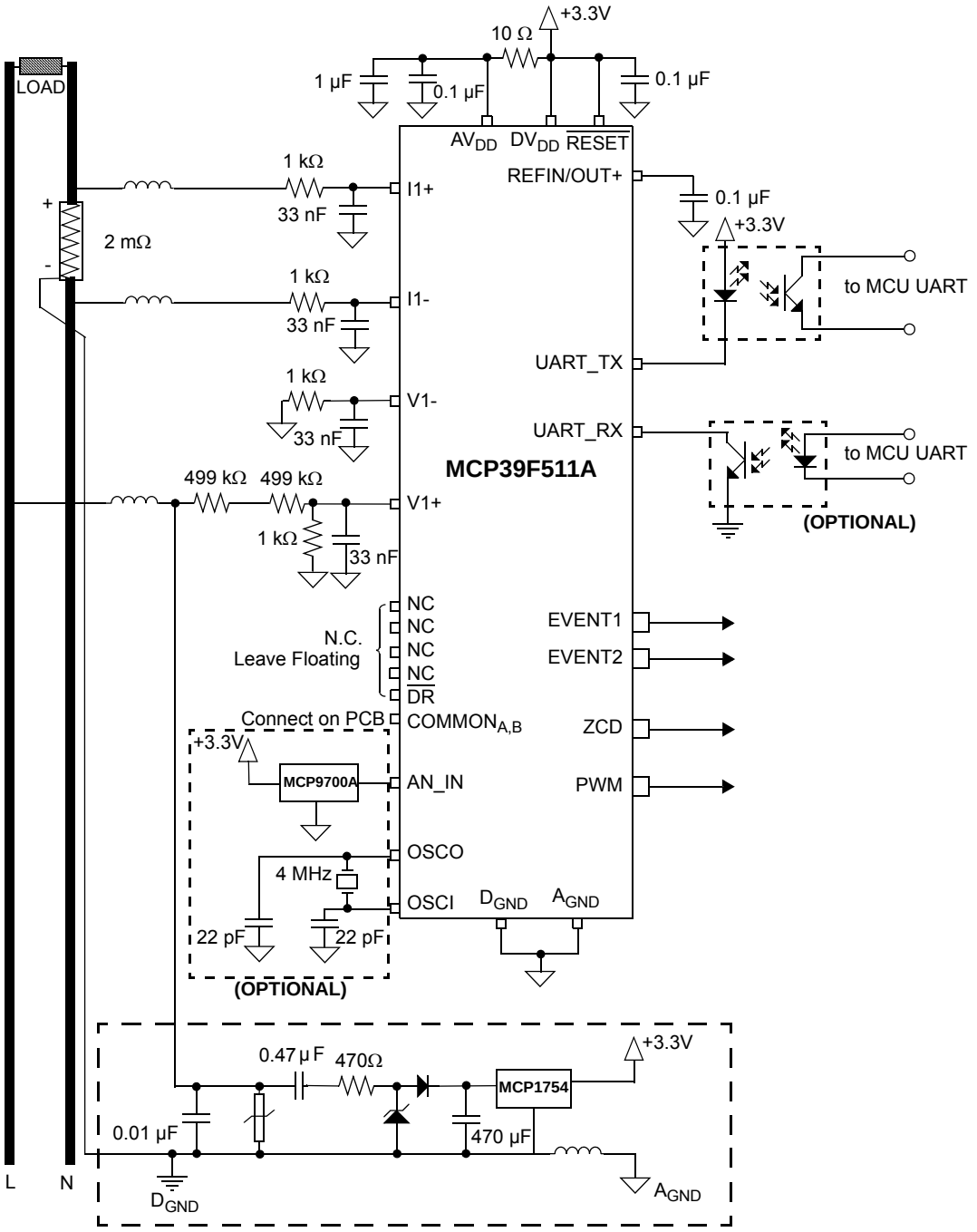


*Includes Exposed Thermal Pad (EP); see Table 3-1.

Functional Block Diagram



MCP39F511A Typical Application – Single Phase, Two-Wire Application Schematic



Note 1: The MCP39F511A demonstration board uses a switching power supply, however a low-cost capacitive-based supply, as shown here, is sufficient for many applications.

2: The external sensing components shown here, a 2 mΩ shunt, two 499 kΩ and 1 kΩ resistors for the 1000:1 voltage divider, are specifically chosen to match the default values for the calibration registers defined in **Section 6.0 "Register Descriptions"**. By choosing low-tolerance components of these values (for instance 1% tolerance), measurement accuracy in the 2-3% range can be achieved with zero calibration (AC only, offset calibration may be needed in DC mode). See **Section 9.0 "MCP39F511A Calibration"** for more information.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

DV_{DD} ..... -0.3 to +4.5V
AV_{DD} ..... -0.3 to +4.0V
Digital inputs and outputs w.r.t. A_{GND} .....-0.3V to +4.0V
Analog Inputs (I+,I-,V+,V-) w.r.t. A_{GND} .....-2V to +2V
V_{REF} input w.r.t. A_{GND} ....-0.6V to AV_{DD} +0.6V
Maximum Current out of D_{GND} pin.....300 mA
Maximum Current into DV_{DD} pin.....250 mA
Maximum Output Current Sunk by Digital IO .....25 mA
Maximum Current Sourced by Digital IO.....25 mA
Storage temperature .....-65°C to +150°C
Ambient temperature with power applied.....-40°C to +125°C
Soldering temperature of leads (10 seconds) ..... +300°C
ESD on the analog inputs (HBM,MM).....4.0 kV, 200V
ESD on all other pins (HBM,MM).....4.0 kV, 200V

† **Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

1.1 Specifications

TABLE 1-1: ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD}, DV_{DD} = +2.7 to +3.6V, T_A = -40°C to +125°C, MCLK = 4 MHz, PGA GAIN = 1.

Characteristic	Sym.	Min.	Typ.	Max.	Units	Test Conditions
Power Measurement						
Active Power **(Note 1)**	P	—	±0.1	—	%	4000:1 Dynamic range on current channel **(Note 2)**
Reactive Power **(Note 1)**	Q	—	±0.1	—	%	4000:1 Dynamic range on current channel **(Note 2)**
Apparent Power **(Note 1)**	S	—	±0.1	—	%	4000:1 Dynamic range on current channel **(Note 2)**
Current RMS **(Note 1)**	I_{RMS}	—	±0.1	—	%	4000:1 Dynamic range on current channel **(Note 2)**
Voltage RMS **(Note 1)**	V_{RMS}	—	±0.1	—	%	4000:1 (DC mode), 20:1 (AC mode) Dynamic range on voltage channel **(Note 2, 8)**
Power Factor **(Note 1)**	Φ	—	±0.1	—	%	
Line Frequency **(Note 1)**	LF	—	±0.1	—	%	
Calibration, Calculation and Event Detection Times						
Auto-Calibration Time	t_{CAL}	—	2^N x $(1/f_{LINE})$	—	ms	**Note 3**

Note 1: Calculated from reading the register values with no averaging, single computation cycle with accumulation interval of 4 line cycles.
2: Specification by design and characterization; not production tested.
3: N = Value in the Accumulation Interval Parameter register. The default value of this register is 2 or T_{CAL} = 80 ms for 50 Hz line.
4: Applies to Voltage Sag and Voltage Surge events only.
5: Applies to all gains. Offset and gain errors depend on the PGA gain setting. See **Section 2.0 "Typical Performance Curves"** for typical performance.
6: V_{IN} = 1.2 V_{PP} = 424 mV_{RMS} @ 50/60 Hz. This parameter is established by characterization and is not 100% tested.
7: Variation applies to internal clock and UART only. All calculated output quantities can be temperature compensated to the performance listed in the respective specification.
8: The internal ADC clock frequency is affected by the amplitude of the AC signal applied on the voltage channel, decreasing the overall accuracy if the amplitude is low. In DC mode, the internal ADC clock frequency is constant.

TABLE 1-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD}, DV_{DD} = +2.7 to +3.6V, T_A = -40°C to +125°C, MCLK = 4 MHz, PGA GAIN = 1.

Characteristic	Sym.	Min.	Typ.	Max.	Units	Test Conditions
Minimum Time for Voltage Surge/Sag Detection	t_{AC_SASU}	—	5, see Section 7.2	—	ms	Note 4
24-Bit Delta-Sigma ADC Performance						
Analog Input Absolute Voltage	V_{IN}	-1	—	+1	V	
Analog Input Leakage Current	A_{IN}	—	1	—	nA	
Differential Input Voltage Range	(I1+ – I1-), (V1+ – V1-)	-600/GAIN	—	+600/GAIN	mV	V_{REF} = 1.2V, proportional to V_{REF}
Offset Error	V_{OS}	-1	—	+1	mV	
Offset Error Drift		—	0.5	—	µV/°C	
Gain Error	GE	-4	—	+4	%	Note 5
Gain Error Drift		—	1	—	ppm/°C	
Differential Input Impedance	Z_{IN}	232	—	—	kΩ	G = 1
		142	—	—	kΩ	G = 2
		72	—	—	kΩ	G = 4
		38	—	—	kΩ	G = 8
		36	—	—	kΩ	G = 16
		33	—	—	kΩ	G = 32
Signal-to-Noise and Distortion Ratio	SINAD	92	94.5	—	dB	Note 6
Total Harmonic Distortion	THD	—	-106.5	-103	dBc	Note 6
Signal-to-Noise Ratio	SNR	92	95	—	dB	Note 6
Spurious Free Dynamic Range	SFDR	—	111	—	dB	Note 6
Crosstalk	CTALK	—	-122	—	dB	
AC Power Supply Rejection Ratio	AC PSRR	—	-73	—	dB	AV_{DD} and DV_{DD} = 3.3V + 0.6V_{PP}, 100 Hz, 120 Hz, 1 kHz
DC Power Supply Rejection Ratio	DC PSRR	—	-73	—	dB	AV_{DD} and DV_{DD} = 3.0 to 3.6V
DC Common Mode Rejection Ratio	DC CMRR	—	-105	—	dB	V_{CM} varies from -1V to +1V
10-Bit SAR ADC Performance for Temperature Measurement						
Resolution	N_R	—	10	—	bits	

Note 1: Calculated from reading the register values with no averaging, single computation cycle with accumulation interval of 4 line cycles.

2: Specification by design and characterization; not production tested.

3: N = Value in the Accumulation Interval Parameter register. The default value of this register is 2 or T_{CAL} = 80 ms for 50 Hz line.

4: Applies to Voltage Sag and Voltage Surge events only.

5: Applies to all gains. Offset and gain errors depend on the PGA gain setting. See **Section 2.0 "Typical Performance Curves"** for typical performance.

6: V_{IN} = 1.2 V_{PP} = 424 mV_{RMS} @ 50/60 Hz. This parameter is established by characterization and is not 100% tested.

7: Variation applies to internal clock and UART only. All calculated output quantities can be temperature compensated to the performance listed in the respective specification.

8: The internal ADC clock frequency is affected by the amplitude of the AC signal applied on the voltage channel, decreasing the overall accuracy if the amplitude is low. In DC mode, the internal ADC clock frequency is constant.

TABLE 1-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD}, DV_{DD} = +2.7 to +3.6V, T_A = -40°C to +125°C, MCLK = 4 MHz, PGA GAIN = 1.						
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Absolute Input Voltage	V_{IN}	D_{GND} - 0.3	—	D_{VDD} + 0.3	V	
Recommended Impedance of Analog Voltage Source	R_{IN}	—	—	2.5	kΩ	
Integral Nonlinearity	I_{NL}	—	±1	±2	LSb	
Differential Nonlinearity	D_{NL}	—	±1	±1.5	LSb	
Gain Error	G_{ERR}	—	±1	±3	LSb	
Offset Error	E_{OFF}	—	±1	±2	LSb	
Temperature Measurement Rate		—	$f_{LINE}/2^N$	—	sps	**Note 7**
Clock and Timings						
UART Baud Rate	UDB	1.2	9.6	115.2	kbps	See **Section 3.2** for protocol details
Master Clock and Crystal Frequency	f_{MCLK}	-2%	4	+2%	MHz	
Capacitive Loading on OSCO pin	COSC2	—	—	15	pF	When an external clock is used to drive the device
Internal Oscillator Tolerance	f_{INT_OSC}	—	2	—	%	-40 to +85°C only (**Note 7**)
Internal Voltage Reference						
Internal Voltage Reference Tolerance	V_{REF}	-2%	1.2	+2%	V	V_{REFEXT} = 0, T_A = +25°C only
Temperature Coefficient	TCV_{REF}	—	7	—	ppm/°C	T_A = -40°C to +125°C, V_{REFEXT} = 0
Output Impedance	$ZOUTV_{REF}$	—	2	—	kΩ	V_{REFEXT} = 0
Current, V_{REF}	$AI_{DD}V_{REF}$	—	25	—	µA	V_{REFEXT} = 0 SHUTDOWN<1:0> = 11

Note 1: Calculated from reading the register values with no averaging, single computation cycle with accumulation interval of 4 line cycles.

2: Specification by design and characterization; not production tested.

3: N = Value in the Accumulation Interval Parameter register. The default value of this register is 2 or T_{CAL} = 80 ms for 50 Hz line.

4: Applies to Voltage Sag and Voltage Surge events only.

5: Applies to all gains. Offset and gain errors depend on the PGA gain setting. See **Section 2.0 "Typical Performance Curves"** for typical performance.

6: V_{IN} = 1.2 V_{PP} = 424 mV_{RMS} @ 50/60 Hz. This parameter is established by characterization and is not 100% tested.

7: Variation applies to internal clock and UART only. All calculated output quantities can be temperature compensated to the performance listed in the respective specification.

8: The internal ADC clock frequency is affected by the amplitude of the AC signal applied on the voltage channel, decreasing the overall accuracy if the amplitude is low. In DC mode, the internal ADC clock frequency is constant.

TABLE 1-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD}, DV_{DD} = +2.7 to +3.6V, T_A = -40°C to +125°C, MCLK = 4 MHz, PGA GAIN = 1.

Characteristic	Sym.	Min.	Typ.	Max.	Units	Test Conditions
Voltage Reference Input						
Input Capacitance		—	—	10	pF	
Absolute Voltage on V_{REF+} Pin	V_{REF+}	A_{GND} + 1.1V	—	A_{GND} + 1.3V	V	
Power Specifications						
Operating Voltage	AV_{DD}, DV_{DD}	2.7	—	3.6	V	
DV_{DD} Start Voltage to Ensure Internal Power-On Reset Signal	V_{POR}	D_{GND}	—	0.7	V	
DV_{DD} Rise Rate to Ensure Internal Power-On Reset Signal	SDV_{DD}	0.05	—	—	V/ms	0–3.3V in 0.1s, 0–2.5V in 60 ms
AV_{DD} Start Voltage to Ensure Internal Power-On Reset Signal	V_{POR}	A_{GND}	—	2.1	V	
AV_{DD} Rise Rate to Ensure Internal Power-On Reset Signal	SAV_{DD}	0.042	—	—	V/ms	0 – 2.4V in 50 ms
Operating Current	I_{DD}	—	13	—	mA	
Data EEPROM Memory						
Cell Endurance	EPS	100,000	—	—	E/W	
Self-Timed Write Cycle Time	T_{IWD}	—	4	—	ms	
Number of Total Write/Erase Cycles Before Refresh	R_{REF}	—	10,000,000	—	E/W	
Characteristic Retention	T_{RETDD}	40	—	—	years	Provided no other specifications are violated
Supply Current During Programming	I_{DDPD}	—	7	—	mA	

Note 1: Calculated from reading the register values with no averaging, single computation cycle with accumulation interval of 4 line cycles.

2: Specification by design and characterization; not production tested.

3: N = Value in the Accumulation Interval Parameter register. The default value of this register is 2 or T_{CAL} = 80 ms for 50 Hz line.

4: Applies to Voltage Sag and Voltage Surge events only.

5: Applies to all gains. Offset and gain errors depend on the PGA gain setting. See **Section 2.0 "Typical Performance Curves"** for typical performance.

6: V_{IN} = 1.2 V_{PP} = 424 mV_{RMS} @ 50/60 Hz. This parameter is established by characterization and is not 100% tested.

7: Variation applies to internal clock and UART only. All calculated output quantities can be temperature compensated to the performance listed in the respective specification.

8: The internal ADC clock frequency is affected by the amplitude of the AC signal applied on the voltage channel, decreasing the overall accuracy if the amplitude is low. In DC mode, the internal ADC clock frequency is constant.

TABLE 1-2: SERIAL DC CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD}, DV_{DD} = +2.7 to+ 3.6V, T_A = -40°C to +125°C, MCLK = 4 MHz						
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
High-Level Input Voltage	V_{IH}	0.8 DV_{DD}	—	DV_{DD}	V	
Low-Level Input Voltage	V_{IL}	0	—	0.2 DV_{DD}	V	
High-Level Output Voltage	V_{OH}	3	—	—	V	I_{OH} = -3.0 mA, V_{DD} = 3.6V
Low-Level Output Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 4.0 mA, V_{DD} = 3.6V
Input Leakage Current	I_{LI}	—	—	1	µA	
			0.050	0.100		Digital Output pins only (ZCD, PWM, EVENT1, EVENT2)

TABLE 1-3: TEMPERATURE SPECIFICATIONS

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD}, DV_{DD} = +2.7 to +3.6V.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Temperature Ranges						
Operating Temperature Range	T_A	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 28LD 5x5 QFN	θ_{JA}	—	36.9	—	°C/W	

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are **not** tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, AV_{DD} = +3.3V, DV_{DD} = +3.3V, T_A = +25°C, GAIN = 1, V_{IN} = -0.5 dBFS at 60 Hz.

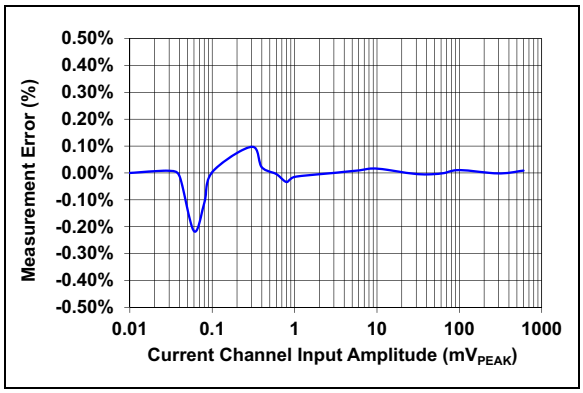


FIGURE 2-1: *Active Power, Gain = 1.*

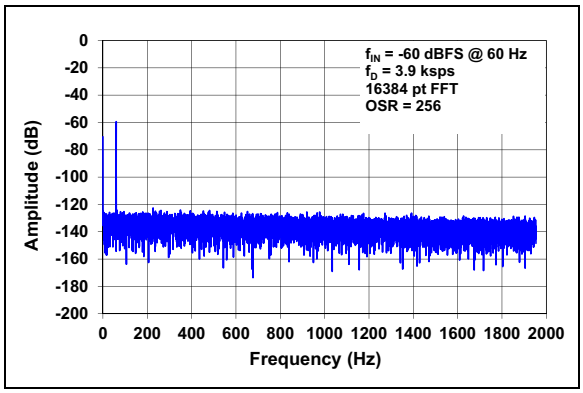


FIGURE 2-4: *Spectral Response.*

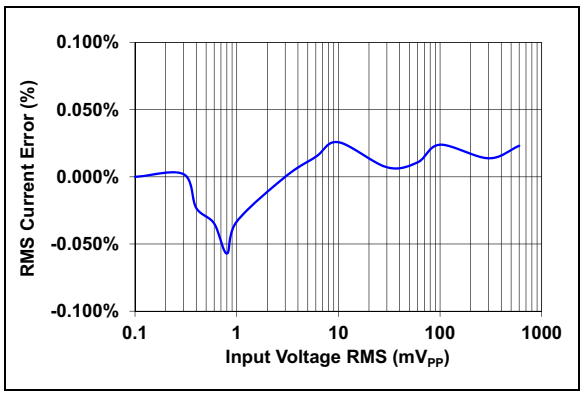


FIGURE 2-2: *RMS Current, Gain = 1.*

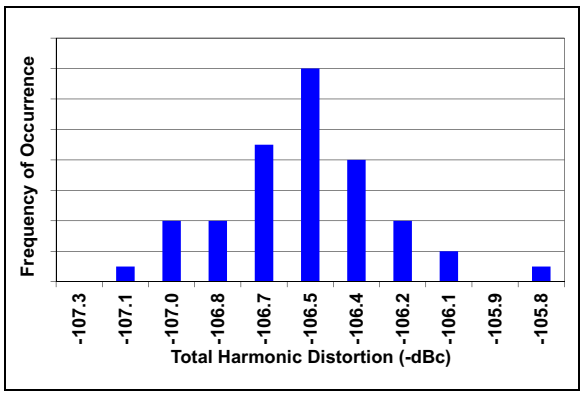


FIGURE 2-5: *THD Histogram.*

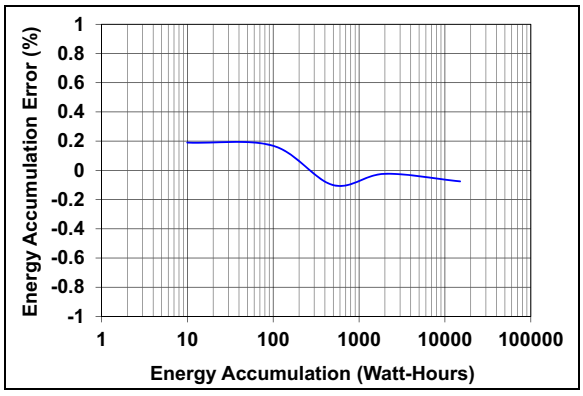


FIGURE 2-3: *Energy, Gain = 8.*

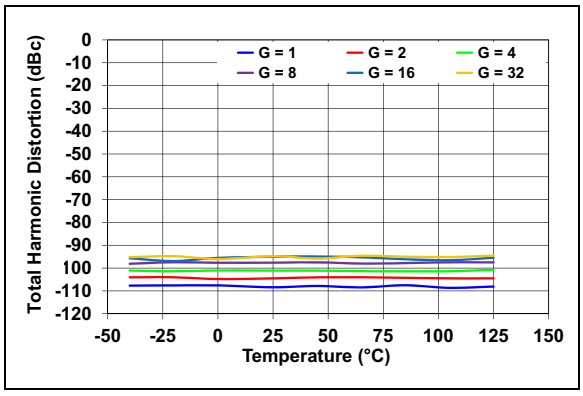


FIGURE 2-6: *THD vs. Temperature.*

Note: Unless otherwise indicated, AV_{DD} = 3.3V, DV_{DD} = 3.3V, T_A = +25°C, GAIN = 1, V_{IN} = -0.5 dBFS at 60 Hz.

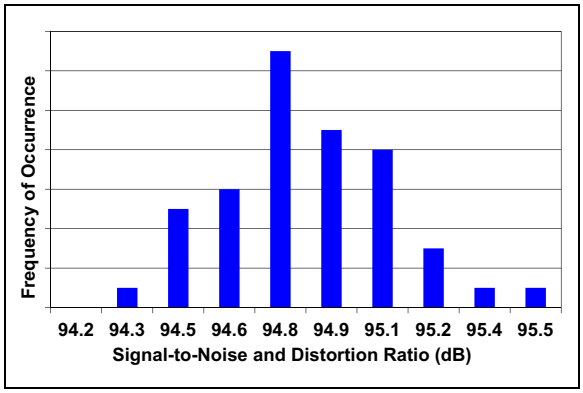


FIGURE 2-7: *SNR Histogram.*

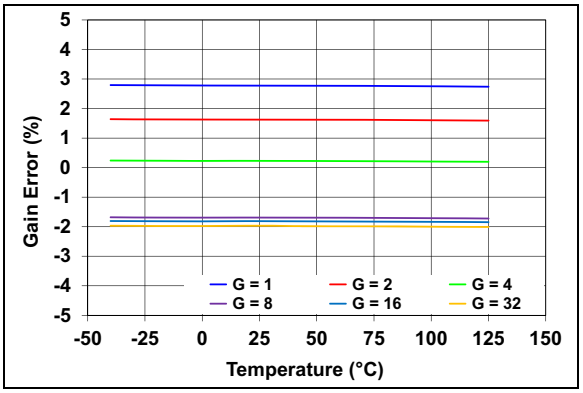


FIGURE 2-9: *Gain Error vs. Temperature.*

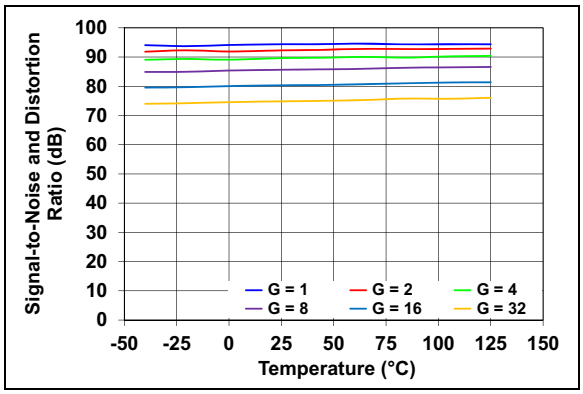


FIGURE 2-8: *SINAD vs. Temperature.*

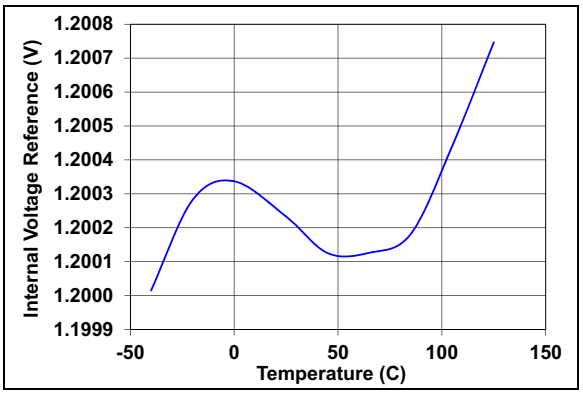


FIGURE 2-10: *Internal Voltage Reference vs. Temperature.*

3.0 PIN DESCRIPTION

The description of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP39F511A 5x5 QFN	Symbol	Function
1	EVENT1	Event 1 Output pin
2, 3, 8, 9	NC	No Connect (must be left floating)
4	UART_RX	UART Communication RX pin
5	$COMMON_A$	Common pin A, to be connected to pin 13 ($COMMON_B$)
6	OSCI	Oscillator Crystal Connection pin or External Clock Input pin
7	OSCO	Oscillator Crystal Connection pin
10	$\overline{RESET}$	Reset pin for Delta-Sigma ADCs
11	AV_{DD}	Analog Power Supply pin
12	UART_TX	UART Communication TX pin
13	$COMMON_B$	Common pin B, to be connected to pin 5 ($COMMON_A$)
14	PWM	Pulse-Width Modulation (PWM) Output pin
15	EVENT2	Event 2 Output pin
16	I1+	Noninverting Current Channel Input for 24-bit ΔΣ ADC
17	I1-	Inverting Current Channel Input for 24-bit ΔΣ ADC
18	V1-	Inverting Voltage Channel Input for 24-bit ΔΣ ADC
19	V1+	Noninverting Voltage Channel Input for 24-bit ΔΣ ADC
20	AN_IN	Analog Input for SAR ADC
21	A_{GND}	Analog Ground Pin, return path for internal analog circuitry
22	ZCD	Zero Crossing Detection Output
23	REFIN+/OUT	Noninverting Voltage Reference Input and Internal Reference Output pin
24, 27	D_{GND}	Digital Ground pin, return path for internal digital circuitry
25	DV_{DD}	Digital Power Supply pin
26	$\overline{MCLR}$	Master Clear for device
28	$\overline{DR}$	Data Ready (must be left floating)
29	EP	Exposed Thermal Pad (to be connected to pins 24 and 27 (D_{GND}))

3.1 Event Output Pins (EVENTn)

These digital output pins can be configured to act as output flags based on various internal raise conditions. Control is modified through the Event Configuration register.

3.2 UART Communication Pins (UART_RX, UART_TX)

The MCP39F511A device contains an asynchronous full-duplex UART. The UART communication is eight bits with Start and Stop bit. See **Section 4.3 "UART Settings"** for more information.

3.3 Common Pins ($COMMON_A$ and $_B$)

$COMMON_A$ and $COMMON_B$ pins are internal connections for the MCP39F511A. These two pins should be connected together in the application.

3.4 Oscillator Pins (OSCI/OSCO)

OSCI and OSCO provide the master clock for the device. Appropriate load capacitance should be connected to these pins for proper operation. An optional 4 MHz crystal can be connected to these pins. If a crystal of external clock source is not detected, the device will clock from the internal 4 MHz oscillator.

3.5 Reset Pin ($\overline{RESET}$)

This pin is active-low and places the Delta-Sigma ADCs, PGA, internal V_{REF} and other blocks associated with the Analog Front End (AFE) in a Reset state when pulled low. This input is Schmitt-triggered.

3.6 Analog Power Supply Pin (AV_{DD})

AV_{DD} is the power supply pin for the analog circuitry within the MCP39F511A.

This pin requires appropriate bypass capacitors and should be maintained to +2.7V and +3.6V for specified operation. It is recommended to use 0.1 µF ceramic capacitors.

3.7 Pulse-Width Modulator (PWM)

This digital output is a dedicated PWM output that can be controlled through the PWM Frequency and PWM Duty Cycle registers. See **Section 8.0 "Pulse Width Modulation (PWM)"** for more information.

3.8 24-Bit Delta-Sigma ADC Differential Current Channel Input Pins (I1+/I1-)

I1- and I1+ are the two fully-differential current-channel inputs for the Delta-Sigma ADCs.

The linear and specified region of the channels are dependent on the PGA gain. This region corresponds to a differential voltage range of ±600 mV_{PEAK}/GAIN with V_{REF} = 1.2V.

The maximum absolute voltage, with respect to A_{GND}, for each In+/- input pin is ±1V with no distortion and ±6V with no breaking after continuous voltage.

3.9 24-Bit Delta-Sigma ADC Differential Voltage Channel Inputs (V1-/V1+)

V1- and V1+ are the two fully-differential voltage-channel inputs for the Delta-Sigma ADCs.

The linear and specified region of the channels are dependent on the PGA gain. This region corresponds to a differential voltage range of ±600 mV_{PEAK}/GAIN with V_{REF} = 1.2V.

The maximum absolute voltage, with respect to A_{GND}, for each V_N+/- input pin is ±1V with no distortion and ±2V with no breaking after continuous voltage.

3.10 Analog Input (AN_IN)

This is the input to the analog-to-digital converter that can be used for temperature measurement and compensation. If temperature compensation is required in the application, it is advised to connect the low-power active thermistor IC MCP9700A to this pin. If temperature compensation is not required, this can be used as a general purpose analog-to-digital converter input.

3.11 Analog Ground Pin (A_{GND})

A_{GND} is the ground connection to internal analog circuitry (ADCs, PGA, voltage reference, POR). If an analog ground plane is available on the PCB, it is recommended that this pin be tied to that plane.

3.12 Zero Crossing Detection (ZCD)

This digital output pin is the output of the zero crossing detection circuit of the IC. The output here will be a logic output with edges that transition at each zero crossing of the voltage channel input. For more information see **Section 5.13 "Zero Crossing Detection (ZCD)"**.

3.13 Noninverting Reference Input/Internal Reference Output Pin (REFIN+/OUT)

This pin is the noninverting side of the differential voltage reference input for the Delta-Sigma ADCs or the internal voltage reference output.

For optimal performance, bypass capacitances should be connected between this pin and A_{GND} at all times, even when the internal voltage reference is used. However, these capacitors are not mandatory to ensure proper operation.

3.14 Digital Ground Connection Pins (D_{GND})

D_{GND} is the ground connection to internal digital circuitry (SINC filters, oscillator, serial interface). If a digital ground plane is available, it is recommended to tie this pin to the digital plane of the PCB. This plane should also reference all other digital circuitry in the system.

3.15 Digital Power Supply Pin (DV_{DD})

DV_{DD} is the power supply pin for the digital circuitry within the MCP39F511A. This pin requires appropriate bypass capacitors and should be maintained between +2.7V and +3.6V for specified operation. It is recommended to use 0.1 µF ceramic capacitors.

3.16 Data-Ready Pin ($\overline{DR}$)

The data-ready pin indicates if a new Delta-Sigma A/D conversion result is ready to be processed. This pin is for indication only and should be left floating. After each conversion is finished, a low pulse will take place on the data-ready pin to indicate the conversion result is ready and an interrupt is generated in the calculation engine (CE). This pulse is synchronous with the line frequency to ensure an integer number of samples for each line cycle.

Note:	This pin is internally connected to the IRQ of the calculation engine and should be left floating.

3.17 Exposed Thermal Pad (EP)

This pin is the exposed thermal pad. It must be connected to pin 24 (D_{GND}).

NOTES:

4.0 COMMUNICATION PROTOCOL

The communication protocol for the MCP39F511A device is based on the Simple Sensor Interface (SSI) protocol. This protocol is used for point-to-point communication from a single-host microcontroller (MCU) to a single-slave MCP39F511A device.

All communication to the device occurs in frames. Each frame consists of a header byte, the number of bytes in the frame, command packet (or command packets) and a checksum. It is important to note that the maximum number of bytes in either a receive or transmit frame is 35.

Note:	If a custom communication protocol is desired, please contact a Microchip sales office.

This approach allows for single, secure transmission from the host processor to the MCP39F511A device with either a single command or multiple commands. No command in a frame is processed until the entire frame is complete and the checksum and number of bytes are validated.

The number of bytes in an individual command packet depend on the specific command. For example, to set the instruction pointer, three bytes are needed in the packet: the command byte and two bytes for the address you want to set to the pointer. The first byte in a command packet is always the command byte.

This protocol can also be used to set up transmission from the MCP39F511A device on specific registers. A predetermined single-wire transmission frame is defined for one-wire interfaces. The Auto-Transmit mode can be initiated by setting the SINGLE_WIRE bit in the System Configuration register, allowing for single-wire communication within the application. See **Section 4.8 "Single-Wire Transmission Mode"** for more information on this communication.

4.1 Device Responses

After the reception of a communication frame, the MCP39F511A device has three possible responses, which will be returned with or without data depending on the frame received. These responses are:

- Acknowledge (ACK, 0x06): Frame received with success, commands understood and commands executed with success.
- Negative Acknowledge (NAK, 0x15): Frame received with success, however commands not executed with success, commands not understood or some other error in the command bytes.
- Checksum Fail (CSFAIL, 0x51): Frame received with success, however the checksum of the frame did not match the bytes in the frame.

Note:	There is one unique device ID response that is used to determine which MCP39FXXX device is present: [NAK(0x15) + ID_BYTE]. If the command received is a single byte (0x5A) instead of a command frame, the response is NAK followed by the ID_BYTE. For the MCP39F511A device, the ID_BYTE is 0x04.

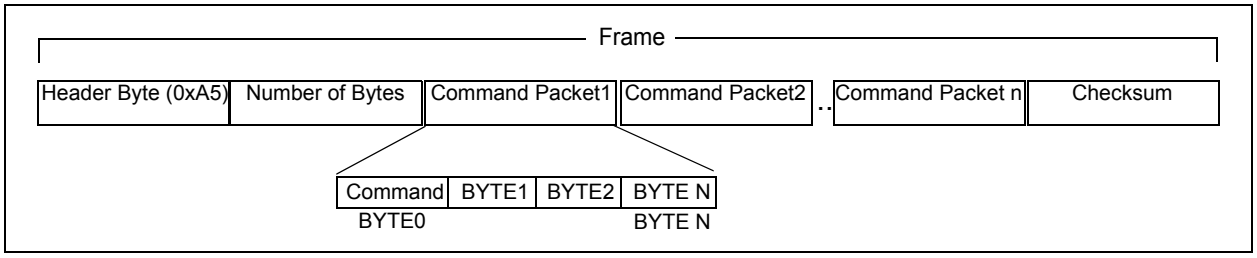


FIGURE 4-1: *Communication Frame MCP39F511A.*

4.2 Checksum

The checksum is generated using simple byte addition and taking the modules to find the remainder after dividing the sum of the entire frame by 256. This operation is done to obtain an 8-bit checksum. All the bytes of the frame are included in the checksum, including the header byte and the number of bytes. If a frame includes multiple command packets, none of the commands will be issued if the frame checksum fails. In this instance, the MCP39F511A device will respond with a CSFAIL response of 0x51.

On commands that are requesting data back from the MCP39F511A device, the frame and checksum are created in the same way, with the header byte becoming an Acknowledge (0x06). Communication examples are given in **Section 4.5 "Example Communication Frames and MCP39F511A Responses"**.

4.3 UART Settings

The default baud rate is 9.6 kbps and can be changed using the UART bits in the **System Configuration Register**. Note that the baud rate is changed at system power-up, so when changing the baud rate, a `Save To Flash` command followed by a power-on cycle is required. The UART operates in 8-bit mode, plus one Start bit and one Stop bit, for a total of 10 bits per byte, as shown in Figure 4-2.

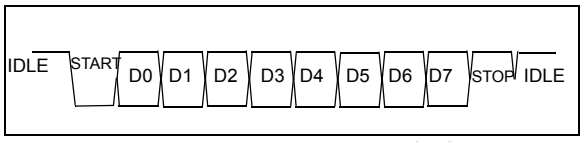


FIGURE 4-2: *UART Transmission, N-8-1.*

4.4 Command List

The following table is a list of all accepted command bytes for the MCP39F511A device. There are 10 possible accepted commands for the MCP39F511A device.

TABLE 4-1: MCP39F511A INSTRUCTION SET

Command #	Command	Command ID	Instruction Parameter	Number of Bytes	Successful Response UART_TX
1	`Register Read, N bytes`	0x4E	NoB(3)	2	ACK, NoB, data, checksum
2	`Register Write, N bytes`	0x4D	NoB(3)	1+N	ACK
3	`Set Address Pointer`	0x41	ADDRESS	3	ACK
4	`Save Registers To Flash`	0x53	None	1	ACK
5	`Page Read EEPROM`	0x42	PAGE	2	ACK, NoB, data, checksum
6	`Page Write EEPROM`	0x50	PAGE	18	ACK
7	`Bulk Erase EEPROM`	0x4F	None	1	ACK
8	`Auto-Calibrate Gain`	0x5A	None	**Note 1**	
9	`Auto-Calibrate Reactive Gain`	0x7A	None	**Note 1, 2**	
10	`Auto-Calibrate Frequency`	0x76	None	**Note 1, 2**	
11	`Save Energy Counters to EEPROM`	0x45	None	1	ACK

Note 1: See **Section 9.0 "MCP39F511A Calibration"** for more information.

2: AC mode only

3: NoB represents total number of bytes in frame

4.5 Example Communication Frames and MCP39F511A Responses

Tables 4-2 to 4-11 show exact hexadecimal communication frames as recommended to be sent to the MCP39F511A device from the system MCU. The values here can be used as direct examples for writing the code to communicate to the MCP39F511A device.

TABLE 4-2: REGISTER READ, N BYTES COMMAND (Note 1)

Byte #	Value	Description	Response from MCP39F511A
1	0xA5	Header Byte	
2	0x08	Number of Bytes in Frame	
3	0x41	Command (`Set Address Pointer`)	
4	0x00	Address High	
5	0x02	Address Low	
6	0x4E	Command (`Register Read, N Bytes`)	
7	0x20	Number of Bytes to Read (32)	
8	0x5E	Checksum	ACK + NoB (35) + data (32) + checksum

Note 1: This example `Register Read, N bytes` frame, as it is written here, can be used to poll a subset of the output data, starting at the top, address 0x02, and reading 32 data bytes back or 35 bytes total in the frame.

TABLE 4-3: REGISTER WRITE, N BYTES COMMAND (Note 1)

Byte #	Value	Description	Response from MCP39F511A
1	0xA5	Header Byte	
2	0x0C	Number of Bytes in Frame	
3	0x41	Command (`Set Address Pointer`)	
4	0x00	Address High	
5	0x94	Address Low	
6	0x4D	Command (`Register Write, N Bytes`)	
7	0x04	Number of Bytes to Write (4)	
8–11	*Data*	Data Bytes (4 total data bytes)	
12	Checksum	Checksum	ACK

Note 1: This `Register Write, N Bytes` frame, as it is written here, can be used to write the System Configuration register, which controls the device configuration, including the ADC. See Register 6-2 for more information.

TABLE 4-4: SET ADDRESS POINTER COMMAND (Note 1)

Byte #	Value	Description	Response from MCP39F511A
1	0xA5	Header Byte	
2	0x06	Number of Bytes in Frame	
3	0x41	Command (`Set Address Pointer`)	
4	0x00	Address High	
5	0x02	Address Low	
6	0xF8	Checksum	ACK

Note 1: The `Set Address Pointer` command is typically included inside of a frame that includes a read or write command, as shown in Tables 4-2 and 4-3. There is typically no reason for this command to have its own frame, but is shown here as an example.

TABLE 4-5: SAVE TO FLASH COMMAND

Byte #	Value	Description	Response from MCP39F511A
1	0xA5	Header Byte	
2	0x04	Number of Bytes in Frame	
3	0x53	Command (`Save To Flash`)	
4	0xFC	Checksum	ACK

TABLE 4-6: PAGE READ EEPROM COMMAND

Byte #	Value	Description	Response from MCP39F511A
1	0xA5	Header Byte	
2	0x05	Number of Bytes in Frame	
3	0x42	Command (`Page Read EEPROM`)	
4	0x01	Page Number (example: 1)	
5	0xF8	Checksum	ACK + NoB (19) + EEPROM Page Data (16) + Checksum

TABLE 4-7: PAGE WRITE EEPROM COMMAND

Byte #	Value	Description	Response from MCP39F511A
1	0xA5	Header Byte	
2	0x15	Number of Bytes in Frame	
3	0x50	Command (`Page Write EEPROM`)	
4	0x01	Page Number (e.g. 1)	
5-20	*Data*	EEPROM Data (16 bytes/page)	
21	Checksum	Checksum	ACK

TABLE 4-8: BULK ERASE EEPROM COMMAND

Byte #	Value	Description	Response from MCP39F511A
1	0xA5	Header Byte	
2	0x04	Number of Bytes in Frame	
3	0x4F	Command (`Bulk Erase EEPROM`)	
4	0xF8	Checksum	ACK

TABLE 4-9: AUTO-CALIBRATE GAIN COMMAND

Byte #	Value	Description	Response from MCP39F511A
1	0xA5	Header Byte	
2	0x04	Number of Bytes in Frame	
3	0x5A	Command (`Auto-Calibrate Gain`)	
4	0x03	Checksum	ACK (or NAK if unable to calibrate)[1]

Note 1: See **Section 9.0 "MCP39F511A Calibration"** for more information.

TABLE 4-10: AUTO-CALIBRATE REACTIVE GAIN COMMAND

Byte #	Value	Description	Response from MCP39F511A
1	0xA5	Header Byte	
2	0x04	Number of Bytes in Frame	
3	0x7A	Command (`Auto-Calibrate Reactive Gain`)	
4	0x23	Checksum	ACK (or NAK if unable to calibrate)[1]

Note 1: See **Section 9.0 "MCP39F511A Calibration"** for more information.

TABLE 4-11: AUTO-CALIBRATE FREQUENCY COMMAND

Byte #	Value	Description	Response from MCP39F511A
1	0xA5	Header Byte	
2	0x04	Number of Bytes in Frame	
3	0x76	Command (`Auto-Calibrate Frequency`)	
4	0x1F	Checksum	ACK (or NAK if unable to calibrate)[1]

Note 1: See **Section 9.0 "MCP39F511A Calibration"** for more information.

4.6 Command Descriptions

4.6.1 REGISTER READ, N BYTES (0x4E)

The `Register Read, N bytes` command returns the N bytes that follow whatever the current address pointer is set to. It should typically follow a `Set Address Pointer` command and can be used in conjunction with other read commands. An Acknowledge NoB, Data and Checksum is the response for this command. The maximum number of bytes that can be read with this command is 32. If there are other read commands within a frame, the maximum number of bytes that can be read is 32 minus the number of bytes being read in the frame. With this command, the data is returned LSb first.

4.6.2 REGISTER WRITE, N BYTES (0x4D)

The `Register Write, N bytes` command is followed by N bytes that will be written to whatever the current address pointer is set to. It should typically follow a `Set Address Pointer` command and can be used in conjunction with other write commands. An Acknowledge is the response for this command. The maximum number of bytes that can be written with this command is 32. If there are other write commands within a frame, the maximum number of bytes that can be written is 32 minus the number of bytes being written in the frame. With this command, the data is written to the LSb first.

4.6.3 SET ADDRESS POINTER (0x41)

This command is used to set the address pointer for all read and write commands. This command is expecting the address pointer as the command parameter in the following two bytes, Address High byte followed by Address Low byte. The address pointer is two bytes in length. If the address pointer is within the acceptable addresses of the device, an Acknowledge will be returned.

4.6.4 SAVE REGISTERS TO FLASH (0x53)

The `Save Registers To Flash` command makes a copy of all the calibration and configuration registers to Flash. This includes all R/W registers in the register set. The response to this command is an Acknowledge.

4.6.5 PAGE READ EEPROM (0x42)

The `Page Read EEPROM` command returns 16 bytes of data that are stored in an individual page on the MCP39F511A. A more complete description of the memory organization of the EEPROM can be found in **Section 10.0 "EEPROM"**. This command is expecting the EEPROM page as the command parameter or the following byte. The response to this command is an Acknowledge NoB, 16-bytes of data and CRC Check-sum.

4.6.6 PAGE WRITE EEPROM (0x50)

The `Page Write EEPROM` command is expecting 17 additional bytes in the command parameters, which are EEPROM page plus 16 bytes of data. A more complete description of the memory organization of the EEPROM can be found in **Section 10.0 "EEPROM"** The response to this command is an Acknowledge.

4.6.7 BULK ERASE EEPROM (0x4F)

The `Bulk Erase EEPROM` command will erase the entire EEPROM array and return it to a state of 0xFFFF for each memory location of EEPROM. A more complete description of the memory organization of the EEPROM can be found in **Section 10.0 "EEPROM"**. The response to this command is an Acknowledge.

4.6.8 AUTO-CALIBRATE GAIN (0x5A)

The `Auto-Calibrate Gain` command initiates the single-point calibration that is all that is typically required for the system. This command calibrates the RMS current, RMS voltage and active power based on the target values written in the corresponding registers. See **Section 9.0 "MCP39F511A Calibration"** for more information on device calibration. The response to this command is an Acknowledge.

4.6.9 AUTO-CALIBRATE REACTIVE POWER GAIN (0X7A)

The `Auto-Calibrate Reactive Gain` command initiates a single-point calibration to match the measured reactive power to the target reactive power. This is typically done at PF = 0.5. See **Section 9.0 "MCP39F511A Calibration"** for more information on device calibration.

4.6.10 AUTO-CALIBRATE FREQUENCY (0x76)

For applications not using an external crystal and running the MCP39F511A device off the internal oscillator, a gain calibration to the line frequency indication is required. The Gain Line Frequency register is set such that the frequency indication matches what is set in the Line Frequency Reference register. See **Section 9.0 "MCP39F511A Calibration"** for more information on device calibration.

4.6.11 SAVE ENERGY COUNTERS TO EEPROM (0x45)

The `Save Energy Counters to EEPROM` command makes a copy of the energy counters to EEPROM. Import active and reactive energy counters are saved in PAGE 0. Export active and reactive energy counters are saved in PAGE 1. The bytes are written at incremental addresses, starting with the LSb. The response to this command is an Acknowledge.

4.7 Notation for Register Types

The following notation has been adopted for describing the various registers used in the MCP39F511A:

TABLE 4-12: SHORT-HAND NOTATION FOR REGISTER TYPES

Notation	Description
u64	Unsigned, 64-bit register
u32	Unsigned, 32-bit register
s32	Signed, 32-bit register
u16	Unsigned, 16-bit register
s16	Signed, 16-bit register
b32	32-bit register containing discrete Boolean bit settings

4.8 Single-Wire Transmission Mode

In Single-Wire Transmission mode, at the end of each computation cycle, the device automatically transmits a frame of power data. This allows for single-wire communication after the device has been configured.

The single-wire transmission frame consists of 20 bytes: three Header bytes, one checksum and 16 bytes of power data (including RMS current, RMS voltage, active power, reactive power and line frequency).

TABLE 4-13: SINGLE-WIRE TRANSMISSION FRAME (Note 1)

#	Byte
1	HEADERBYTE (0xAB)
2	HEADERBYTE2 (0xCD)
3	HEADERBYTE3 (0xEF)
4	CURRENT RMS – Byte 0
5	CURRENT RMS – Byte 1
6	CURRENT RMS – Byte 2
7	CURRENT RMS – Byte 3
8	VOLTAGE RMS – Byte 0
9	VOLTAGE RMS – Byte 1
10	ACTIVE POWER – Byte 0
11	ACTIVE POWER – Byte 1
12	ACTIVE POWER – Byte 2
13	ACTIVE POWER – Byte 3
14	REACTIVE POWER – Byte 0
15	REACTIVE POWER – Byte 1
16	REACTIVE POWER – Byte 2
17	REACTIVE POWER – Byte 3
18	LINE FREQUENCY – Byte 0
19	LINE FREQUENCY – Byte 1
20	CHECKSUM

Note 1: For custom single-wire transmission packets, contact a Microchip sales office.

NOTES:

5.0 CALCULATION ENGINE (CE) DESCRIPTION

5.1 Computation Cycle Overview

The MCP39F511A device uses a coherent sampling algorithm to phase lock the sampling rate to the line frequency with an integer number of samples per line cycle (56), and reports all power output quantities at a 2^N number of line cycles. This is defined as a computation cycle and is dependent on the line frequency, so any change in the line frequency will change the update rate of the power outputs.

Assuming that the input frequency is 50 Hz, the sampling speed is 56 * 50 = 2800 samples/second. For the default accumulation interval parameter of 2, the computational cycle is 56 * 4 divided by the sampling speed (the result is 80 ms).

In DC mode, the sampling speed is fixed at approximately 1953 samples/second. For the default value of the accumulation interval parameter (2), the computational cycle is 56 * 4 divided by the sampling speed (the result is approximately 114.7 ms).

5.1.1 LINE FREQUENCY

The coherent sampling algorithm is also used to calculate the Line Frequency Output register, which is updated every computation cycle. The correction factor for line frequency measurement is the Gain Line Frequency register, which is used during the line frequency calibration, see **Section 9.6.1 "Using the Auto-Calibrate Frequency Command"**. Note that the resolution of the Line Frequency Output register is fixed, and the resolution is 1 milliHz.

5.1.2 POWER ON RESET (POR) WITH AC DETECTION BEHAVIOR

At Power-on Reset, the calculation engine must initialize the AFE and also initialize all the peripherals, prior to being able to start the first computation cycle. In addition, the device must detect whether or not an AC signal is present and if so, determine the correct coherent sampling clock values. This process is given sufficient time for correct initialization and the start-up time is 500 ms for a 50 Hz line, and 417 ms for a 60 Hz line.

The high pass filters are turned off to let pass both DC and AC signals. If the number of zero crossings detected during this time on the voltage channel is less than 10 (to filter out false detections), the device will automatically switch to DC mode.

5.1.3 DC DETECTION AND DC MODE

The device uses an internal counter based on the sampling rate of the AFE to determine if an AC signal is not present and if the device should switch to DC mode. If an AC signal is not present for this time period (same as above, based on the number of zero crossings detected on the voltage channel), the device will switch to DC mode, turning off the high pass filters and setting the frequency output to zero.

5.2 Accumulation Interval Parameter

The accumulation interval is defined as an 2^N number of line cycles, where N is the value in the Accumulation Interval Parameter register. N can be as low as 0 (for the fastest update rate), but no bigger than 8.

5.3 Raw Voltage and Currents Signal Conditioning

The first set of signal conditioning that occurs inside the MCP39F511A is shown in Figure 5-1. All conditions set in this diagram effect all of the output registers (RMS current, RMS voltage, Active power, Reactive power, Apparent power, etc.). The gain of the PGA, the Shutdown and Reset status of the 24-bit ADCs are all controlled through the System Configuration Register.

For DC applications, offset can be removed by using the OFFCAL_CH0 and OFFCAL_CH1 registers for current offset and voltage offset, respectively. The OFFCAL_MSB register holds the most significant byte (MSB) for both the OFFCAL_CH0 (current) and OFFCAL_CH1 (voltage) calibration values and together add to the full 24-bit value written directly into the internal offset registers of the ADC. The Phase Compensation register is used to compensate for any external phase error between the voltage and current channels.

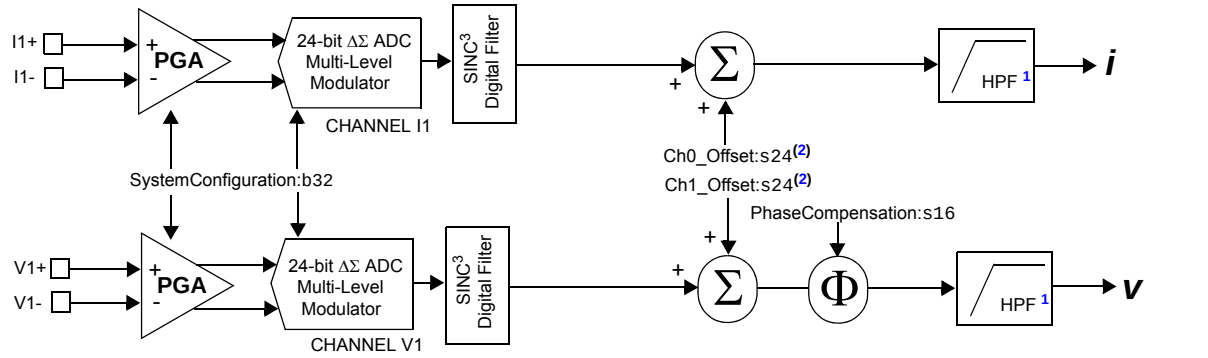
See **Section 9.0 "MCP39F511A Calibration"** for more information on device calibration.

5.4 RMS Current and RMS Voltage

The MCP39F511A device provides true RMS measurements. The MCP39F511A device has two simultaneous sampling 24-bit A/D converters for the current and voltage measurements. The root mean square calculations are performed on 2^N current and voltage samples, where N is defined by the register Accumulation Interval Parameter.

EQUATION 5-1: RMS CURRENT AND VOLTAGE

$$I_{RMS} = \sqrt{\frac{\sum_{n=0}^{2^N-1} (i_n)^2}{2^N}} \qquad V_{RMS} = \sqrt{\frac{\sum_{n=0}^{2^N-1} (v_n)^2}{2^N}}$$



Note 1: High-Pass Filters (HPFs) are automatically disabled in the absence of an AC signal on the voltage channel.

2: Ch0_Offset and Ch1_Offset are 24-bit values. The 24-bit two's complement MSB first coding values are calculated internally using the corresponding byte from the OFFCAL_MSB register and OFFCAL_CHn 16-bit values. The result is added to the output code of the corresponding channel bit-by-bit.

FIGURE 5-1: *Channel I1 and V1 Signal Flow.*

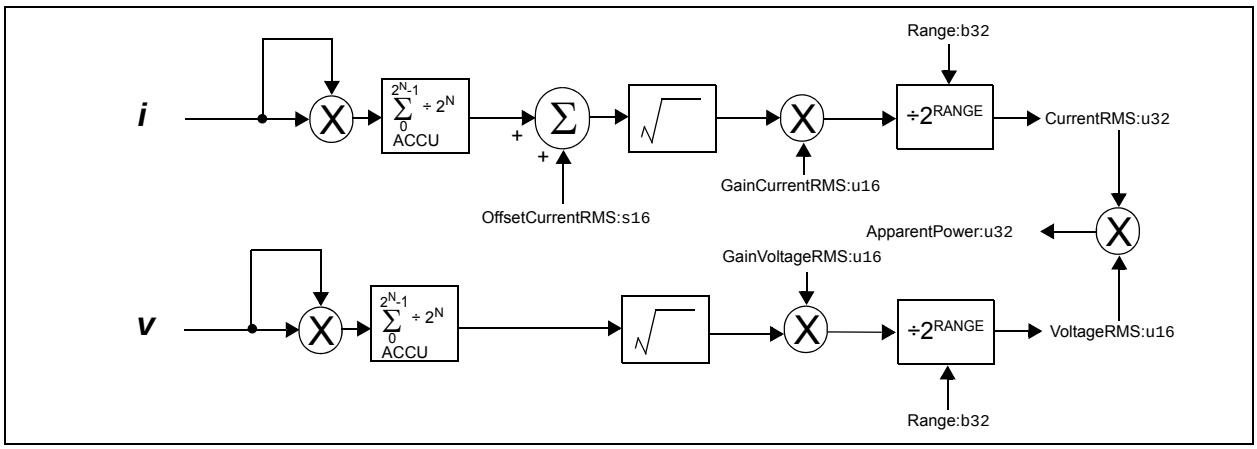


FIGURE 5-2: *RMS Current and Voltage Calculation Signal Flow.*

5.5 Power and Energy

The MCP39F511A offers signed power numbers for active and reactive power, import and export registers for active energy, and four-quadrant reactive power measurement. For this device, import power or energy is considered positive (power or energy being consumed by the load), and export power or energy is considered negative (power or energy being delivered by the load). The following figure represents the measurements obtained by the MCP39F511A.

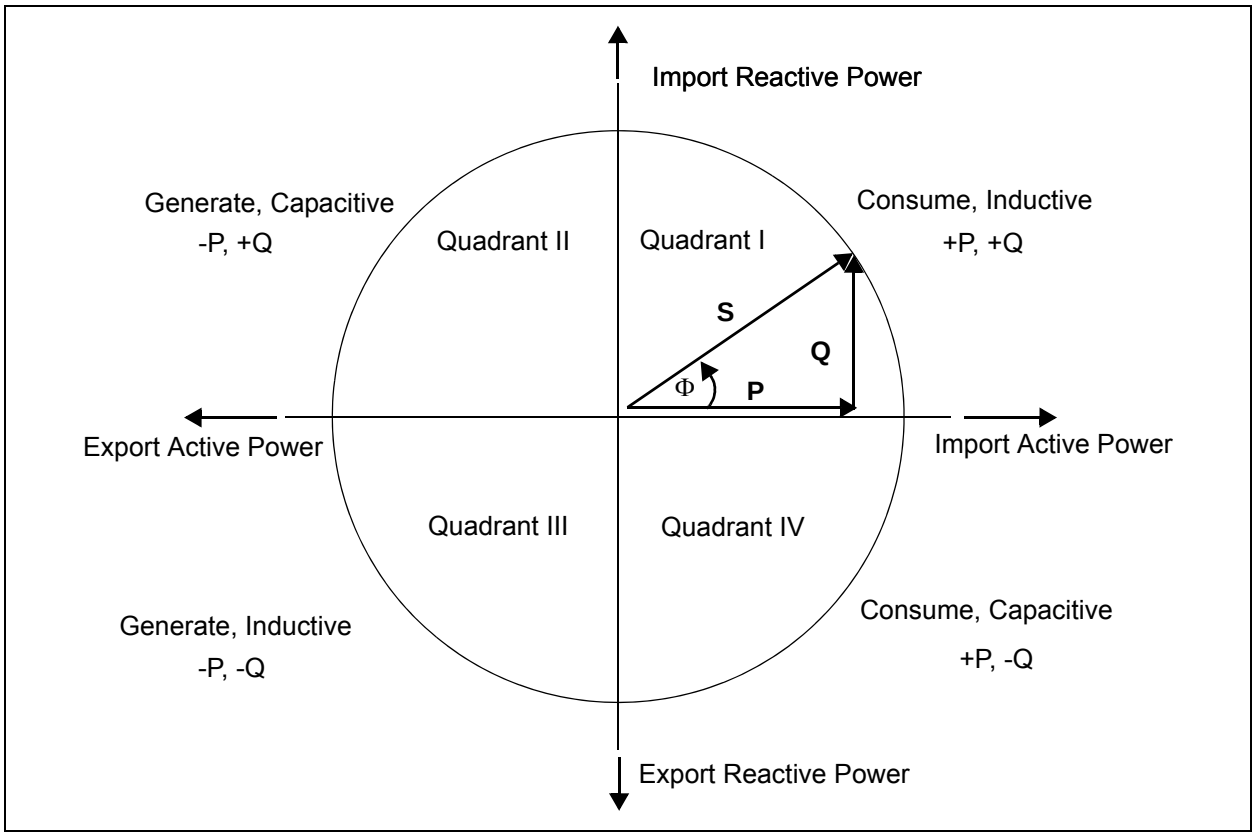


FIGURE 5-3: *The Power Circle and Triangle (S = Apparent, P = Active, Q = Reactive).*

5.6 Energy Accumulation

Energy accumulation for all four energy registers (Import/Export, Active/Reactive) occurs at the end of each computation cycle, if the energy accumulation has been turned on. See **Section 6.3 "System Status Register"** on the Energy Control register. A no-load threshold test is done to make sure the measured energy is not below the no-load threshold, if it is above, the accumulation occurs with a default energy resolution of 1 mWh for all of the energy registers.

5.6.1 NO-LOAD THRESHOLD

The no-load threshold is set by modifying the value in the No-Load Threshold register. The unit for this register is power with a default resolution of 0.01W. The default value is 100 or 1.00W. Any power that is below 1W will not be accumulated into any of the energy registers.

5.7 Apparent Power (S)

This 32-bit register is the output register for the final apparent power indication. It is the product of RMS current and RMS voltage as shown in Equation 5-2.

EQUATION 5-2: APPARENT POWER (S)

$$S = I_{RMS} \times V_{RMS}$$

For scaling of the apparent power indication, the calculation engine uses the register Apparent Power Divisor Digits. This is described in the following register operations, per Equation 5-3.

EQUATION 5-3: APPARENT POWER (S)

$$S = \frac{CurrentRMS \times VoltageRMS}{10^{AparentPowerDivisorDigits}}$$

5.8 Active Power (P)

The MCP39F511A has two simultaneous sampling A/D converters. For the active power calculation, the instantaneous current and instantaneous voltages are multiplied together to create instantaneous power. This instantaneous power is then converted to active power by averaging or calculating the DC component.

Equation 5-4 controls the number of samples used in this accumulation prior to updating the Active Power output register.

Please note that although this register is unsigned, the direction of the active power (import or export) can be determined by the Active Power Sign bit located in the System Status Register.

EQUATION 5-4: ACTIVE POWER

$$P = \frac{1}{2^N} \sum_{k=0}^{k=2^N-1} V_k \times I_k$$

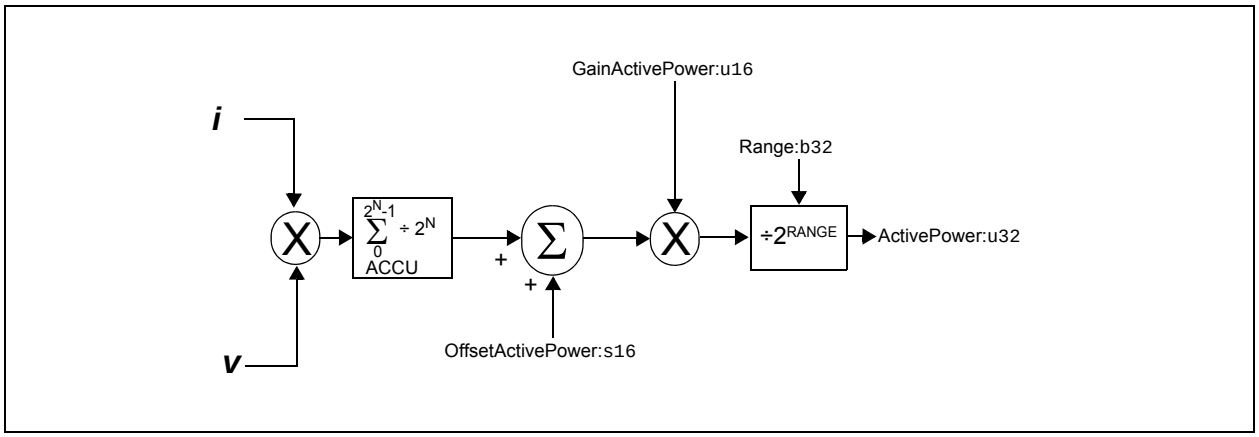


FIGURE 5-4: *Active Power Calculation Signal Flow.*

5.9 Power Factor (PF)

Power factor is calculated by the ratio of P to S or active power divided by apparent power.

EQUATION 5-5: POWER FACTOR

$$PF = \frac{P}{S}$$

The power factor reading is stored in a signed 16-bit register (Power Factor). This register is a signed, 2's complement register with the MSb representing the polarity of the power factor. A positive power factor means Active power is being imported, a negative power factor represents export active power. The sign of the reactive power component is used to tell if the current is lagging the voltage, with a positive sign meaning an inductive load and a negative sign meaning capacitive. Each LSb is then equivalent to a weight of 2^{-15}. A maximum register value of 0x7FFF corresponds to a power factor of 1. The minimum register value of 0x8000 corresponds to a power factor of -1.

5.10 Reactive Power (Q)

In the MCP39F511A device, reactive power is calculated using a 90 degree phase shift in the voltage channel. The same accumulation principles apply as with active power where ACCU acts as the accumulator. Any light load or residual power can be removed by using the Offset Reactive Power register. Gain is corrected by the Gain Reactive Power register. The final output is an unsigned 32-bit value located in the Reactive Power register.

Please note that although this register is unsigned, the direction of the power can be determined by the Reactive Power Sign bit in the system Status register.

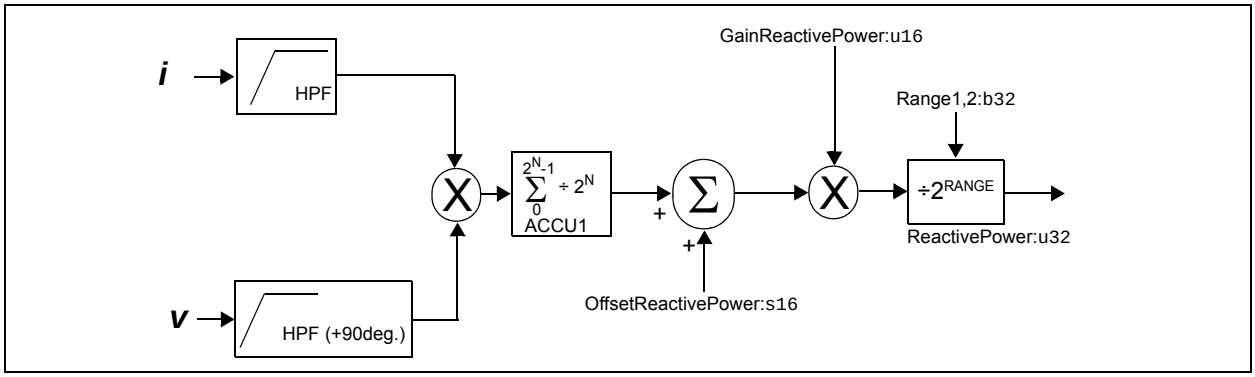


FIGURE 5-5: *Reactive Power Calculation Signal Flow.*

5.11 10-Bit Analog Input

The least 10 significant bits of the 16-bit Analog Input register contain the output of the 10-bit ADC. The conversion rate of the analog input occurs once every computation cycle.

The thermistor voltage can be used for temperature compensation of the calculation engine. See **Section 9.7 "Temperature Compensation"** for more information.

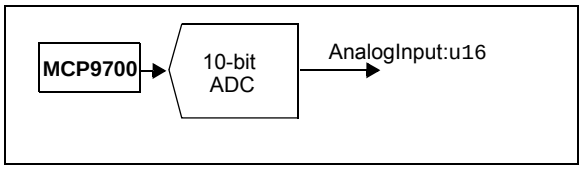


FIGURE 5-6: *Using an Analog Out Temperature Sensor for Automatic Temperature Compensation.*

5.12 Minimum and Maximum Recordings

The MCP39F511A device has the ability to record minimum and maximum outputs and keep them in a total of four registers (two minimum and two maximum) based on the value of address pointers located in the four registers listed in this section.

A minimum and maximum test is done after each calculation interval. If the current measurement value of the value directed to by the pointer is smaller or larger than the value in the Minimum or Maximum register, the record is updated appropriately.

The registers are:

- MinMaxPointer1 → MinimumRecord1, Maximum-Record1
- MinMaxPointer2 → MinimumRecord2, Maximum-Record2

Only the Output Quantity register addresses can be tracked by the Min/Max pointers. Output Quantity registers are defined as those from voltage RMS to apparent power (addresses 0x0006 to 0x001A). All other addresses will be ignored by the calculation engine.

Please note that the 64-bit energy registers can not be tracked through the Minimum and Maximum Recording registers.

5.13 Zero Crossing Detection (ZCD)

The zero crossing detection block generates a logic pulse output on the ZCD pin that is coherent with the zero crossing of the input AC signal present on voltage input pins (V1+, V1-). The ZCD pin can be enabled and disabled by the corresponding bit in the **System Configuration Register** register. When enabled, this produces a square wave with a frequency that is equivalent to that of the AC signal present on the voltage input. Figure 5-7 represents the signal on the ZCD pin superimposed with the AC signal present on the voltage input in this mode.

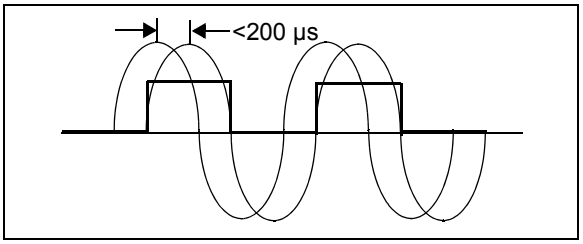


FIGURE 5-7: *Zero Crossing Detection Operation (Noninverted, Nonpulse).*

A second mode is available that produces a 100 µs pulse at each zero crossing, at a frequency that is twice that of the AC signal present on the voltage input, shown in Figure 5-8.

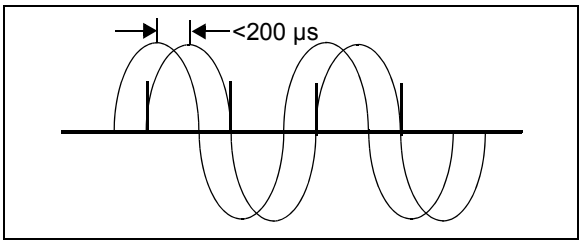


FIGURE 5-8: *Zero Crossing Detection Operation (Noninverted, Pulsed).*

Switching modes is done by setting the corresponding bit in the **System Configuration Register**. In addition, either the toggling of this pin, or the pulse, can be inverted. The ZCD Inversion bit is also in the System Configuration register.

There are two bits in the System Configuration register that can be used to modify the zero crossing. The zero crossing output can be inverted by setting the Inversion bit, or the zero crossing can be a 100 µs pulse at each zero crossing, by setting the Pulse bit.

Note that a low-pass filter is included in the signal path that allows the zero crossing detection circuit to pass the fundamental frequency, while filtering out unwanted high frequency signals. An internal compensation circuit is then used to gain back the phase delay introduced by the low-pass filter resulting in a latency of less than 200 µs.

6.0 REGISTER DESCRIPTIONS

6.1 Complete Register Map

The following table describes the registers for the MCP39F511A device.

TABLE 6-1: MCP39F511A REGISTER MAP

Address	Register Name	Section Number	Read/ Write	Data Type	Description
Output Registers					
0x0000	Instruction Pointer	6.2	R	u16	Address pointer for read or write commands
0x0002	System Status	6.3	R	b16	System Status register
0x0004	System Version	6.4	R	u16	System version date code information for MCP39F511A, set at the Microchip factory; format YYWW
0x0006	Voltage RMS	5.4	R	u16	RMS voltage output
0x0008	Line Frequency	9.6	R	u16	Line frequency output
0x000A	Thermistor Voltage	9.7	R	u16	Thermistor voltage for temperature compensation. Output of the 10-bit SAR ADC.
0x000C	Power Factor	5.9	R	s16	Power factor output
0x000E	Current RMS	5.4	R	u32	RMS current output
0x0012	Active Power **(Note 1)**	5.8	R	u32	Active power output
0x0016	Reactive Power **(Note 1)**	5.10	R	u32	Reactive power output
0x001A	Apparent Power	5.7	R	u32	Apparent power output
0x001E	Import Active Energy Counter	5.6	R	u64	Accumulator for active energy, import
0x0026	Export Active Energy Counter	5.6	R	u64	Accumulator for active energy, export
0x002E	Import Reactive Energy Counter	5.6	R	u64	Accumulator for reactive energy, import
0x0036	Export Reactive Energy Counter	5.6	R	u64	Accumulator for reactive energy, export
0x003E	Minimum Record 1	5.12	R	u32	Minimum value of the output quantity address in Min/Max Pointer 1 register
0x0042	Minimum Record 2	5.12	R	u32	Minimum Value of the output quantity address in Min/Max Pointer 2 register
0x0046	Maximum Record 1	5.12	R	u32	Maximum Value of the output quantity address in Min/Max Pointer 1 register
0x004A	Maximum Record 2	5.12	R	u32	Maximum Value of the output quantity address in Min/Max Pointer 2 register

Note 1: The registers are unsigned, however their sign is kept as a separate bit in the System Status register.

2: These registers are reserved for EMI filter compensation when necessary for power supply monitoring. They may require specific adjustment depending on PSU parameters, please contact the local Microchip office for further support.

TABLE 6-1: MCP39F511A REGISTER MAP (CONTINUED)

Address	Register Name	Section Number	Read/ Write	Data Type	Description
Calibration Registers (AC mode)					
0x004E	Calibration Register Delimiter	9.8	R/W	u16	May be used to initiate loading of the default calibration coefficients at start-up
0x0050	Gain Current RMS	9.3.1	R/W	u16	Gain calibration factor for RMS current (AC mode)
0x0052	Gain Voltage RMS	9.3.1	R/W	u16	Gain calibration factor for RMS voltage (AC mode)
0x0054	Gain Active Power	9.3.1	R/W	u16	Gain calibration factor for active power (AC mode)
0x0056	Gain Reactive Power	9.3	R/W	u16	Gain calibration factor for reactive power (AC mode)
0x0058	Reserved	—	—	u16	Reserved
0x005A	Offset Current RMS	9.5.1	R/W	s16	Offset calibration factor for RMS current (AC mode)
0x005C	Offset Active Power	9.5.1	R/W	s16	Offset calibration factor for active power (AC mode)
0x005E	Offset Reactive Power	9.5.1	R/W	s16	Offset calibration factor for reactive power (AC mode)
0x0060	Gain Line Frequency	9.6.1	R/W	u16	Gain calibration factor for line frequency (AC mode)
0x0062	Phase Compensation	9.4	R/W	s16	Phase Compensation (AC Mode)
EMI Filter Compensation Registers (Note 2)					
0x0064	VoltageDropComp	9.8	R/W	u16	Voltage drop compensation (DC and AC mode)
0x0066	InCapCurrentComp	9.8	R/W	u16	Input capacitor current compensation (AC mode)
0x0068	RangeVdropInCapComp	9.8	R/W	u16	Scaling factors for the voltage drop and input capacitor current compensation
0x006A	Reserved	—	—	u16	Reserved
Calibration Registers (DC mode)					
0x006C	DC Gain Current RMS	9.3.1	R/W	u16	Gain calibration factor for RMS current (DC mode)
0x006E	DC Gain Voltage RMS	9.3.1	R/W	u16	Gain calibration factor for RMS voltage (DC mode)
0x0070	DC Gain Active Power	9.3.1	R/W	u16	Gain calibration factor for active power (DC mode)
0x0072	DC Offset Current RMS	9.5.1	R/W	s16	Offset calibration factor for RMS current (DC mode)
0x0074	DC Offset Active Power	9.5.1	R/W	s16	Offset calibration factor for active power (DC mode)
0x0076	Reserved	—	—	u16	Reserved
0x0078	Reserved	—	—	u16	Reserved

Note 1: The registers are unsigned, however their sign is kept as a separate bit in the System Status register.

2: These registers are reserved for EMI filter compensation when necessary for power supply monitoring. They may require specific adjustment depending on PSU parameters, please contact the local Microchip office for further support.

TABLE 6-1: MCP39F511A REGISTER MAP (CONTINUED)

Address	Register Name	Section Number	Read/ Write	Data Type	Description
ADC Offset Registers					
0x007A	OFFCAL_MSB	9.5.2	R/W	b16	MSbs of the 24-bit offset values for CH0 (current channel) and CH1 (voltage channel)
0x007C	OFFCAL_CH0	9.5.2	R/W	b16	Lower 16-bit of the 24-bit offset for CH0 (current channel)
0x007E	OFFCAL_CH1	9.5.2	R/W	b16	Lower 16-bit of the 24-bit offset for CH1 (voltage channel)
Temperature Compensation Registers					
0x0080	TempPosCompFrequency	**9.7**	R/W	u16	Temperature compensation for frequency for T > TCAL
0x0082	TempNegCompFrequency	**9.7**	R/W	u16	Temperature compensation for frequency for T < TCAL
0x0084	TempPosCompCurrent	**9.7**	R/W	u16	Temperature compensation for current for T > TCAL
0x0086	TempNegCompCurrent	**9.7**	R/W	u16	Temperature compensation for current for T < TCAL
0x0088	TempPosCompPower	**9.7**	R/W	u16	Temperature compensation for power for T > TCAL
0x008A	TempNegCompPower	**9.7**	R/W	u16	Temperature compensation for power for T < TCAL
0x008C	Reserved	—	R	u16	Reserved
0x008E	Reserved	—	R	u16	Reserved
0x0090	Reserved	—	R	u16	Reserved
0x0092	Reserved	—	R	u16	Reserved
Design Configuration Registers					
0x94	System Configuration	6.5	R/W	b32	Control for device configuration, including ADC configuration
0x98	Event Configuration	7.0	R/W	b32	Settings for the event pins including relay control
0x9C	Range	6.6	R/W	b32	Scaling factor for outputs
0xA0	Calibration Current	9.3.1	R/W	u32	Target current to be used during single-point calibration
0xA4	Calibration Voltage	9.3.1	R/W	u16	Target voltage to be used during single-point calibration
0xA6	Calibration Power Active	9.3.1	R/W	u32	Target active power to be used during single-point calibration
0xAA	Calibration Power Reactive	9.3.1	R/W	u32	Target active power to be used during single-point calibration
0x00AE	Reserved	—	R	u32	Reserved
0x00B2	Reserved	—	R	u32	Reserved
0x00B6	Reserved	—	R	u32	Reserved
0x00BA	Reserved	—	R	u16	Reserved
0x00BC	Reserved	—	R	u16	Reserved

Note 1: The registers are unsigned, however their sign is kept as a separate bit in the System Status register.

2: These registers are reserved for EMI filter compensation when necessary for power supply monitoring. They may require specific adjustment depending on PSU parameters, please contact the local Microchip office for further support.

TABLE 6-1: MCP39F511A REGISTER MAP (CONTINUED)

Address	Register Name	Section Number	Read/ Write	Data Type	Description
0x00BE	App Power Divisor Digits	5.7	R/W	u16	AppPowerDivisorDigits sets the RMS (IRMS and VRMS) indications precision and the desired precision for apparent power.
0x00C0	Accumulation Interval Parameter	5.2	R/W	u16	N for 2^N number of line cycles to be used during a single computation cycle
0xC2	PWM Period	8.2	R/W	u16	Input register controlling PWM period
0xC4	PWM Duty Cycle	8.3	R/W	u16	Input register controlling PWM duty cycle
0x00C6	MinMaxPointer1	5.12	R/W	u16	Address pointer for Min/Max 1 outputs
0x00C8	MinMaxPointer2	5.12	R/W	u16	Address pointer for Min/Max 2 outputs
0x00CA	Line Frequency Reference	9.6.1	R/W	u16	Reference value for the nominal line frequency
0x00CC	Thermistor Voltage Calibration	9.7	R/W	u16	Thermistor calibration value for temperature compensation of the calculation engine
0x00CE	Voltage Sag Limit	7.2	R/W	u16	RMS voltage threshold at which an event flag is recorded
0x00D0	Voltage Surge Limit	7.2	R/W	u16	RMS voltage threshold at which an event flag is recorded
0x00D2	Over Current Limit	7.2	R/W	u32	RMS current threshold at which an event flag is recorded
0x00D6	Over Power Limit	7.2	R/W	u32	Active power limit at which an event flag is recorded
0x00DA	Overtemperature Limit	7.2.1	R/W	u16	Limit at which an overtemperature event flag is recorded
0x00DC	Voltage Low Threshold	7.3	R/W	u16	Input voltage save to EE Low threshold
0x00DE	Voltage High Threshold	7.3	R/W	u16	Input voltage Save to EE High threshold
0x00E0	No Load Threshold	5.6.1	R/W	u16	No load threshold for energy counting

Note 1: The registers are unsigned, however their sign is kept as a separate bit in the System Status register.

2: These registers are reserved for EMI filter compensation when necessary for power supply monitoring. They may require specific adjustment depending on PSU parameters, please contact the local Microchip office for further support.

6.2 Address Pointer Register

This unsigned 16-bit register contains the address to which all read and write instructions occur. This register is only written through the `Set Address Pointer` command and is otherwise outside the writable range of register addresses.

6.3 System Status Register

The System Status register is a read-only register and can be used to detect the various states of pin levels as defined in Register 6-1.

REGISTER 6-1: SYSTEM STATUS REGISTER

R-x	R-x	R-x	U-0	R-x	R-x	U-0	U-0
DCMODE	SIGN_DCCURR	SIGN_DCVOLT	—	EVENT2	EVENT1	—	—
bit 15							bit 8

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
XTALOSC	OVERTEMP	SIGN_PR	SIGN_PA	OVERPOW	OVERCUR	VSURGE	VSAG
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **DCMODE:** Mode of the meter, detected automatically.
`1` = DC mode
`0` = AC mode

bit 14 **SIGN_DCCURR:** Sign of DC Current RMS.
`1` = DC Current RMS is positive
`0` = DC Current RMS is negative

bit 13 **SIGN_DCVOLT:** Sign of DC Voltage RMS.
`1` = DC Voltage RMS is positive
`0` = DC Voltage RMS is negative

bit 12 **Unimplemented**: Read as ‘`0`’

bit 11 **EVENT2:** State of Event2 detection algorithm. This bit is latched and must be cleared.
`1` = Event 2 has occurred
`0` = Event 2 has not occurred

bit 10 **EVENT1:** State of Event1 detection algorithm. This bit is latched and must be cleared.
`1` = Event 1 has occurred
`0` = Event 1 has not occurred

bit 9-8 **Unimplemented**: Read as ‘`0`’

bit 7 **XTALOSC:** State of the Oscillator.
`1` = XTAL oscillator is enabled
`0` = XTAL oscillator is off, internal oscillator enabled

bit 6 **OVERTEMP**: State of the Overtemperature detection algorithm.
`1` = Overtemperature threshold has been broken
`0` = Overtemperature threshold has not been broken

bit 5 **SIGN_PR:** Sign of Reactive Power.
`1` = Reactive Power is positive, inductive and is in quadrants 1,2
`0` = Reactive Power is negative, is capacitive and is in quadrants 3,4

REGISTER 6-1: SYSTEM STATUS REGISTER (CONTINUED)

bit 4 **SIGN_PA:** Sign of Active Power (import/export sign of active power).
1 = Active Power is positive (import) and is in quadrants 1,4
0 = Active Power is negative (export) and is in quadrants 2,3

bit 3 **OVERPOW:** State of Overpower detection algorithm. An over power event has occurred in the system.
1 = Overpower threshold has been broken
0 = Overpower threshold has not been broken

bit 2 **OVERCUR:** State of the Overcurrent detection algorithm. An over current event has occurred in the system.
1 = Overcurrent threshold has been broken
0 = Overcurrent threshold has not been broken

bit 1 **VSURGE:** State of Voltage Surge detection algorithm. This bit is latched and must be cleared.
1 = Surge threshold has been broken
0 = Surge threshold has not been broken

bit 0 **VSAG:** State of Voltage Sag detection algorithm. This bit is latched and must be cleared.
1 = Sag threshold has been broken
0 = Sag threshold has not been broken

6.4 System Version Register

The System Version register is hard-coded by Microchip Technology Incorporated and contains calculation engine date code information. The System Version register is a date code in the YYWW format, with year and week number in decimal (for instance, 0x1810 = 2018, 10th week).

6.5 System Configuration Register

The System Configuration register contains bits for the following control:

- PGA settings
- ADC Reset State
- ADC Shutdown State
- UART baud rate
- Single Wire Auto-Transmission
- ZCD pin behavior
- Temperature compensation
- PWM
- Energy counting

These options are described in the following sections.

6.5.1 PROGRAMMABLE GAIN AMPLIFIERS (PGA)

The two Programmable Gain Amplifiers (PGAs) reside at the front-end of each 24-bit Delta-Sigma ADC. They have two functions:

- Translate the common mode of the input from A_{GND} to an internal level between A_{GND} and A_{VDD}
- Amplify the input differential signal

The translation of the common mode does not change the differential signal but enters the common mode so that the input signal can be properly amplified.

The PGA block can be used to amplify very low signals, but the differential input range of the Delta-Sigma modulator must not be exceeded. The PGA is controlled by the PGA_CHn<2:0> bits in Register 6-2 the System Configuration register. Table 6-2 represents the gain settings for the PGAs.

TABLE 6-2: PGA CONFIGURATION SETTING (Note 1)

Gain PGA_CHn<2:0>			Gain (V/V)	Gain (dB)	V_{IN} Range (V)
0	0	0	1	0	±0.6
0	0	1	2	6	±0.3
0	1	0	4	12	±0.15
0	1	1	8	18	±0.075
1	0	0	16	24	±0.0375
1	0	1	32	30	±0.01875

Note 1: This table is defined with V_{REF} = 1.2V. The two undefined settings, 110 and 111 are G=1.

6.5.2 24-BIT ADC RESET MODE (SOFT RESET MODE)

24-bit ADC Reset mode (also called Soft Reset) can only be entered through setting high the RESET<1:0> bits in the System Configuration Register register. This mode is defined as the condition where the converters are active but their output is forced to '0'.

6.5.3 ADC SHUTDOWN MODE

ADC Shutdown mode is defined as a state where the converters and their biases are OFF, consuming only leakage current. When the Shutdown bit is reset to '0', the analog biases will be enabled, as well as the clock and the digital circuitry.

Each converter can be placed in Shutdown mode independently. This mode is only available through programming of the SHUTDOWN<1:0> bits in the System Configuration Register register.

Note: The PHASE register can be used to serially Soft Reset the ADCs, without using the RESET bits in the Configuration register, if the same value is written in the PHASE register.

REGISTER 6-2: SYSTEM CONFIGURATION REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1
—	—	PGA_CH1<2:0>			PGA_CH0<2:0>		
bit 31							bit 24

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 23							bit 16

R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
UART<2:0>[1]			ZCD_INV	ZCD_PULS	ZCD_OUTPUT_DIS	—	SINGLE_WIRE
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TEMPCOMP	RESET<1:0>		SHUTDOWN<1:0>		VREFEXT	PWM_CNTRL	ENRG_CNTRL
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-30 **Unimplemented**: Read as '0'

bit 29-27 **PGA_CH1 <2:0>:** PGA Setting for the voltage channel.
111 = Reserved (Gain = 1)
110 = Reserved (Gain = 1)
101 = Gain is 32
100 = Gain is 16
011 = Gain is 8
010 = Gain is 4
001 = Gain is 2
000 = Gain is 1 **(Default)**

bit 26-24 **PGA_CH0 <2:0>:** PGA Setting for the current channel.
111 = Reserved (Gain = 1)
110 = Reserved (Gain = 1)
101 = Gain is 32
100 = Gain is 16
011 = Gain is 8 **(Default)**
010 = Gain is 4
001 = Gain is 2
000 = Gain is 1

bit 23-16 **Unimplemented**: Read as '0'

REGISTER 6-2: SYSTEM CONFIGURATION REGISTER (CONTINUED)

bit 15-13 **UART<2:0>:** UART Baud Rate bits **(Note 1)**
111 = 1200
110 = 2400
101 = 4800
100 = 9600 **(Default)**
011 = 19200
010 = 38400
001 = 57600
000 = 115200

bit 12 **ZCD_INV:** Zero Crossing Detection Output Inverse
1 = ZCD is inverted
0 = ZCD is not inverted **(Default)**

bit 11 **ZCD_PULS:** Zero Crossing Detection Pulse mode
1 = ZCD output is 100 µs pulses on zero crossings
0 = ZCD Output changes logic state on zero crossings **(Default)**

bit 10 **ZCD_OUTPUT_DIS:** Disable the Zero Crossing output pin
1 = ZCD output is disabled
0 = ZCD output is enabled **(Default)**

bit 9 **Unimplemented:** Read as '0'

bit 8 **SINGLE_WIRE:** Single-Wire Enable bit
1 = Single-wire transmission is enabled
0 = Single-wire transmission is disabled **(Default)**

bit 7 **TEMPCOMP:** Temperature-Compensation Enable bit
1 = Temperature compensation is enabled
0 = Temperature compensation is disabled **(Default)**

bit 6-5 **RESET <1:0>:** Reset mode setting for ADCs
11 = Both I1 and V1 are in Reset mode
10 = V1 ADC is in Reset mode
01 = I1 ADC is in Reset mode
00 = Neither ADC is in Reset mode **(Default)**

bit 4-3 **SHUTDOWN <1:0>:** Shutdown mode setting for ADCs
11 = Both I1 and V1 are in Shutdown
10 = V1 ADC is in Shutdown
01 = I1 ADC is in Shutdown
00 = Neither ADC is in Shutdown **(Default)**

bit 2 **VREFEXT:** Internal Voltage Reference Shutdown Control
1 = Internal Voltage Reference Disabled
0 = Internal Voltage Reference Enabled **(Default)**

bit 1 **PWM_CNTRL:** PWM Control
1 = PWM is turned on
0 = PWM is turned off **(Default)**

bit 0 **ENRG_CNTRL:** Energy Accumulation Control bit
1 = Energy is ON and all registers are accumulating
0 = Energy accumulation is turned off and all energy accumulation registers are reset to 0 **(Default)**

Note 1: The baud rate is only changed at system power-up, so a `Save To Flash` command is required after changing the baud rate.

6.6 Range Register

The Range register is a 32-bit register that contains the number of right-bit shifts for the following outputs, divided into separate bytes defined below:

- RMS Current
- RMS Voltage
- Power (Active, Reactive, Apparent)

Note that the power range byte operates across both the active and reactive output registers and sets the same scale.

The purpose of this register is two fold: the number of right-bit shifting (division by 2^{RANGE}) must be:

- High enough to prevent overflow in the output register,
- Low enough to allow for the desired output resolution.

It is the user's responsibility to set this register correctly to ensure proper output operation for a given meter design.

For further information and example usage, see **Section 9.3 "Single-Point Gain Calibrations at Unity Power Factor"**.

REGISTER 6-3: RANGE REGISTER

R-0	R-0	R-0	R-1	R-1	R-0	R-1	R-1
Energy<7:0>							
bit 31							bit 24

R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1	R/W-0	R/W-1
POWER<7:0>							
bit 23							bit 16

R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0
CURRENT<7:0>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-0
VOLTAGE<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **ENERGY<7:0>:** Sets the number of right-bit shifts for the Energy output registers. Note that the value is read-only and is calculated automatically as 29 – Accumulation Interval.

bit 23-16 **POWER<7:0>:** Sets the number of right-bit shifts for the Active and Reactive Power output registers

bit 15-8 **CURRENT<7:0>:** Sets the number of right-bit shifts for the Current RMS output register

bit 7-0 **VOLTAGE<7:0>:** Sets the number of right-bit shifts for the Voltage RMS output register

NOTES:

7.0 EVENT OUTPUT PINS/EVENT CONFIGURATION REGISTER

7.1 Event Pins

The MCP39F511A device has two event pins that can be configured in three possible configurations. These configurations are:

1. No event is mapped to the pin
2. Voltage Surge, Voltage Sag, Overcurrent, Overtemperature or Overpower event is mapped to the pin. More than one event can be mapped to the same pin.
3. Manual control of two pins, independently

These three configurations allow for the control of external interrupts or hardware that is dependent on the measured power, current or voltage. The Event Configuration register below describes how these events and pins can be configured.

Note:	If an event is mapped to a pin, manual control of the respective pin is not possible. To enable manual control, no event has to be mapped to the pin.

7.2 Limits

There are five limit registers associated with these events:

- Overtemperature limit
- Voltage Sag limit
- Voltage Surge limit
- Overcurrent limit
- Overpower limit

Each of these limits are compared to the respective output registers of voltage, current and power. It is recommended that they have the same unit for comparison, e.g. 0.1V, or 0.01W.

7.2.1 OVERTEMPERATURE LIMIT

The Overtemperature Limit register is compared to the 10-bit SAR output (Thermistor Voltage Register) and is a number between 0 and 1023.

When the threshold is passed, the corresponding event flags and event pins (if mapped) are set.

7.2.2 VOLTAGE SAG AND VOLTAGE SURGE DETECTION

The event alarms for Voltage Sag and Voltage Surge work differently compared to the Overcurrent and Overpower events, which are tested against every computation cycle. These two event alarms are designed to provide a much faster interrupt if the condition occurs. Note that neither of these two events have a respective Hold register associated with them, since the detection time is less than one line cycle.

The calculation engine keeps track of a trailing mean square of the input voltage, as defined by the following equation:

EQUATION 7-1:

$$V_{SA} = \frac{2 \times f_{LINE}}{f_{SAMPLE}} \times \left[\sum_{n = -\frac{f_{SAMPLE}}{2 \times f_{LINE}} - 1}^{0} V_n^2 \right]$$

Therefore, at each data-ready occurrence, the value of V_{SA} is compared to the programmable threshold set in the Voltage Sag Limit register and Voltage Surge Limit register to determine if a flag should be set. If either of these events are mapped to either the Event1 or Event2 pin, a logic-high interrupt will be given on these pins.

The Sag or Surge events can be used to quickly determine if a power failure has occurred in the system.

7.2.3 OVERCURRENT LIMIT

The Over Current Limit register is compared to the Current RMS register. When the threshold is passed, the corresponding event flags and event pins (if mapped) are set.

7.2.4 OVERPOWER LIMIT

The Over Power Limit register is compared to the Active Power register. When the threshold is passed, the corresponding event flags and event pins (if mapped) are set.

7.3 Voltage Low and Voltage High Threshold

The MCP39F511A device offers two additional registers for monitoring the input voltage, the Voltage Low Threshold and Voltage High Threshold registers.

When the input voltage crosses (high to low) the value held in the VoltageLowThreshold register, a write to the device EEPROM will be triggered (saving the Energy counters).

To avoid multiple writes to EEPROM, a hysteresis is implemented using VoltageHighThreshold register.

At power-up, when the input voltage crosses (low to high) the value held in the VoltageHighThreshold register, a read from the device EEPROM is triggered automatically (loading the energy counters). There are no event bits defined for this feature.

REGISTER 7-1: EVENT CONFIGURATION REGISTER

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	OVER-TEMP_PIN2	OVER-TEMP_PIN1	OVERTEMP_CL[2]	OVERTEMP_LA	OVER-TEMP_TST
bit 31							bit 24

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OVER-POW_PIN2	OVER-CUR_PIN2	VSURGE_PIN 2	VSAG_PIN2	OVER-POW_PIN1	OVERCUR_PIN1	VSURGE_PIN1	VSAG_PIN1
bit 23							bit 16
R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
EVENT2_MC[1]	EVENT1_MC[1]	—	—	OVERCUR_CL[2]	OVERPOW_CL[2]	VSUR_CL[2]	VSAG_CL[2]
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
VSUR_LA	VSAG_LA	OVER-POW_LA	OVERCUR_LA	VSUR_TST	VSAG_TST	OVERPOW_TST	OVERCUR_TST
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bits 31-29 **Unimplemented:** Read as ‘0’

bit 28 **OVERTEMP_PIN2:** Event pin 2 operation for the Overtemperature event
1 = Event mapped to Event2 pin only
0 = Event not mapped to a pin **(Default)**

bit 27 **OVERTEMP_PIN1:** Event pin 1 operation for the Overtemperature event
1 = Event mapped to Event1 pin only
0 = Event not mapped to a pin **(Default)**

bit 26 **OVERTEMP_CL:** Reset or clear bit for the Overtemperature event **(Note 2)**
1 = Event is cleared
0 = Event is not cleared **(Default)**

bit 25 **OVERTEMP_LA:** Latching control of the Overtemperature event
1 = Event is latched and needs to be cleared to be reset
0 = Event does not latch **(Default)**

bit 24 **OVERTEMP_TST:** Test control of the Overtemperature event
1 = Simulated event is turned on
0 = Simulated event is turned off **(Default)**

bit 23 **OVERPOW_PIN2:** Event pin 2 operation for the Overpower event
1 = Event mapped to Event2 pin only
0 = Event not mapped to a pin **(Default)**

bit 22 **OVERCUR_PIN2:** Event pin 2 operation for the Overcurrent event
1 = Event mapped to Event2 pin only
0 = Event not mapped to a pin **(Default)**

bit 21 **VSURGE_PIN2:** Event pin 2 operation for the Voltage Surge event
1 = Event mapped to Event2 pin only
0 = Event not mapped to a pin **(Default)**

bit 20 **VSAG_PIN2:** Event pin 2 operation for the Voltage Sag event
1 = Event mapped to Event2 pin only
0 = Event not mapped to a pin **(Default)**

REGISTER 7-1: EVENT CONFIGURATION REGISTER (CONTINUED)

bit 19 **OVERPOW_PIN1:** Event pin 1 operation for the Overpower event
1 = Event mapped to Event1 pin only
0 = Event not mapped to a pin **(Default)**

bit 18 **OVERCUR_PIN1:** Event pin 1 operation for the Overcurrent event
1 = Event mapped to Event1 pin only
0 = Event not mapped to a pin **(Default)**

bit 17 **VSURGE_PIN1:** Event pin 1 operation for the Voltage Surge event
1 = Event mapped to Event1 pin only
0 = Event not mapped to a pin **(Default)**

bit 16 **VSAG_PIN1:** Event pin 1 operation for the Voltage Sag event
1 = Event mapped to Event1 pin only
0 = Event not mapped to a pin **(Default)**

bit 15 **EVENT2_MC:** Manual control over EVENT pin 2 (**Note 1**)
1 = EVENT pin 2 set
0 = EVENT pin 2 clear

bit 14 **EVENT1_MC:** Manual control over EVENT pin 1 (**Note 1**)
1 = EVENT pin 1 set
0 = EVENT pin 1 clear

bits 13-12 **Unimplemented:** Read as '0'

bit 11 **OVERCUR_CL:** Reset or clear bit for the Overcurrent event **(Note 2)**
1 = Event is cleared
0 = Event is not cleared **(Default)**

bit 10 **OVERPOW_CL:** Reset or clear bit for the Overpower event **(Note 2)**
1 = Event is cleared
0 = Event is not cleared **(Default)**

bit 9 **VSUR_CL:** Reset or clear bit for the Voltage Surge event **(Note 2)**
1 = Event is cleared
0 = Event is not cleared **(Default)**

bit 8 **VSAG_CL:** Reset or clear bit for the Voltage Sag event **(Note 2)**
1 = Event is cleared
0 = Event is not cleared **(Default)**

bit 7 **VSUR_LA:** Latching control of the Voltage Surge event
1 = Event is latched and needs to be cleared
0 = Event does not latch **(Default)**

bit 6 **VSAG_LA:** Latching control of the Voltage Sag event
1 = Event is latched and needs to be cleared
0 = Event does not latch **(Default)**

bit 5 **OVERPOW_LA:** Latching control of the Overpower event
1 = Event is latched and needs to be cleared
0 = Event does not latch **(Default)**

bit 4 **OVERCUR_LA:** Latching control of the Overcurrent event
1 = Event is latched and needs to be cleared
0 = Event does not latch **(Default)**

bit 3 **VSUR_TST:** Test control of the Voltage Surge event
1 = Simulated event is turned on
0 = Simulated event is turned off **(Default)**

bit 2 **VSAG_TST:** Test control of the Voltage Sag event
1 = Simulated event is turned on
0 = Simulated event is turned off **(Default)**

bit 1 **OVERPOW_TST:** Test control of the Overpower event
1 = Simulated event is turned on
0 = Simulated event is turned off **(Default)**

REGISTER 7-1: EVENT CONFIGURATION REGISTER (CONTINUED)

bit 0 **OVERCUR_TST:** Test control of the Overcurrent event
1 = Simulated event is turned on
0 = Simulated event is turned off **(Default)**

Note 1: Manual control is possible only when no event is mapped to the pin.

2: Writing a 1 to the Clear bit clears the event, either real or simulated through test bits, and then returns to a state of 0.

8.0 PULSE WIDTH MODULATION (PWM)

8.1 Overview

The PWM output pin gives up to a 10-bit resolution of a pulse-width modulated signal. The PWM output is controlled by an internal timer inside the MCP39F511A device, F_{TIMER} described in this section, with a base frequency of 16 MHz. The base period is defined as P_{TIMER} and is 1/[16 MHz]. This 16 MHz time base is fixed due to the 4 MHz internal oscillator or 4 MHz external crystal.

The output of the PWM is active only when **PWM_CNTRL** bit in System Configuration register is set. The PWM output is turned off when the **PWM_CNTRL** bit is cleared.

The PWM output (Figure 8-2) has a time base (period) and a time that the output stays high (duty cycle). The frequency of the PWM is the inverse of the period (1/period).

There are two registers that control the PWM output, PWM period and PWM duty cycle.

The 8-bit PWM Period is controlled by a 16-bit register that contains the period bits and also the prescaler bits. The PWM Period bits are the most significant eight bits in the register, and the prescaler value is represented by the least two significant bits. These two values together create the PWM Period; see Figure 8-1.

The 10-bit PWM duty cycle is controlled by a 16-bit register where the most eight significant bits are the 8 MSb and the 2 LSb, corresponding to the 2 LSbs of the 10-bit value.

An example of the register's values are shown here with 255 for PWM frequency (8-bit value) and 1023 for the Duty cycle (10-bit value), prescaler set to divide by 16 (1:0).

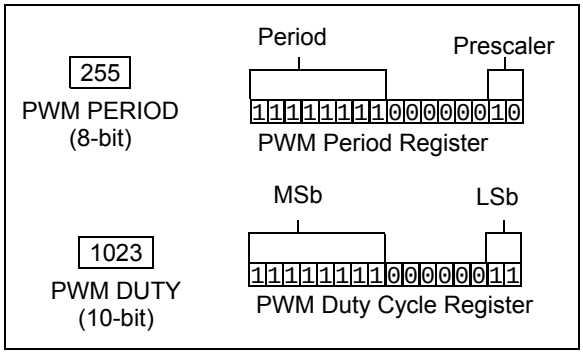


FIGURE 8-1: *PWM Period and Duty-Cycle Registers.*

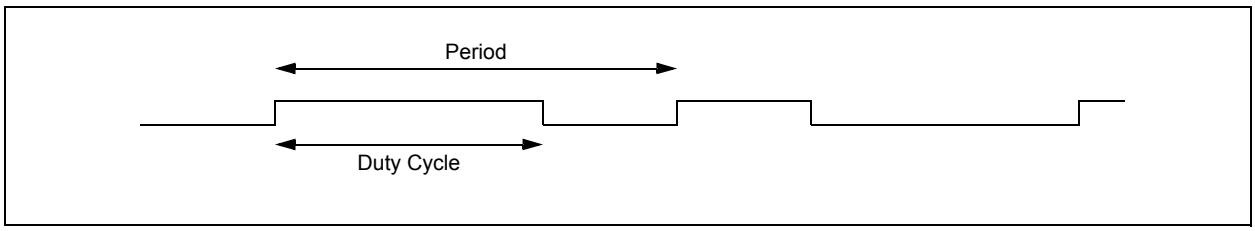


FIGURE 8-2: *PWM Output.*

8.2 PWM Period

The PWM period is specified by writing the PWM Period bits of the PWM Period register. The PWM period can be calculated using Equation 8-1.

EQUATION 8-1:

$$PWM\ Period = [(PWM\_Frequency) + 1] \times 2 \times P_{TIMER} \times (Prescale\ Value)$$

The PWM Period is defined as 1/[PWM Frequency]. When P_{TIMER} is equal to PWM Period, the following two events occur on the next increment cycle:

- The PWM timer is cleared
- The PWM pin is set. Exception: If the PWM Duty Cycle equals 0%, the PWM pin will not be set.

8.3 PWM Duty Cycle

The PWM duty cycle is specified by writing to the PWM Duty Cycle register. Up to 10-bit resolution is available. The PWM Duty Cycle register contains the eight MSbs and the two LSbs. The following equations are used to calculate the PWM duty cycle as a percentage or as time:

EQUATION 8-2:

$$PWM\ Duty\ Cycle\ (\%) = (PWM\_DUTY\ CYCLE>)/(4 \times PWM\_FREQUENCY)$$

$$PWM\ Duty\ Cycle\ (time\ in\ s) = (PWM\_DUTY\_CYCLE) \times PWM\_TIMER\_PERIOD/2 \times (Prescale\ Value)$$

PWM duty cycle can be written to at any time, but the duty cycle value is not latched until after a period is complete.

The PWM registers and a two-bit internal latch are used to double-buffer the PWM duty cycle. This double-buffering is essential for glitch-less PWM operation.

The maximum PWM resolution (bits) for a given PWM frequency is shown in Equation 8-3.

EQUATION 8-3: MAXIMUM PWM RESOLUTION BASED ON A FUNCTION OF PWM FREQUENCY

$$PWM\ Resolution\ (max) = \frac{\log\left(\frac{2 \cdot F_{TIMER}}{F_{PWM}}\right)}{\log(2)} bits$$

Note: If the PWM duty cycle value is longer than the PWM period, the PWM pin will not be cleared.

TABLE 8-1: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS WITH PWM_TIMER_FREQ = 16 MHz (DEFAULT)

PWM Frequency	1.95 kHz	31.25 kHz	62.5 kHz	125 kHz	2.67 MHz	4 MHz
Timer Prescaler	16	1	1	1	1	1
PWM Frequency Value	FFh	FFh	7Fh	3Fh	02h	01h
Maximum Resolution (bits)	10	10	9	4	3	2

REGISTER 8-1: PWM PERIOD REGISTER

R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
PWM_P<7:0>							
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	PRE<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **PWM_P<7:0>:** 8-bit PWM period value

bit 7-2 **Unimplemented:** Read as ‘0‘

bit 1-0 **PRE<1:0>:** PWM Prescaler
11 = Unused
10 = 1:16
01 = 1:4
00 = 1:1 **(Default)**

REGISTER 8-2: PWM DUTY-CYCLE REGISTER

R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DUTY<9:2>							
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	DUTY<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **DUTY<9:2>:** Upper 8 bits of 10-bit duty cycle value

bit 7-2 **Unimplemented:** Read as ‘0‘

bit 1-0 **DUTY<1:0>:** Lower 2 bits of 10-bit duty cycle value

9.0 MCP39F511A CALIBRATION

9.1 Overview

Calibration compensates for the ADC gain error, component tolerances and overall noise in the system. The device provides an on-chip calibration algorithm that allows simple system calibration to be performed quickly. The excellent analog performance of the A/D converters on the MCP39F511A allows for a single-point calibration and a single calibration command to achieve accurate measurements in AC mode. In DC mode, offset calibration is usually required.

Calibration can be done by either using the predefined Auto-Calibration commands, or by writing directly to the calibration registers. If additional calibration points are required (AC offset, phase compensation, DC offset), the corresponding calibration registers are available to the user and will be described separately in this section.

9.2 Calibration Order

The proper steps for calibration need to be maintained.

Here is a summary on the order of calibration steps:

In AC mode

1. Line Frequency Calibration
2. Gain Calibration at PF=1
3. Phase Calibration at PF=0.5 (optional)
4. Reactive Gain Calibration at PF=0.5

In DC mode

1. Offset Calibration
2. Gain Calibration

9.3 Single-Point Gain Calibrations at Unity Power Factor

When using the device in AC mode with the high-pass filters turned on, most offset errors are removed and only a single-point gain calibration is required.

Setting the gain registers to properly produce the desired outputs can be done manually by writing to the appropriate register. The alternative method is to use the auto-calibration commands described in this section.

9.3.1 USING THE AUTO-CALIBRATION GAIN COMMAND

By applying stable reference voltages and currents that are equivalent to the values that reside in the target Calibration Current, Calibration Voltage and Calibration Active Power registers, the `Auto-Calibration Gain` command can then be issued to the device.

After a successful calibration (response = ACK), a `Save Registers to Flash` command can then be issued to save the calibration constants calculated by the device.

The following registers are set when the `Auto-Calibration Gain` command is issued:

AC mode

- Gain Current RMS
- Gain Voltage RMS
- Gain Active Power

DC Mode

- DC Gain Current RMS
- DC Gain Voltage RMS
- DC Gain Active Power

When this command is issued, the MCP39F511A attempts to match the expected values to the measured values for all three output quantities by changing the gain register based on the following formula:

EQUATION 9-1:

$$GAIN_{NEW} = GAIN_{OLD} \bullet \frac{Expected}{Measured}$$

The same formula applies for voltage RMS, current RMS and active power. Since the gain registers for all three quantities are 16-bit numbers, the ratio of the expected value to the measured value (which can be modified by changing the Range register) and the previous gain must be such that the equation yields a valid number. Here the limits are set to be from 25,000 to 65,535. A new gain within this range for all three limits will return an ACK for a successful calibration, otherwise the command returns a NAK for a failed calibration attempt.

It is the user's responsibility to ensure that the proper range settings, PGA settings and hardware design settings are correct to allow for successful calibration using this command.

The value of the Thermistor Voltage register is automatically transfered to the Ambient Temperature Reference Voltage register after executing the command. This value is used internally by the temperature compensation algorithm, if enabled.

9.3.2 EXAMPLE OF RANGE SELECTION FOR VALID CALIBRATION

In this example, the user applies a calibration current of 1A to an uncalibrated system. The indicated value in the Current RMS register is 2300 with the system's specific shunt value, PGA gain, etc. The user expects to see a value of 1000 in the Current RMS register when 1A current is applied, meaning 1.000A with 1 mA resolution. Other given values are:

- The existing value for gain current RMS is 33480
- The existing value for Range is 12

By using Equation 9-1, the calculation for $Gain_{NEW}$ yields:

EQUATION 9-2:

$$GAIN_{NEW} = GAIN_{OLD} \times \frac{Expected}{Measured} = 33480 \times \frac{1000}{2300} = 14556$$

$$14556 < 25,000$$

When using the `Auto-Calibration Gain` command, the result would be a failed calibration or a NAK returned form the MCP39F511A, because the resulting $Gain_{NEW}$ is less than 25,000.

The solution is to use the Range register to bring the measured value closer to the expected value, such that a new gain value can be calculated within the limits specified above.

The Range register specifies the number of right-bit shifts (equivalent to divisions by 2) after the multiplication with the Gain Current RMS register. Refer to **Section 5.0 "Calculation Engine (CE) Description"** for information on the Range register.

Incrementing the Range register by 1 unit, an additional right-bit shift or ÷2 is included in the calculation. Increasing the current range from 12 to 13 yields the new measured Current RMS register value of 2300/2 = 1150. The expected (1000) and measured (1150) are much closer now, so the expected new gain should be within the limits:

EQUATION 9-3:

$$GAIN_{NEW} = GAIN_{OLD} \times \frac{Expected}{Measured} = 33480 \times \frac{1000}{1150} = 29113$$

$$25,000 < 29113 < 65535$$

The resulting new gain is within the limits and the device successfully calibrates current RMS and returns an ACK.

Notice that the range can be set to 14 and the resulting new gain will still be within limits ($Gain_{NEW}$ = 58226). However, since this gain value is close to the limit of the 16-bit Gain register, variations from system to system (component tolerances, etc.) might create a scenario where the calibration is not successful on some units and there would be a yield issue. The best approach is to choose a range value that places the new gain in the middle of the bounds of the gain registers described above.

In a second example, when applying 1A, the user expects an output of 1.0000A with 0.1 mA resolution. The example is starting with the same initial values:

EQUATION 9-4:

$$GAIN_{NEW} = GAIN_{OLD} \times \frac{Expected}{Measured} = 33480 \times \frac{10000}{2300} = 145565$$

$$145565 > 65535$$

The $Gain_{NEW}$ is much larger than the 16-bit limit of 65535, so fewer right-bit shifts must be introduced to get the measured value closer to the expected value. The user needs to compute the number of bit shifts that will give a value lower than 65535. To estimate this number:

EQUATION 9-5:

$$\frac{145565}{65535} = 2.2$$

2.2 rounds to the closest integer value of 2. The range value changes to 12 – 2 = 10; there are 2 less right-bit shifts.

The new measured value will be 2300 x 2^2 = 9200.

EQUATION 9-6:

$$GAIN_{NEW} = GAIN_{OLD} \times \frac{Expected}{Measured} = 33480 \times \frac{10000}{9200} = 36391$$

$$25,000 < 36391 < 65535$$

The resulting new gain is within the limits and the device successfully calibrates current RMS and returns an ACK.

9.4 Calibrating the Phase Compensation Register

Phase compensation is provided to adjust for any phase delay between the current and voltage path. This procedure requires sinusoidal current and voltage waveforms, with a significant phase shift between them, and significant amplitudes. The recommended displacement power factor for calibration is 0.5. The procedure for calculating the phase compensation register is as follows:

1. Determine what the difference is between the angle corresponding to the measured power factor (PF_{MEAS}) and the angle corresponding to the expected power factor (PF_{EXP}), in degrees.

EQUATION 9-7:

$$PF_{MEAS} = \frac{Value\ in\ PowerFactor\ Register}{32768}$$

$$ANGLE_{MEAS}(^{\circ}) = acos(PF_{MEAS}) \times \frac{180}{\Pi}$$

$$ANGLE_{EXP}(^{\circ}) = acos(PF_{EXP}) \times \frac{180}{\Pi}$$

2. Convert this from degrees to the resolution provided in Equation 9-8. There are 56 samples per line cycle. One line cycle is 360 degrees, so for each sample the angle is 360 degrees/56 samples = 6.42857 degrees/sample. Since the phase compensation has a bit of sign, the maximum angle error that can be compensated is only half, that is ±3.21 degrees. Converting the angle to 8-bit resolution gives 256/6.42857 degrees = 39.82 with 40 as an approximation.

EQUATION 9-8:

$$\Phi = (ANGLE_{MEAS} - ANGLE_{EXP}) \times 40$$

3. Combine this additional phase compensation to whatever value is currently in the phase compensation, and update the register. Equation 9-9 should be computed in terms of an 8-bit 2's complement-signed value. The 8-bit result is placed in the least significant byte of the 16-bit Phase Compensation register.

EQUATION 9-9:

$$PhaseCompensation_{NEW} = PhaseCompensation_{OLD} + \Phi$$

Based on Equation 9-9, the maximum angle in degrees that can be compensated is approximately ±3.2 degrees. If a larger phase shift is required, contact your local Microchip sales office.

9.5 Offset/No-Load Calibrations

During offset calibrations, it is recommended that no line voltage or current be applied to the system. The system should be in a no-load condition.

9.5.1 AC OFFSET CALIBRATION

There are three registers associated with the AC Offset Calibration:

- Offset Current RMS
- Offset Active Power
- Offset Reactive Power

When computing the AC offset values, the respective gain and range registers should be taken into consideration according to the block diagrams in Figures 5-2 and 5-4.

After a successful offset calibration, a `Save Registers to Flash` command can then be issued to save the calibration constants calculated by the device.

9.5.2 DC OFFSET CALIBRATION

In DC applications, the high-pass filters on the current and voltage channels are turned off. There are two registers associated with the DC Offset Calibration:

- DC Offset Current RMS
- DC Offset Active Power

In addition to that, full access to the ADC's internal 24-bit Offset registers is provided.

REGISTER 9-1: OFFCAL_MSB

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
OFFCAL_CH1_MSB<7:0>							
bit 15							bit 8

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
OFFCAL_CH0_MSB<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **OFFCAL_CH1_MSB<7:0>:** MSB of the 24-bit offset for CH1 (voltage channel)

bit 7-0 **OFFCAL_CH0_MSB<7:0>:** MSB of the 24-bit offset for CH0 (current channel)

REGISTER 9-2: OFFCAL_CH0

R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-1
OFFCAL_CH0<15:8>							
bit 15							bit 8

R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OFFCAL_CH0<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **OFFCAL_CH0<15:0>:** Lower 16-bit of the 24-bit offset for CH0 (current channel)

REGISTER 9-3: OFFCAL_CH1

R/W-1	R/W-1	R/W-1	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0
OFFCAL_CH1<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OFFCAL_CH1<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **OFFCAL_CH1<15:0>:** Lower 16-bit of the 24-bit offset for CH1 (voltage channel)

Note 1: The 24-bit two's complement MSb first coding values are calculated internally using the corresponding byte from the OFFCAL_MSB register and OFFCAL_CHn 16-bit values. The result is added to the output code of the corresponding channel bit-by-bit.

9.6 Calibrating the Line Frequency Register

The Line Frequency register contains a 16-bit number with a value equivalent to the input-line frequency as it is measured on the voltage channel. When in DC mode, this calculation is turned off and the register will be equal to zero.

The measurement of the line frequency is only valid from 45 to 65 Hz.

9.6.1 USING THE AUTO-CALIBRATE FREQUENCY COMMAND

By applying a stable reference voltage with a constant line frequency that is equivalent to the value that resides in the Line Frequency Ref, the `Auto-Calibrate Frequency` command can then be issued to the device.

After a successful calibration (response = ACK), a `Save Registers to Flash` command can then be issued to save the calibration constants calculated by the device. Issuing the command in DC mode generates a NAK response.

The following register is set when the `Auto-Calibrate Frequency` command is issued:

• Gain Line Frequency

Note that the command is only required when running off the internal oscillator. The formula used to calculate the new gain is shown in Equation 9-1.

9.7 Temperature Compensation

MCP39F511A measures the indication of the temperature sensor and uses the value to compensate the temperature variation of the shunt resistance and the frequency of the internal RC oscillator.

The same formula applies for line frequency, current RMS, active power and reactive power. The temperature compensation coefficient depends on the 16-bit unsigned integer value of the corresponding compensation register.

EQUATION 9-10:

$$y = x \times (1 + c \times (T - T_{CAL}))$$

$$c = \frac{TemperatureCompensation\ Register}{2^M}$$

Where:

- x = Uncompensated output (corresponding to line frequency, current RMS, active power and reactive power)
- y = Compensated output
- c = Temperature compensation coefficient (depending on the shunt's temperature coefficient of resistance or on the internal RC oscillator temperature frequency drift). There are six registers two for line frequency compensation, two for current compensation and two for power compensation (active and reactive). TempPosComp registers are used when T is greater than $T_{CAL.}$ TempNegComp registers are used when T is less than $T_{CAL.}$
- T = Thermistor voltage (in 10-bit ADC units)
- T_{CAL} = Ambient temperature reference voltage. It should be set at the beginning of the calibration procedure, by reading the thermistor voltage and writing its value to the ambient temperature reference voltage register. The auto-calibration gain command does this automatically.

At the calibration temperature, the effect of the compensation coefficients is null. The coefficients need to be tuned when the difference between the calibration temperature and the device temperature is significant. It is recommended to use the default values as starting points.

9.8 EMI Input Filter Compensation

The typical EMI input filter location in a power supply is between the AC inlet and the meter, and as a result the components of the filter (capacitors and inductors) affect the accuracy of the meter.

The current RMS measurement is affected by the input capacitor and the exact value depends on the frequency and the input voltage.

The current flowing through the input capacitor can be compensated using the InCapCurrentComp register (enabled in AC mode only).

EQUATION 9-11:

$$y = x + \frac{c \times f \times V}{2^M}$$

Where:

- x = Uncompensated current RMS
- y = Compensated current RMS
- c = Compensation value found in InCapCurrentComp register
- f = Measured frequency
- V = Measured voltage RMS
- M = INCAPCURRENT value found in RANGEVDROPINCAPCOMP register

EXAMPLE 9-1:

A 1 μF input capacitor at 220V [rms], 50 Hz corresponds to an offset current of . 0.0691A [rms].

$$c = \frac{(y - x) \times 2^M}{(f \times V)}$$

Where

- y - x = offset current
- M = 32 (default value)
- c = 691 * 4294967296 / (50000 * 2200)
- c = 26980, this is the value that should be written to the InCapCurrentComp register

The PCB traces and the inductors resistance cause a voltage drop when high currents are flowing through them.

The higher the current is, the higher the error of the voltage RMS measurement.

This voltage drop can be compensated using the VoltageDropComp register (enabled in DC and AC mode).

EQUATION 9-12:

$$y = x + \frac{c \times I}{2^M}$$

Where:

- x = Uncompensated voltage RMS
- y = Compensated voltage RMS
- c = Compensation value found in VoltageDropComp register
- I = Measured current RMS
- M = VOLTAGEDROP value found in RANGEVDROPINCAPCOMP register

EXAMPLE 9-2:

A 0.1 Ω resistor at 10A [rms] corresponds to an offset voltage of 1V [rms].

$$c = \frac{(y - x) \times 2^M}{I}$$

Where:

- y -x = offset value
- M = 28 (default value)
- c = 10 * 268435456 / 100000
- c = 26843, this is the value that should be written to the VoltageDropComp register

REGISTER 9-4: VOLTAGEDROPCOMP

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
VOLTAGEDROPCOMP<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
VOLTAGEDROPCOMP<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **VOLTAGEDROPCOMP<15:0>:** Voltage Drop Compensation register

REGISTER 9-5: INCAPCURRENTCOMP

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INCAPCURRENTCOMP<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INCAPCURRENTCOMP<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **INCAPCURRENTCOMP<15:0>:** Input Capacitor Current Compensation register

REGISTER 9-6: RANGEVDROPINCAPCOMP

R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0
VOLTAGEDROP<7:0>							
bit 15							bit 8

R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INCAPCURRENT<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **VOLTAGEDROP<7:0>:** Sets the number of right-bit shifts for the VoltageDropComp register

bit 7-0 **INCAPCURRENT<7:0>:** Sets the number of right-bit shifts for the InCapCurrentComp register

9.9 Retrieving Factory Default Calibration Values

After user calibration and a `Save to Flash` command has been issued, it is possible to retrieve the factory default calibration values. This can be done by writing 0xA5A5 to the calibration delimiter register, issuing a `Save to Flash`, and then resetting the part. This procedure will retrieve all factory default calibration values and will remain in this state until calibration has been performed again, and a `Save to Flash` command has been issued.

10.0 EEPROM

The data EEPROM is organized as 16-bit wide memory. Each word is directly addressable, and is readable and writable across the entire V_{DD} range. The MCP39F511A device has 256 16-bit words of EEPROM that is organized in 32 pages for a total of 512 bytes.

There are three commands that support access to the EEPROM array.

- `EEPROM Page Read` (0x42)
- `EEPROM Page Write` (0x50)
- `EEPROM Bulk Erase` (0x4F)

TABLE 10-1: EXAMPLE EEPROM COMMANDS AND DEVICE RESPONSE

Command	Command ID BYTE 0	BYTE 1-N	# Bytes	Successful Response
`Page Read EEPROM`	0x42	PAGE	2	ACK, NoB, data, checksum
`Page Write EEPROM`	0x50	PAGE + DATA (16)	18	ACK
`Bulk Erase EEPROM`	0x4F	None	1	ACK

TABLE 10-2: MCP39F511A EEPROM ORGANIZATION

Page		00	02	04	06	08	0A	0C	0E
0	0000	0000	0000	0000	0000	0000	0000	0000	0000
1	0010	0000	0000	0000	0000	0000	0000	0000	0000
2	0020	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
3	0030	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
4	0040	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
5	0050	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
6	0060	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
7	0070	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
8	0080	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
9	0090	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
10	00A0	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
11	00B0	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
12	00C0	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
13	00D0	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
14	00E0	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
15	00F0	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
16	0100	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
17	0110	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
18	0120	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
19	0130	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
20	0140	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
21	0150	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
22	0160	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
23	0170	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
24	0180	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
25	0190	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
26	01A0	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
27	01B0	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
28	01C0	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
29	01D0	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
30	01E0	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF

Note 1: Pages 0 and 1 are reserved for saving the energy counters at power-down. The locations are accessible, but writing to them may interfere with the energy counters functionality.

TABLE 10-2: MCP39F511A EEPROM ORGANIZATION

Page		00	02	04	06	08	0A	0C	0E
31	01F0	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF

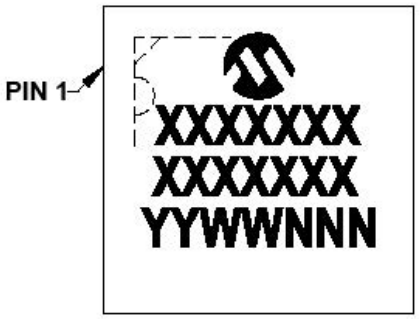
Note 1: Pages 0 and 1 are reserved for saving the energy counters at power-down. The locations are accessible, but writing to them may interfere with the energy counters functionality.

NOTES:

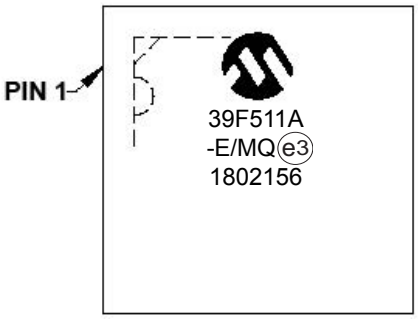
11.0 PACKAGING INFORMATION

11.1 Package Marking Information

28-Lead QFN (5x5x0.9 mm)



Example

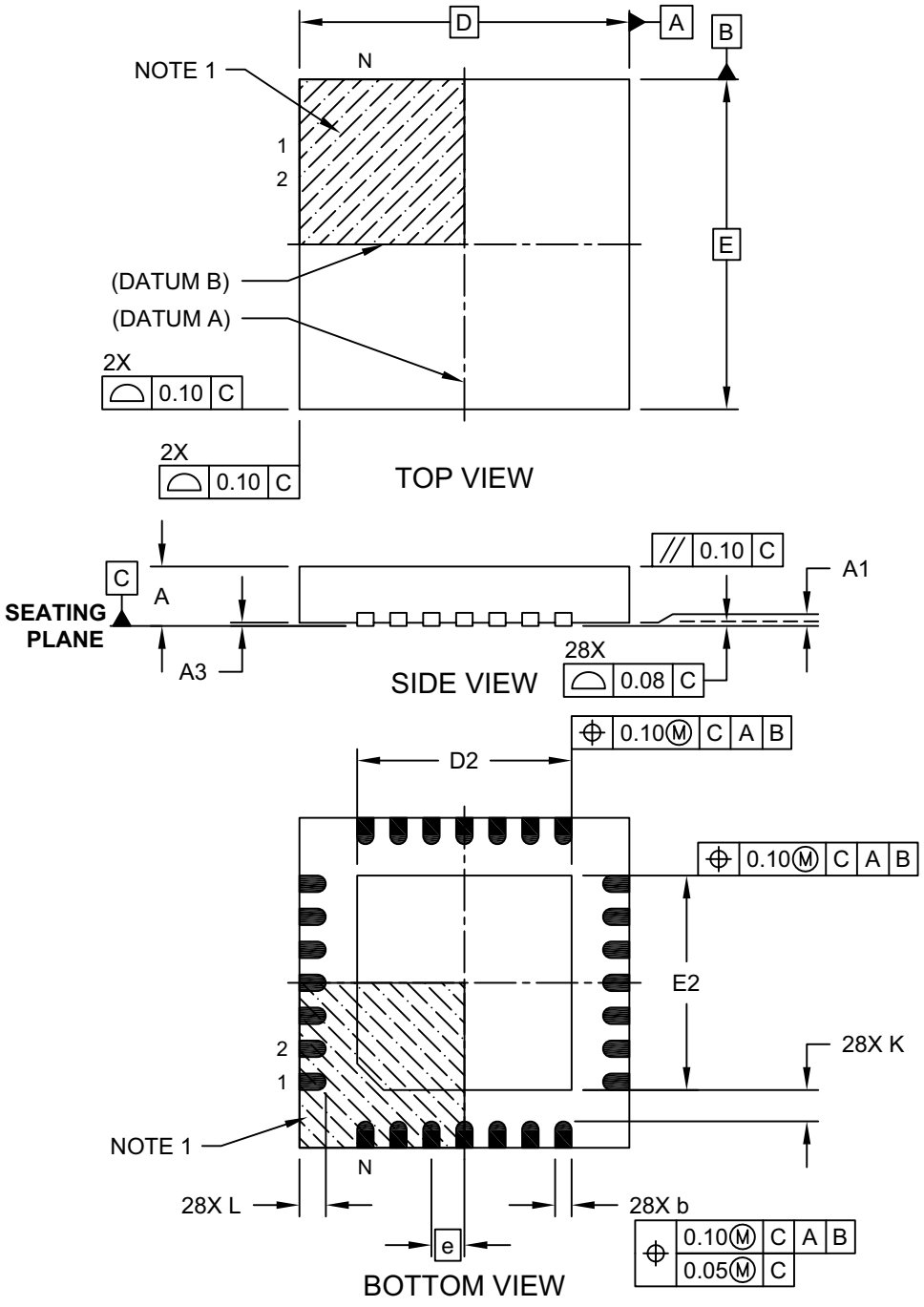


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

28-Lead Plastic Quad Flat, No Lead Package (MQ) – 5x5x0.9 mm Body [QFN or VQFN]

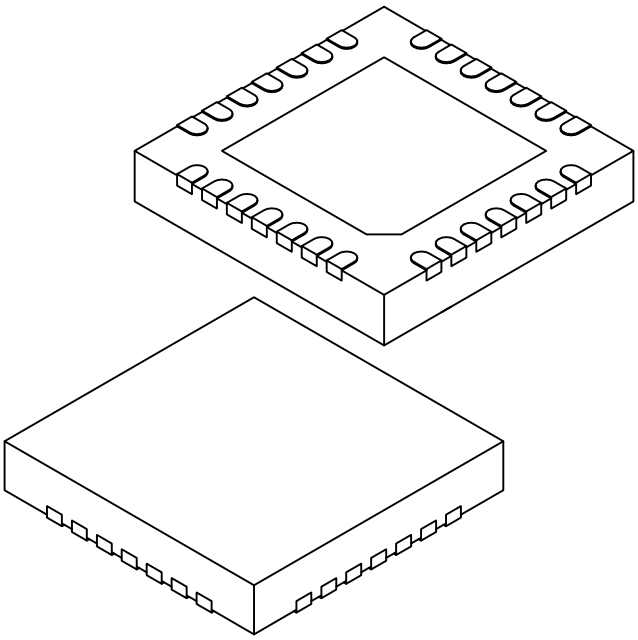
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-140C Sheet 1 of 2

28-Lead Plastic Quad Flat, No Lead Package (MQ) – 5x5x0.9 mm Body [QFN or VQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		5.00 BSC	
Exposed Pad Width	E2	3.15	3.25	3.35
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.15	3.25	3.35
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.35	0.40	0.45
Contact-to-Exposed Pad	K	0.20	-	-

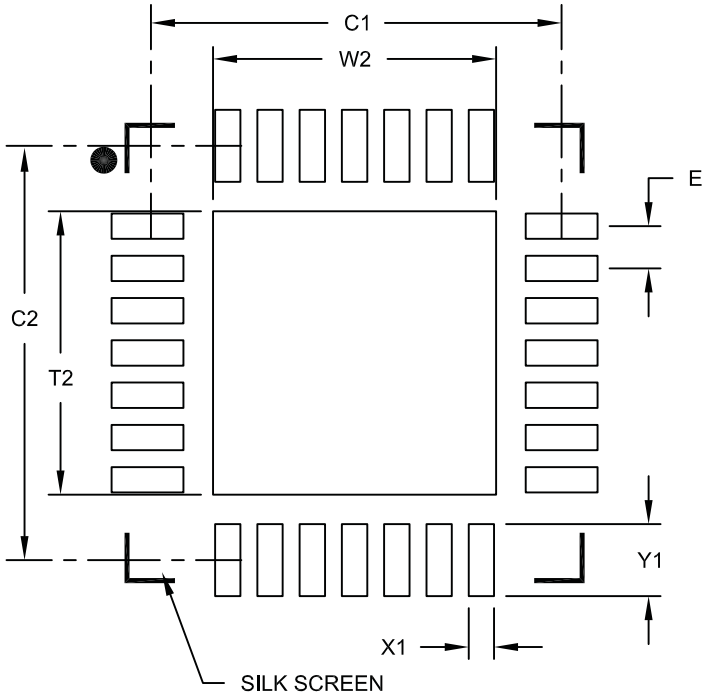
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-140C Sheet 2 of 2

28-Lead Plastic Quad Flat, No Lead Package (MQ) – 5x5 mm Body [QFN] Land Pattern With 0.55 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	W2			3.35
Optional Center Pad Length	T2			3.35
Contact Pad Spacing	C1		4.90	
Contact Pad Spacing	C2		4.90	
Contact Pad Width (X28)	X1			0.30
Contact Pad Length (X28)	Y1			0.85

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2140A

APPENDIX A: REVISION HISTORY

Revision A (June 2018)

- Original release of this document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X](1)	X	/XX
Device	Tape and Reel	Temperature Range	Package

Device:	MCP39F511A:Power-Monitoring IC with Calculation and Energy Accumulation
Tape and Reel Option:	Blank = Standard packaging (tube or tray) T = Tape and Reel (1)
Temperature Range:	E = -40°C to +125°C
Package:	MQ = Plastic Quad Flat, No Lead Package – 5x5x0.9 mm body (QFN), 28-lead

Examples:

a) MCP39F511A-E/MQ: Extended temperature, 28LD 5x5 QFN package

b) MCP39F511AT-E/MQ: Tape and Reel, Extended temperature, 28LD 5x5 QFN package

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip sales office for package availability for the Tape and Reel option.

NOTES:

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