24-Bit, 8.5 mW, 115 dB, 32 kHz ADC

Known Good Die

AD7766-2-KGD

FEATURES

- Oversampled successive approximation (SAR) architecture
- High performance ac and dc accuracy, low power 115.5 dB
  - typical dynamic range, 32 kHz output data rate (ODR)
  - −112 dB typical total harmonic distortion (THD)
- Exceptionally low power
  - 8.5 mW, 32 kHz ODR
  - High dc accuracy
  - 24 bits, no missing codes (NMC)
  - Integral nonlinearity (INL): ±6 ppm (typical), ±15 ppm (maximum)
- Low temperature drift
  - Zero error drift: 15 nV/°C typical
  - Gain error drift: 0.4 ppm/°C typical
- On-chip low-pass FIR filter
  - Linear phase response
  - Pass-band ripple: ±0.005 dB maximum
  - Stop-band attenuation: 100 dB minimum
- 2.5 V supply with 1.8 V/2.5 V/3 V/3.6 V logic interface options
- Flexible interfacing options
  - Synchronization of multiple devices
  - Daisy-chain capability
  - Power-down function
- Temperature range: −40°C to +105°C

APPLICATIONS

- Low power PCI/USB data acquisition systems
- Low power wireless acquisition systems
- Vibration analysis
- Instrumentation
- High precision medical acquisition

GENERAL DESCRIPTION

The AD7766-2-KGD is a high performance, 24-bit, oversampled SAR analog-to-digital converter (ADC). The AD7766-2-KGD combines the benefits of a large dynamic range and input bandwidth, consuming 8.5 mW power.

Ideal for ultralow power data acquisition (such as PCI-based and USB-based systems), the AD7766-2-KGD provides 24-bit resolution. The combination of exceptional signal-to-noise ratio (SNR), wide dynamic range, and outstanding dc accuracy make the AD7766-2-KGD ideally suited for measuring small signal changes over a wide dynamic range. This device is particularly suitable for applications where small changes on the input are measured on larger ac or dc signals. In such an application, the AD7766-2-KGD accurately gathers both ac and dc information.

FUNCTIONAL BLOCK DIAGRAM

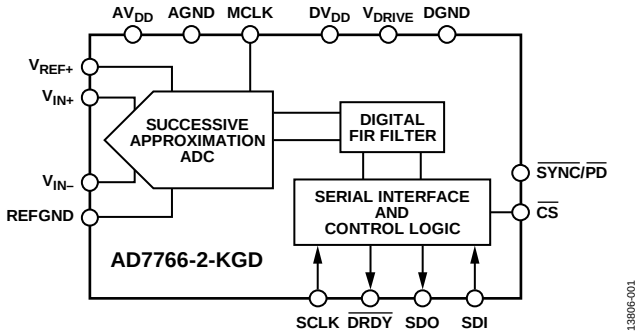

Figure 1.

The AD7766-2-KGD includes an on-board digital filter (complete with linear phase response) that acts to eliminate out-of-band noise by filtering the oversampled input voltage. The oversampled architecture also reduces front-end antialiasing requirements. Other features of the AD7766-2-KGD include a $\overline{\text{SYNC}}/\overline{\text{PD}}$ (synchronization/power-down) pin that allows synchronizing of multiple AD7766-2-KGD devices or that powers down the AD7766-2-KGD. The addition of an SDI pin provides the option of daisy chaining multiple AD7766-2-KGD devices.

The AD7766-2-KGD operates from a 2.5 V supply using a 5 V reference. The device operates from −40°C to +105°C.

Additional application and technical information can be found in the AD7766-2 data sheet.

Known Good Die (KGD): this die is fully guaranteed to data sheet specifications.

RELATED DEVICES

Table 1. 24-Bit ADCs

Part No.	Description
AD7760	2.5 MSPS, 100 dB dynamic range,[1] on-board differential amp and reference buffer, parallel, variable decimation
AD7762/ AD7763	625 kSPS, 109 dB dynamic range,[1] on-board differential amp and reference buffer, parallel/serial, variable decimation
AD7764	312 kSPS, 109 dB dynamic range,[1] on-board differential amp and reference buffer, variable decimation (pin)
AD7765	156 kSPS, 112 dB dynamic range,[1] on-board differential amp and reference buffer, variable decimation (pin)
AD7767	128 kSPS, 109.5 dB,[1] 15 mW, 18-bit INL, serial interface
AD7767-1	64 kSPS 112.5 dB,[1] 10.5 mW, 18-bit INL, serial interface
AD7767-2	32 kSPS, 115.5 dB,[1] 8.5 mW, 18-bit INL, serial interface

[1] Dynamic range at maximum output data rate.

Rev. 0 Document Feedback

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TABLE OF CONTENTS

REVISION HISTORY

1/16—Revision 0: Initial Version

SPECIFICATIONS

AV_{DD} = DV_{DD} = 2.5 V ± 5%, V_{DRIVE} = 1.8 V to 3.6 V, V_{REF+} = 5 V, MCLK = 1 MHz, common-mode input = $V_{REF+}/2$, T_A = −40°C to +105°C, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OUTPUT DATA RATE (ODR)	Decimate by 32			32	kHz
ANALOG INPUT					
Differential Input Voltage	$V_{IN+} - V_{IN-}$			$\pm V_{REF+}$	V p-p
Absolute Input Voltage	V_{IN+}	−0.1		$+V_{REF+} + 0.1$	V
	V_{IN-}	−0.1		$+V_{REF+} + 0.1$	V
Common-Mode Input Voltage		$V_{REF+}/2 - 5\%$	$V_{REF+}/2$	$V_{REF+}/2 + 5\%$	V
Input Capacitance			22		pF
DYNAMIC PERFORMANCE	Decimate by 32, ODR = 32 kHz				
Dynamic Range	Shorted inputs	114	115.5		dB
Signal-to-Noise Ratio (SNR)	Full-scale input amplitude, 1 kHz tone	112	113.5		dB
Spurious-Free Dynamic Range (SFDR)	Full-scale input amplitude, 1 kHz tone		−128	−116	dB
Total Harmonic Distortion (THD)	Full-scale input amplitude, 1 kHz tone		−112	−103	dB
Intermodulation Distortion (IMD)	Tone A = 11.7 kHz, Tone B = 12.3 kHz				dB
Second-Order Terms			−137		dB
Third-Order Terms			−108		dB
DC ACCURACY	For all devices				
Resolution	No missing codes	24			Bits
Differential Nonlinearity	Guaranteed monotonic to 24 bits				
Integral Nonlinearity	16-bit linearity		±6	±15	ppm
Zero Error			20		µV
Gain Error			0.0075	0.075	% FS
Zero Error Drift			15		nV/°C
Gain Error Drift			0.4		ppm/°C
Common-Mode Rejection Ratio	50 Hz tone		−110		dB
DIGITAL FILTER RESPONSE					
Group Delay			37/ODR		µs
Settling Time (Latency)	Complete settling		74/ODR		µs
Pass-Band Ripple				±0.005	dB
Pass Band			0.453 × ODR		Hz
−3 dB Bandwidth			0.49 × ODR		Hz
Stop-Band Frequency			0.547 × ODR		Hz
Stop-Band Attenuation		100			dB
REFERENCE INPUT					
V_{REF+} Input Voltage		2.4		$2 \times AV_{DD}$	V
DIGITAL INPUTS (Logic Levels)					
Logic Low Voltage (V_{IL})		−0.3		$+0.3 \times V_{DRIVE}$	V
Logic High Voltage (V_{IH})		$0.7 \times V_{DRIVE}$		$V_{DRIVE} + 0.3$	V
Input Leakage Current				±1	µA/pin
Input Capacitance			5		pF
Master Clock Rate				1.024	MHz
Serial Clock Rate				$1/t_8$	Hz
DIGITAL OUTPUTS					
Data Format	Serial 24 bits, twos complement (MSB first)				
Logic Low Voltage (V_{OL})	Sink current (I_{SINK}) = +500 µA			0.4	V
Logic High Voltage(V_{OH})	Source current (I_{SOURCE}) = −500 µA	$V_{DRIVE} - 0.3$			V

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER REQUIREMENTS					
AV_{DD}	±5%		2.5		V
DV_{DD}	±5%		2.5		V
V_{DRIVE}		1.7	2.5	3.6	V
CURRENT SPECIFICATIONS	MCLK = 1.024 MHz				
Operational Current	32 kHz output data rate				
Analog Quiescent Current (AI_{DD})			1.3	1.5	mA
Digital Quiescent Current (DI_{DD})			1.37	1.86	mA
Reference Current (I_{REF})			0.35	0.425	mA
Static Current with MCLK Stopped					
AI_{DD}			0.9	1	mA
DI_{DD}			1	93	µA
Power-Down Mode Current					
AI_{DD}			0.1	6	µA
DI_{DD}			1	93	µA
POWER DISSIPATION	MCLK = 1.024 MHz				
Operational Power	32 kHz output data rate		8.5	10.5	mW

TIMING SPECIFICATIONS

AV_{DD} = DV_{DD} = 2.5 V ± 5%, V_{DRIVE} = 1.7 V to 3.6 V, V_{REF+} = 5 V, common-mode input = $V_{REF+}/2$, T_A = −40°C (T_{MIN}) to +105°C (T_{MAX}), unless otherwise noted. Sample tested during initial release to ensure compliance. All input signals are specified with rise time (t_R) = fall time (t_F) = 5 ns (10% to 90% of DV_{DD}) and timed from a voltage level of 1.7 V.

Table 3.

Parameter	Limit at t_{MIN}, t_{MAX}	Unit	Description
$\overline{DRDY}$ OPERATION			See Figure 2
t_1	510	ns typ	MCLK rising edge to $\overline{DRDY}$ falling edge
t_2[1]	100	ns min	MCLK high pulse width
t_3[1]	900	ns max	MCLK low pulse width
t_4	71	ns typ	MCLK rising edge to $\overline{DRDY}$ rising edge
t_5	492	ns typ	$\overline{DRDY}$ pulse width
t_{READ}	$t_{\overline{DRDY}} - t_5$	ns typ	$\overline{DRDY}$ low period, read data during this period
$t_{\overline{DRDY}}$	$32 \times t_{MCLK}$	ns typ	$\overline{DRDY}$ period
READ OPERATION			See Figure 3 and Figure 4
t_6	0	ns min	$\overline{DRDY}$ falling edge to $\overline{CS}$ setup time
t_7	6	ns max	$\overline{CS}$ falling edge to SDO tristate disabled
t_8	60	ns max	Data access time after SCLK falling edge (V_{DRIVE} = 1.7 V)
	50	ns max	Data access time after SCLK falling edge (V_{DRIVE} = 2.3 V)
	25	ns max	Data access time after SCLK falling edge (V_{DRIVE} = 2.7 V)
	24	ns max	Data access time after SCLK falling edge (V_{DRIVE} = 3.0 V)
t_9	10	ns min	SCLK falling edge to data valid hold time (V_{DRIVE} = 3.6 V)
t_{10}	10	ns min	SCLK high pulse width
t_{11}	10	ns min	SCLK low pulse width
t_{SCLK}	$1/t_8$	sec min	Minimum SCLK period (not shown in the timing figures)
t_{12}	6	ns max	Bus relinquish time after $\overline{CS}$ rising edge
t_{13}	0	ns min	$\overline{CS}$ rising edge to $\overline{DRDY}$ rising edge
READ OPERATION WITH $\overline{CS}$ LOW			See Figure 3
t_{14}	0	ns min	$\overline{DRDY}$ falling edge to data valid setup time
t_{15}	0	ns max	$\overline{DRDY}$ rising edge to data valid hold time
DAISY-CHAIN OPERATION			See Figure 5
t_{16}	1	ns min	SDI valid to SCLK falling edge setup time
t_{17}	2	ns max	SCLK falling edge to SDI valid hold time
$\overline{SYNC}/\overline{PD}$ OPERATION			See Figure 6
t_{18}	1	ns typ	$\overline{SYNC}/\overline{PD}$ falling edge to MCLK rising edge
t_{19}	20	ns typ	MCLK rising edge to $\overline{DRDY}$ rising edge going into $\overline{SYNC}/\overline{PD}$ mode
t_{20}	1	ns min	$\overline{SYNC}/\overline{PD}$ rising edge to MCLK rising edge
t_{21}	510	ns typ	MCLK rising edge to $\overline{DRDY}$ falling edge coming out of $\overline{SYNC}/\overline{PD}$ mode
$t_{SETTLING}$	2357	t_{MCLK}	Filter settling time (in MCLK periods) after a reset or power-down

[1] t_2 and t_3 allow a ~90% to 10% duty cycle to be used for the MCLK input, where the minimum is 10% for the clock high time and 90% for MCLK low time. The maximum MCLK frequency is 1.024 MHz.

Timing Diagrams

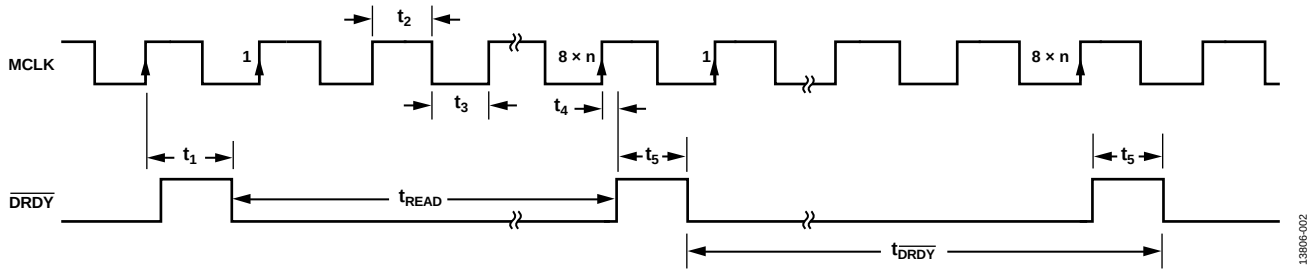

Figure 2. $\overline{DRDY}$ vs. MCLK Timing Diagram, n = 4 (Decimate by 32)

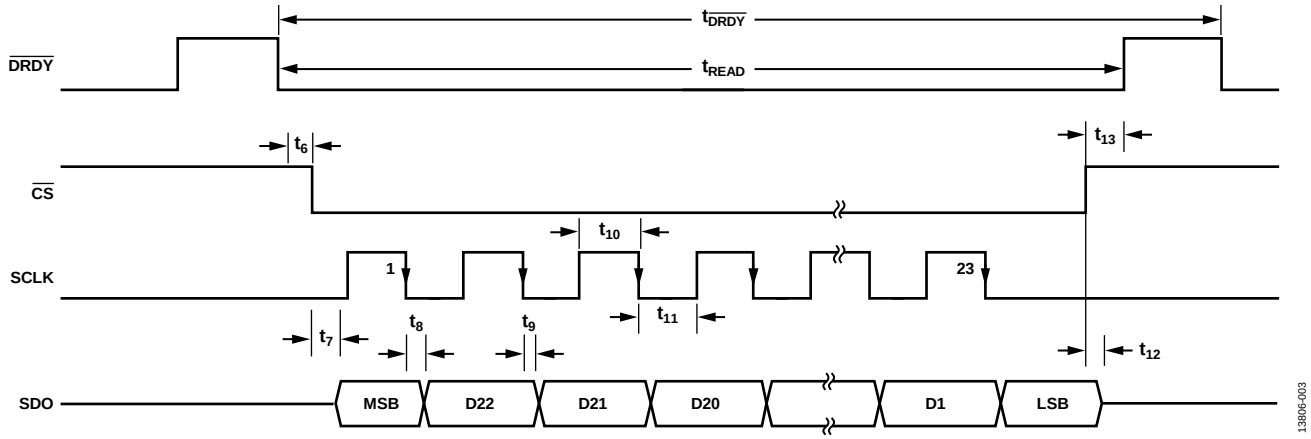

Figure 3. Serial Timing Diagram, Reading Data Using $\overline{CS}$

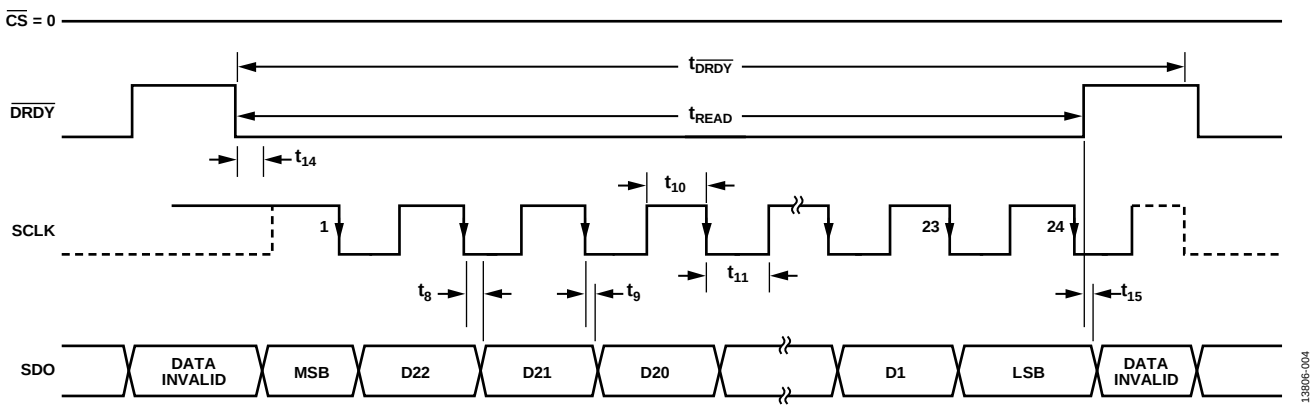

Figure 4. Serial Timing Diagram, Reading Data Setting $\overline{CS}$ Logic Low

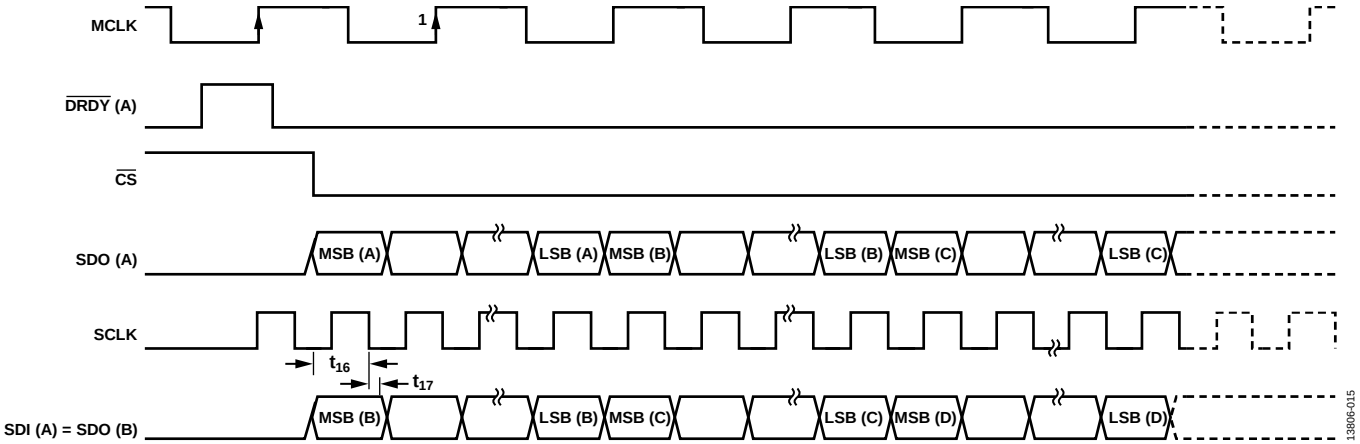

Figure 5. Daisy-Chain SDI Setup and Hold Timing

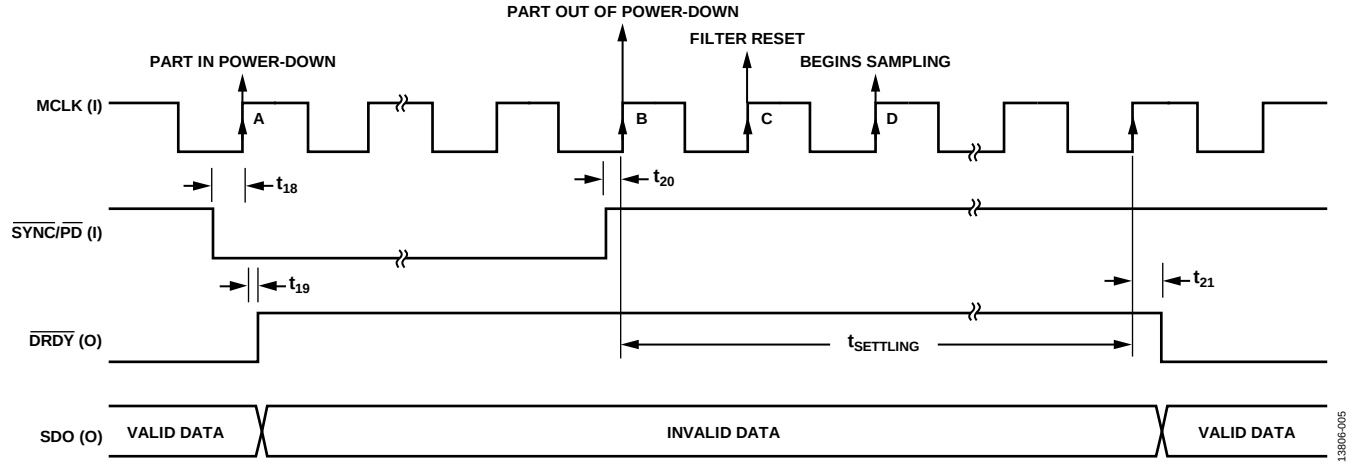

Figure 6. Reset, Synchronization, and Power-Down Timing

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
AV_{DD} to AGND	−0.3 V to +3 V
DV_{DD} to DGND	−0.3 V to +3 V
AV_{DD} to DV_{DD}	−0.3 V to +0.3 V
V_{REF+} to REFGND	−0.3 V to +7 V
REFGND to AGND	−0.3 V to +0.3 V
V_{DRIVE} to DGND	−0.3 V to +6 V
V_{IN+}, V_{IN-} to AGND	−0.3 V to V_{REF}+ + 0.3 V
Digital Inputs to DGND	−0.3 V to V_{DRIVE} + 0.3 V
Digital Outputs to DGND	−0.3 V to V_{DRIVE} + 0.3 V
AGND to DGND	−0.3 V to +0.3 V
Input Current to Any Pin Except Supplies[1]	±10 mA
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Electrostatic Discharge (ESD)	1 kV

[1] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

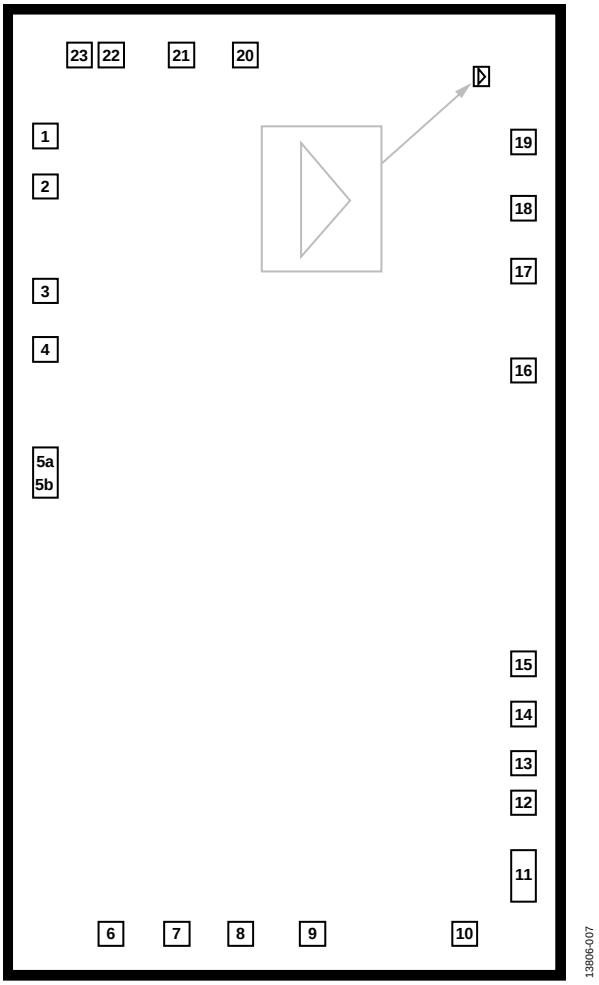

Figure 7. Pad Configuration

Table 5. Pad Function Descriptions

Pad No.	X-Axis (µm)	Y-Axis (µm)	Mnemonic	Pad Type	Description
1	−773	+1064	REFGND	Single	Reference Ground. Ground connection for the reference voltage. Decouple the input reference voltage (V_{REF+}) to this pin.
2	−773	+916	REFGND	Single	Reference Ground. Ground connection for the reference voltage. Decouple the input reference voltage (V_{REF+}) to this pin.
3	−773	+600	V_{IN+}	Single	Positive Input of the Differential Analog Input.
4	−773	+426	V_{IN-}	Single	Negative Input of the Differential Analog Input.
5a	−773	+93	AGND	Double	Power Supply Ground for Analog Circuitry.
5b	−773	+18	AGND	Double	Power Supply Ground for Analog Circuitry.
6	−561	−1326	$\overline{SYNC}$/$\overline{PD}$	Single	Synchronization ($\overline{SYNC}$) Pin. The $\overline{SYNC}$ pin can synchronize multiple AD7766-2-KGD devices. Power-Down Input Pin ($\overline{PD}$). The $\overline{PD}$ pin puts the AD7766-2-KGD device into power-down mode

Pad No.	X-Axis (µm)	Y-Axis (µm)	Mnemonic	Pad Type	Description
7	−353	−1319	DV_{DD}	Single	Digital Power Supply Input, 2.5 V. In cases where a logic voltage of 2.5 V for interfacing is used (2.5 V applied to V_{DRIVE} pin), the DV_{DD} and V_{DRIVE} pins can be connected to the same voltage supply rail.
8	−141	−1317	DV_{DD}	Single	Digital Power Supply Input, 2.5 V. In cases where a logic voltage of 2.5 V for interfacing is used (2.5 V applied to V_{DRIVE} pin), the DV_{DD} and V_{DRIVE} pins can be connected to the same voltage supply rail.
9	+105	−1340	V_{DRIVE}	Single	Logic Power Supply Input, 1.8 V to 3.6 V. The voltage supplied at this pin determines the operating voltage of the digital logic interface.
10	+601	−1336	V_{DRIVE}	Single	Logic Power Supply Input, 1.8 V to 3.6 V. The voltage supplied at this pin determines the operating voltage of the digital logic interface.
11	+799	−1161	SDO	Double	Serial Data Output. The conversion result from the AD7766-2-KGD is output on the SDO pin as a 24-bit, twos complement, MSB first, serial data stream.
12	+784	−944	DGND	Single	Digital Logic Power Supply Ground.
13	+784	−826	DGND	Single	Digital Logic Power Supply Ground.
14	+784	−677	DGND	Single	Digital Logic Power Supply Ground.
15	+800	−517	$\overline{DRDY}$	Single	Data Ready Output. A falling edge on the $\overline{DRDY}$ signal indicates that a new conversion data result is available in the output register of the AD7766-2-KGD.
16	+800	+363	SCLK	Single	Serial Clock Input. The SCLK input provides the serial clock for all serial data transfers with AD7766-2-KGD devices.
17	+800	+663	MCLK	Single	Master Clock Input. The sampling frequency of the AD7766-2-KGD is equal to the MCLK frequency.
18	+800	+850	SDI	Single	Serial Data Input. This pin is the daisy-chain input of the AD7766-2-KGD.
19	+800	+1051	$\overline{CS}$	Single	Chip Select Input. The $\overline{CS}$ input selects a specific AD7766-2-KGD device and acts as an enable on the SDO pin. In cases where $\overline{CS}$ is used, the MSB of the conversion result is clocked onto the SDO line on the $\overline{CS}$ falling edge. The $\overline{CS}$ input allows multiple AD7766-2-KGD devices to share the same SDO line. This function allows the user to select the appropriate device by supplying it with a logic low $\overline{CS}$ signal, which enables the SDO pin of the concerned device.
20	−125	+1319	AV_{DD}	Single	Analog Power Supply, 2.5 V.
21	−333	+1319	AV_{DD}	Single	Analog Power Supply, 2.5 V.
22	−561	+1317	V_{REF+}	Single	Reference Input for the AD7766-2-KGD. Apply an external reference to this input pin. The V_{REF+} input ranges from 2.4 V to 5 V. The reference voltage input is independent of the voltage magnitude applied to the AV_{DD} pin.
23	−667	+1317	V_{REF+}	Single	Reference Input for the AD7766-2-KGD. Apply an external reference to this input pin. The V_{REF+} input ranges from 2.4 V to 5 V. The reference voltage input is independent of the voltage magnitude applied to the AV_{DD} pin.

OUTLINE DIMENSIONS

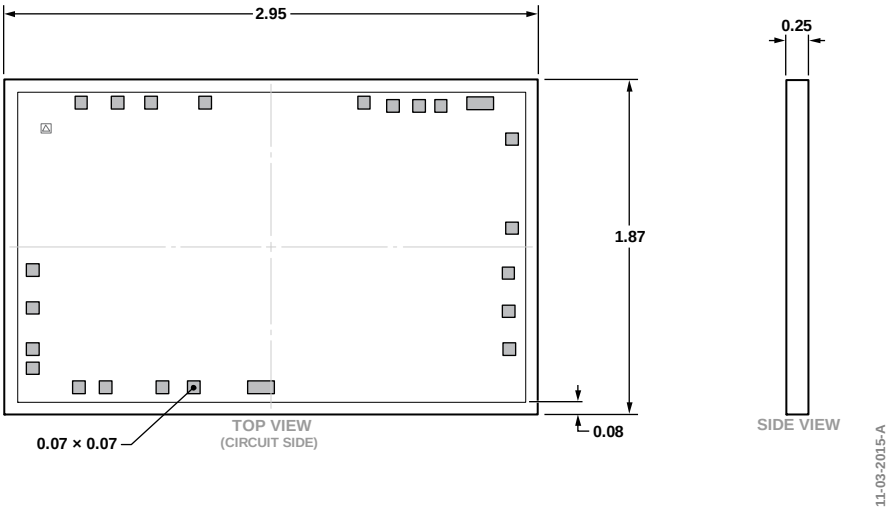

Figure 8. 23-Pad Bare Die [CHIP]
(C-23-1)
Dimensions shown in millimeters

DIE SPECIFICATIONS AND ASSEMBLY RECOMMENDATIONS

Table 6. Die Specifications

Parameter	Value	Unit
Chip Size	2870 (x) × 1790 (y)	µm
Scribe Line Width	80 (x) × 80 (y)	µm
Die Size	2950 (x) × 1870 (y)	µm
Thickness	305	µm
Backside	Bare silicon	Not applicable
Passivation	Nitride	Not applicable
Bond Pads (Minimum)	70 × 70	µm
Bond Pad Composition	AlCu (0.5%)	%
ESD	1	kV

Table 7. Assembly Recommendations

Assembly Component	Recommendation
Die Attach	No special recommendations
Bonding Method	Gold ball or aluminum wedge
Bonding Sequence	Pad 1 and Pad 2 first

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD7766-2-KGD-WP	−40°C to +105°C	23-Pad Bare Die [CHIP], Waffle Pack	C-23-1