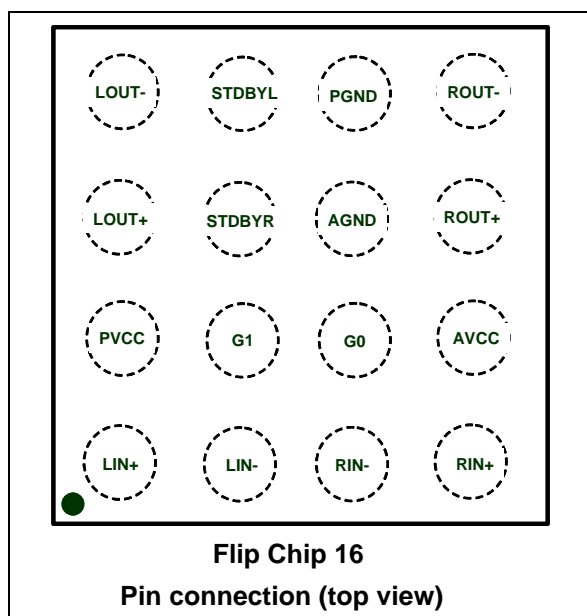


## Filter-free Flip Chip stereo 2 x 2.5 W class D audio power amplifier

Datasheet - production data



### Features

- Operates from  $V_{CC} = 2.5$  to  $5.5$  V
- Dedicated standby mode active low for each channel
- Output power per channel:  $1.15$  W at  $5$  V or  $0.63$  W at  $3.6$  V into  $8\ \Omega$  with 1% THD+N max.
- Output power per channel:  $1.85$  W at  $5$  V into  $4\ \Omega$  with 1% THD+N max.
- Output short-circuit protection
- Four gain setting steps: 6, 12, 18, 24 dB
- Low current consumption
- PSSR: 63 dB typ. at 217 Hz.
- Fast startup phase: 7.8 ms
- Thermal shutdown protection
- Flip Chip 16 bump lead-free package

**Table 1. Device summary**

Order code	Temperature range	Package	Packing	Marking
TS2012EIJT	-40 °C to +85 °C	Flip Chip 16	Tape and reel	K0

### Applications

- Cellular phones
- PDA

### Description

The TS2012EI is a fully-differential stereo class D power amplifier able to drive up to  $1.15$  W into an  $8\ \Omega$  load at  $5$  V per channel. It achieves better efficiency compared to typical class AB audio amps.

The device has four different gain settings utilizing two digital pins: G0 and G1.

Pop and click reduction circuitry provides low on/off switch noise while allowing the device to start within 8 ms.

Two standby pins (active low) allow each channel to be switched off separately.

The TS2012EI is available in a Flip Chip 16 bump lead-free package.

# Contents

<b>1</b>	<b>Absolute maximum ratings and operating conditions</b>	<b>3</b>
<b>2</b>	<b>Typical application</b>	<b>5</b>
<b>3</b>	<b>Electrical characteristics</b>	<b>7</b>
3.1	Electrical characteristics tables	7
3.2	Electrical characteristic curves	13
<b>4</b>	<b>Application information</b>	<b>21</b>
4.1	Differential configuration principle	21
4.2	Gain settings	21
4.3	Common mode feedback loop limitations	21
4.4	Low frequency response	22
4.5	Decoupling of the circuit	23
4.6	Wake-up time ( $t_{WU}$ ) and shutdown time ( $t_{STBY}$ )	23
4.7	Consumption in shutdown mode	25
4.8	Single-ended input configuration	25
4.9	Output filter considerations	26
4.10	Short-circuit protection	26
4.11	Thermal shutdown	27
<b>5</b>	<b>Package information</b>	<b>28</b>
<b>6</b>	<b>Revision history</b>	<b>31</b>

# 1 Absolute maximum ratings and operating conditions

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply voltage <sup>(1)</sup>	6	V
$V_{in}$	Input voltage <sup>(2)</sup>	GND to $V_{CC}$	V
$T_{oper}$	Operating free air temperature range	-40 to + 85	°C
$T_{stg}$	Storage temperature	-65 to +150	°C
$T_j$	Maximum junction temperature	150	°C
$R_{thja}$	Thermal resistance junction to ambient <sup>(3)</sup>	200	°C/W
$P_d$	Power dissipation	Internally limited <sup>(4)</sup>	
ESD	HBM: human body model <sup>(5)</sup>	2	kV
	MM: machine model <sup>(6)</sup>	200	V
Latch-up	Latch-up immunity	200	mA
$V_{STBY}$	Standby pin maximum voltage	GND to $V_{CC}$	V
	Lead temperature (soldering, 10sec)	260	°C
	Output short-circuit protection <sup>(7)</sup>		

1. All voltage values are measured with respect to the ground pin.
2. The magnitude of the input signal must never exceed  $V_{CC} + 0.3\text{ V} / \text{GND} - 0.3\text{ V}$ .
3. The device is protected in case of over temperature by a thermal shutdown active at 150°C.
4. Exceeding the power derating curves during a long period will cause abnormal operation.
5. Human body model: 100 pF discharged through a 1.5 kΩ resistor between two pins of the device, done for all couples of pin combinations with other pins floating.
6. Machine model: a 200 pF cap is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω), done for all couples of pin combinations with other pins floating.
7. Implemented short-circuit protection protects the amplifier against damage by short-circuit between positive and negative outputs of each channel and between outputs and ground.

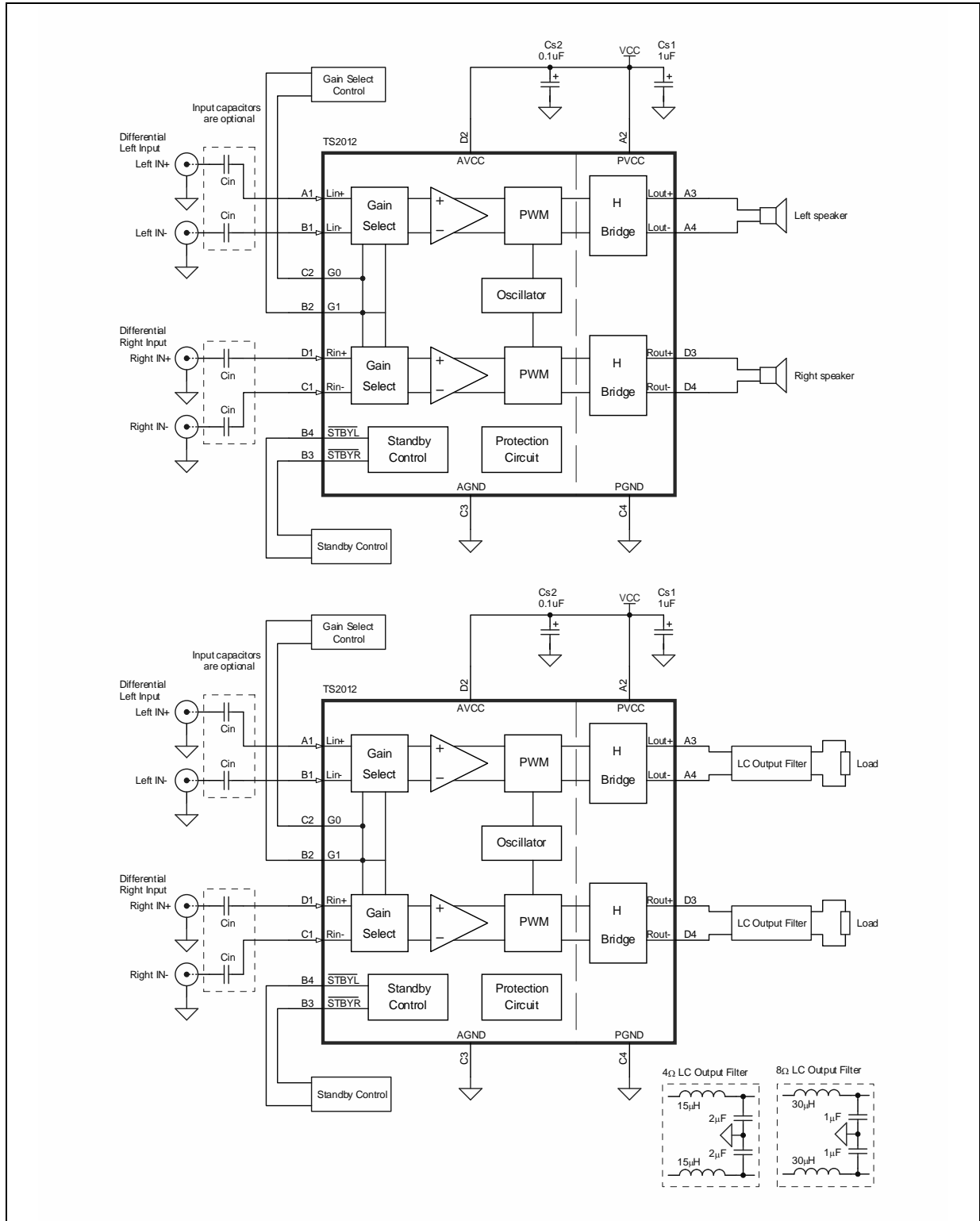
Table 3. Operating conditions

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply voltage	2.5 to 5.5	V
$V_{in}$	Input voltage range	GND to $V_{CC}$	V
$V_{ic}$	Input common mode voltage <sup>(1)</sup>	GND+0.5V to $V_{CC}$ -0.9V	V
$V_{STBY}$	Standby voltage input <sup>(2)</sup> Device ON Device in STANDBY <sup>(3)</sup>	$1.4 \leq V_{STBY} \leq V_{CC}$ $GND \leq V_{STBY} \leq 0.4$	V
$R_L$	Load resistor	$\geq 4$	$\Omega$
$V_{IH}$	GO, G1 - high level input voltage <sup>(4)</sup>	$1.4 \leq V_{IH} \leq V_{CC}$	V
$V_{IL}$	GO, G1 - low level input voltage	$GND \leq V_{IL} \leq 0.4$	V
$R_{thja}$	Thermal resistance junction to ambient <sup>(5)</sup>	90	$^{\circ}C/W$

1.  $|V_{oo}| \leq 40$  mV max with all differential gains except 24 dB. For 24 dB gain, input decoupling capacitors are mandatory.
2. Without any signal on standby pin, the device is in standby (internal 300 k $\Omega$  +/-20% pull-down resistor).
3. Minimum current consumption is obtained when  $V_{STBY} = GND$ .
4. Between GO, G1 pins and  $GND$ , there is an internal 300 k $\Omega$  (+/-20%) pull-down resistor. When pins are floating, the gain is 6 dB. In full standby (left and right channels OFF), these resistors are disconnected (HiZ input).
5. With a 4-layer PCB.

## 2 Typical application

Figure 1. Typical application schematics



**Table 4. External component description**

Components	Functional description
$C_{S1}, C_{S2}$	Supply capacitor that provides power supply filtering.
$C_{in}$	Input coupling capacitors (optional) that block the DC voltage at the amplifier input terminal. The capacitors also form a high pass filter with $Z_{in}$ ( $F_{cl} = 1 / (2 \times \pi \times Z_{in} \times C_{in})$ ). Be aware that value of $Z_{in}$ is changing with gain setting.

**Table 5. Pin description**

Pin number	Pin name	Description
A1	Lin+	Left channel positive differential input
A2	PVCC	Power supply voltage
A3	Lout+	Left channel positive output
A4	Lout-	Left channel negative output
B1	Lin-	Left channel negative differential input
B2	G1	Gain select pin (MSB)
B3	STBYR	Standby pin (active low) for right channel output
B4	STBYL	Standby pin (active low) for left channel output
C1	Rin-	Right channel negative differential input
C2	G0	Gain select pin (LSB)
C3	AGND	Analog ground
C4	PGND	Power ground
D1	Rin+	Right channel positive differential input
D2	AVCC	Analog supply voltage
D3	Rout+	Right channel positive output
D4	Rout-	Right channel negative output

### 3 Electrical characteristics

#### 3.1 Electrical characteristics tables

Table 6.  $V_{CC} = +5\text{ V}$ ,  $GND = 0\text{ V}$ ,  $V_{ic} = 2.5\text{ V}$ ,  $T_{amb} = 25^\circ\text{ C}$  (unless otherwise specified)

Symbol	Parameters and test conditions	Min.	Typ.	Max.	Unit
$I_{CC}$	Supply current No input signal, no load, both channels		5	7	mA
$I_{STBY}$	Standby current No input signal, $V_{STBY} = GND$		1	2	$\mu\text{A}$
$V_{oo}$	Output offset voltage Floating inputs, $G = 6\text{ dB}$ , $R_L = 8\ \Omega$			25	mV
$P_o$	Output power THD + N = 1% max, $f = 1\text{ kHz}$ , $R_L = 4\ \Omega$ THD + N = 1% max, $f = 1\text{ kHz}$ , $R_L = 8\ \Omega$ THD + N = 10% max, $f = 1\text{ kHz}$ , $R_L = 4\ \Omega$ THD + N = 10% max, $f = 1\text{ kHz}$ , $R_L = 8\ \Omega$		1.85 1.15 2.5 1.6		W
THD + N	Total harmonic distortion + noise $P_o = 0.8\text{ W}$ , $G = 6\text{ dB}$ , $f = 1\text{ kHz}$ , $R_L = 8\ \Omega$		0.5		%
Efficiency	Efficiency per channel $P_o = 1.85\text{ W}$ , $R_L = 4\ \Omega + 15\ \mu\text{H}$ $P_o = 1.16\text{ W}$ , $R_L = 8\ \Omega + 15\ \mu\text{H}$		78 88		%
PSRR	Power supply rejection ratio with inputs grounded $C_{in} = 1\ \mu\text{F}$ <sup>(1)</sup> , $f = 217\text{ Hz}$ , $R_L = 8\ \Omega$ , Gain = 6 dB, $V_{ripple} = 200\text{ mV}_{pp}$		65		dB
Crosstalk	Channel separation $P_o = 0.9\text{ W}$ , $G = 6\text{ dB}$ , $f = 1\text{ kHz}$ , $R_L = 8\ \Omega$		90		dB
CMRR	Common mode rejection ratio $C_{in} = 1\ \mu\text{F}$ , $f = 217\text{ Hz}$ , $R_L = 8\ \Omega$ , Gain = 6 dB, $\Delta V_{ICM} = 200\text{ mV}_{pp}$		63		dB
Gain	Gain value with no load $G1 = G0 = V_{IL}$ $G1 = V_{IL}$ and $G0 = V_{IH}$ $G1 = V_{IH}$ and $G0 = V_{IL}$ $G1 = G0 = V_{IH}$	5.5 11.5 17.5 23.5	6 12 18 24	6.5 12.5 18.5 24.5	dB
$Z_{in}$	Single-ended input impedance Referred to ground Gain = 6 dB Gain = 12 dB Gain = 18 dB Gain = 24 dB	24 24 12 6	30 30 15 7.5	36 36 18 9	k $\Omega$
$F_{PWM}$	Pulse width modulator base frequency	190	280	370	kHz

**Table 6.  $V_{CC} = +5\text{ V}$ ,  $GND = 0\text{ V}$ ,  $V_{ic} = 2.5\text{ V}$ ,  $T_{amb} = 25^\circ\text{ C}$  (unless otherwise specified) (continued)**

Symbol	Parameters and test conditions	Min.	Typ.	Max.	Unit
SNR	Signal to noise ratio (A-weighting) $P_o = 1.1\text{ W}$ , $G = 6\text{ dB}$ , $R_L = 8\ \Omega$		99		dB
$t_{WU}$	Total wake-up time <sup>(2)</sup>	9	13	16.5	ms
$t_{STBY}$	Standby time <sup>(2)</sup>	11	15.8	20	ms
$V_N$	Output voltage noise $f = 20\text{ Hz}$ to $20\text{ kHz}$ , $R_L = 8\ \Omega$				$\mu\text{V}_{RMS}$
	Unweighted (filterless, $G = 6\text{ dB}$ )		61		
	A-weighted (filterless, $G = 6\text{ dB}$ )		31		
	Unweighted (with LC output filter, $G = 6\text{ dB}$ )		59		
	A-weighted (with LC output filter, $G = 6\text{ dB}$ )		31		
	Unweighted (filterless, $G = 24\text{ dB}$ )		87		
	A-weighted (filterless, $G = 24\text{ dB}$ )		52		
	A-weighted (with LC output filter, $G = 24\text{ dB}$ )		87		
A-weighted (with LC output filter, $G = 24\text{ dB}$ )		53			

1. Dynamic measurements -  $20 \cdot \log(\text{rms}(V_{out})/\text{rms}(V_{ripple}))$ .  $V_{ripple}$  is the superimposed sinus signal to  $V_{CC}$  at  $f = 217\text{ Hz}$ .
2. See [Section 4.6: Wake-up time \( \$t\_{WU}\$ \) and shutdown time \( \$t\_{STBY}\$ \) on page 23.](#)



Table 7.  $V_{CC} = +3.6\text{ V}$ ,  $GND = 0\text{ V}$ ,  $V_{IC} = 1.8\text{ V}$ ,  $T_{amb} = 25^\circ\text{ C}$  (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$I_{CC}$	Supply current No input signal, no load, both channels		3.5	5.5	mA
$I_{STBY}$	Standby current No input signal, $V_{STBY} = GND$		0.7	2	$\mu\text{A}$
$V_{oo}$	Output offset voltage Floating inputs, $G = 6\text{ dB}$ , $R_L = 8\ \Omega$			25	mV
$P_o$	Output power THD + N = 1% max, $f = 1\text{ kHz}$ , $R_L = 4\ \Omega$ THD + N = 1% max, $f = 1\text{ kHz}$ , $R_L = 8\ \Omega$ THD + N = 10% max, $f = 1\text{ kHz}$ , $R_L = 4\ \Omega$ THD + N = 10% max, $f = 1\text{ kHz}$ , $R_L = 8\ \Omega$		0.96 0.63 1.3 0.8		W
THD + N	Total harmonic distortion + noise $P_o = 0.45\text{ W}$ , $G = 6\text{ dB}$ , $f = 1\text{ kHz}$ , $R_L = 8\ \Omega$		0.35		%
Efficiency	Efficiency per channel $P_o = 0.96\text{ W}$ , $R_L = 4\ \Omega + 15\ \infty\text{H}$ $P_o = 0.63\text{ W}$ , $R_L = 8\ \Omega + 15\ \infty\text{H}$		78 88		%
PSRR	Power supply rejection ratio with inputs grounded $C_{in} = 1\ \mu\text{F}$ <sup>(1)</sup> , $f = 217\text{ Hz}$ , $R_L = 8\ \Omega$ , Gain = 6 dB, $V_{ripple} = 200\text{ mV}_{pp}$		65		dB
Crosstalk	Channel separation $G = 6\text{ dB}$ , $f = 1\text{ kHz}$ , $R_L = 8\ \Omega$		90		
CMRR	Common mode rejection ratio $C_{in} = 1\ \mu\text{F}$ , $f = 217\text{ Hz}$ , $R_L = 8\ \Omega$ , Gain = 6 dB, $\Delta V_{ICM} = 200\text{ mV}_{pp}$		62		dB
Gain	Gain value with no load $G1 = G0 = V_{IL}$ $G1 = V_{IL}$ and $G0 = V_{IH}$ $G1 = V_{IH}$ and $G0 = V_{IL}$ $G1 = G0 = V_{IH}$	5.5 11.5 17.5 23.5	6 12 18 24	6.5 12.5 18.5 24.5	dB
$Z_{in}$	Single-ended input impedance Referred to ground Gain = 6 dB Gain = 12 dB Gain = 18 dB Gain = 24 dB	24 24 12 6	30 30 15 7.5	36 36 18 9	k $\Omega$
$F_{PWM}$	Pulse width modulator base frequency	190	280	370	kHz
SNR	Signal-to-noise ratio (A-weighting) $P_o = 0.6\text{ W}$ , $G = 6\text{ dB}$ , $R_L = 8\ \Omega$		96		dB
$t_{WU}$	Total wake-up time <sup>(2)</sup>	7.5	11.3	15	ms

**Table 7.  $V_{CC} = +3.6\text{ V}$ ,  $GND = 0\text{ V}$ ,  $V_{ic} = 1.8\text{ V}$ ,  $T_{amb} = 25^\circ\text{ C}$  (unless otherwise specified) (continued)**

Symbol	Parameter	Min.	Typ.	Max.	Unit
$t_{STBY}$	Standby time <sup>(2)</sup>	10	13.8	18	ms
$V_N$	Output voltage noise $f = 20\text{ Hz to } 20\text{ kHz}$ , $R_L = 8\ \Omega$				$\mu\text{V}_{RMS}$
	Unweighted (filterless, $G = 6\text{ dB}$ )		54		
	A-weighted (filterless, $G = 6\text{ dB}$ )		28		
	Unweighted (with LC output filter, $G = 6\text{ dB}$ )		52		
	A-weighted (with LC output filter, $G = 6\text{ dB}$ )		27		
	Unweighted (filterless, $G = 24\text{ dB}$ )		80		
	A-weighted (filterless, $G = 24\text{ dB}$ )		50		
	A-weighted (with LC output filter, $G = 24\text{ dB}$ )		79		
	A-weighted (with LC output filter, $G = 24\text{ dB}$ )		49		

1. Dynamic measurements -  $20 \cdot \log(\text{rms}(V_{out})/\text{rms}(V_{ripple}))$ .  $V_{ripple}$  is the superimposed sinus signal to  $V_{CC}$  at  $f = 217\text{ Hz}$ .
2. See [Section 4.6: Wake-up time \( \$t\_{WU}\$ \) and shutdown time \( \$t\_{STBY}\$ \) on page 23](#).

Table 8.  $V_{CC} = +2.5\text{ V}$ ,  $GND = 0\text{ V}$ ,  $V_{IC} = 1.25\text{ V}$ ,  $T_{amb} = 25\text{ }^\circ\text{C}$  (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$I_{CC}$	Supply current No input signal, no load, both channels		2.8	4	mA
$I_{STBY}$	Standby current No input signal, $V_{STBY} = GND$		0.45	2	$\mu\text{A}$
$V_{oo}$	Output offset voltage Floating inputs, $G = 6\text{ dB}$ , $R_L = 8\ \Omega$			25	mV
$P_o$	Output power THD + N = 1% max, $f = 1\text{ kHz}$ , $R_L = 4\ \Omega$ THD + N = 1% max, $f = 1\text{ kHz}$ , $R_L = 8\ \Omega$ THD + N = 10% max, $f = 1\text{ kHz}$ , $R_L = 4\ \Omega$ THD + N = 10% max, $f = 1\text{ kHz}$ , $R_L = 8\ \Omega$		0.45 0.3 0.6 0.38		W
THD + N	Total harmonic distortion + noise $P_o = 0.2\text{ W}$ , $G = 6\text{ dB}$ , $f = 1\text{ kHz}$ , $R_L = 8\ \Omega$		0.2		%
Efficiency	Efficiency per channel $P_o = 0.45\text{ W}$ , $R_L = 4\ \Omega + 15\ \mu\text{H}$ $P_o = 0.3\text{ W}$ , $R_L = 8\ \Omega + 15\ \mu\text{H}$		78 87		%
PSRR	Power supply rejection ratio with inputs grounded $C_{in} = 1\ \mu\text{F}$ <sup>(1)</sup> , $f = 217\text{ Hz}$ , $R_L = 8\ \Omega$ , Gain = 6 dB, $V_{ripple} = 200\text{ mV}_{pp}$		65		dB
Crosstalk	Channel separation $G = 6\text{ dB}$ , $f = 1\text{ kHz}$ , $R_L = 8\ \Omega$		90		
CMRR	Common mode rejection ratio $C_{in} = 1\ \mu\text{F}$ , $f = 217\text{ Hz}$ , $R_L = 8\ \Omega$ , Gain = 6 dB, $\Delta V_{ICM} = 200\text{ mV}_{pp}$		62		dB
Gain	Gain value with no load $G1 = G0 = V_{IL}$ $G1 = V_{IL}$ and $G0 = V_{IH}$ $G1 = V_{IH}$ and $G0 = V_{IL}$ $G1 = G0 = V_{IH}$	5.5 11.5 17.5 23.5	6 12 18 24	6.5 12.5 18.5 24.5	dB
$Z_{in}$	Single-ended input impedance Referred to ground Gain = 6 dB Gain = 12 dB Gain = 18 dB Gain = 24 dB	24 24 12 6	30 30 15 7.5	36 36 18 9	$\text{k}\Omega$
$F_{PWM}$	Pulse width modulator base frequency	190	280	370	kHz
SNR	Signal-to-noise ratio (A-weighting) $P_o = 0.28\text{ W}$ , $G = 6\text{ dB}$ , $R_L = 8\ \Omega$		93		dB
$t_{WU}$	Total wake-up time <sup>(2)</sup>	3	7.8	12	ms

**Table 8.  $V_{CC} = +2.5\text{ V}$ ,  $GND = 0\text{ V}$ ,  $V_{ic} = 1.25\text{ V}$ ,  $T_{amb} = 25\text{ °C}$  (unless otherwise specified) (continued)**

Symbol	Parameter	Min.	Typ.	Max.	Unit
$t_{STBY}$	Standby time <sup>(2)</sup>	8	12	16	ms
$V_N$	Output voltage noise $f = 20\text{ Hz to } 20\text{ kHz}$ , $R_L = 8\ \Omega$				$\mu\text{V}_{RMS}$
	Unweighted (filterless, $G = 6\text{ dB}$ )		51		
	A-weighted (filterless, $G = 6\text{ dB}$ )		26		
	Unweighted (with LC output filter, $G = 6\text{ dB}$ )		49		
	A-weighted (with LC output filter, $G = 6\text{ dB}$ )		26		
	Unweighted (filterless, $G = 24\text{ dB}$ )		77		
	A-weighted (filterless, $G = 24\text{ dB}$ )		49		
	A-weighted (with LC output filter, $G = 24\text{ dB}$ )		76		
	A-weighted (with LC output filter, $G = 24\text{ dB}$ )		48		

1. Dynamic measurements -  $20 \cdot \log(\text{rms}(V_{out})/\text{rms}(V_{ripple}))$ .  $V_{ripple}$  is the superimposed sinus signal to  $V_{CC}$  at  $f = 217\text{ Hz}$ .
2. See [Section 4.6: Wake-up time \( \$t\_{WU}\$ \) and shutdown time \( \$t\_{STBY}\$ \) on page 23](#).

### 3.2 Electrical characteristic curves

The graphs shown in this section use the following abbreviations.

- $R_L + 15 \mu\text{H}$  or  $30 \mu\text{H}$  = pure resistor + very low series resistance inductor.
- Filter = LC output filter ( $1 \mu\text{F} + 30 \mu\text{H}$  for  $4 \Omega$  and  $0.5 \mu\text{F} + 15 \mu\text{H}$  for  $8 \Omega$ ).

All measurements are done with  $C_{S1} = 1 \mu\text{F}$  and  $C_{S2} = 100 \text{ nF}$  (Figure 2), except for the PSRR where  $C_{S1}$  is removed (Figure 3).

Figure 2. Test diagram for measurements

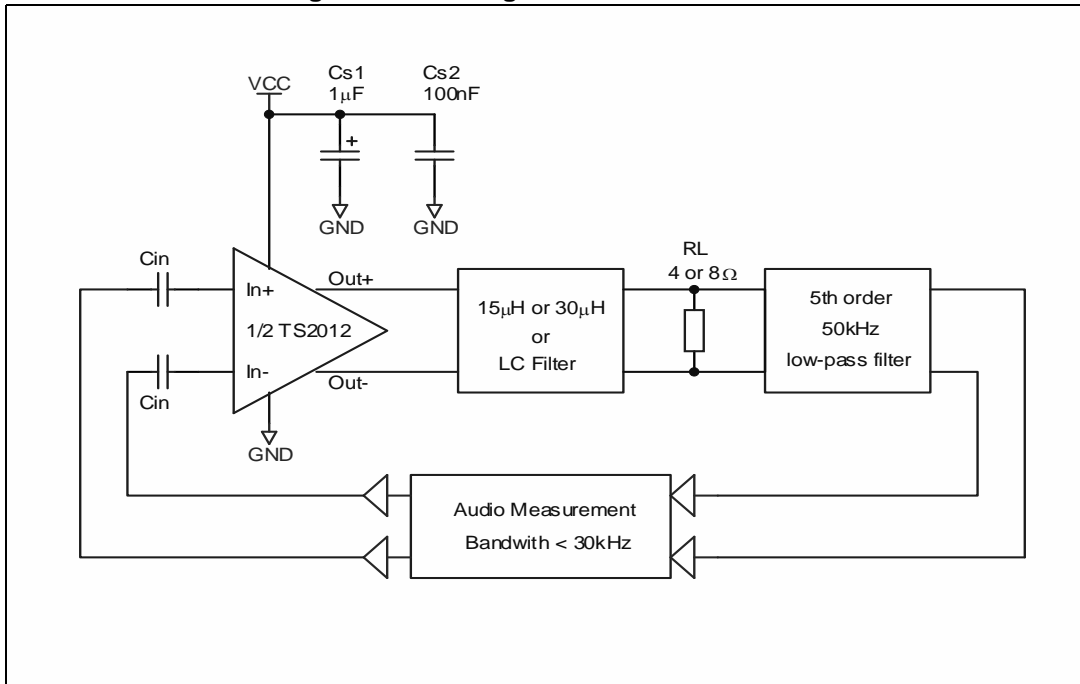


Figure 3. Test diagram for PSRR measurements

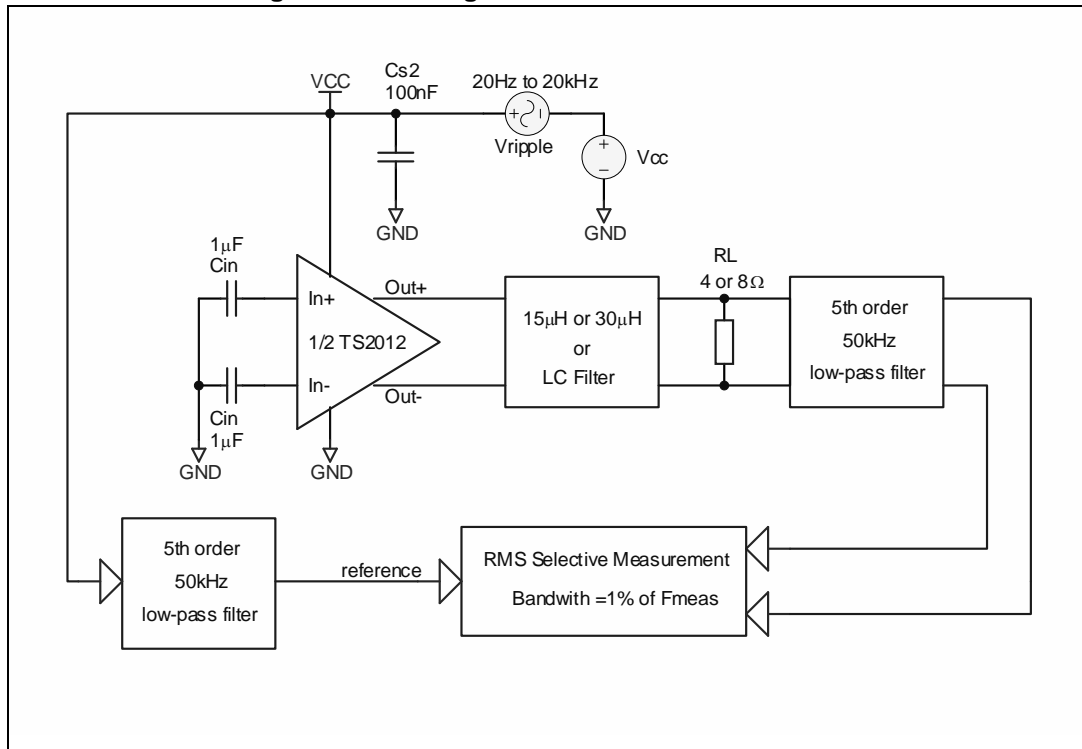


Figure 4. Current consumption vs. power supply voltage

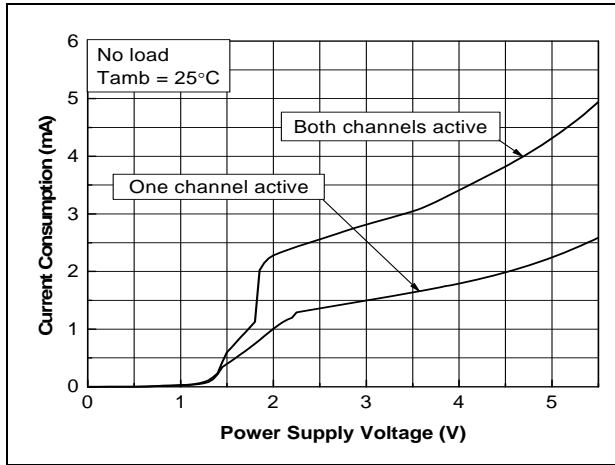


Figure 5. Current consumption vs. standby voltage (one channel)

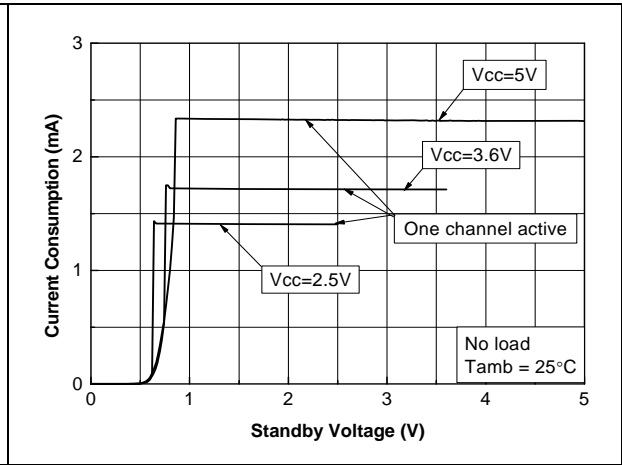


Figure 6. Efficiency vs. output power (one channel)

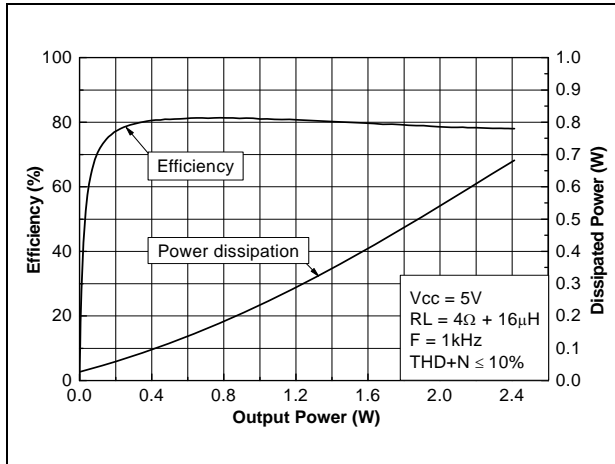


Figure 7. Efficiency vs. output power (one channel)

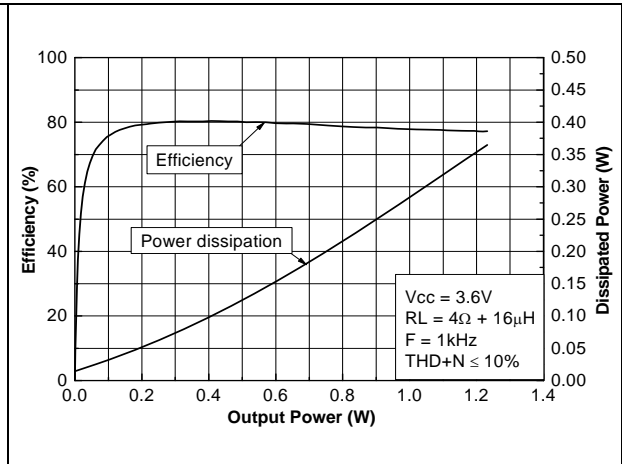


Figure 8. Efficiency vs. output power (one channel)

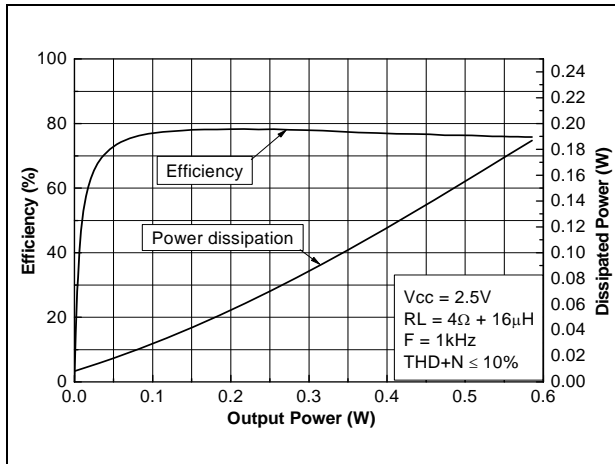


Figure 9. Efficiency vs. output power (one channel)

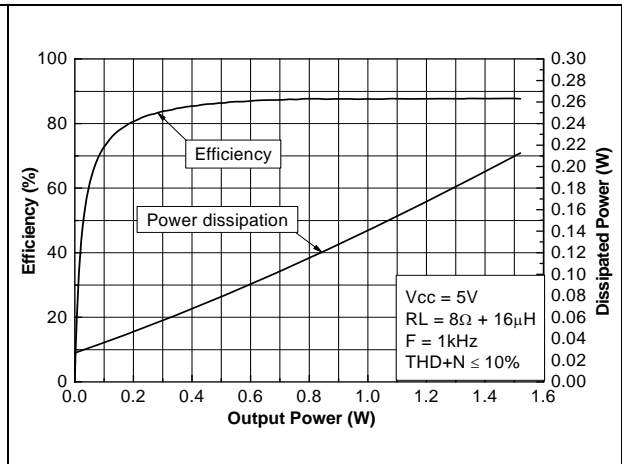


Figure 10. Efficiency vs. output power (one channel)

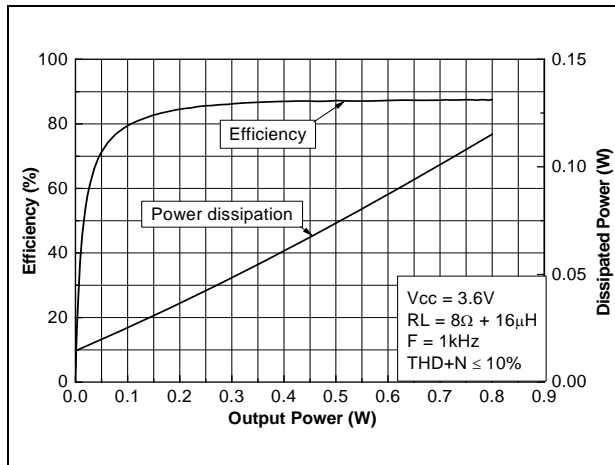


Figure 11. Efficiency vs. output power (one channel)

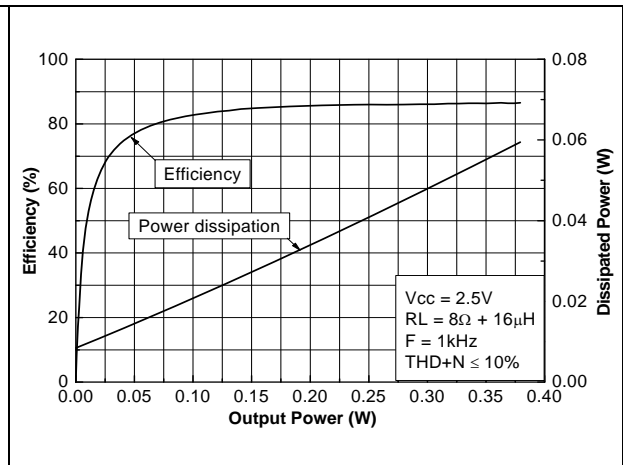


Figure 12. PSRR vs. frequency

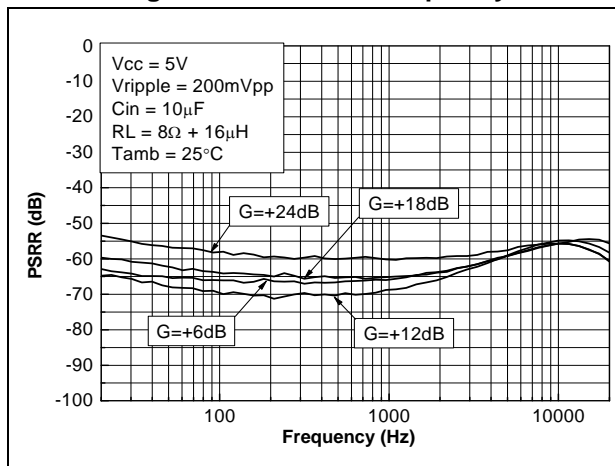


Figure 13. PSRR vs. frequency

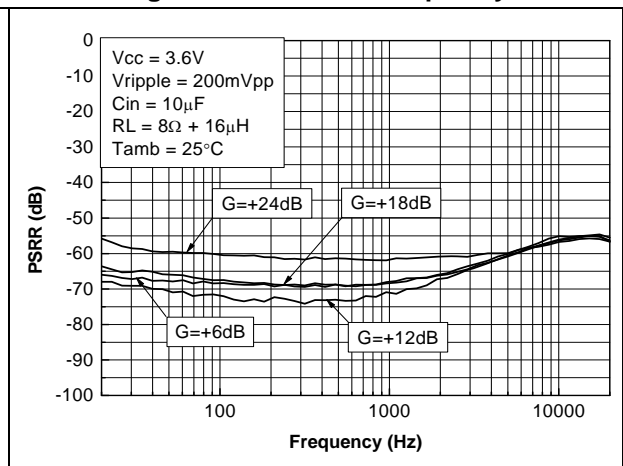


Figure 14. PSRR vs. frequency

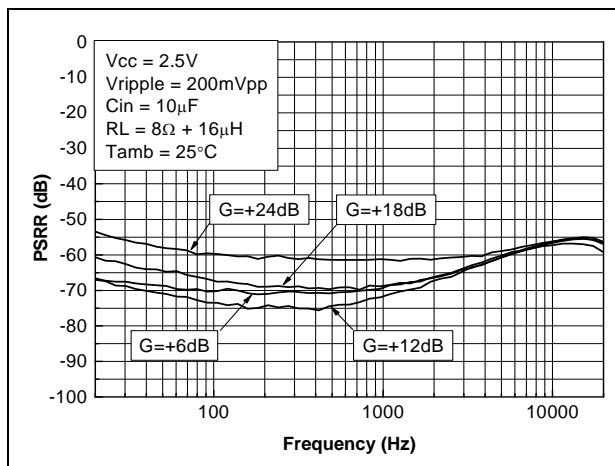


Figure 15. PSRR vs. common mode input voltage

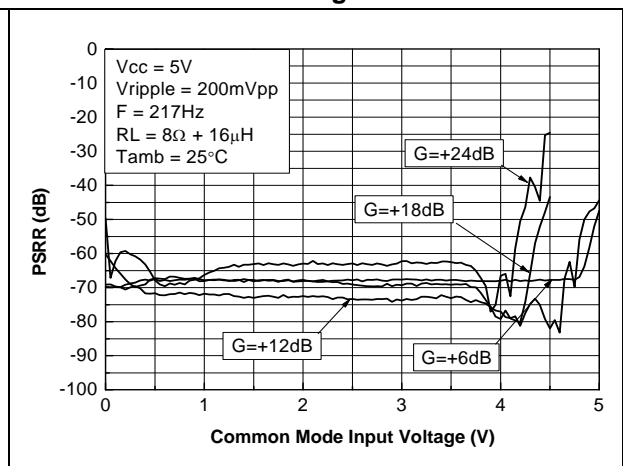




Figure 16. PSRR vs. common mode input voltage

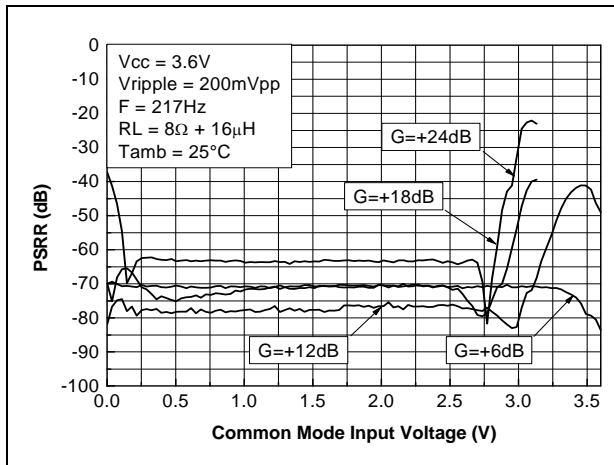


Figure 17. PSRR vs. common mode input voltage

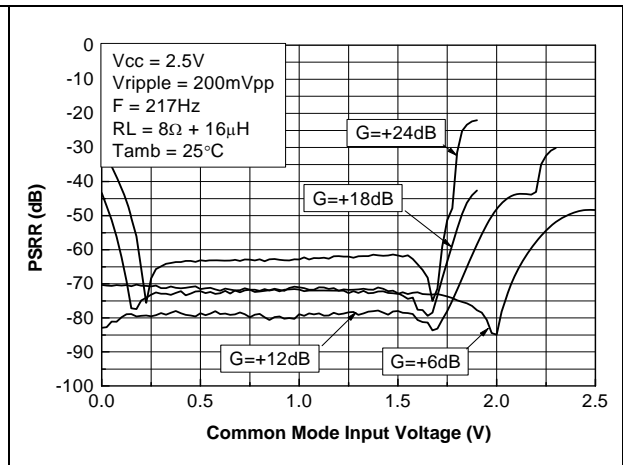


Figure 18. CMRR vs. frequency

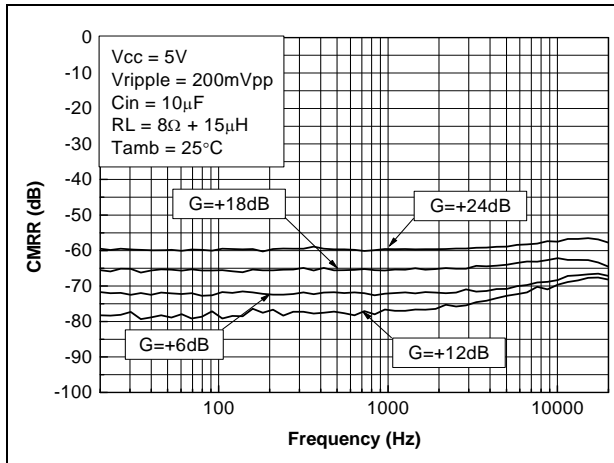


Figure 19. CMRR vs. frequency

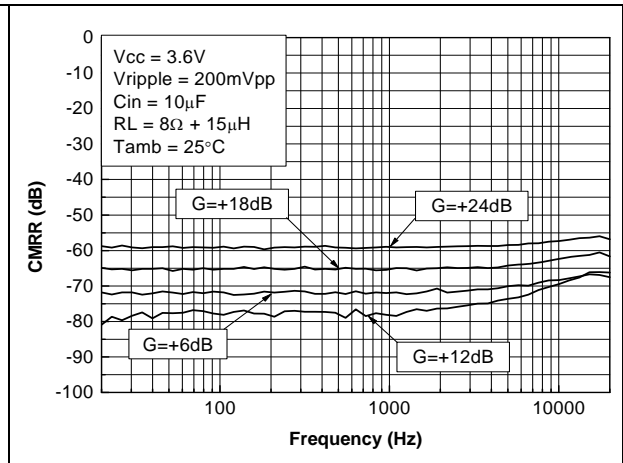


Figure 20. CMRR vs. frequency

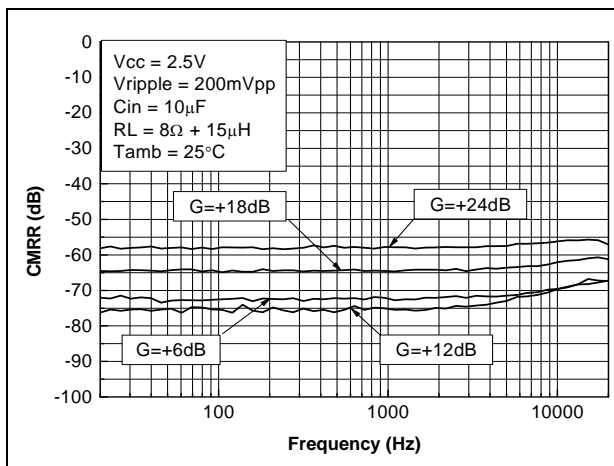


Figure 21. CMRR vs. common mode input voltage

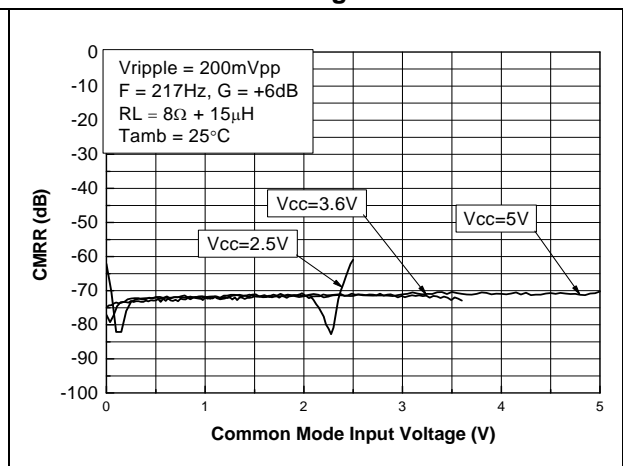


Figure 22. CMRR vs. common mode input voltage

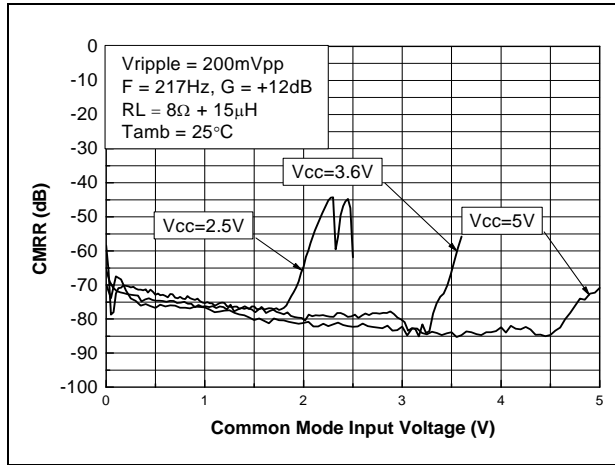


Figure 23. CMRR vs. common mode input voltage

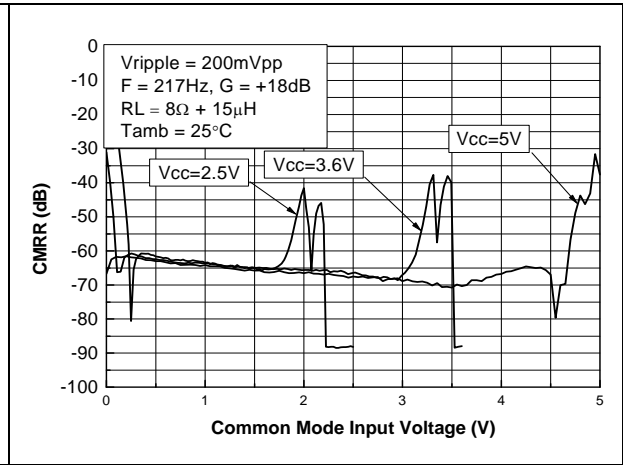


Figure 24. CMRR vs. common mode input voltage

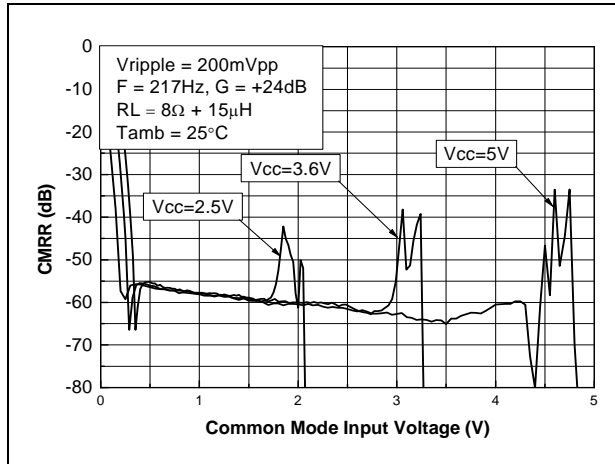


Figure 25. THD+N vs. output power

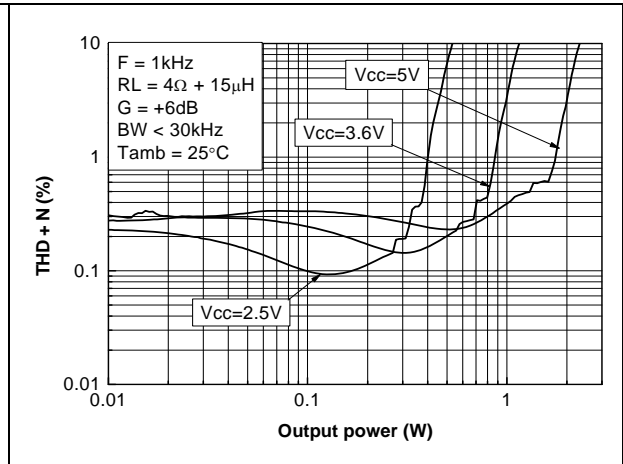


Figure 26. THD+N vs. output power

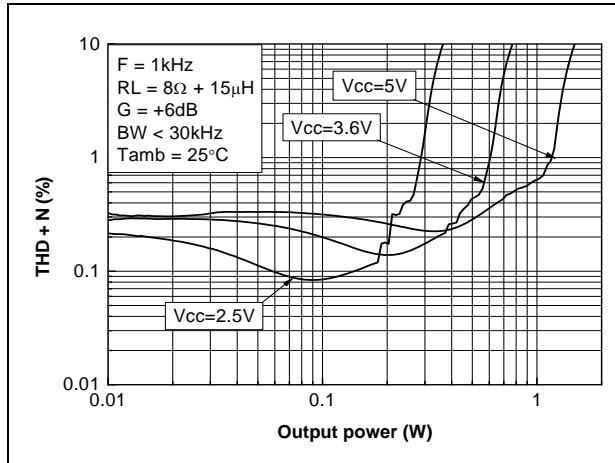


Figure 27. THD+N vs. frequency

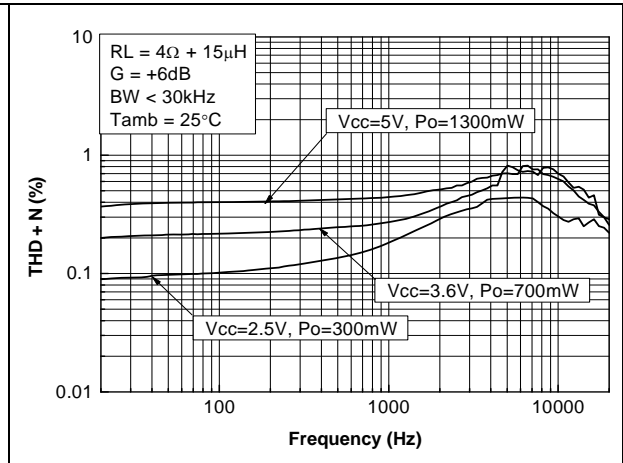


Figure 28. THD+N vs. frequency

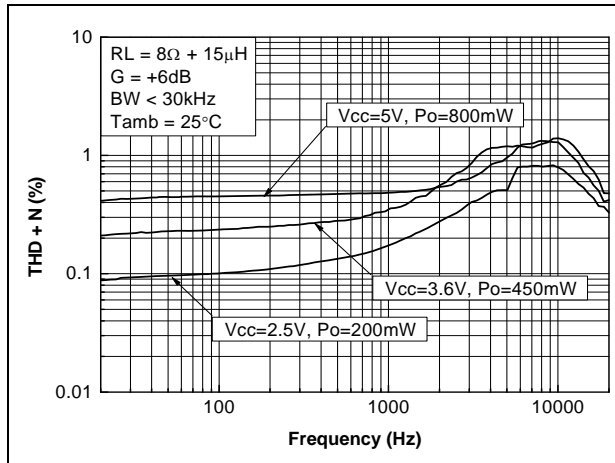


Figure 29. Crosstalk vs. frequency

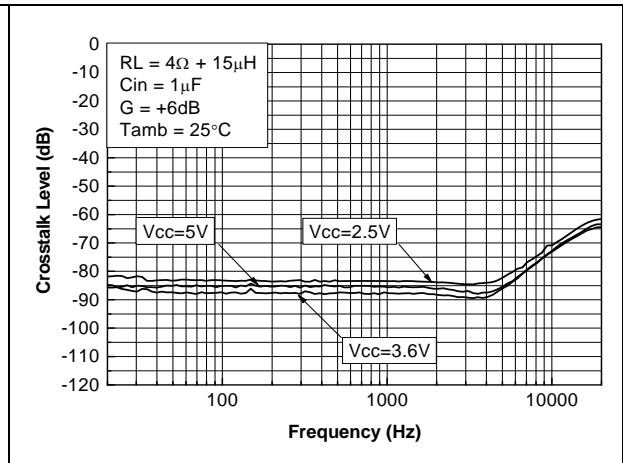


Figure 30. Crosstalk vs. frequency

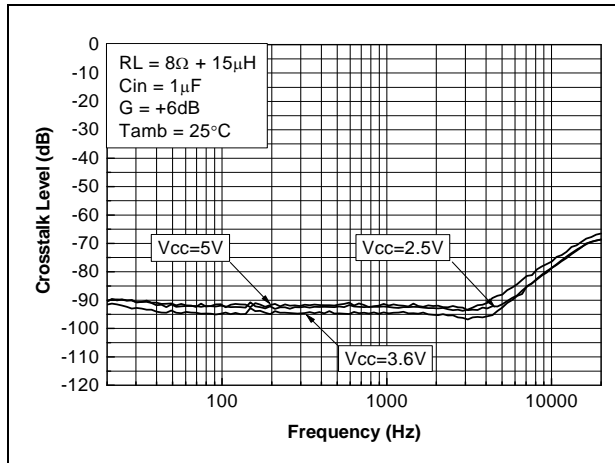


Figure 31. Output power vs. power supply voltage

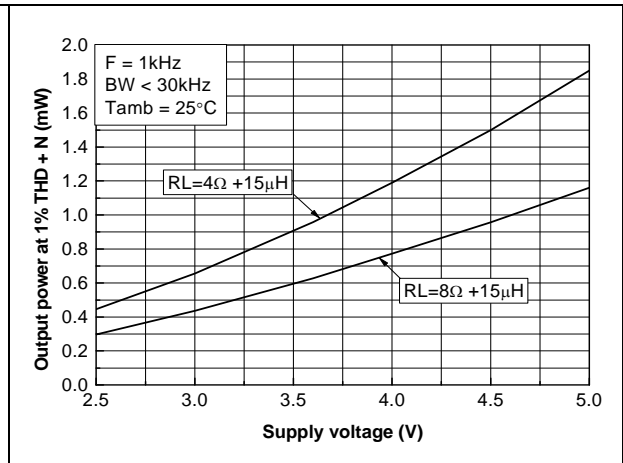


Figure 32. Output power vs. power supply voltage

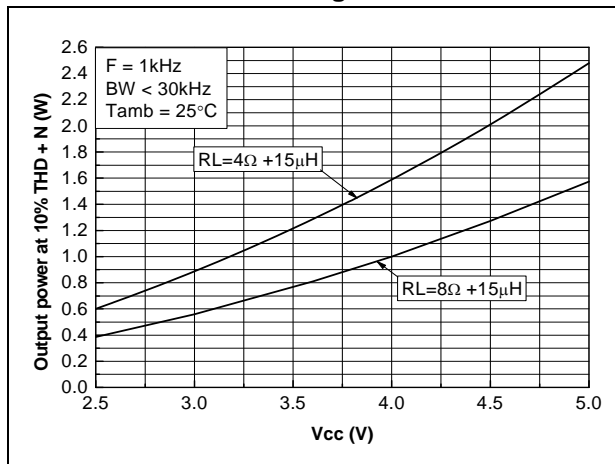


Figure 33. Power derating curves

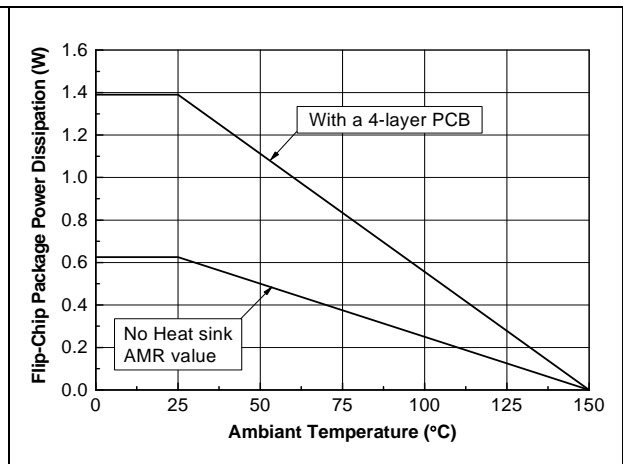


Figure 34. Startup and shutdown phase  
 $V_{CC} = 5\text{ V}$ ,  $G = 6\text{ dB}$ ,  $C_{in} = 1\text{ }\mu\text{F}$ , inputs grounded

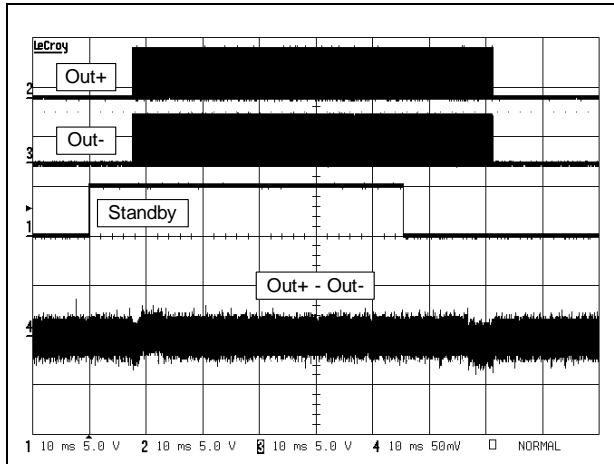
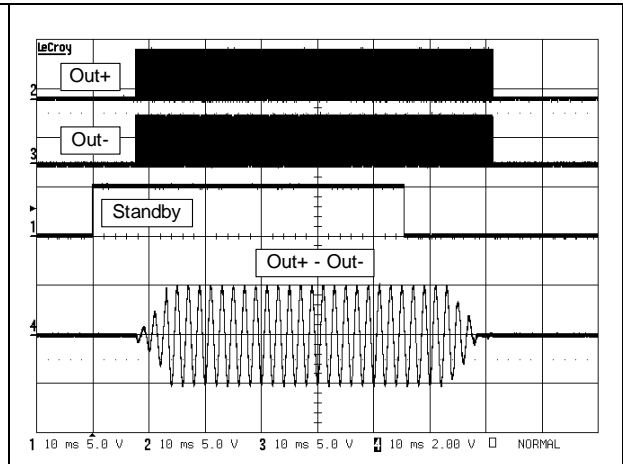


Figure 35. Startup and shutdown phase  
 $V_{CC} = 5\text{ V}$ ,  $G = 6\text{ dB}$ ,  $C_{in} = 1\text{ }\mu\text{F}$ ,  $V_{in} = 2\text{ V}_{pp}$ ,  
 $F = 500\text{ Hz}$



## 4 Application information

### 4.1 Differential configuration principle

The TS2012EI is a monolithic fully-differential input/output class D power amplifier. The TS2012EI also includes a common-mode feedback loop that controls the output bias value to average it at  $V_{CC}/2$  for any DC common mode input voltage. This allows the device to always have a maximum output voltage swing, and by consequence, maximize the output power. Moreover, as the load is connected differentially compared with a single-ended topology, the output is four times higher for the same power supply voltage.

The **advantages** of a full-differential amplifier are:

- high PSRR (power supply rejection ratio),
- high common mode noise rejection,
- virtually zero pop without additional circuitry, giving a faster start-up time compared to conventional single-ended input amplifiers,
- easier interfacing with differential output audio DACs,
- no input coupling capacitors required thanks to the common mode feedback loop.

### 4.2 Gain settings

In the flat region of the frequency-response curve (no input coupling capacitor or internal feedback loop + load effect), the differential gain can be set to 6, 12 18, or 24 dB, depending on the logic level of the G0 and G1 pins, as shown in [Table 9](#).

**Table 9. Gain settings with G0 and G1 pins**

G1	G0	Gain (dB)	Gain (V/V)
0	0	6	2
0	1	12	4
1	0	18	8
1	1	24	16

*Note:* Between pins G0, G1 and GND there is an internal 300 k $\Omega$  (+/-20%) resistor. When the pins are floating, the gain is 6 dB. In full standby (left and right channels OFF), these resistors are disconnected (HiZ input).

### 4.3 Common mode feedback loop limitations

As explained previously, the common mode feedback loop allows the output DC bias voltage to be averaged at  $V_{CC}/2$  for any DC common mode bias input voltage.

Due to the  $V_{ic}$  limitation of the input stage (see [Table 3: Operating conditions on page 4](#)), the common mode feedback loop can fulfill its role only within the defined range.

### 4.4 Low frequency response

If a low frequency bandwidth limitation is required, it is possible to use input coupling capacitors. In the low-frequency region, the input coupling capacitor  $C_{in}$  starts to have an effect.  $C_{in}$  forms, with the input impedance  $Z_{in}$ , a first order high-pass filter with a -3 dB cut-off frequency (see [Table 6](#) to [Table 8](#)).

$$F_{CL} = \frac{1}{2 \cdot \pi \cdot Z_{in} \cdot C_{in}}$$

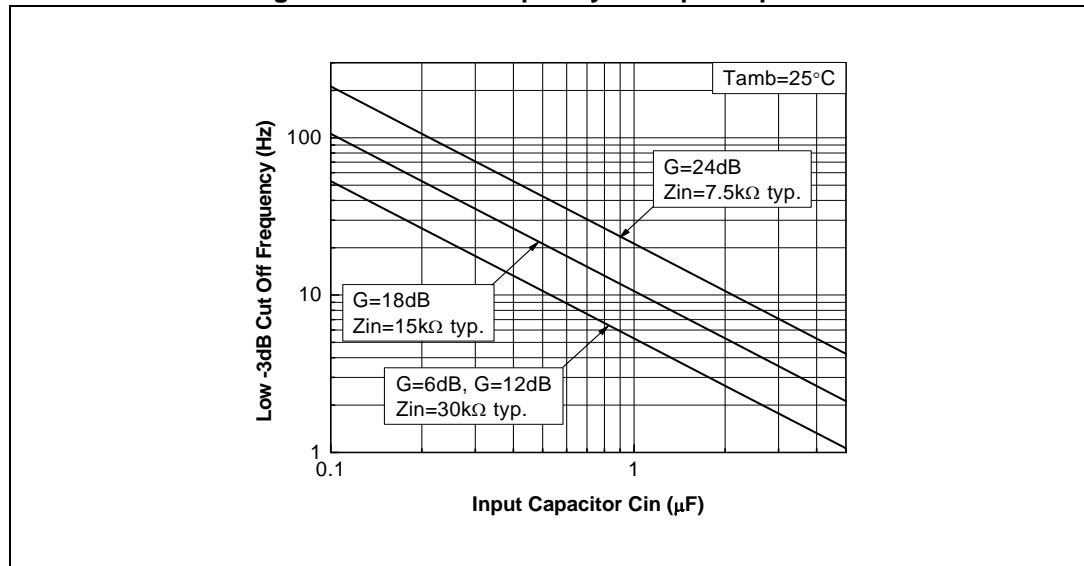
So, for a desired cut-off frequency  $F_{CL}$ ,  $C_{in}$  is calculated as follows.

$$C_{in} = \frac{1}{2 \cdot \pi \cdot Z_{in} \cdot F_{CL}}$$

with  $F_{CL}$  in Hz,  $Z_{in}$  in  $\Omega$  and  $C_{in}$  in F.

The input impedance  $Z_{in}$  is for the whole power supply voltage range and it changes with the gain setting. There is also a tolerance around the typical values (see [Table 6](#) to [Table 8](#)).

**Figure 36. Cut-off frequency vs. input capacitor**



## 4.5 Decoupling of the circuit

Power supply capacitors, referred to as  $C_{S1}$  and  $C_{S2}$ , are needed to correctly bypass the TS2012EI.

The TS2012EI has a typical switching frequency of 280 kHz and an output fall and rise time of approximately 5 ns. Due to these very fast transients, careful decoupling is mandatory.

A 1  $\mu$ F ceramic capacitor ( $C_{S1}$ ) between PVCC and PGND and one additional ceramic capacitor 0.1  $\mu$ F ( $C_{S2}$ ) are enough. A 1  $\mu$ F capacitor must be located as close as possible to the device PVCC pin in order to avoid any extra parasitic inductance or resistance created by a long track wire. Parasitic loop inductance, in relation with  $di/dt$ , introduces overvoltage that decreases the global efficiency of the device and may cause, if this parasitic inductance is too high, a breakdown of the TS2012EI. For filtering low-frequency noise signals on the power line, you can use a  $C_{S1}$  capacitor of 4.7  $\mu$ F or more.

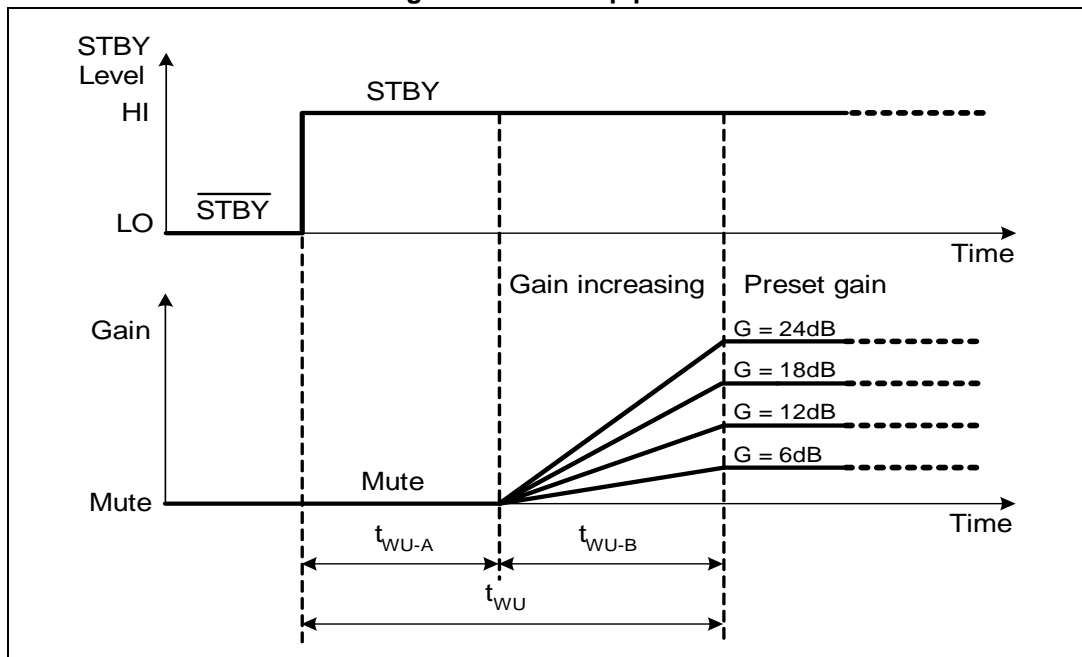
In addition, even if a ceramic capacitor has an adequate high frequency ESR (equivalent series resistance) value, its current capability is also important. A size of 0603 is a good compromise, particularly when a 4  $\Omega$  load is used.

Another important parameter is the rated voltage of the capacitor. A 1  $\mu$ F/6.3 V capacitor used at 5 V, loses about 50% of its value. With a power supply voltage of 5 V, the decoupling value, instead of 1  $\mu$ F, could be reduced to 0.5  $\mu$ F. As  $C_S$  has particular influence on the THD+N in the medium-to-high frequency region, this capacitor variation becomes decisive. In addition, less decoupling means higher overshoots, which can be problematic if they reach the power supply AMR value (6 V).

## 4.6 Wake-up time ( $t_{WU}$ ) and shutdown time ( $t_{STBY}$ )

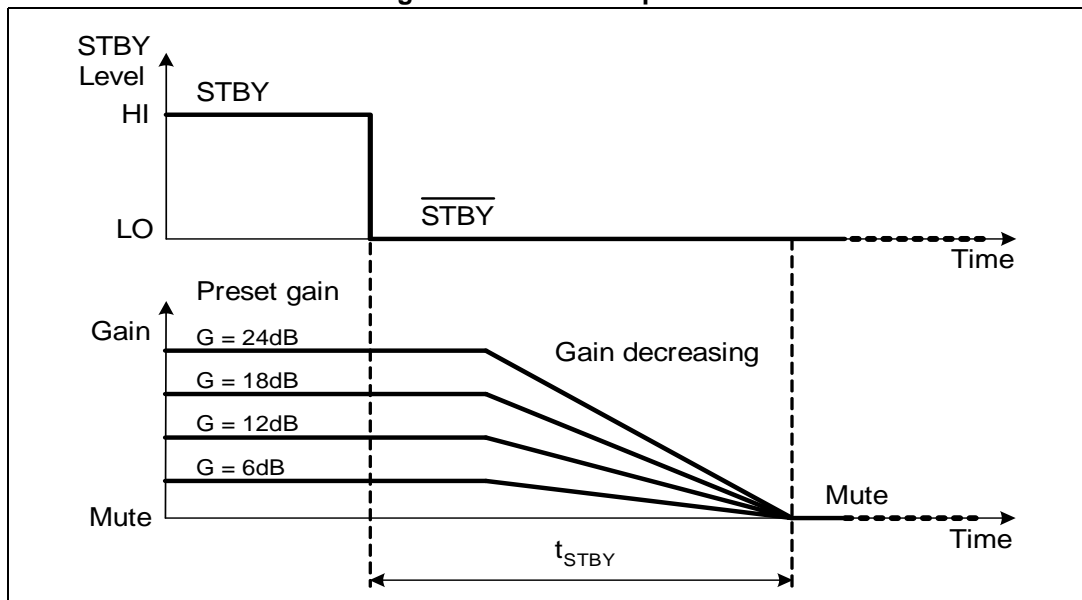
During the wake-up sequence when the standby is released to set the device ON, there is a delay. The wake-up sequence of the TS2012EI consists of two phases. During the first phase  $t_{WU-A}$ , a digitally-generated delay, mutes the outputs. Then, the gain increasing phase  $t_{WU-A}$  begins. The gain increases smoothly from the mute state to the preset gain selected by the digital pins G0 and G1. This startup sequence avoids any pop noise during startup of the amplifier. Refer to [Figure 37: Wake-up phase](#)

Figure 37. Wake-up phase



When the standby command is set, the time required to set the output stage to high impedance and to put the internal circuitry in shutdown mode is called the standby time. This time is used to decrease the gain from its nominal value set by the digital pins G0 and G1 to mute and avoid any pop noise during shutdown. The gain decreases smoothly until the outputs are muted ([Figure 38](#)).

Figure 38. Shutdown phase





### 4.7 Consumption in shutdown mode

Between the shutdown pin and GND there is an internal 300 kΩ (+/-20%) resistor. This resistor forces the TS2012EI to be in shutdown when the shutdown input is left floating.

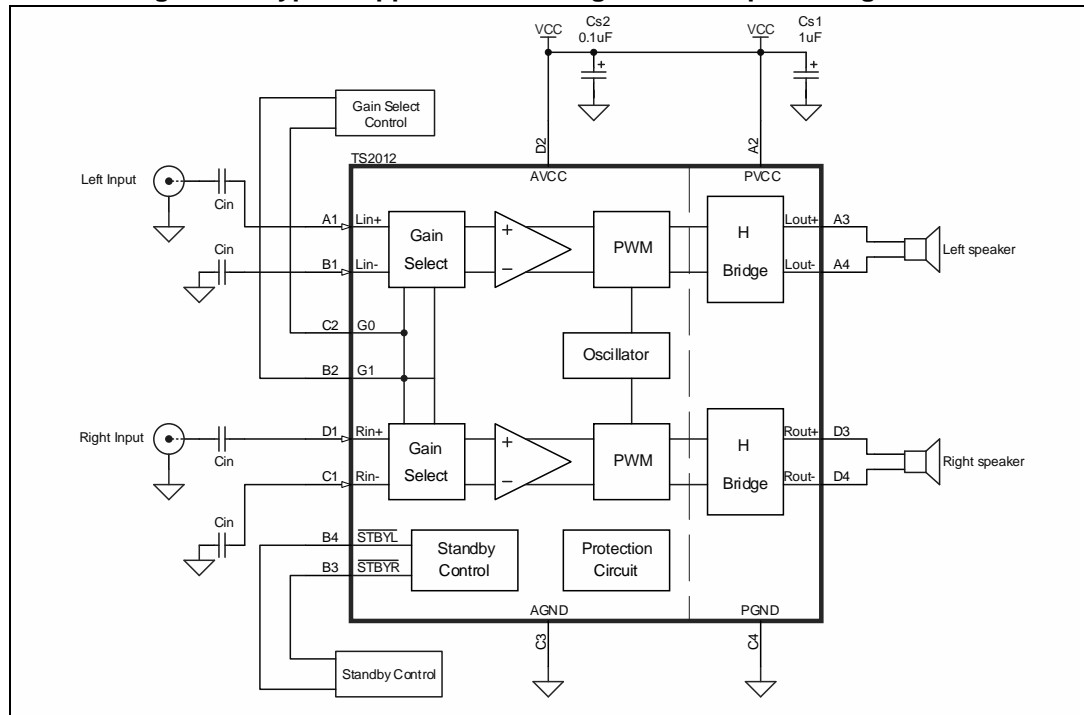
However, this resistor also introduces additional shutdown power consumption if the shutdown pin voltage is not at 0 V.

With a 0.4 V shutdown voltage pin for example, you must add  $0.4 \text{ V} / 300 \text{ k}\Omega = 1.3 \mu\text{A}$  typical ( $0.4 \text{ V} / 240 \text{ k}\Omega = 1.66 \mu\text{A}$  maximum) for each shutdown pin to the standby current specified in [Table 6](#) to [Table 8](#). Of course, this current will be provided by the external control device for the standby pins.

### 4.8 Single-ended input configuration

It is possible to use the TS2012EI in a single-ended input configuration. However, input coupling capacitors are mandatory in this configuration. [Figure 39](#) shows a typical single-ended input application.

**Figure 39. Typical application for single-ended input configuration**



## 4.9 Output filter considerations

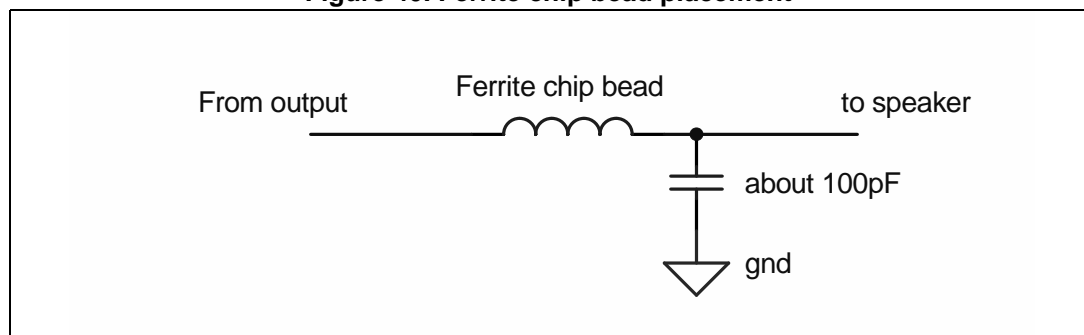
The TS2012EI is designed to operate without an output filter. However, due to very sharp transients on the TS2012EI output, EMI-radiated emissions may cause some standard compliance issues.

These EMI standard compliance issues can appear if the distance between the TS2012EI outputs and loudspeaker terminal are long (typically more than 50 mm, or 100 mm in both directions, to the speaker terminals). Because the PCB layout and internal equipment device are different for each configuration, it is difficult to provide a one-size-fits-all solution.

However, to decrease the probability of EMI issues, there are several simple rules to follow.

- Reduce, as much as possible, the distance between the TS2012EI output pins and the speaker terminals.
- Use a ground plane to "shield" sensitive wires.
- Place, as close as possible to the TS2012EI and in series with each output, a ferrite bead with a rated current of at least 2.5 A and an impedance greater than  $50 \Omega$  at frequencies above 30 MHz. If, after testing, these ferrite beads are not necessary, replace them by a short-circuit.
- Allow extra footprint to place, if necessary, a capacitor to short perturbations to ground ([Figure 40](#)).

**Figure 40. Ferrite chip bead placement**



In the case where the distance between the TS2012EI output and the speaker terminals is too long, it is possible to have low frequency EMI issues due to the fact that the typical operating frequency is 280 kHz. In this configuration, it is necessary to use the output filter represented in [Figure 1 on page 5](#) as close as possible to the TS2012EI.

## 4.10 Short-circuit protection

The TS2012EI includes output short-circuit protection. This protection prevents the device from being damaged in case of fault conditions on the amplifier outputs.

When a channel is in operating mode and a short-circuit occurs between two outputs of the channel or between an output and ground, the short-circuit protection detects this situation and puts the appropriate channel into standby. To put the channel back into operating mode, it is necessary to put the channel's standby pin to logical LO, and then back again to logical HI and wake up the channel.

## 4.11 Thermal shutdown

The TS2012EI device has an internal thermal shutdown protection in the event of extreme temperatures to protect the device from overheating. Thermal shutdown is active when the device reaches 150° C. When the temperature decreases to safe levels, the circuit switches back to normal operation.

## 5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

Figure 41. Flip Chip 16 package mechanical drawing

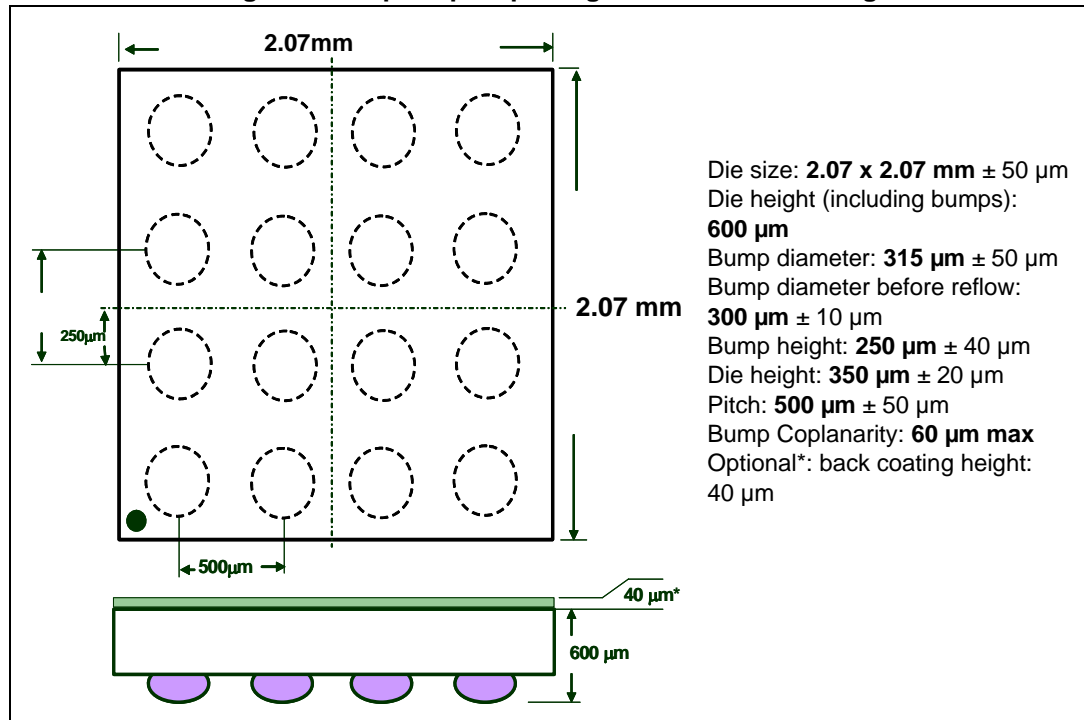


Figure 42. Pinout (top view)

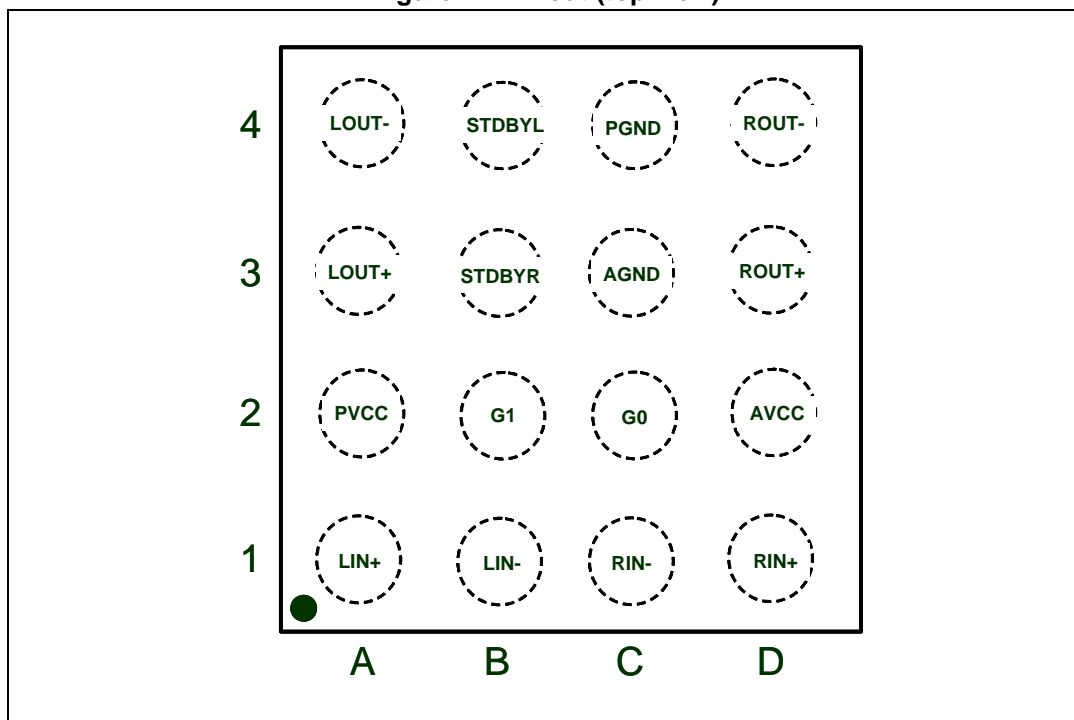


Figure 43. Marking (top view)

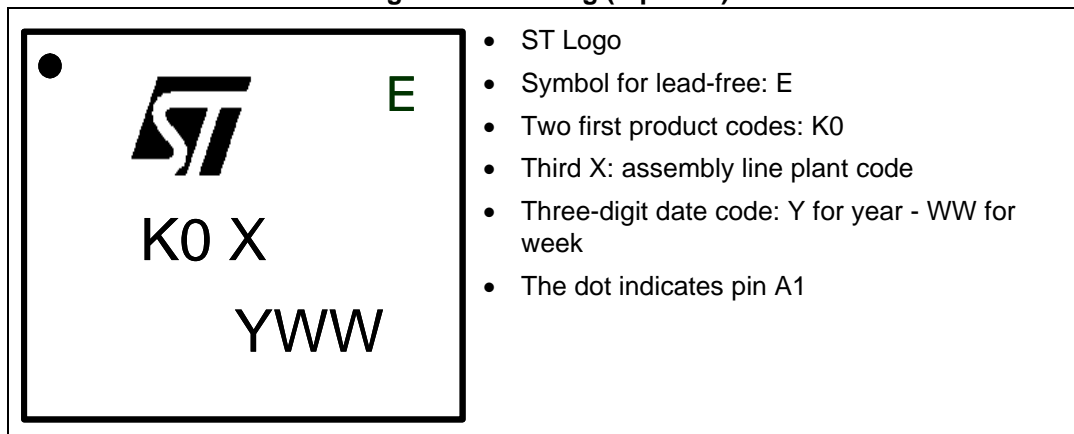


Figure 44. Tape and reel schematics (top view)

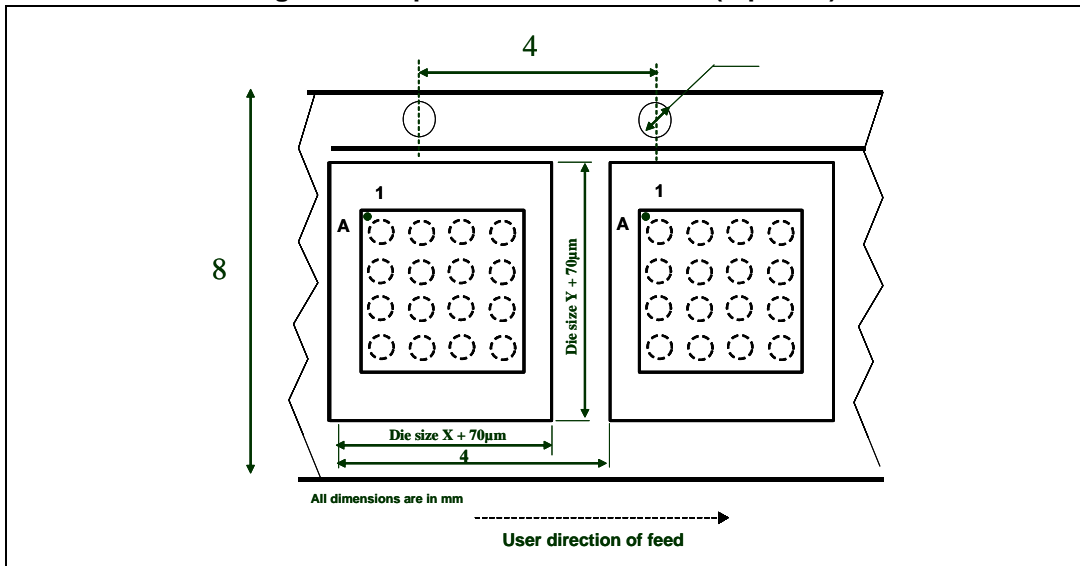
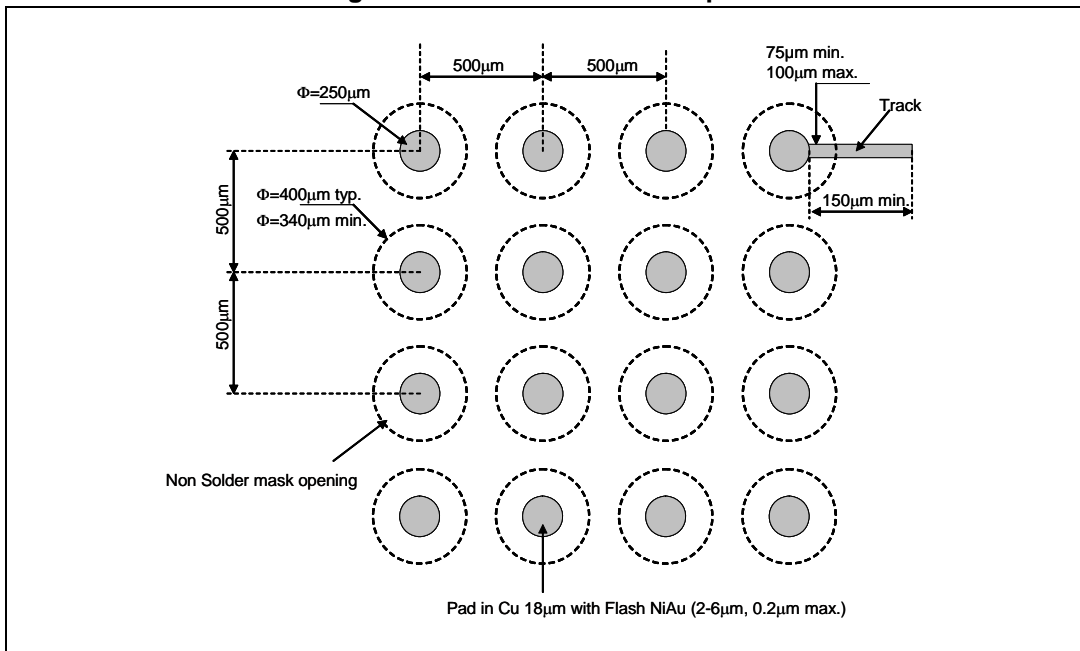


Figure 45. Recommended footprint



## 6 Revision history

Table 10. Document revision history

Date	Revision	Changes
01-Apr-2014	1	Initial release.

**Please Read Carefully:**

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

**UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.**

**ST PRODUCTS ARE NOT DESIGNED OR AUTHORIZED FOR USE IN: (A) SAFETY CRITICAL APPLICATIONS SUCH AS LIFE SUPPORTING, ACTIVE IMPLANTED DEVICES OR SYSTEMS WITH PRODUCT FUNCTIONAL SAFETY REQUIREMENTS; (B) AERONAUTIC APPLICATIONS; (C) AUTOMOTIVE APPLICATIONS OR ENVIRONMENTS, AND/OR (D) AEROSPACE APPLICATIONS OR ENVIRONMENTS. WHERE ST PRODUCTS ARE NOT DESIGNED FOR SUCH USE, THE PURCHASER SHALL USE PRODUCTS AT PURCHASER'S SOLE RISK, EVEN IF ST HAS BEEN INFORMED IN WRITING OF SUCH USAGE, UNLESS A PRODUCT IS EXPRESSLY DESIGNATED BY ST AS BEING INTENDED FOR "AUTOMOTIVE, AUTOMOTIVE SAFETY OR MEDICAL" INDUSTRY DOMAINS ACCORDING TO ST PRODUCT DESIGN SPECIFICATIONS. PRODUCTS FORMALLY ESCC, QML OR JAN QUALIFIED ARE DEEMED SUITABLE FOR USE IN AEROSPACE BY THE CORRESPONDING GOVERNMENTAL AGENCY.**

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2014 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

[www.st.com](http://www.st.com)