MP4050A

Non-Isolated, High-Brightness LED Driver with Enhanced Thermal Feature

The Future of Analog IC Technology

DESCRIPTION

The MP4050A is a constant current LED driver with an integrated 500V MOSFET. It is designed specifically for energy efficient and low-cost LED bulb replacement applications.

The MP4050A is designed to drive high-brightness LEDs from a universal AC grid input or DC input. The accurate output LED current is achieved by an averaging internal current feedback loop. Constant LED current is delivered quietly by switching the internal MOSFET at a frequency regulated above 22kHz.

The MP4050A can be powered directly by the high input voltage. An internal high-voltage current source regulates supply voltage without external circuitry.

Full protections features include integrated thermal current foldback, VCC under-voltage lockout (UVLO), open LED protection (OLP), short-circuit protection (SCP), and over-temperature protection (OTP). These features make the MP4050A an ideal solution for simple, off-line, and non-isolated LED applications.

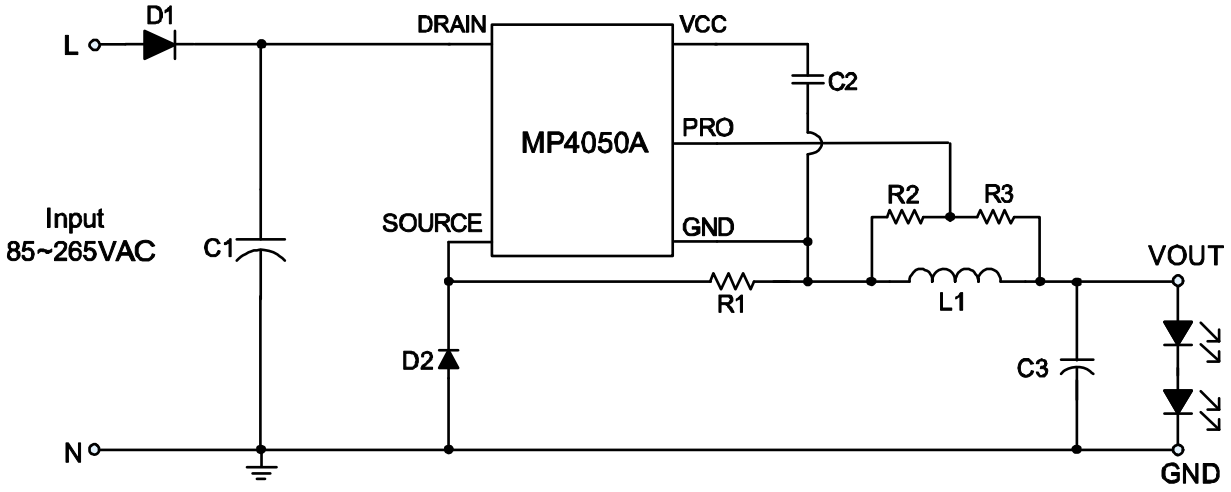
FEATURES

- Constant Current LED Driver
- Integrated 500V/8Ω MOSFET
- Low VCC Operating Current
- Maximum Frequency Limit
- Audible Noise Restrain
- Internal High-Voltage Current Source
- Internal 200ns Leading Edge Blanking
- Integrated Thermal Current Foldback
- Thermal Shutdown (Auto Re-Start with Hysteresis)
- VCC Under-Voltage Lockout with Hysteresis
- Open LED Protection
- Short-Circuit Protection
- Auto-Restart Function
- Available in TSOT23-5/SOIC-8 Packages

APPLICATIONS

- AC/DC or DC/DC LED Driver Application
- General Illumination
- Industrial Lighting
- Automotive/Decorative LED Lighting

TYPICAL APPLICATION

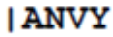


ORDERING INFORMATION

Part Number	Package	Top Marking
MP4050AGJ*	TSOT23-5	*See Below*
MP4050AGS**	SOIC-8	

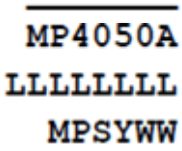
* For Tape & Reel, add suffix –Z (e.g. MP4050AGJ–Z);
** For Tape & Reel, add suffix –Z (e.g. MP4050AGS–Z).

TOP MARKING (TSOT23-5)



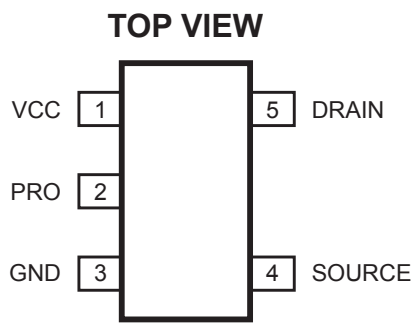
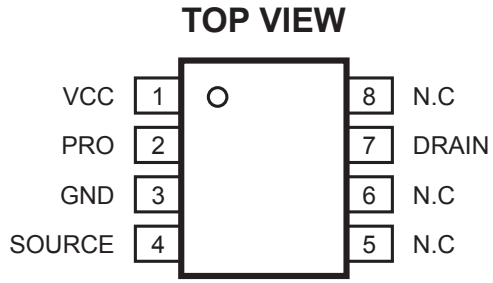
ANV: Product Code of MP4050AGJ;
Y: Year Code.

TOP MARKING (SOIC-8)



MP4050A: Product Code of MP4050AGS;
LLLLLLLL: Lot Number;
MPS: MPS Prefix;
Y: Year Code;
WW: Week Code.

PACKAGE REFERENCE

TSOT23-5	SOIC-8
	

ABSOLUTE MAXIMUM RATINGS (1)

DRAIN to SOURCE .....-0.3V to 500V
VCC, SOURCE to GND .....-0.3V to 6.5V
PRO to GND .....-0.7V to 6.5V
Source Current on PRO 4mA
Continuous Power Dissipation (T_A = +25°C) (2)
TSOT23-5 ..... 1.25W
SOIC-8 ..... 1.3W
Lead Temperature .....260°C
Storage Temperature..... -60°C to +150°C
ESD Capability Human Body Mode 2.0kV
CDM ESD Capability..... 2.0kV

Recommended Operating Conditions (3)

Supply Voltage VCC Range.....4.1V to 5.0V

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
TSOT23-5	100	55	°C/W
SOIC-8	96	45	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

Typical values are VCC =5V, T_J = 25°C, unless otherwise noted.
Minimum and maximum values are at VCC =5V, T_J = -40°C to +125°C, unless otherwise noted, guaranteed by characterization.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Start-Up Current Source (DRAIN)						
Internal Regulator Supply Current	$I_{REGULATOR}$	VCC=0V, V_{DRAIN}=100V	3.8	5	6.1	mA
Leakage Current from DRAIN	I_{D_LKG}	VCC=6V, V_{DRAIN}=500V		14	22	µA
Supply Voltage Management (VCC)						
VCC Increasing Level: Internal Regulator Stops & IC Starts Working	VCC_{OFF}	VCC Rising Edge	4.00	4.35	4.70	V
VCC Normal Level	VCC_{NOR}	Normal Operation		4.25		V
VCC Decreasing Level: Internal Regulator Turn-On	VCC_{ON}	VCC Falling Edge	3.85	4.15	4.50	V
VCC Hysteresis: Regulator On/Off	VCC_{OFF-ON}		0.11	0.20	0.28	V
VCC Decreasing Level: IC Stops	VCC_{STOP}	VCC Falling Edge	3	3.4	3.8	V
VCC Hysteresis: Regulator Off & IC Stops Working	$VCC_{OFF-STOP}$		0.93	1.25	1.6	V
VCC Decreasing Level: Protection Phase Ends	VCC_{PRO}	VCC Falling Edge	1.9	2.35	2.8	V
Internal IC Consumption	I_{CC}	VCC=4.3V, f_{SW}=33kHz, Duty=84%		350	425	µA
Internal IC Consumption at Latch-Off Phase	I_{CC_LATCH}			18	32	µA
Internal MOSFET (DRAIN to SOURCE)						
Breakdown Voltage	V_{BRDSS}	I_D=80µA	500			V
DRAIN SOURCE On-State Resistance	$R_{DS(ON)}$	I_D=10mA, T_J=25°C		8	12	Ω
		VCC=VCC_{STOP} + 50mV, I_D=10mA, T_J=25°C		8	12	Ω
Current Sampling Management (SOURCE)						
Peak Current Limit at Normal Operation	V_{LIMIT}		0.4	0.46	0.52	V
Leading Edge Blanking	t_{LEB}		130	200	310	ns
Feedback Threshold: Turn-On High-Side MOSFET	V_{REF}	Regulate the Average Current	0.187	0.196	0.205	V
Minimum Off-Time Limitation	t_{OFF_MIN}	Normal Operation	3.4	4.7	6.2	µs
	$t_{OFF\_MIN\_ST}$	The 1st 32 Switching Cycles at Start-Up		t_{OFF_MIN} ×3.5		µs
		The 2nd 32 Switching Cycles at Start-Up		t_{OFF_MIN} ×2		µs
		The 3rd 32 Switching Cycles at Start-Up		t_{OFF_MIN} ×1.2		µs
Maximum On-Time Limitation	t_{ON_MAX}		16	25	37	µs

ELECTRICAL CHARACTERISTICS *(continued)*

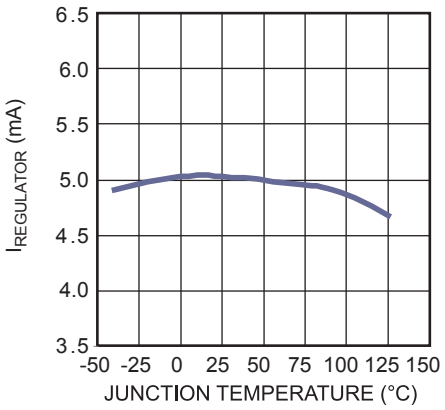
Typical values are VCC =5V, T_J = 25°C, unless otherwise noted.
Minimum and maximum values are at VCC =5V, T_J = -40°C to +125°C, unless otherwise noted, guaranteed by characterization.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Over-Voltage Protection (PRO)						
Over-Voltage Threshold	V_{OVP}		1.85	2	2.15	V
Time Constraint on OVP Comparator	t_{OVP}			21	32	µs
Thermal Protection						
Thermal Foldback Threshold (5)	T_{START}			145		°C
Thermal Shutdown Threshold (5)	T_{SD}			160		°C
Thermal Shutdown Recovery Hysteresis (5)	T_{HYS}			50		°C

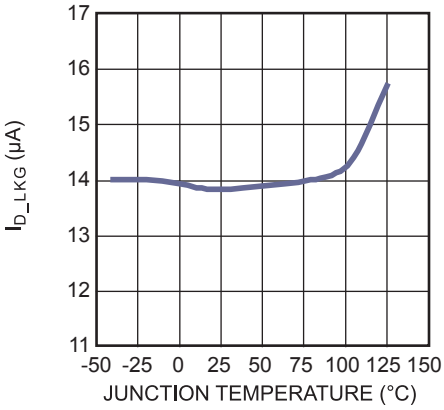
Notes:
5) Guaranteed by characterization.

TYPICAL CHARACTERISTICS

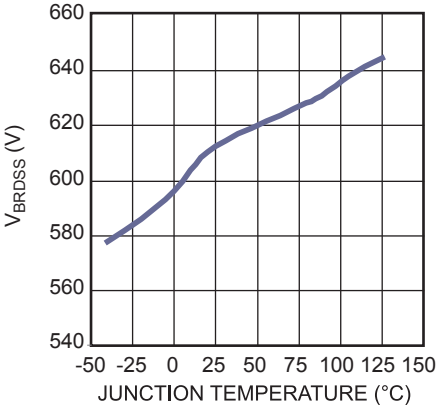
Internal Regulation Currentt vs. Junction Temperature



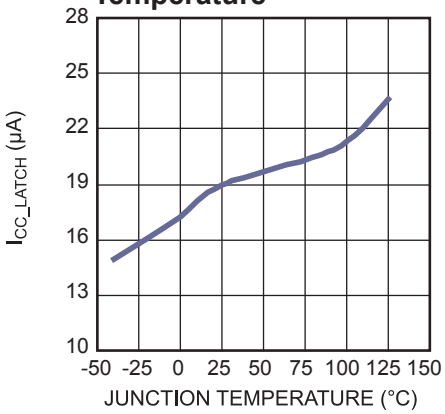
Leakage Current vs. Junction Temperature



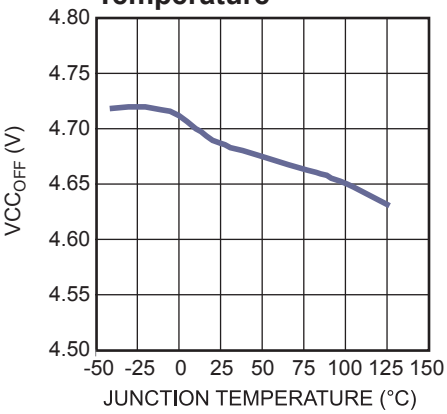
Breakdown Voltage vs. Junction Temperature



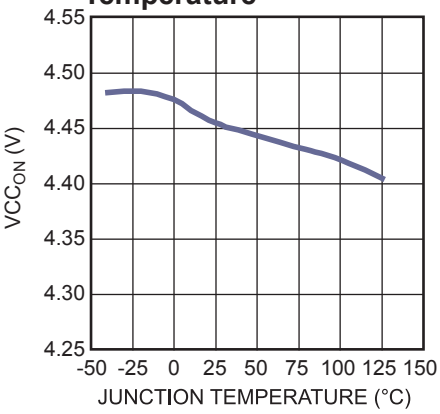
VCC Current In Latch Phase vs. Junction Temperature



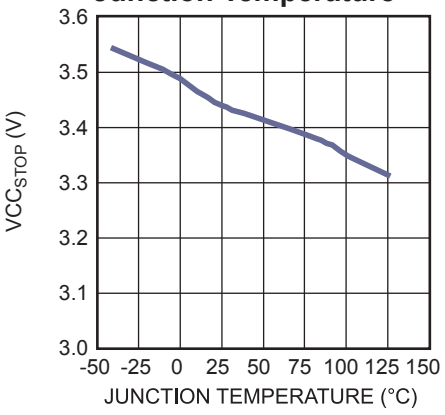
VCC Regulator Off Threshold vs. Junction Temperature



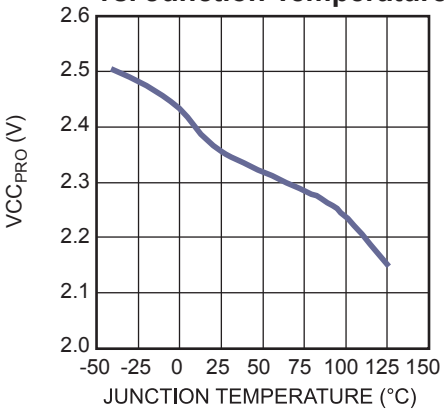
VCC Regulator On Threshold vs. Junction Temperature



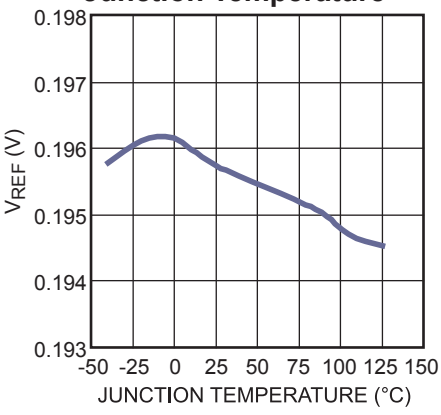
VCC Stop Threshold vs. Junction Temperature



VCC Protection Threshold vs. Junction Temperature

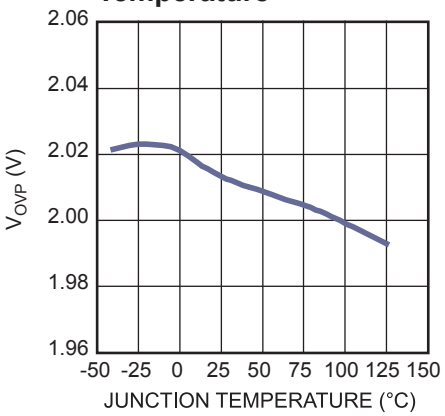


Feedback Reference vs. Junction Temperature

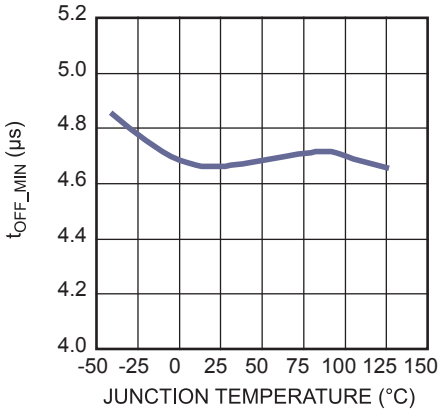


TYPICAL CHARACTERISTICS *(continued)*

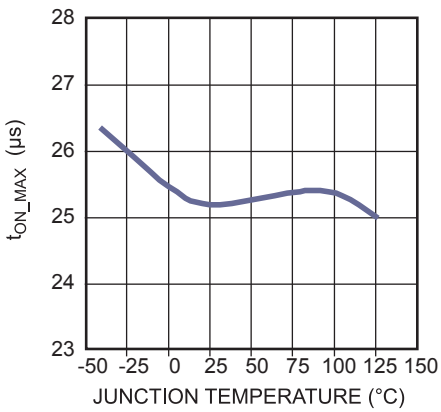
Over-Voltage Protection Reference vs. Junction Temperature



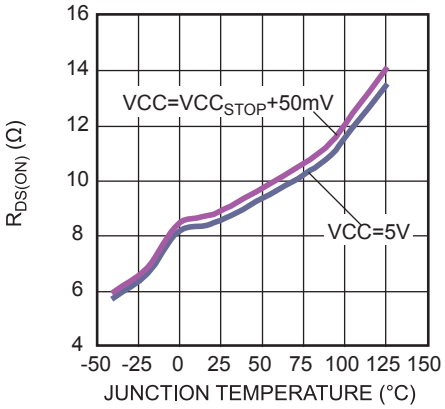
Minimum Off Time vs. Junction Temperature



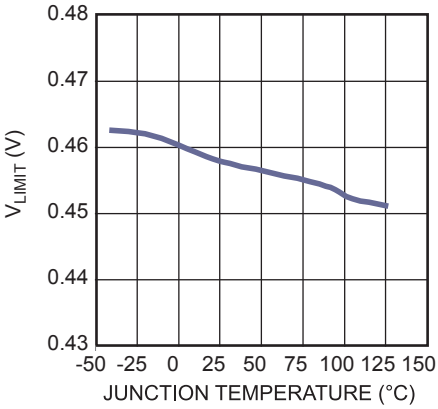
Maximum On Time vs. Junction Temperature



On-State Resistance vs. Junction Temperature



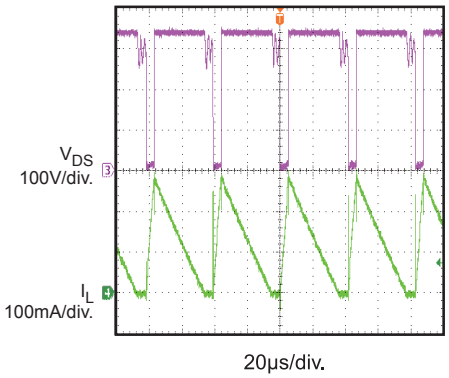
Peak Current Limit vs. Junction Temperature



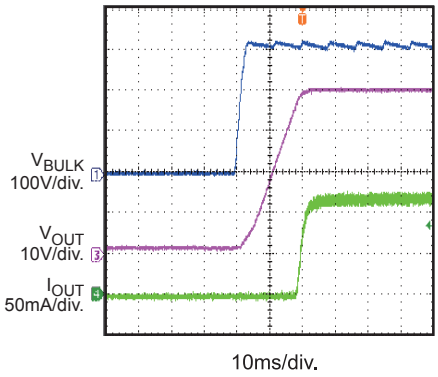
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 230VAC, 13 LEDs in series, V_{OUT} = 40V, I_{LED}=115mA, L = 4.7mH, C_{OUT}=47µF, T_A = 25°C, unless otherwise noted.

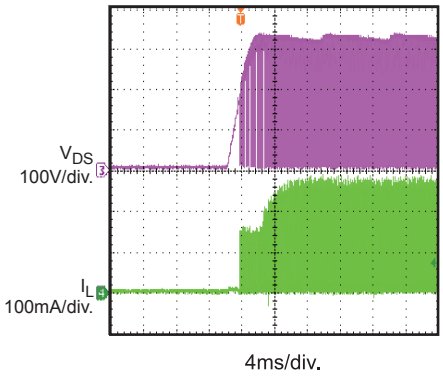
Steady State



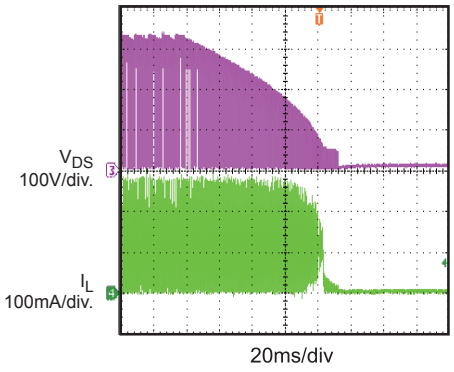
Turn-On Delay



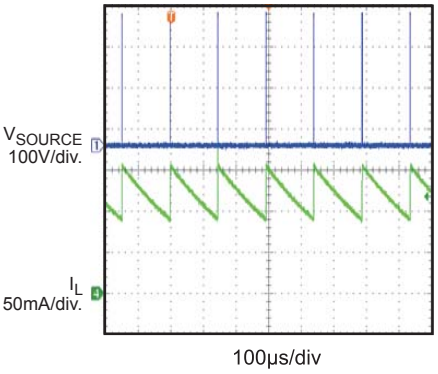
Input Power Start-Up



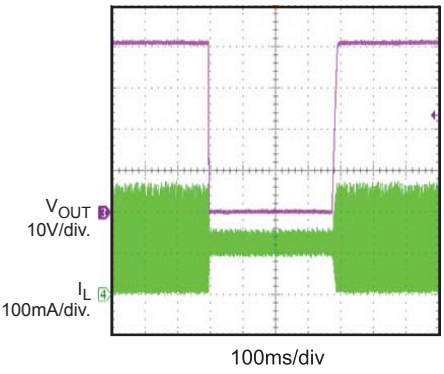
Input Power Shutdown



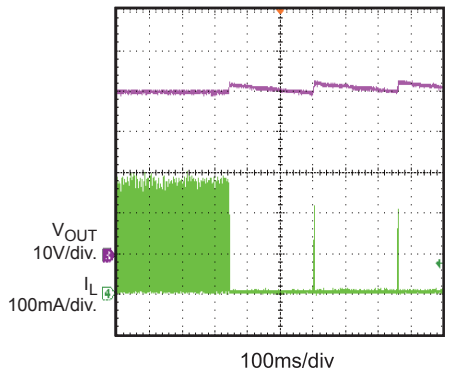
SCP



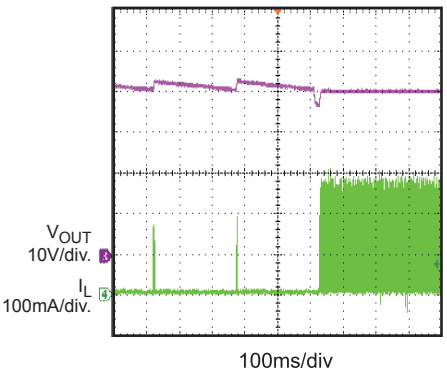
SCP Entry & Recorvery



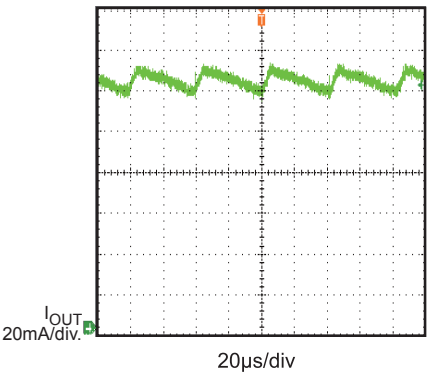
OVP Entry



OVP Recovery



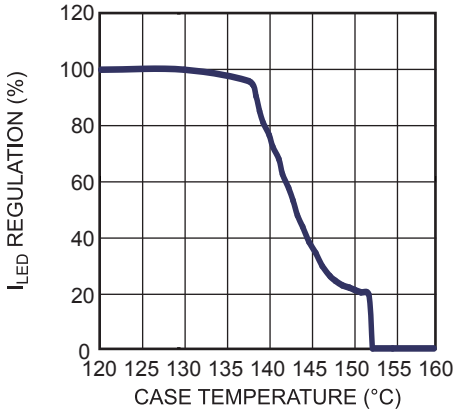
Output-Current Ripple



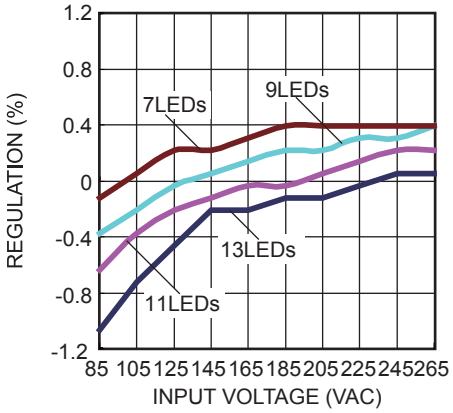
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 230VAC, 13 LEDs in series, V_{OUT} = 40V, I_{LED}=115mA, L = 4.7mH, C_{OUT}=47µF, T_A = 25°C, unless otherwise noted.

Thermal Current Foldback Curve



Line & Load Regulation



PIN FUNCTIONS

Pin #		Name	Description
TSOT23-5	SOIC-8		
1	1	VCC	**Power Supply.** Supply power for the control signals and the high-current MOSFET. Bypass to ground with an external bulk capacitor.
2	2	PRO	**Open LED Detection Input.** During the turn-off interval, if PRO voltage is higher than V_{OVP}, the over-voltage protection is triggered.
3	3	GND	**Ground.** The reference ground for the control signal and the gate drive signal.
4	4	SOURCE	**Source of Internal Power MOSFET & Feedback Input.** Connect current-sensing resistor from SOURCE to GND to set the LED current.
5	7	DRAIN	**Drain of Internal Power MOSFET & Integrated HV Current Source Input.**
--	5, 6, 8	NC	**No Connection.** Do Not Connect**.**

FUNCTION BLOCK DIAGRAM

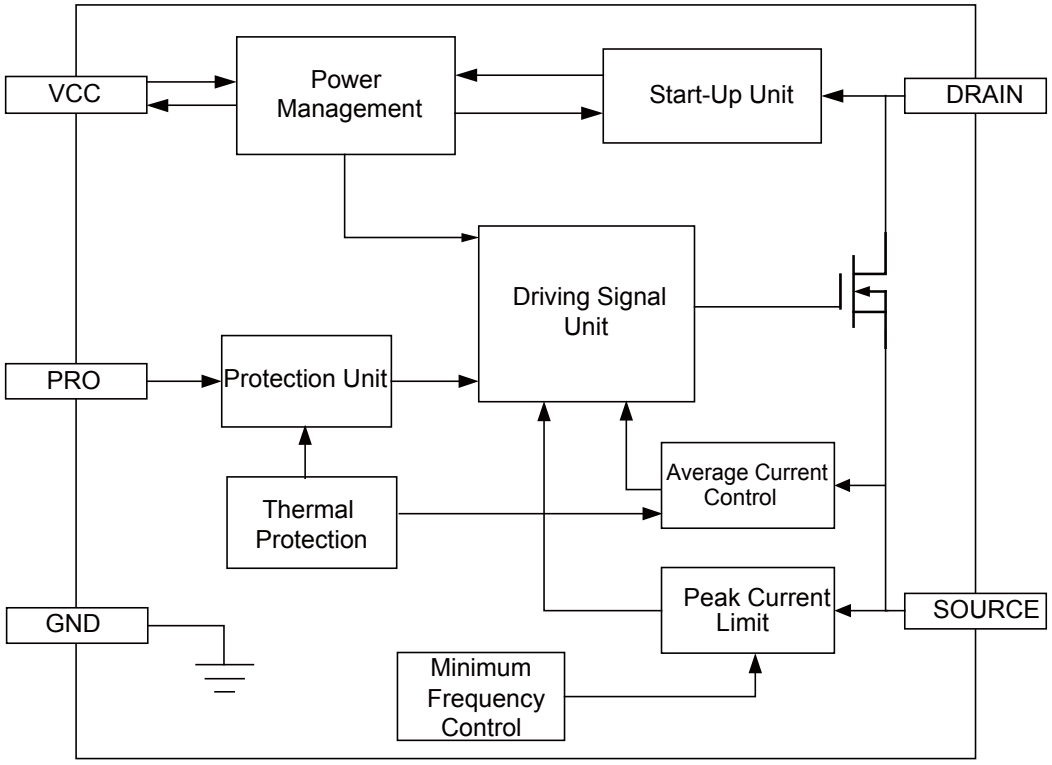


FIGURE 1. Functional Block Diagram

OPERATION

The MP4050A is a non-isolated, cost-effective, high-efficiency converter designed to drive high-brightness LEDs from a universal AC grid input or DC input. As shown in the typical application diagram (see Fig. 1), the regulator is designed to operate with a minimum number of external components.

Start-Up and Under-Voltage Lockout (UVLO)

Initially, the chip is self-supplied by the internal high-voltage VCC regulator (which is drawn from DRAIN). The IC starts switching and the internal high-voltage regulator turns off as soon as the VCC reaches VCC_{OFF}. When VCC drops below VCC_{ON}, the internal high-voltage regulator turns on again to charge the external VCC capacitor. Finally, VCC is regulated at VCC_{NOR} for normal operation.

A small capacitor with several μF capacitances is enough to hold on to the VCC supply voltage. Also, a smaller capacitor reduces component cost. When VCC drops below VCC_{STOP}, the IC stops working and the internal high-voltage regulator re-charges the VCC capacitor.

When fault conditions occur (such as open LED protection or over-temperature protection), the MP4050A stops working, and an 18μA internal sink current source discharges the VCC capacitor. After VCC drops below VCC_{PRO}, the internal high-voltage regulator recharges the VCC capacitor again. The re-start time can be calculated by the following equation,

$$t_{RESTART} = C_{VCC} \times \frac{VCC_{NOR} - VCC_{PRO}}{18\mu A} + C_{VCC} \times \frac{VCC_{OFF} - VCC_{PRO}}{5mA}$$

Fig. 2 shows the typical waveforms with VCC under-voltage lockout.

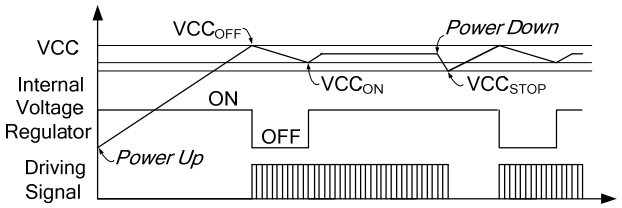


FIGURE 2. VCC Under-Voltage Lockout (UVLO)

Constant-Current Operation

The MP4050A is a fully integrated regulator. The internal feedback logic responds to the internal sample and hold circuit to achieve constant output-current regulation. The voltage of the internal sampling capacitor (V_{FB}) is compared to the internal reference (V_{REF}) when the sampling capacitor voltage (V_{FB}) falls below the reference voltage (which indicates an insufficient output current). Then the integrated MOSFET is turned on. The on period is determined by the peak current limit. After the on period elapses, the integrated MOSFET is turned off (see Fig. 3).

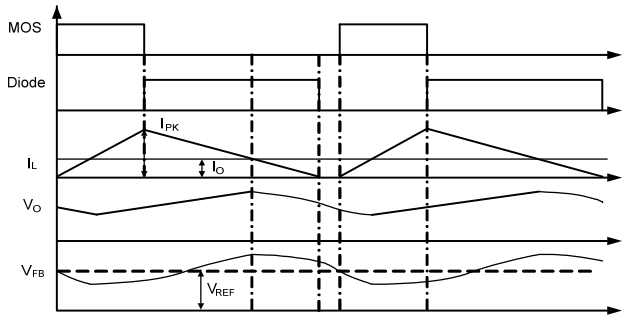


FIGURE 3. V_{FB} vs. I_{OUT}

Thus, by monitoring the internal sampling capacitor voltage, the output current can be regulated. The output current is determined by the following equation:

$$I_{OUT} = \frac{V_{REF}}{R_S}$$

The peak inductor current at normal operation can be obtained with the following equation:

$$I_{PK} = \frac{V_{LIMIT}}{R_S}$$

Where R_S is the sensing resistance connected from SOURCE to GND.

Minimum Operating Frequency Limit

The MP4050A incorporates a minimum operating frequency (22kHz) to eliminate audible noise.

When the operating frequency is less than 22kHz, the internal peak-current regulator decreases the peak-current value to keep the operating frequency constant at about 22kHz.

If the inductance is too large to make the operating frequency drop to the minimum operating frequency, the converter enters CCM operation. Generally, the converter works in DCM when the operating frequency is larger than 22kHz for normal operation.

Minimum Off-Time Limit

A minimum off-time limit is implemented. During normal operation, the minimum off-time limit is 4.7μs. During the start-up period, the minimum off-time limit is shortened gradually from 16.45μs to 4.7μs (see Fig. 4). Each minimum off-time limit maintains 32 switching cycles. This soft-start function enables a safe start-up.

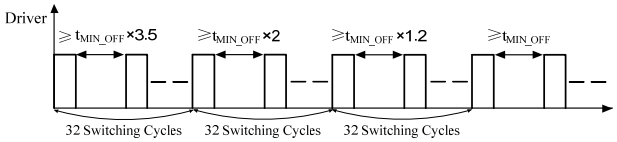


FIGURE 4. Minimum Off-Time Limit at Start-up

Thermal Shutdown (TSD)

To prevent thermal damage to the system and IC, the chip reduces the reference to decrease the output power if the junction temperature exceeds 145°C. This limits the rising temperature speed of the IC. Typically, the reference voltage drops to around 20% when the junction temperature rises to 160°C. If the temperature exceeds 160°C, the MP4050A stops switching, and the IC is latched off. Once the junction temperature drops below 110°C, the chip resumes operation.

Open LED Protection (OLP)

If PRO voltage (V_{PRO}) is higher than V_{OVP} when the MOSFET turns off, the MP4050A stops working, and a re-start cycle begins. Open LED protection operates in hiccup mode. The MP4050A monitors the PRO voltage continuously, and the VCC cap is discharged and charged repeatedly. The MP4050A resumes work once the fault disappears.

Short-Circuit Protection (SCP)

When an LED short circuit occurs, the switching off time is extended. Due to the minimum operating frequency limit, the IC can reduce automatically the switching frequency and achieve close loop control. Then the output power at this condition is limited within a safe range. The MP4050A resumes work in normal operation once the device recovers from the short circuit.

Leading Edge Blanking (LEB)

Internal leading edge blanking (LEB) is employed to prevent a switching pulse from terminating prematurely due to parasitic capacitance discharging when the MOSFET turns on. During the blanking time, the path from SOURCE to the current comparator input is blocked (see Fig. 5)

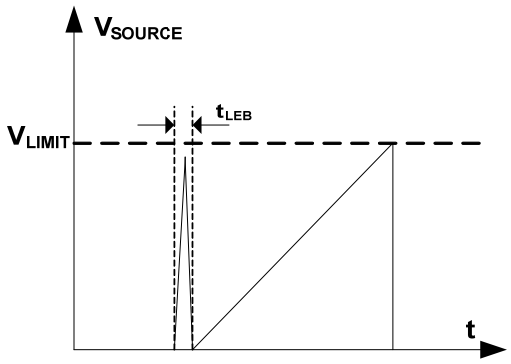


FIGURE 5. Leading Edge Blanking (LEB)

APPLICATION INFORMATION

Component Selection

Input Capacitor

The input capacitor is used to supply DC input voltage to the converter. Fig. 6 shows the typical DC bus voltage waveform of a full-bridge rectifier.

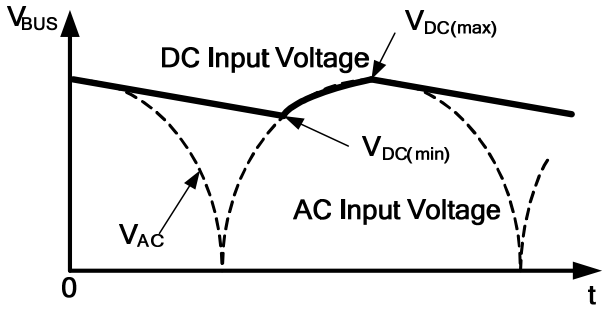


FIGURE 6. Input Voltage Waveform

When a full-bridge rectifier is used, the input capacitor is set usually as 2μF/W for the universal input range. With a low-power output, the half-bridge rectifier can be used with a bigger capacitor.

Very low DC input voltage causes thermal problems in LED applications with buck topology. The minimum DC voltage is limited by the maximum duty cycle of the MP4050A as follows:

$$V_{DC(MIN)} > \frac{V_O \cdot (t_{ON\_MAX} + t_{OFF\_MIN})}{t_{ON\_MAX}}$$

Inductor

The MP4050A has a minimum off-time limit and maximum on-time limit. Both time limits affect the inductance. The maximum and minimum inductance values can be obtained as follows:

$$L_m < L_{MAX} = \frac{(V_{DC(MIN)} - V_O) \cdot t_{ON\_MAX}}{I_{PK}}$$

$$L_m > L_{MIN} = \frac{V_O \cdot t_{OFF\_MIN}}{I_{PK}}$$

If the inductance is too large, the converter enters CCM, and the frequency drops to the minimum operating frequency. If this occurs, the reverse recovery of the freewheeling diode results in more power loss. Normally, it's better to have the converter operate in DCM. The following expression calculates the limit of the minimum operating frequency:

$$L_m < \frac{2 \cdot I_O}{f_{SW\_MIN} \cdot (\frac{1}{V_{DC(MIN)} - V_O} + \frac{1}{V_O}) \cdot I_{PK}^2}$$

Freewheeling Diode

The diode's maximum reverse-voltage rating is higher than the maximum input voltage. The current rating of the diode is determined by the output current (which is larger than 1.5 to 2 times the output current).

Slow recovery diodes cause excessive leading edge current spikes during start-up. The long reverse-recovery time of the freewheeling diode affects efficiency and the operation of the system. An ultrafast diode (t_{rr}<75ns), such as WUGC10JH or EGC10GH, is recommended.

Output Capacitor

An output capacitor is required to filter the inductance current and maintain the DC output voltage.

The output-current ripple is reduced by using a bigger output capacitor. A low ESR capacitor is necessary in low-temperature applications.

If the output-voltage ripple is limited, ceramic, tantalum, or low ESR electrolytic capacitors are recommended. The output-voltage ripple can be estimated by the following equations:

$$V_{CCM\_Ripple} = \frac{\Delta i}{8 f_{SW} C_O} + \Delta i \cdot R_{ESR} \quad \text{in CCM}$$

$$V_{DCM\_Ripple} = \frac{I_O}{f_{SW} C_O} \cdot (\frac{I_{PK} - I_O}{I_{PK}})^2 + I_{PK} \cdot R_{ESR} \quad \text{in DCM}$$

Sensing Resistor

Choose an appropriate sensing resistor for good output-current regulation. The right resistor guarantees stable output-current regulation in high/low temperature conditions. The sensing resistor should have 1% tolerance. Placing two 1% tolerance sensing resistors in parallel further improves the resistance error. A resistor with a ± 400PPM/°C temperature coefficient can be used for better output-current regulation in high/low temperature conditions.

PRO Feedback Resistor Divider

The PRO feedback resistor divider is used to detect an over-voltage fault condition. Fig. 7 shows the PRO feedback resistor divider's connection.

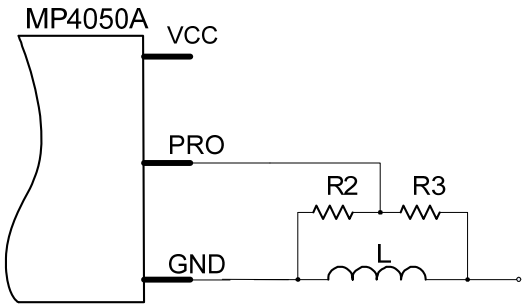


FIGURE 7. PRO Feedback Resistor Divider

The over-voltage protection threshold can be calculated with the following equation:

$$V_{OUT\_OVP} = V_{OVP} \cdot \frac{R2 + R3}{R2} - V_D$$

Where V_D is the freewheeling diode forward voltage drop.

The upper feedback resistor (R3) should be larger than 100kΩ to avoid an efficiency reduction in the application. A 1% tolerance type is recommended to achieve accurate protection when open LED occurs.

R2 has a small 0603 package. Taking the voltage rating of the dielectric into consideration, R3 is recommended to have a minimum 1206 package.

Dummy Load

The dummy load is used to consume the power transferred to the output capacitor in OVP hiccup mode without any power consumption.

Normally, a dummy load less than 1mA is recommended. A dummy load less than 1mA does not deteriorate system efficiency and also guarantees normal, open LED protection.

PRO Decoupling Capacitor

The floating GND is sensitive to the voltage noise spike in a high-side buck solution. Generally, the time constraint on the OVP comparator mechanism is sufficient to shield the noise against an open LED fault mistrigger. Sometimes, a decoupling cap is also applied between PRO and GND.

A ceramic capacitor around 30 pF is used in SOIC-8 package applications. For the smaller TSOT23-5 package, no less than a 100pF ceramic capacitor is recommended. Fig. 8 shows the PRO decoupling capacitor connection.

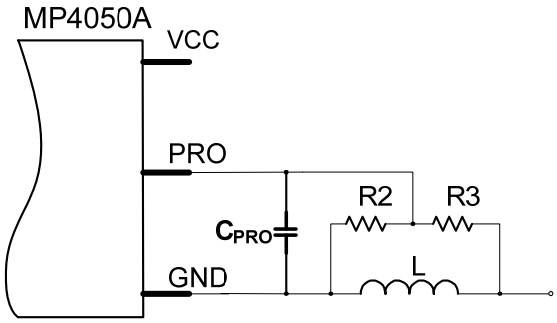


FIGURE 8. Decoupling Capacitor

PRO Time Constant

The MP4050A detects the PRO voltage to judge the open LED condition when internal the MOSEFET turns off. If the PRO decoupling capacitor is connected, the PRO time constant (τ) should satisfy the following expression to guarantee normal open LED protection:

$$\tau = C_{PRO} \cdot \frac{R2 \cdot R3}{R2 + R3} < 1\mu s$$

Power Factor (PF)

The MP4050A is designed mainly for non-isolated, space constrained, and cost sensitive LED driver solutions. The MP4050A is the best option for the PF>0.5 under 120VAC input requirement. The input capacitance is reduced to achieve the highest possible power factor as PF>0.7 @ 120VAC and PF>0.5 @ 230VAC (if the output-current regulation is not limited).

Surge

Select the appropriate input capacitance to obtain good surge performance. With the input capacitor C2 (4.7μF) and C3 (4.7μF) in Fig. 11, the board can pass a 1kV differential input line 1.2/50μs surge test (IEC61000-4-5). It is recommended to increase the input capacitor value to suppress a surge test above 1kV. As for the high PF required, applications with lower input capacitor values give a greater voltage rise. Typically, a metal oxide varistor (MOV) is required to pass a surge test above 1kV.

Table 1 shows the input capacitor values required to pass the differential surge test.

TABLE 1. Recommended Input Capacitance

Surge Voltage	500V	1kV	1.5kV	2kV
C2	3.3μF	4.7μF	4.7μF	Shown in Fig. 9
C3	3.3μF	4.7μF	10μF	

The board can pass the 2kV differential surge test by adopting the circuit setup below (see Fig. 9):

1. Add a MOV RV1 (TVR14431).
2. Add a fuse F1 (SS-5-2A).

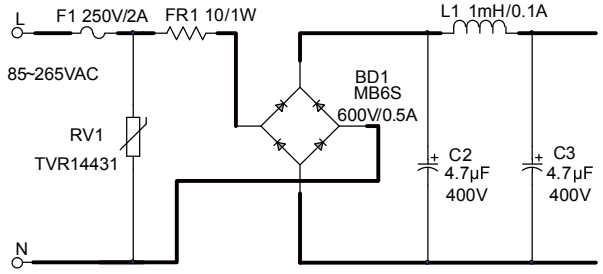
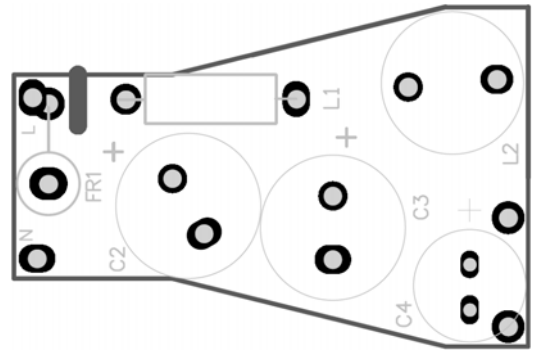
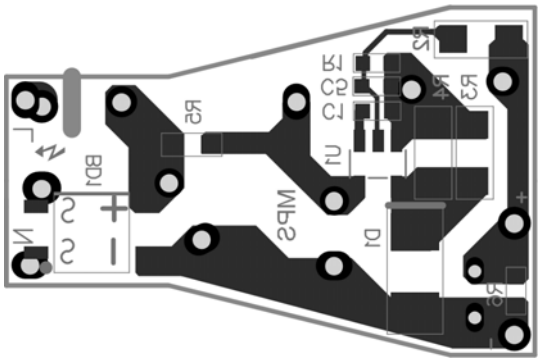


FIGURE 9. 2kV Surge Solution



Top Layer



Bottom Layer

Figure 10. Recommended PCB Layout

PCB Layout Guidelines

Efficient PCB layout is critical to achieve reliable operation, good EMI, and good thermal performance, especially in very small sized LED applications. For best results, refer to Fig. 10 and follow the guidelines below:

1. Keep the loop formed between the DRAIN to SOURCE, inductor, freewheeling diode, and output capacitor as small as possible for better EMI.
2. Ensure the AC input is far away from the switching nodes to minimize the noise coupling that may bypass the input filter.
3. Place the VCC and PRO capacitors close to the IC and GND.
4. Place the PRO feedback resistor as close to PRO as possible and minimize the feedback sampling loop to minimize the noise coupling route.

5. Keep the copper area connected to SOURCE short (in the high-side buck topology) to minimize EMI with the thermal constraints of the design (since SOURCE is a switching node).
6. Maximize the connection of the copper area to DRAIN to improve heat sink (since DRAIN is a static node connected to the DC input).

TYPICAL APPLICATION CIRCUITS

Fig. 11 shows a typical application example of a 40V, 115mA non-isolated, buck topology LED driver using MP4050AGJ.

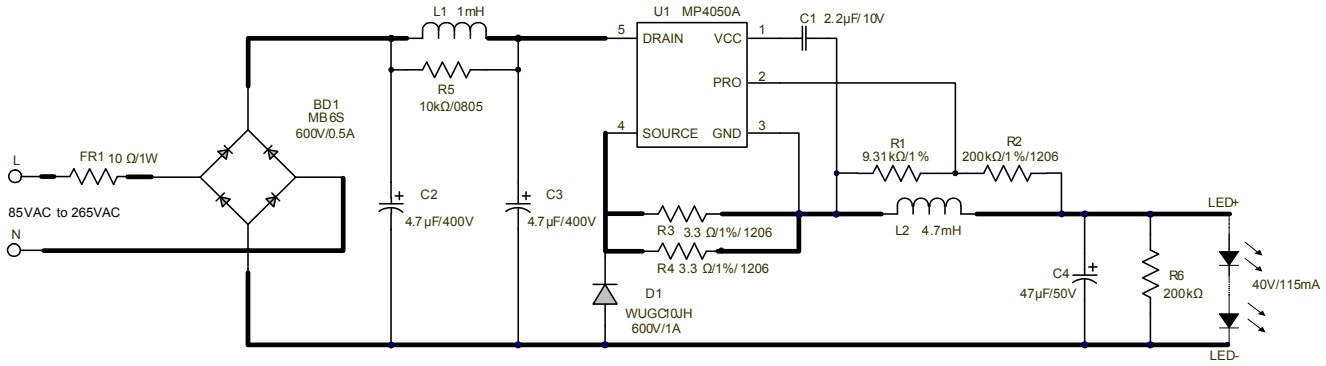
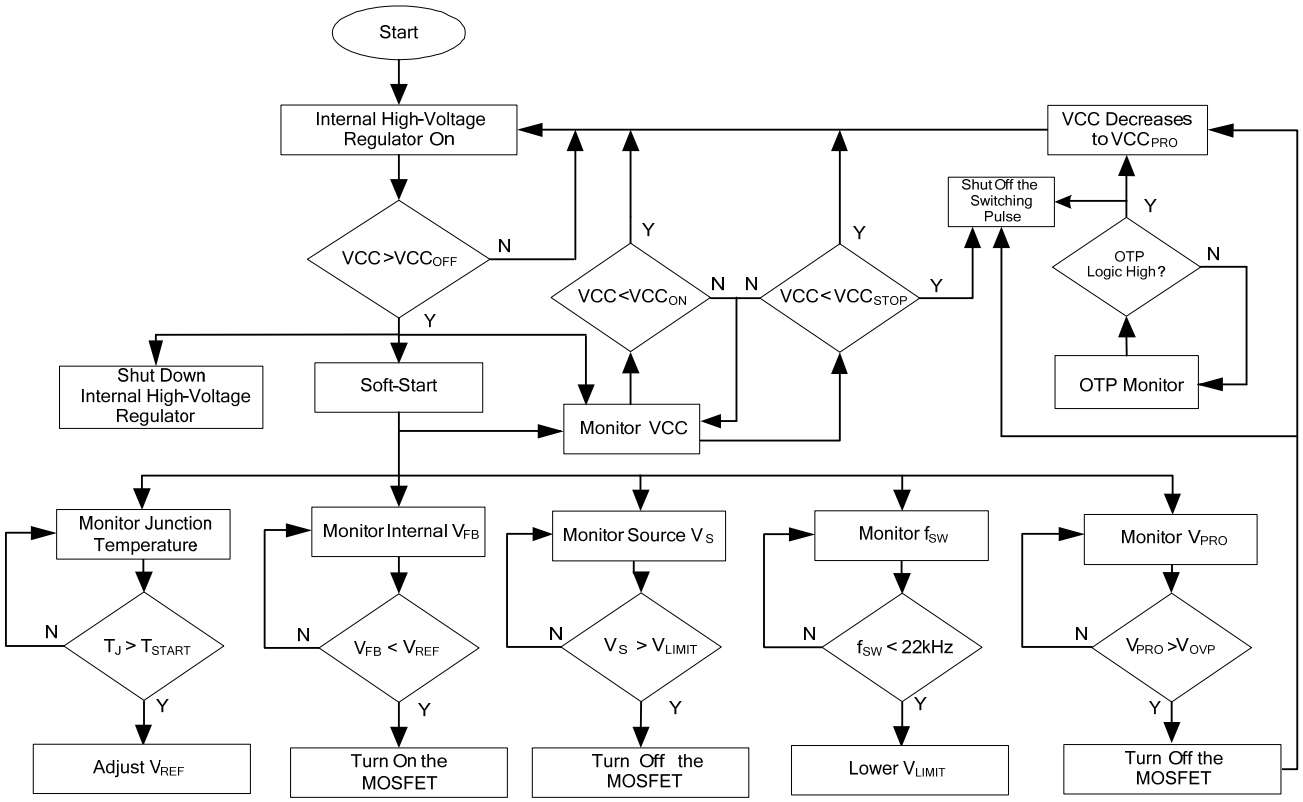


FIGURE 11. Typical Buck Converter Application

FLOW CHART

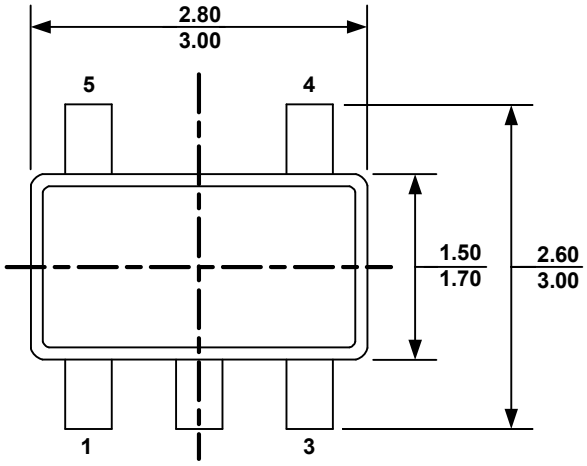


UVLO, OTP, Short-Circuit Protection, Open-LED Protection
All Protections are Auto-Restart

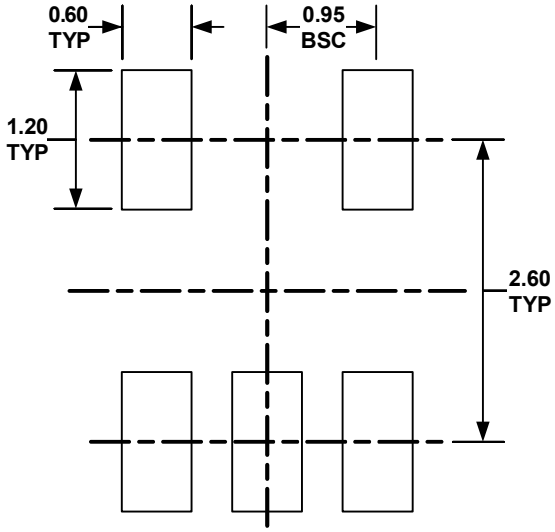
FIGURE 12. Control Flow Chart

PACKAGE INFORMATION

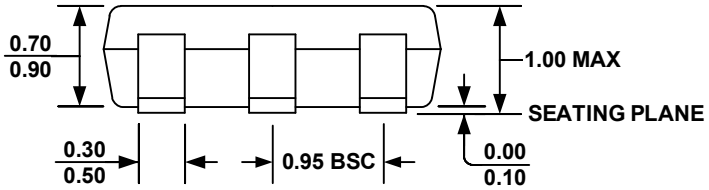
TSOT23-5



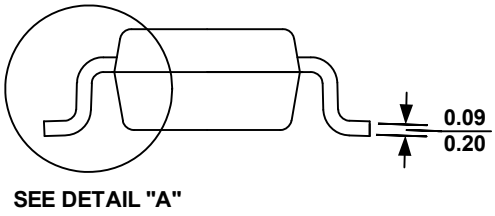
TOP VIEW



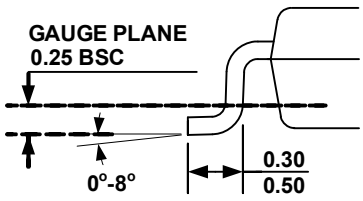
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



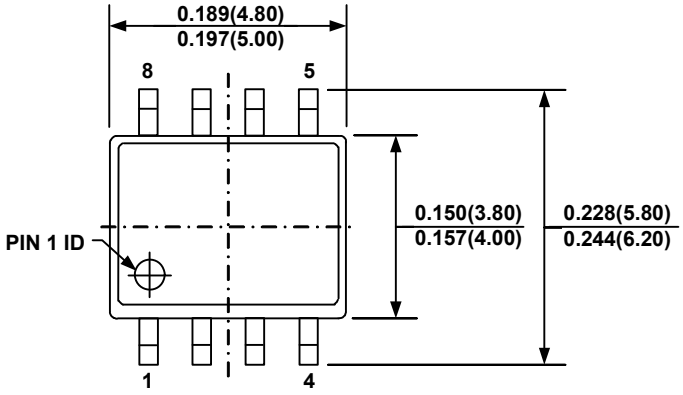
DETAIL "A"

NOTE:

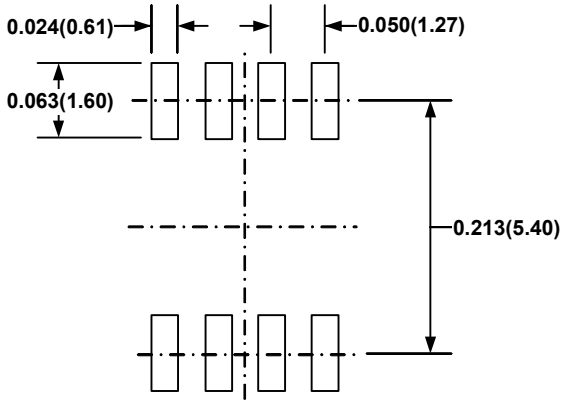
1) ALL DIMENSIONS ARE IN MILLIMETERS
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY(BOTTOM OF LEADS AFTER FORMING) SHALL BE0.10 MILLIMETERS MAX
5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AA.
6) DRAWING IS NOT TO SCALE

PACKAGE INFORMATION *(continued)*

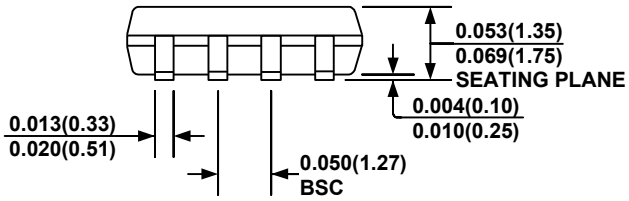
SOIC-8



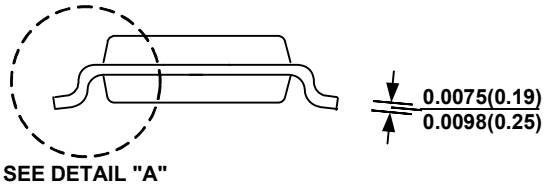
TOP VIEW



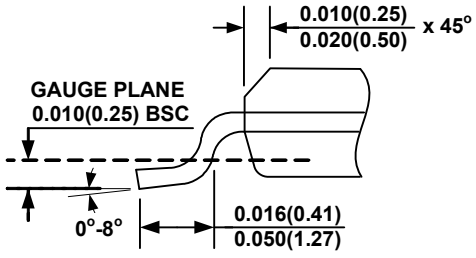
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.