

LOW VOLTAGE 3ch VIDEO AMPLIFIER WITH LPF

■ GENERAL DESCRIPTION

The **NJM2573** is a Low Voltage 3ch Video Amplifier with LPF. Internal 75Ω driver is easy to connect TV monitor directly.

The **NJM2573** corresponds to a clamp and bias inputs, and selection of a clamp/ bias is possible for one circuit, and it corresponds to various video signals.

■ PACKAGE OUTLINE



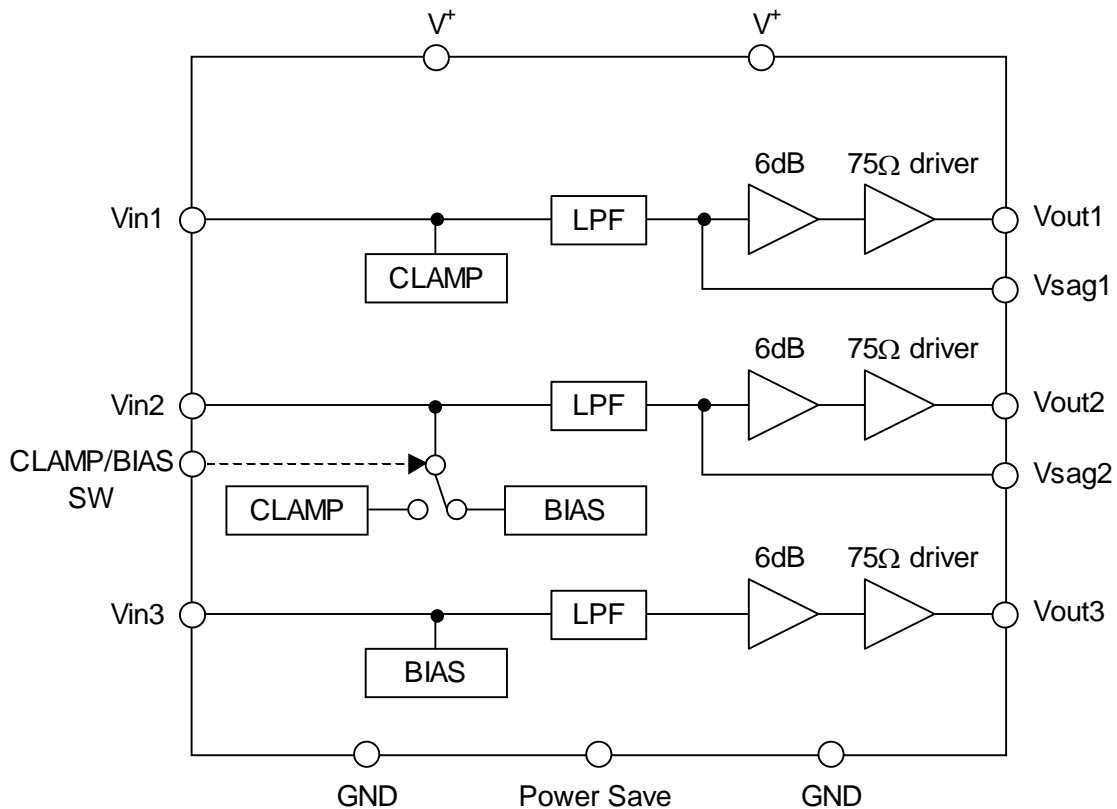
NJM2573V

■ FEATURES

- Operating Voltage 2.8 to 5.5V
- Input type Vin1: CLAMP
Vin2: CLAMP/ BIAS
Vin3: BIAS
- Internal LPF
- Internal 6dB amplifier
- Internal 75Ω Driver Circuit (2-system drive)
- Internal Power Saving Circuit
- Bipolar Technology
- Package Outline SSOP14

Ω

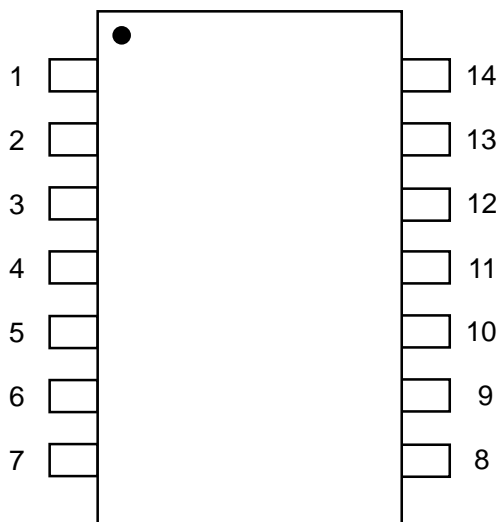
■ BLOCK DIAGRAM



NJM2573

■PIN CONFIGURATION

SSOP14



1. Vsag1
2. V⁺1
3. Vin1
4. Power Save
5. Vin2
6. GND1
7. Vin3
8. CLAMP/BIAS SW
9. Vout3
10. GND2
11. Vout2
12. Vsag2
13. V⁺2
14. Vout1

■ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V ⁺	7.0	V
Power Dissipation	P _D	300	mW
Operating Temperature Range	T _{opr}	-40 to +85	°C
Storage Temperature Range	T _{stg}	-40 to +125	°C

■ELECTRICAL CHARACTERISTICS (V⁺=3.0V,R_L=150Ω,Ta=25°C)

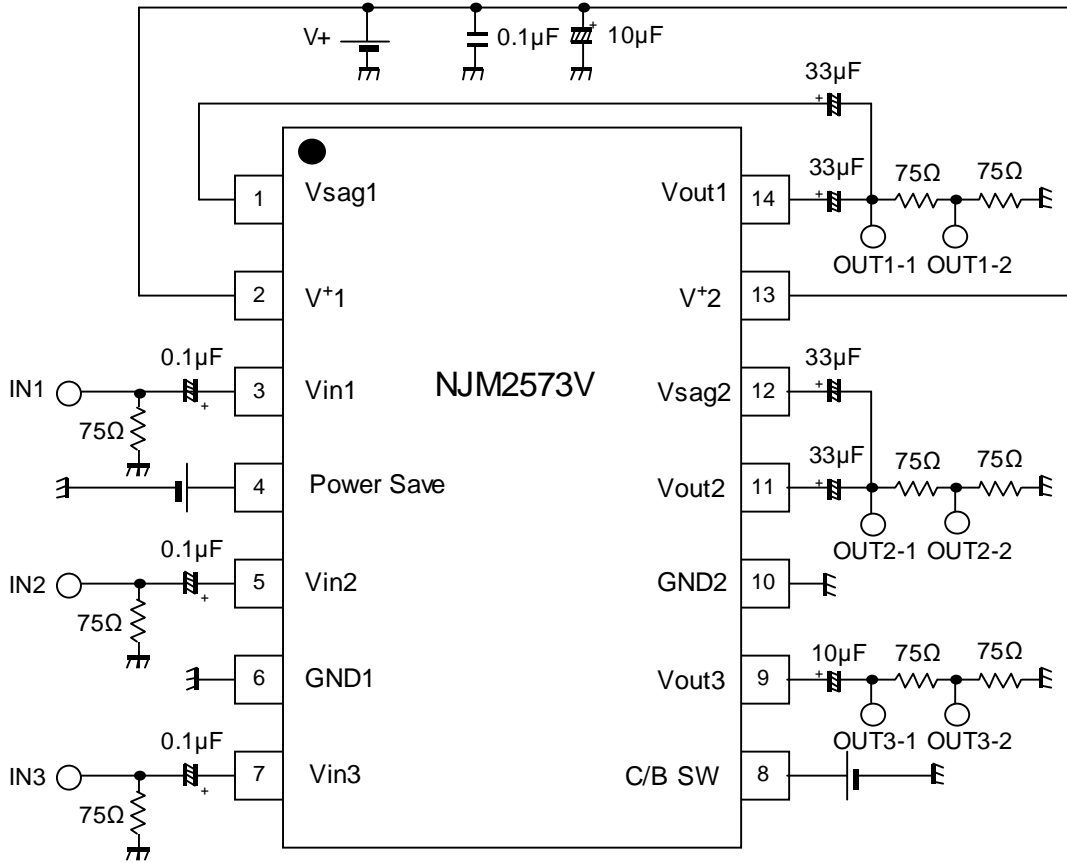
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V _{opr}		2.8	3.0	5.5	V
Operating Current	I _{CC}	No Signal	-	18.0	26.0	mA
Operating Current at Power Save	I _{save}	Power Save Mode	-	60	90	μA
Maximum Output Voltage Swing	V _{omv}	f=1kHz,THD=1%, CLAMP Input	2.2	2.4	-	V _{p-p}
	V _{om} RGB	f=1kHz,THD=1%, BIAS Input	1.4	2.2	-	
Voltage Gain	G _v	V _{in} =100kHz, 1.0V _{p-p} , Sin Signal (CLAMP) V _{in} =100kHz 0.7V _{p-p} , Sin Signal (BIAS)	6.0	6.4	6.8	dB
Low Pass Filter Characteristic	G _{fy} 4.5M	V _{in} =4.5MHz/100kHz, 1.0V _{p-p} (CLAMP) V _{in} =4.5MHz/100kHz, 0.7V _{p-p} (BIAS)	-0.5	0.0	+0.5	dB
	G _{fy} 8M	V _{in} =8MHz/100kHz, 1.0V _{p-p} (CLAMP) V _{in} =8MHz/100kHz, 0.7V _{p-p} (BIAS)	-	-2.0	-	
	G _{fy} 16M	V _{in} =16MHz/100kHz, 1.0V _{p-p} (CLAMP) V _{in} =16MHz/100kHz, 0.7V _{p-p} (BIAS)	-	-12	-	
Cross talk	CT	V _{in} =4.43MHz, 1.0V _{p-p} , Sin Signal (CLAMP) V _{in} =4.43MHz 0.7V _{p-p} , Sin Signal (BIAS)	-	-65	-	dB
Differential Gain	DG	(CLAMP) V _{in} =1.0V _{p-p} Input 10step Video Signal	-	0.2	-	%
Differential Phase	DP	(CLAMP) V _{in} =1.0V _{p-p} Input 10step Video Signal	-	0.2	-	deg
S/N Ratio	SN _v	(CLAMP) V _{in} =1.0V _{p-p} ,100% White Video Signal (BIAS) V _{in} =0.7V _{p-p} ,100% Red field Signal	-	+60	-	dB
2nd. Distortion	H _v	(CLAMP) V _{in} =1.0V _{p-p} , 3.58MHz, Sin Signal, R _L =75Ω (BIAS) V _{in} =0.7V _{p-p} , 3.58MHz, Sin Signal, R _L =75Ω	-	-40	-	dB
SW Change Voltage High Level	V _{thPH}		1.8	-	V ⁺	V
SW Change Voltage Low Level	V _{thPL}		0	-	0.3	

■CONTROL TERMINAL

PARAMETER	STATUS	NOTE
Power Save	H	Power Save: ON
	L	Power Save: OFF
	OPEN	Power Save: OFF
CLAMP/BIAS SW	H	BIAS
	L	CLAMP
	OPEN	CLAMP

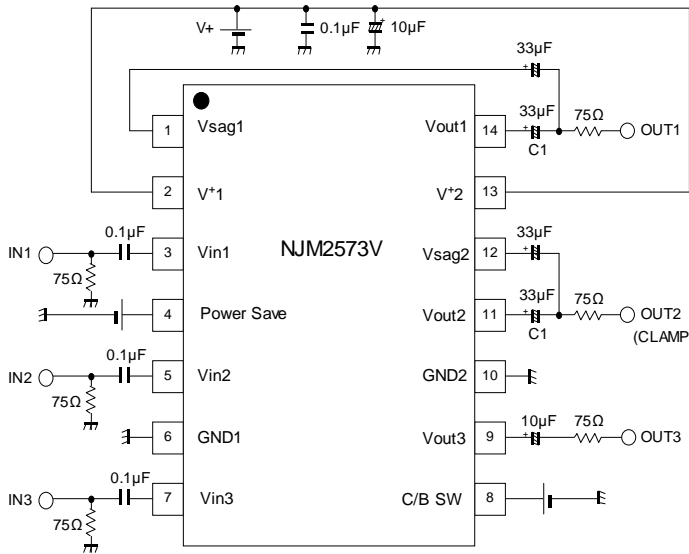
NJM2573

■ TEST CIRCUIT (SSOP14)

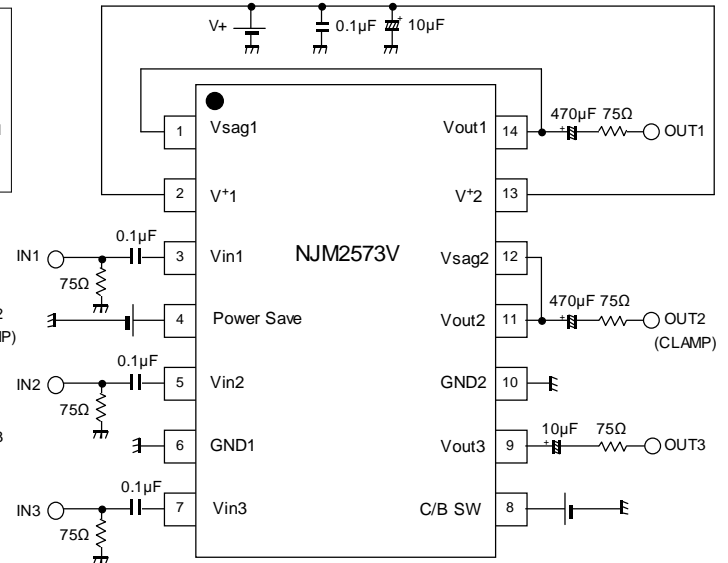


APPLICATION CIRCUIT (VIN2: CLAMP)

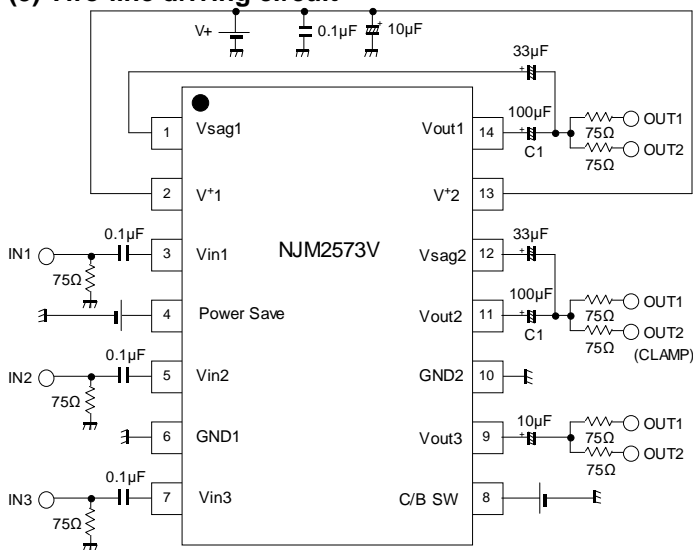
(1) Standard circuit



(2) SAG correction unused circuit



(3) Two-line driving circuit



(1) Standard circuit

The SAG correction reduces output coupling capacitor values.

The capacitor of C1 (33μF) is recommended for the portable application.

However, the 33μF capacitor may deteriorate SAG, and lose synchronization by luminance fluctuation.

Adjust the C1 value, checking the waveform containing a lot of low frequency components like a bounce waveform (In case of worst condition). Change the capacitor of C1 into a large value to improve SAG.

(2) SAG correction unused circuit

Cancel the SAG correction to improve lost synchronization.

Connect the coupling capacitor after connecting the Vout pin and Vsag pin. The recommended value is 470μF or more.

(3) Two-line driving circuit

The NJM2573 drives two-line load of 150Ω.

The capacitance value of C1 should be 100μF or more, because SAG is deteriorated than a standard circuit.

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■EQUIVALENT CIRCUIT

PIN No.	PIN NAME	FUNCTION	INSIDE EQUIVALENT CIRCUIT
1 12	Vsag1 Vsag2	Sag compensation	
2 13	V ⁺ 1 V ⁺ 2	Power Supply	-
3	VIN1	Clamp input	
4	Power Save	Power save	
5	Vin2	Clamp/Bias input	
6 10	GND1 GND2	GND	-

PIN No.	PIN NAME	FUNCTION	INSIDE EQUIVALENT CIRCUIT
7	Vin3	Bias input	
8	CLAMP/ BIAS SW	Clamp/Bias switch	
9	Vout3	Bias output	
11 14	Vout2 Vout1	Clamp/Bias output Clamp output	

■ APPLICATION

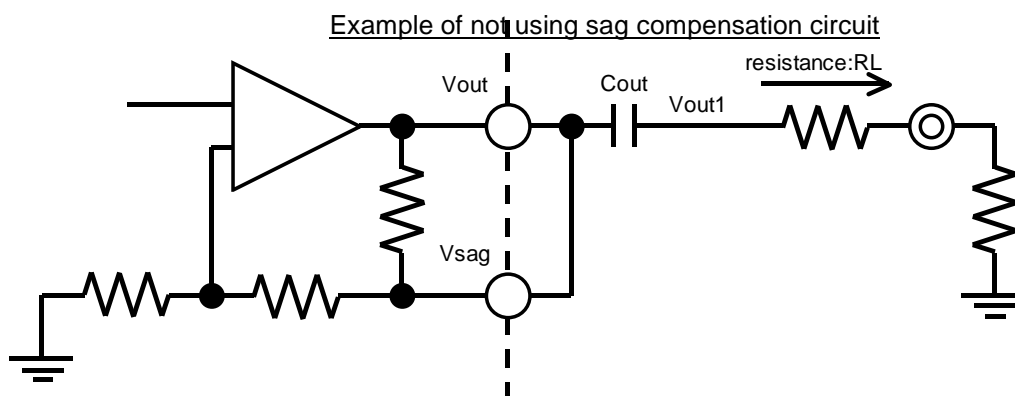
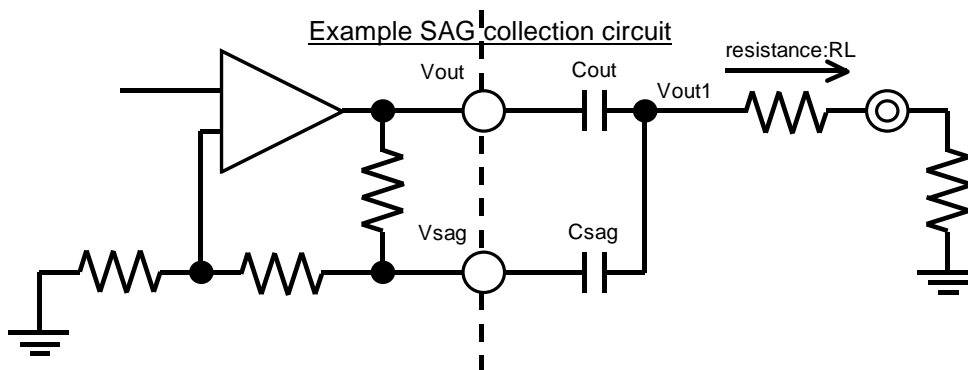
When the power supply voltage is not impressing, don't impress voltage to the control terminal.

APPLICATION

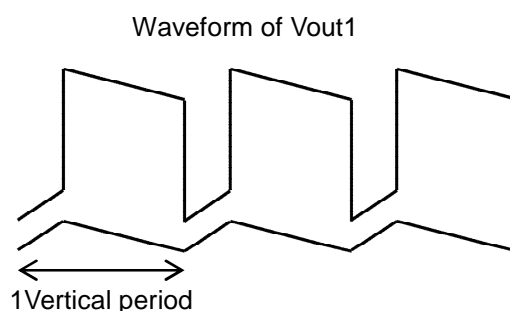
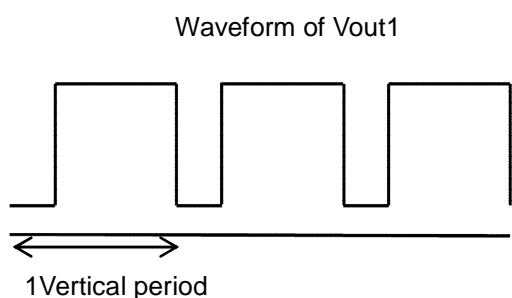
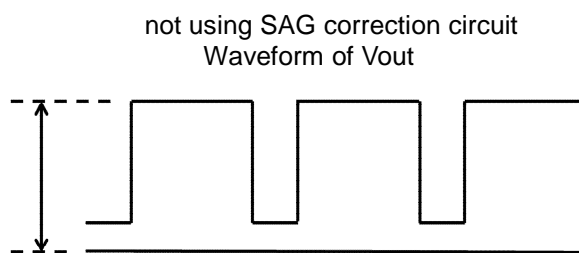
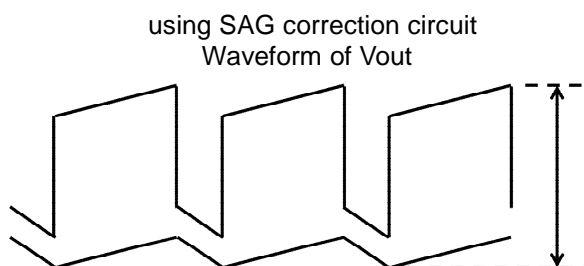
◆ SAG correction circuit

SAG correction circuit is a circuit to correct for low-frequency attenuation by high-pass filter consisting of the output coupling capacitance and load resistance. Low-frequency attenuation raises the sag in the vertical period of the video signal.

Capacitor for V_{sag} (C_{sag}) is connected to the negative feedback of the amplifier. This C_{sag} increase the low frequency gain to correct for the attenuation of low frequency gain.

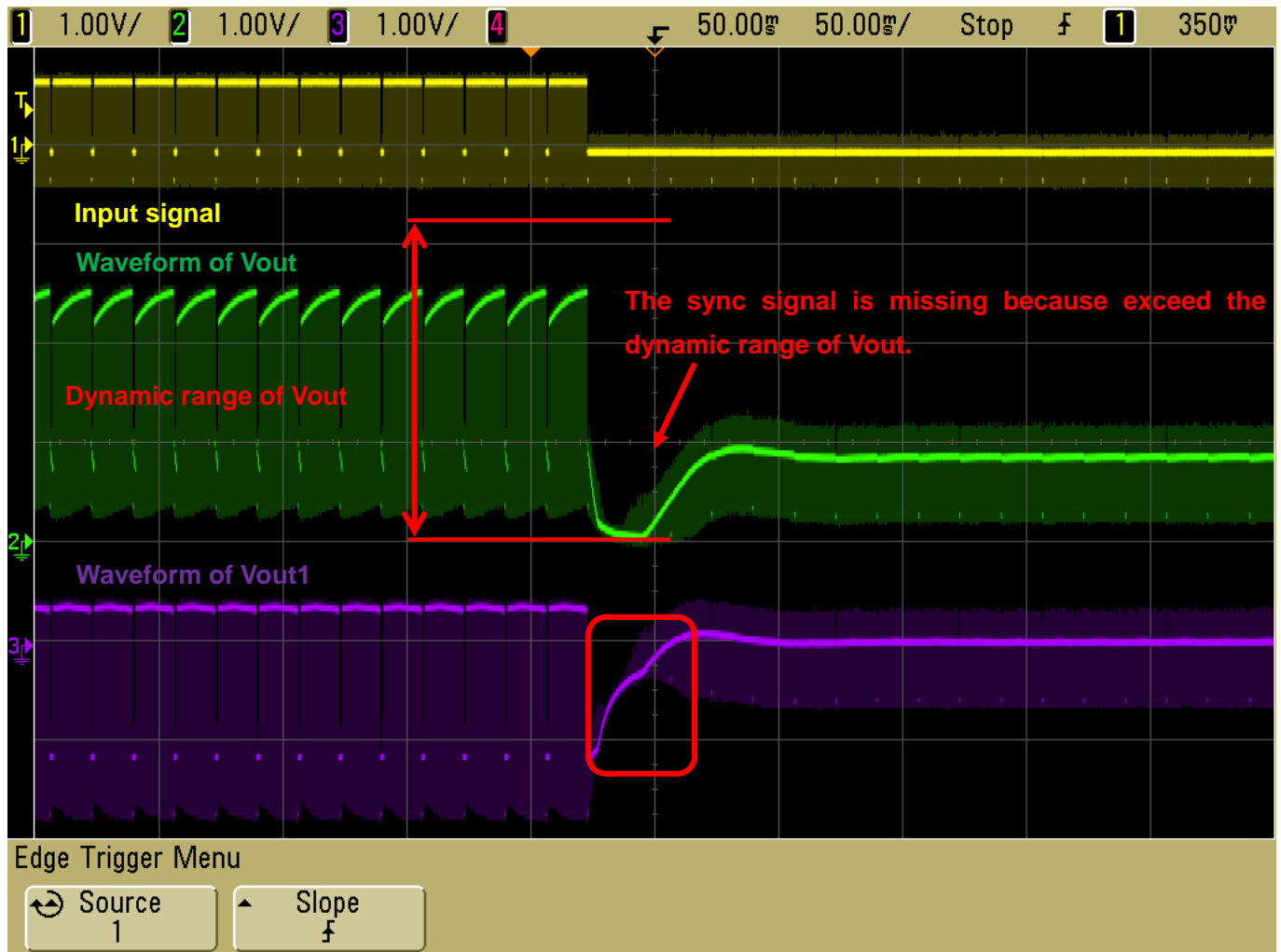


Waveform of Vout terminal and Vout1 terminal



SAG correction circuit generates a low frequency component signal amplified to Vout terminal. Changes of the luminance signal will be low-frequency components, if you want to output a large signal luminance changes. Therefore, generate correction signal of change of a luminance signal to Vout pin. At this time, signal is over the dynamic range of Vout pin. This may cause a lack of sync signal, and waveform distortion.

Please see diagram below (green waveform), if you want to output large changes of a signal luminance, such as 100% white video signal and black signal. Thus, output signal exceed dynamic range of Vout pin and may be the signal lack.



< Countermeasure for waveform distortion >

1. Please using small value the Sag compensation capacitor (VSAG).

It can ensure the dynamic range by using small value the capacitor (VSAG). It because of low-frequency variation of Vout pin is smaller. However, the output (VOUT) must be use large capacitor for this reason sag characteristics become exacerbated.

2. Please do not use the sag correction circuit.

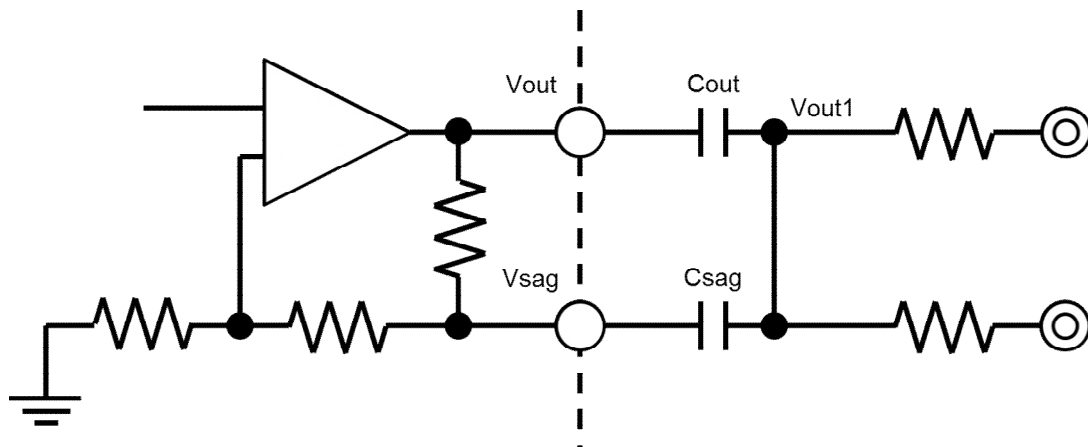
Signal can output within dynamic range for reason it does not change the DC level of the output terminal.

However, the output (VOUT) must be use large capacitor for this reason sag characteristics become exacerbated.

< Dual drive at using SAG correction circuit >

Using sag correction circuit at dual drive circuit is below. Dual drives are less load resistance. Thus, the cut-off frequency of HPF that is composed of the output capacitor and load resistance will be small. Therefore, the sag characteristics deteriorate.

Please size up to the output capacitor (Vout) for not to deteriorate the sag characteristics.



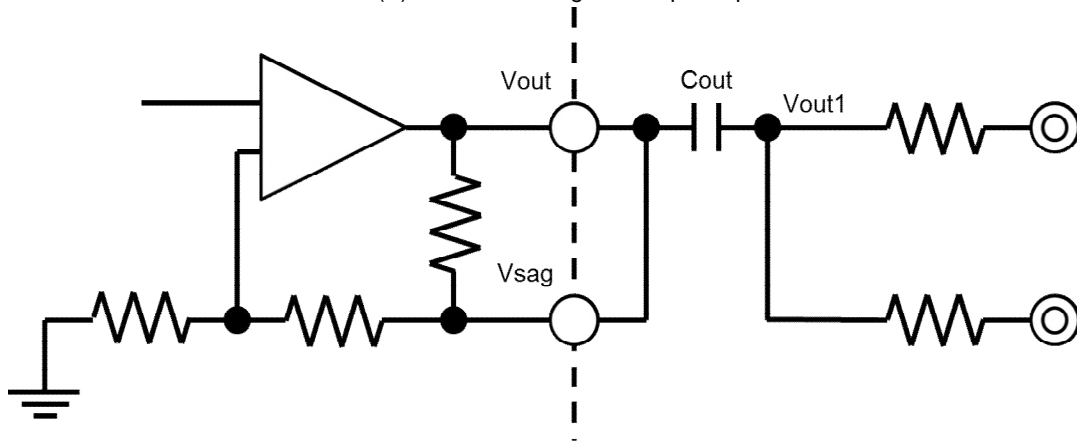
< Dual drive at not using SAG correction circuit >

We recommended two-example dual drive circuit with not use sag correction circuit. Please change the configuration to be used according to the situation. Please configure to meet the following conditions. Then you can adjust the characteristics of each configuration.

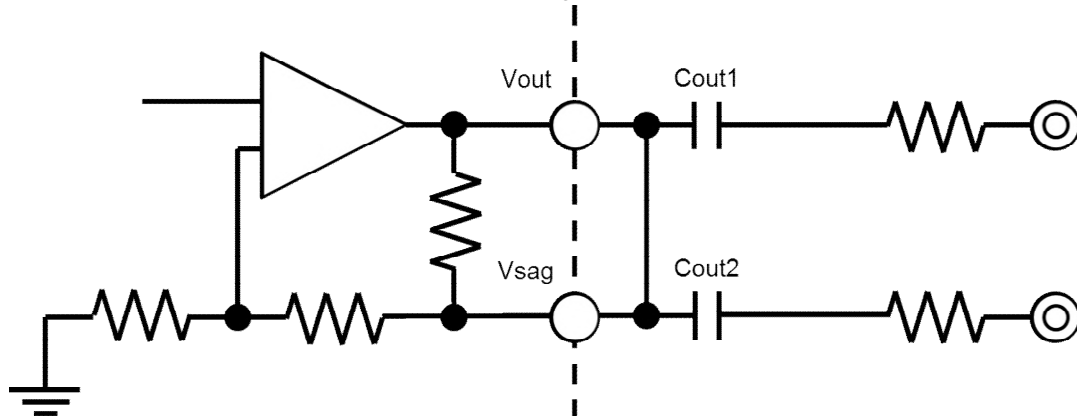
$$C_{out} = C_{out1} + C_{out2}$$

$$C_{out1} = C_{out2}$$

(A) In case of using one output capacitor



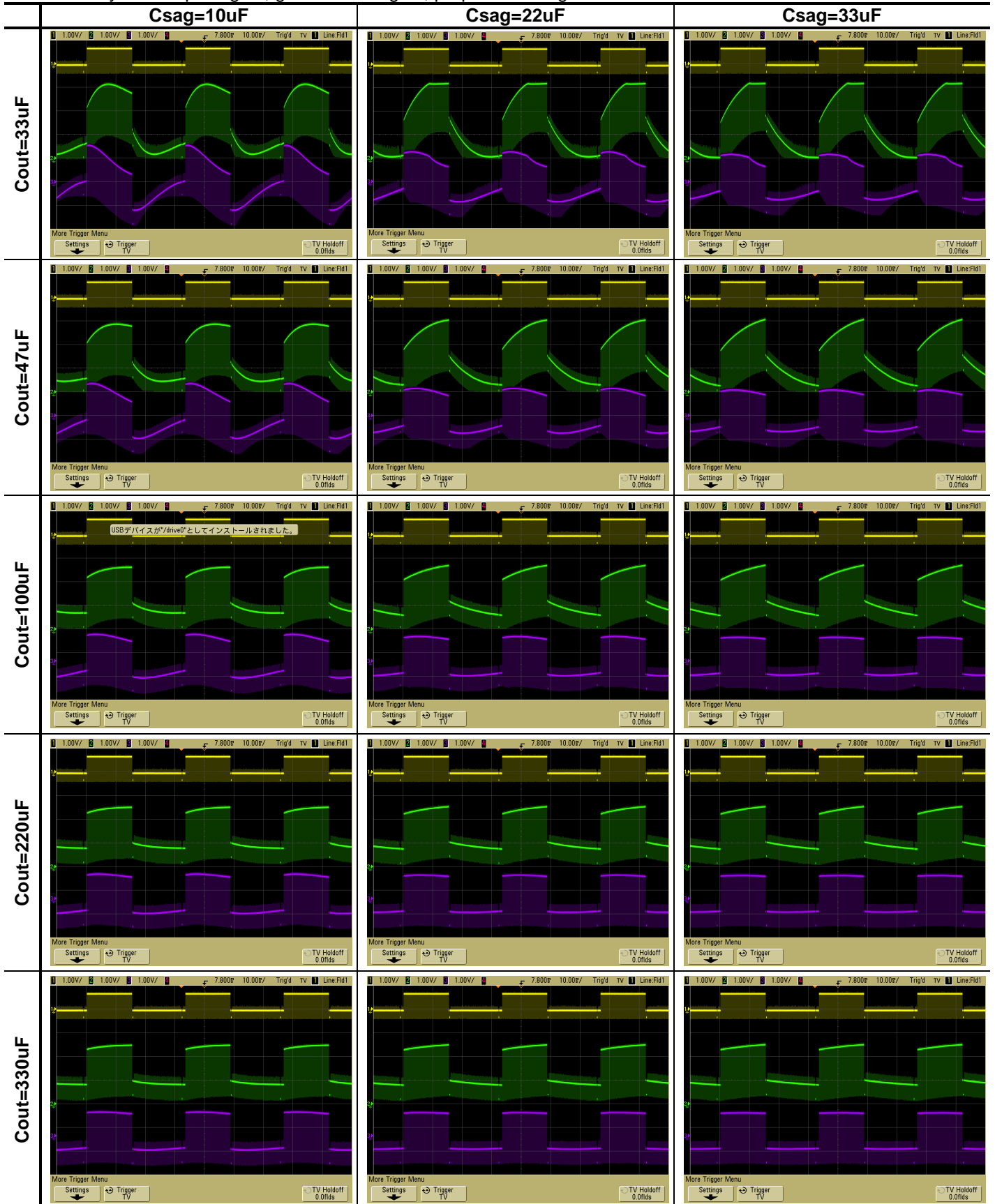
(B) In case of using two output capacitors



< Using SAG correction circuit >

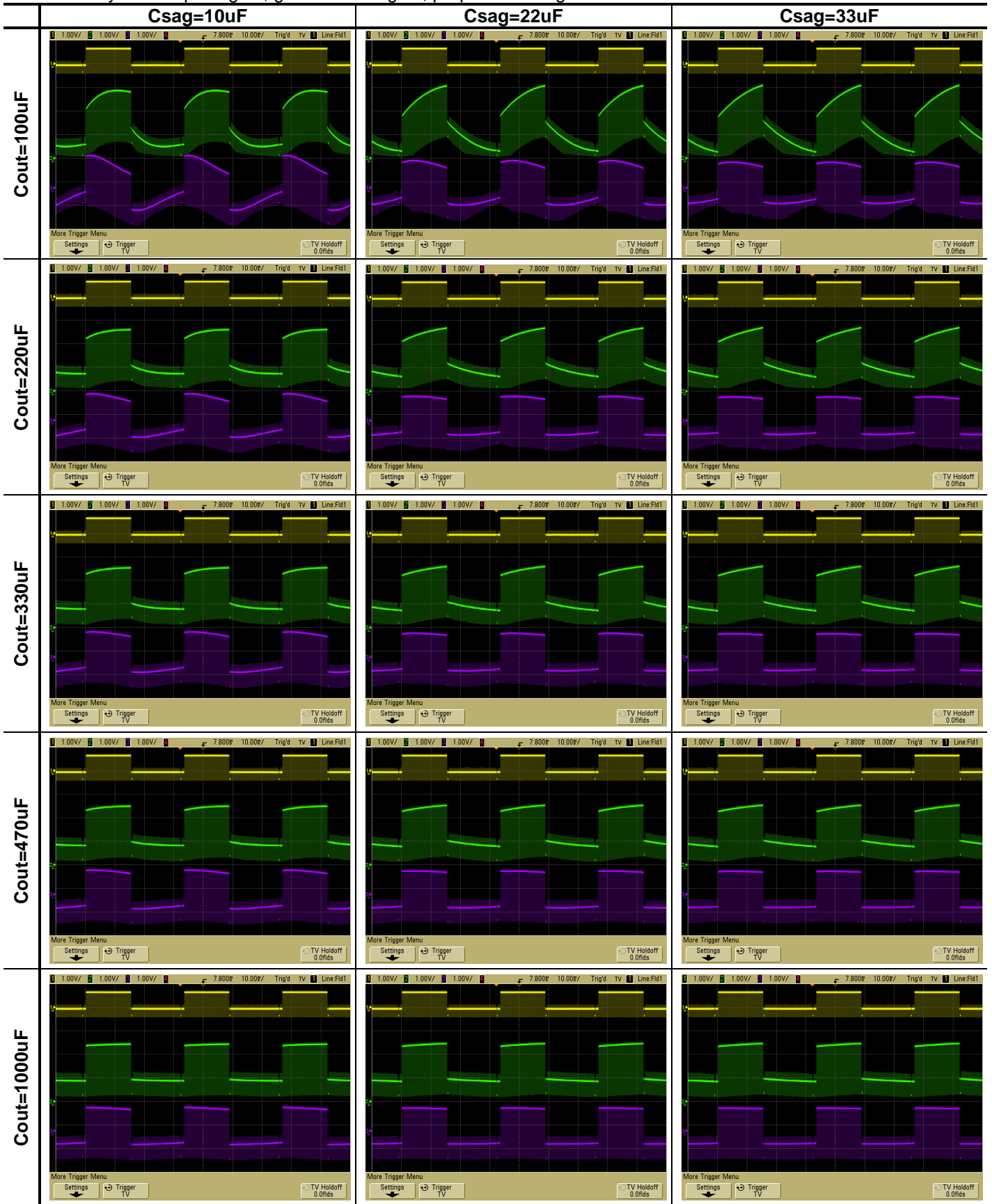
Input signal: bounce signal (IRE0%, IRE100%, 30Hz), resistance=150Ω

Waveform: yellow: input signal, green: Vout signal, purple: Vout1 signal



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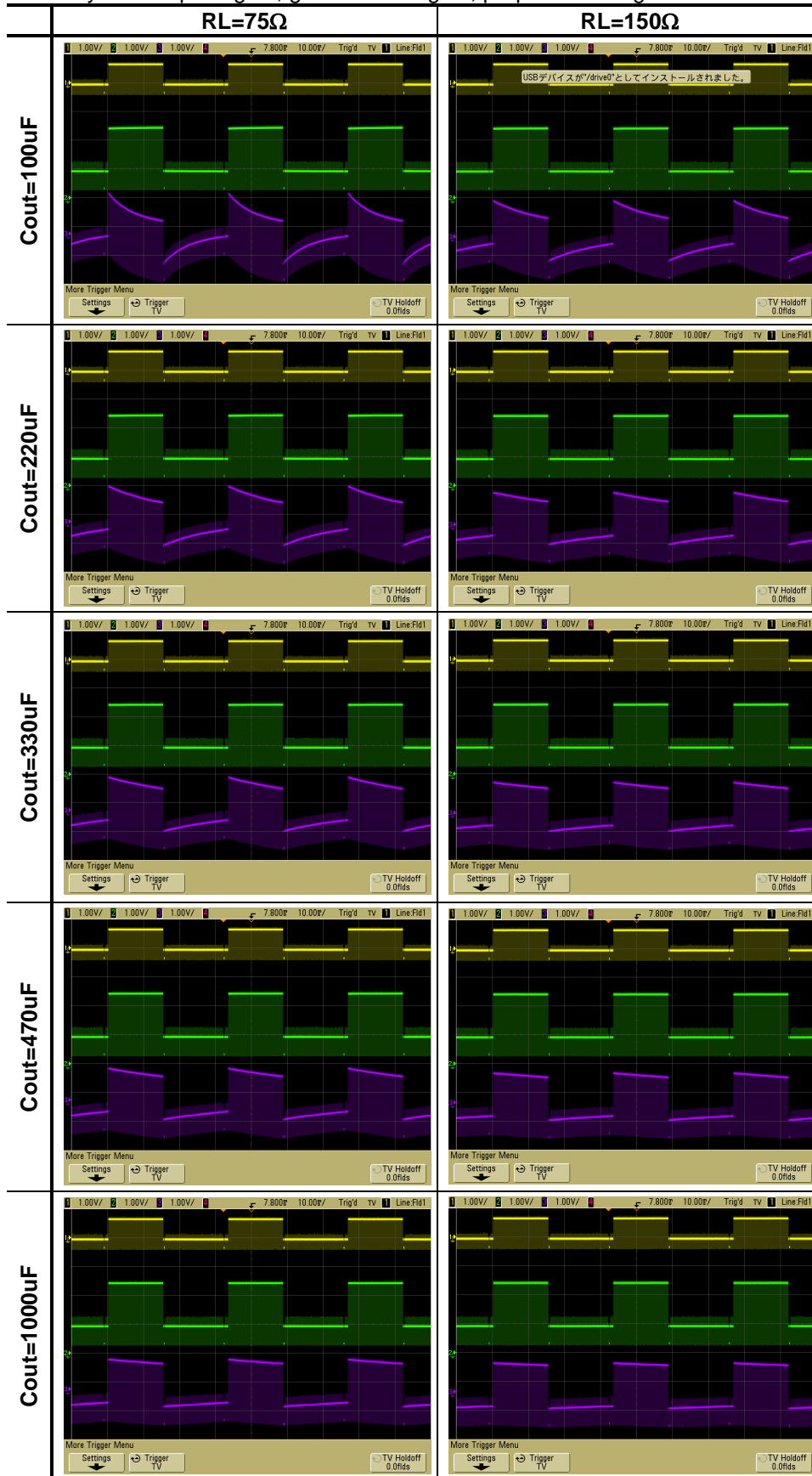
Input signal: bounce signal (IRE0%, IRE100%, 30Hz), resistance=75Ω
 Waveform: yellow: input signal, green: Vout signal, purple: Vout1 signal



< Not using SAG correction circuit >

Input signal: bounce signal (IRE0%, IRE100%, 30Hz), resistance=150Ω

Waveform: yellow: input signal, green: Vout signal, purple: Vout1 signal

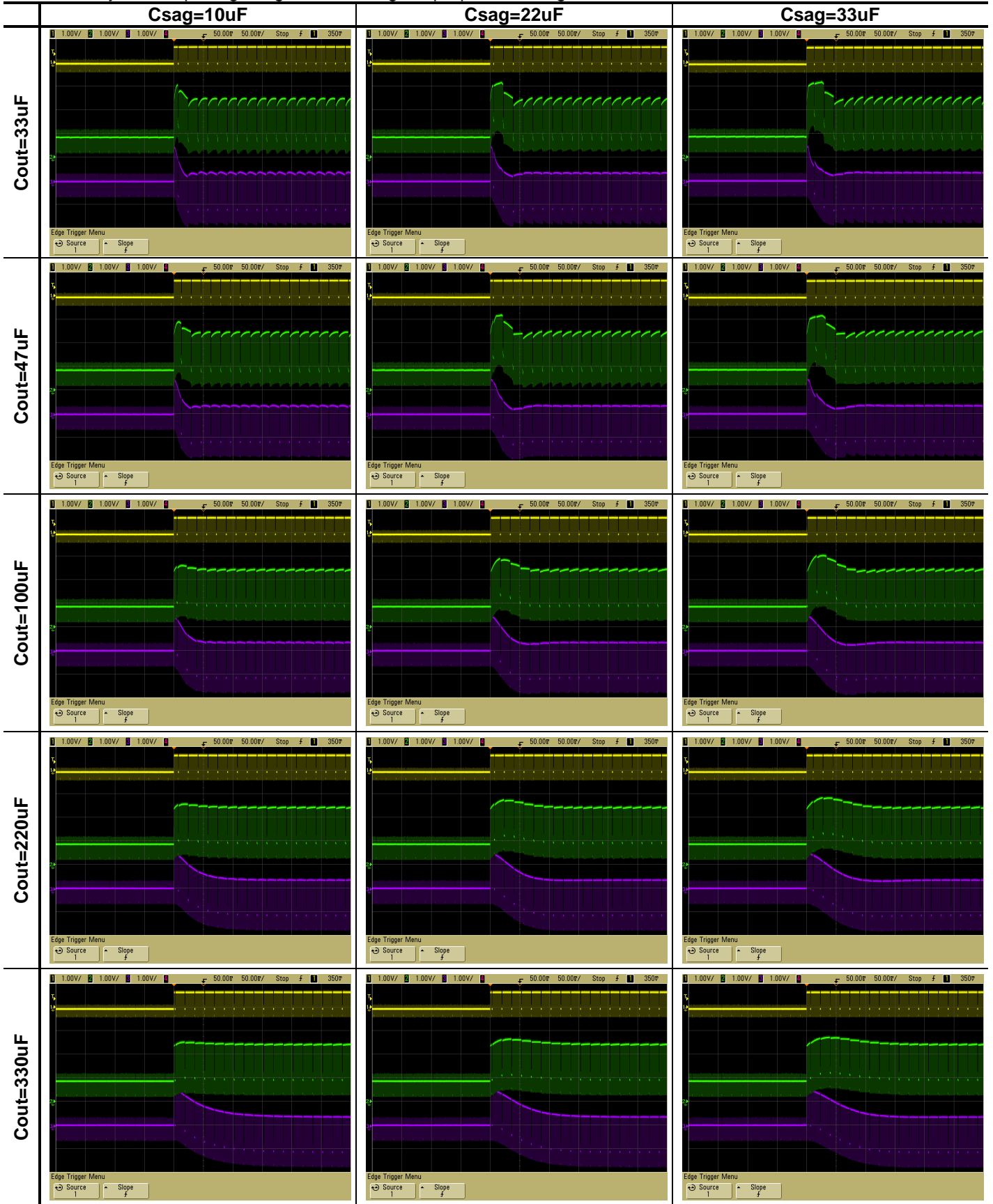


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< Using SAG correction circuit >

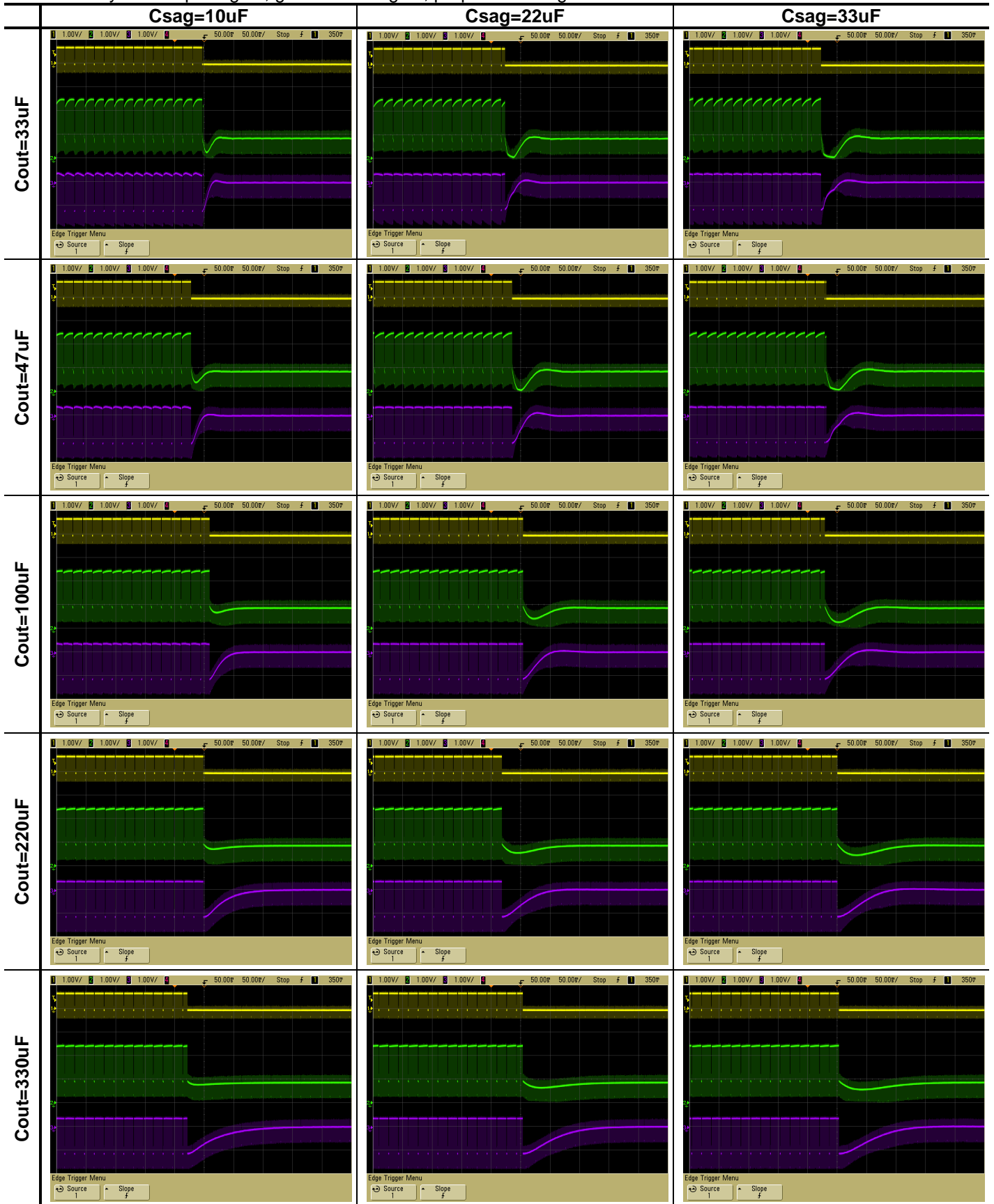
Input signal: Black to White 100%, resistance 150Ω

Waveform: yellow: input signal, green: Vout signal, purple: Vout1 signal



Input signal: White100% to Black, resistance150Ω

Waveform: yellow: input signal, green: Vout signal, purple: Vout1 signal

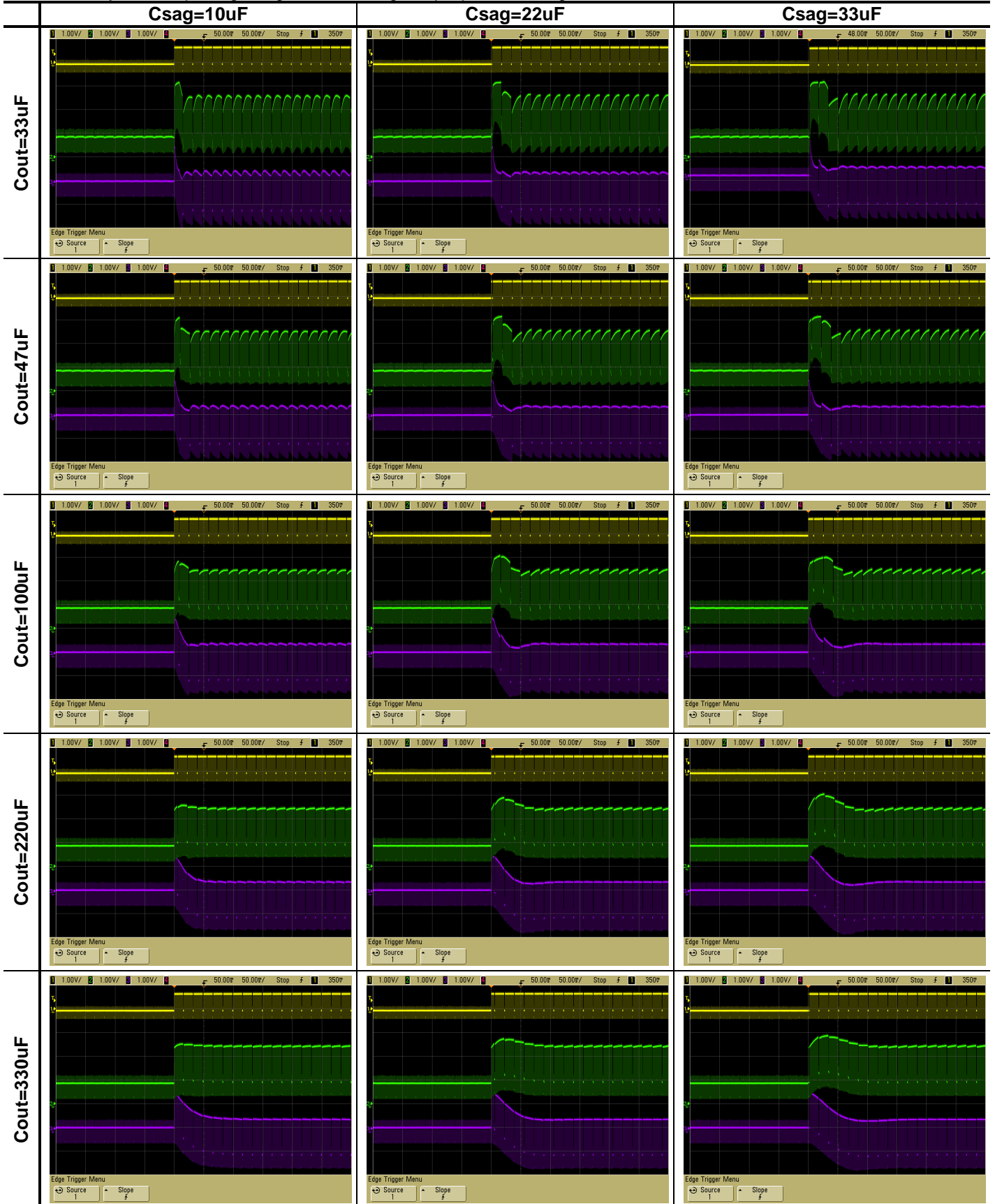


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< Using SAG correction circuit >

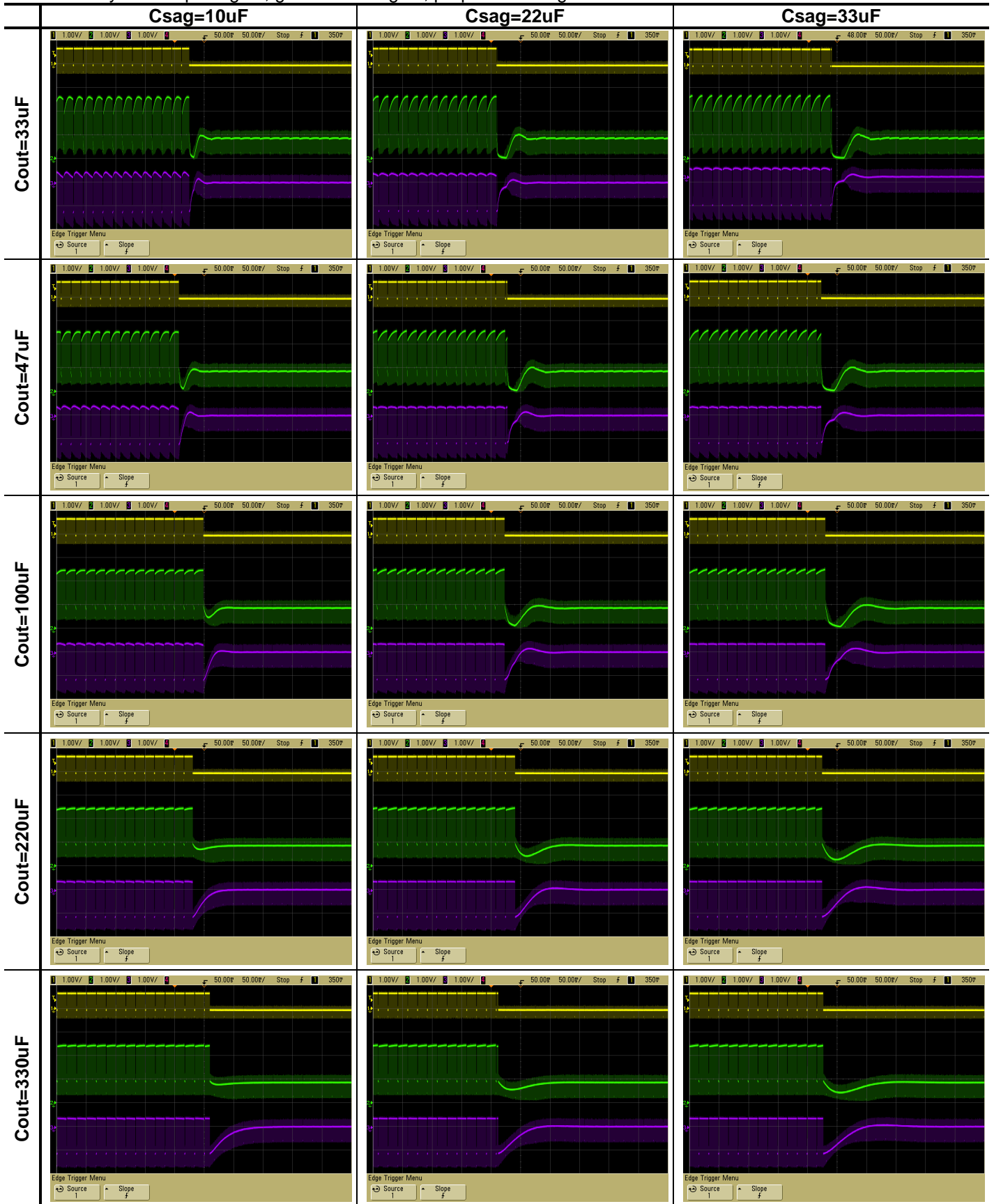
Input signal: Black to White 100%, resistance=75Ω

Waveform: yellow: input signal, green: Vout signal, purple: Vout1 signal



Input signal: White100% to Black, resistance=75Ω

Waveform: yellow: input signal, green: Vout signal, purple: Vout1 signal



◆Clamp circuit

1. Operation of Sync-tip-clamp

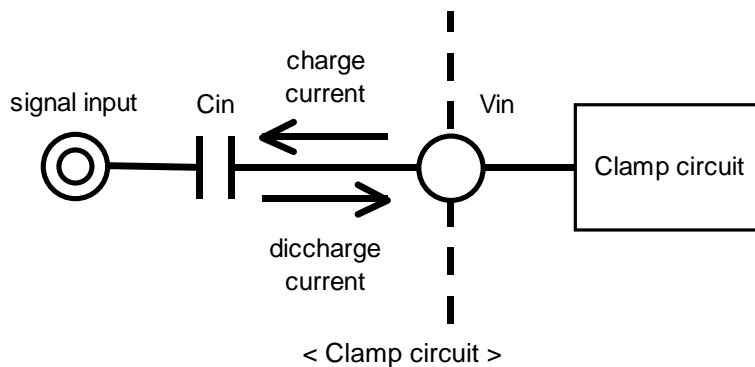
Input circuit will be explained. Sync-tip clamp circuit (below the clamp circuit) operates to keep a sync tip of the minimum potential of the video signal. Clamp circuit is a circuit of the capacitor charging and discharging of the external input C_{in} . It is charged to the capacitor to the external input C_{in} at sync tip of the video signal. Therefore, the potential of the sync tip is fixed.

And it is discharged charge by capacitor C_{in} at period other than the video signal sync tip. This is due to a small discharge current to the IC.

In this way, this clamp circuit is fixed sync tip of video signal to a constant potential from charging of C_{in} and discharging of C_{in} at every one horizontal period of the video signal.

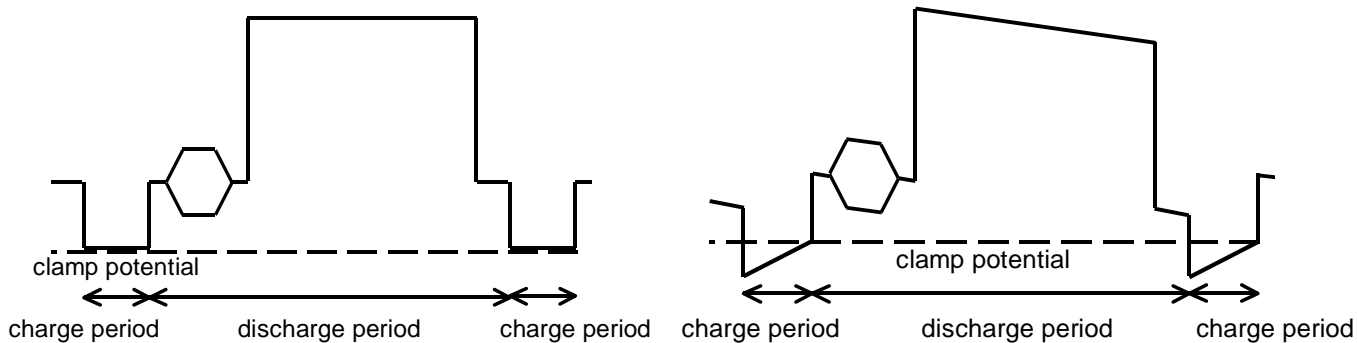
The minute current be discharged an electrical charge from the input capacitor at the period other than the sync tip of video signals. Decrease of voltage on discharge is dependent on the size of the input capacitor C_{in} .

If you decrease the value of the input capacitor, will cause distortion, called the H sag. Therefore, the input capacitor recommend on more than 0.1 μ F.



A. C_{in} is large

B. C_{in} is small (H sag experience)



< Waveform of input terminal >

2. Input impedance

The input impedance of the clamp circuit is different at the capacitor discharge period and the charge period.

The input impedance of the charging period is a few $k\Omega$. On the other hand, the input impedance of the discharge period is several $M\Omega$. Because is a small discharge-current through to the IC.

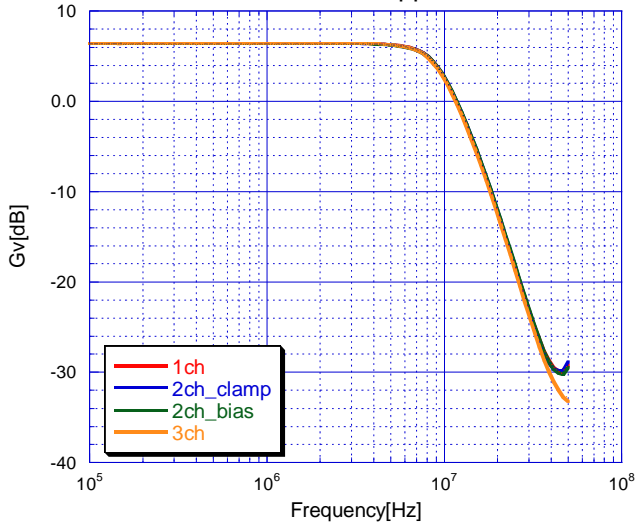
Thus the input impedance will vary depending on the operating state of the clamp circuit.

3. Impedance of signal source

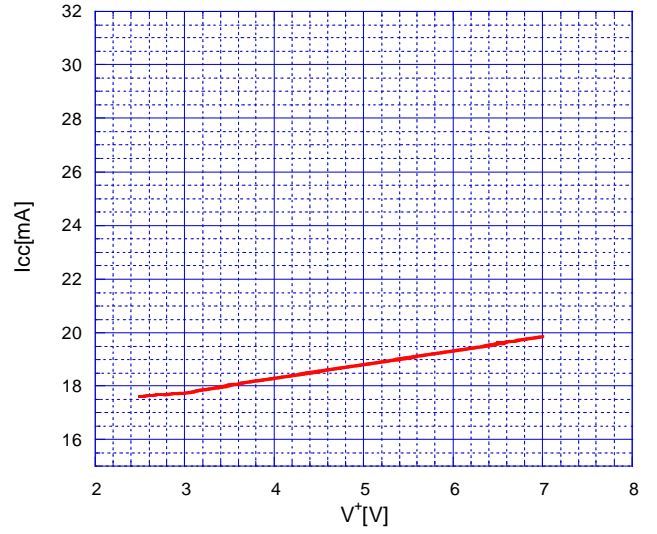
Source impedance to the input terminal, please lower than 200 Ω . A high source impedance, the signal may be distorted. If so, please to connect a buffer for impedance conversion.

■ TYPICAL CHARACTERISTICS

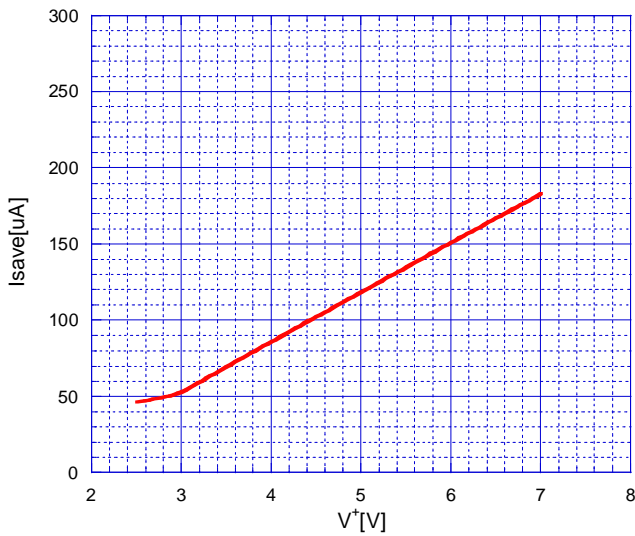
Voltage Gain vs. Frequency
Vin=1.0Vpp



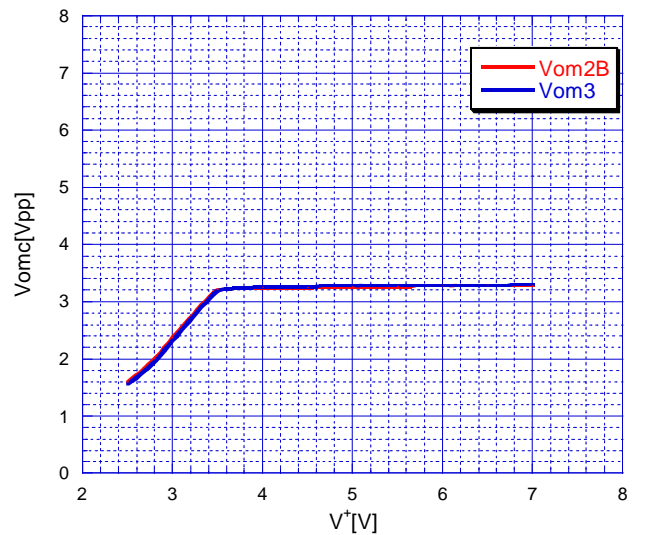
V⁺ vs I_{cc}



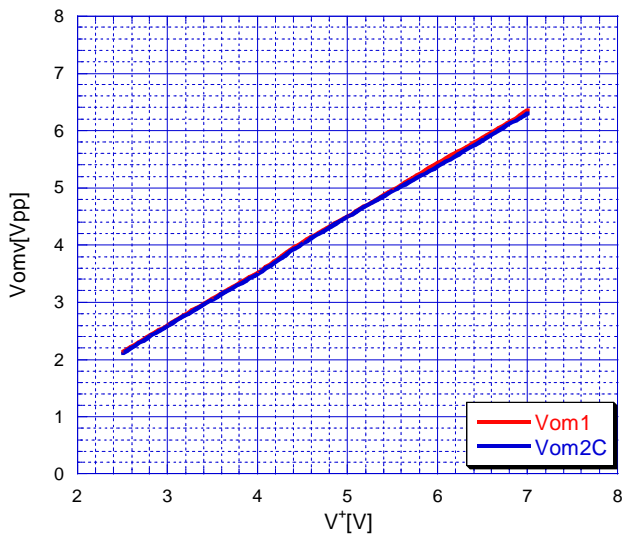
V⁺ vs I_{save}



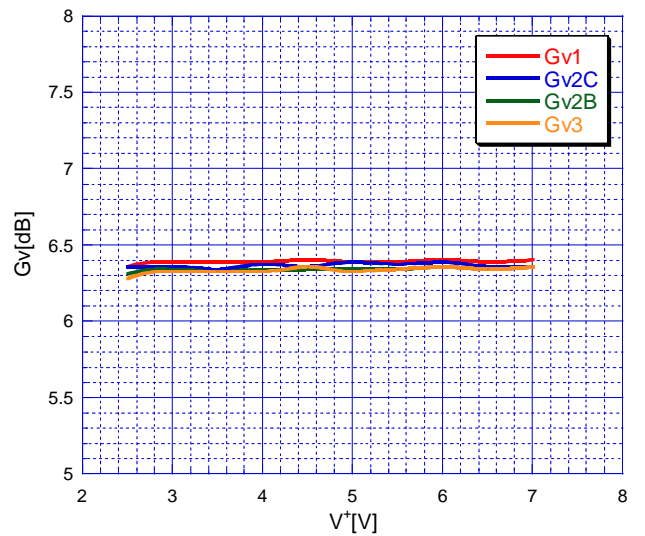
V⁺ vs Vomc



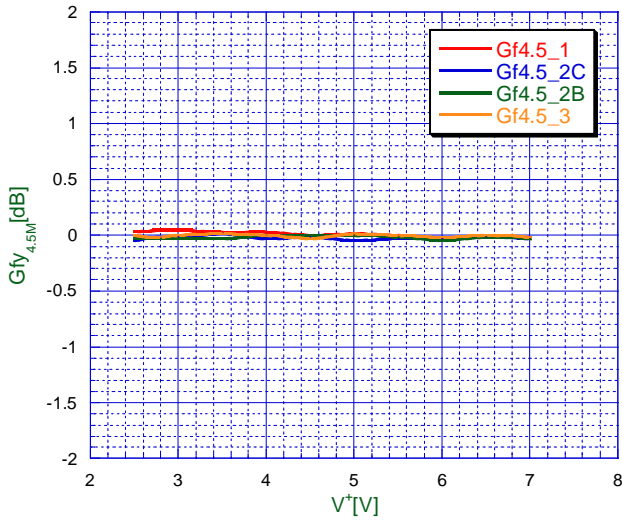
V⁺ vs Vomv



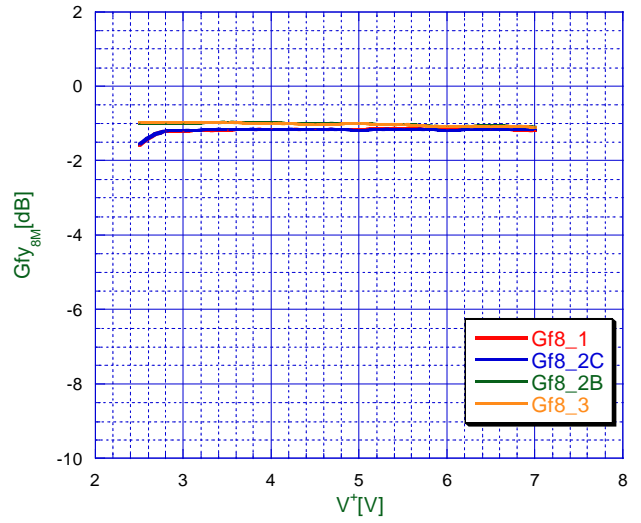
V⁺ vs Gv



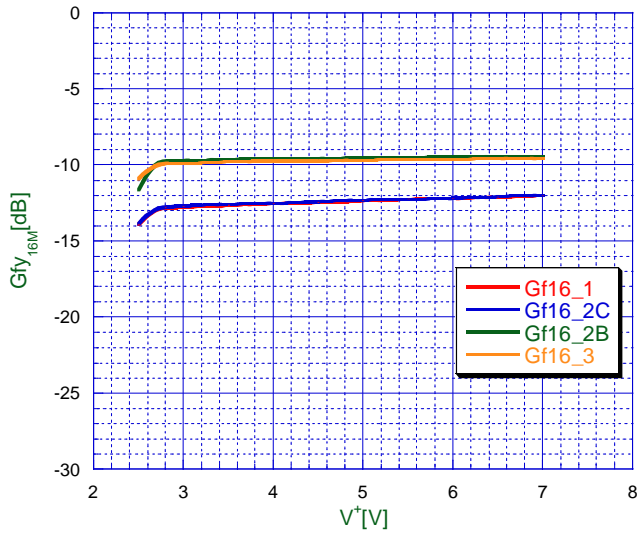
V⁺ vs Gfy_{4.5M}



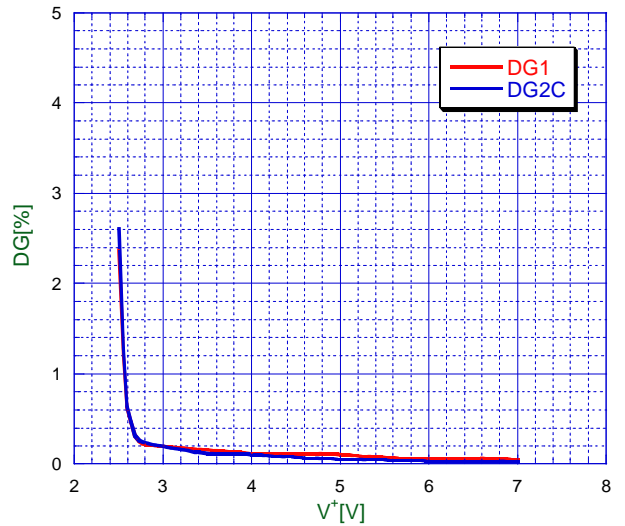
V⁺ vs Gfy_{8M}



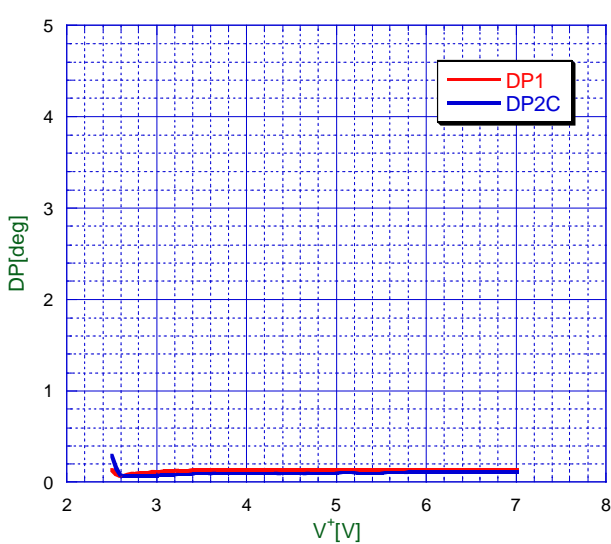
V⁺ vs Gfy_{16M}



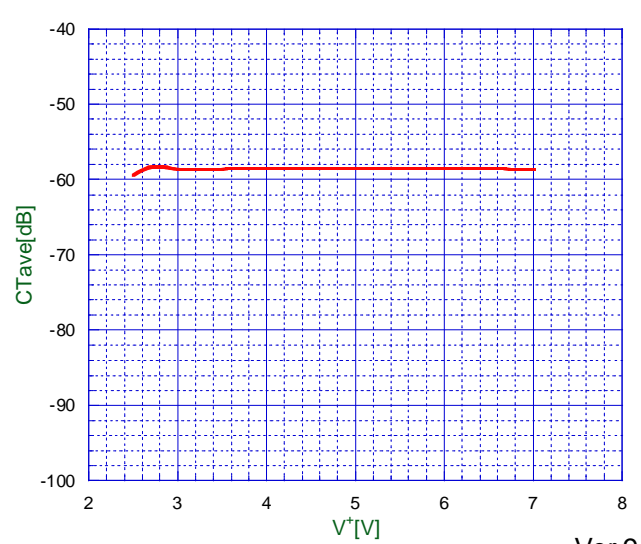
V⁺ vs DG



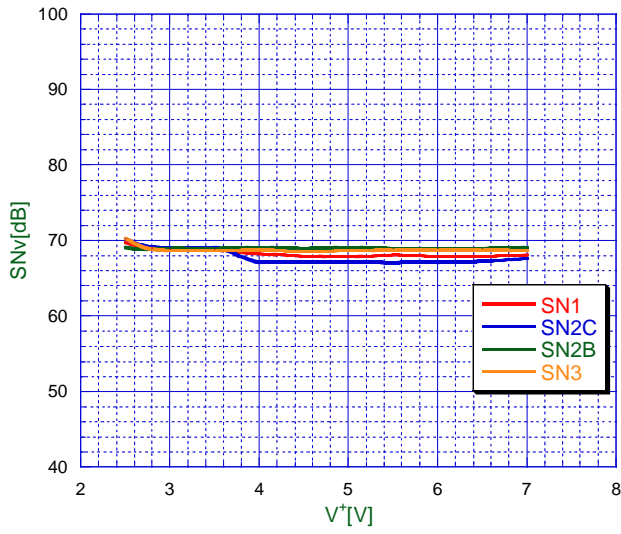
V⁺ vs DP



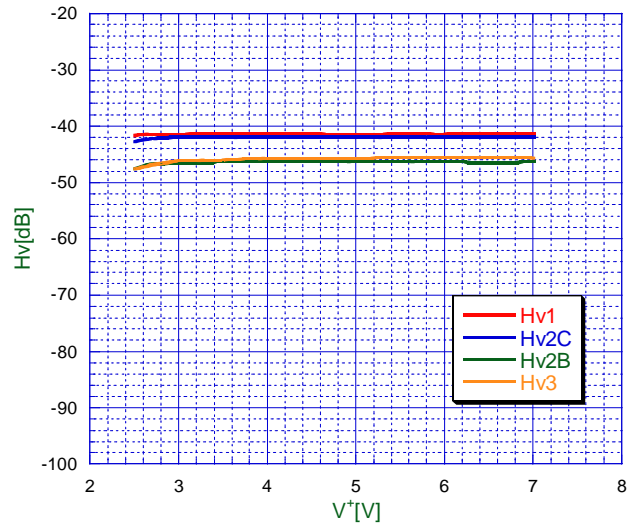
V⁺ vs CTave



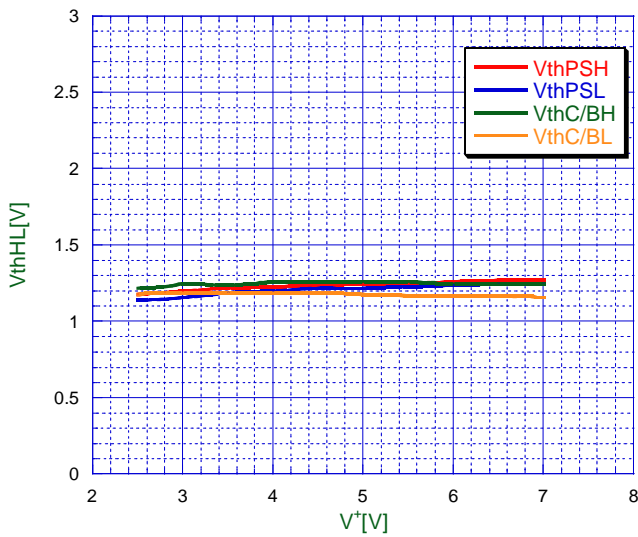
V⁺ vs SNv



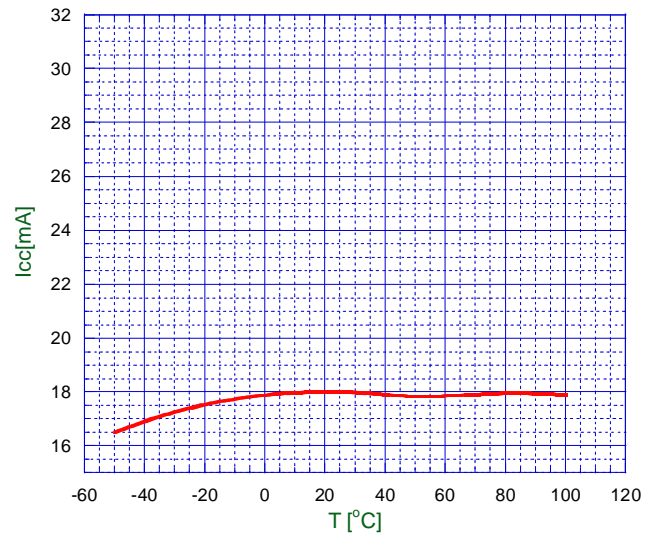
V⁺ vs Hv



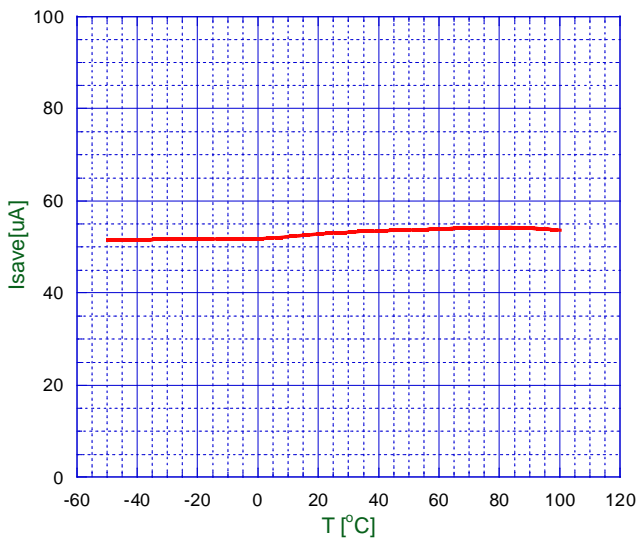
V⁺ vs VthHL



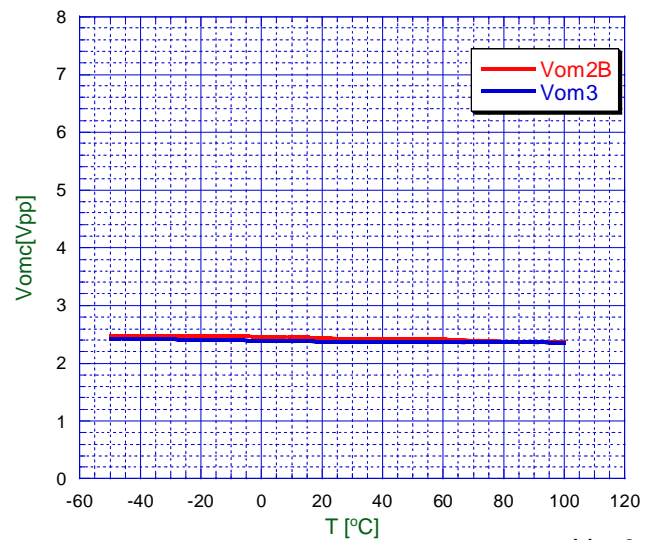
T vs Icc



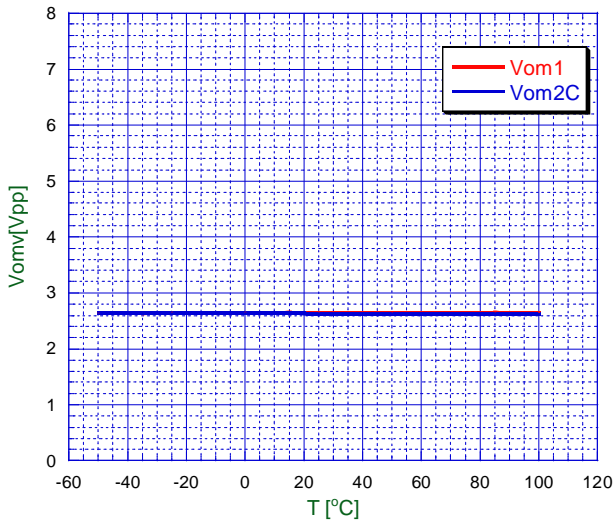
T vs Isave



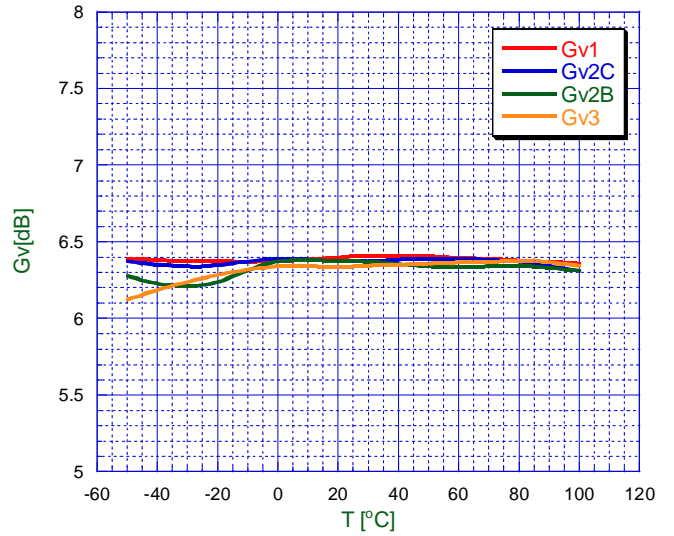
T vs Vomc



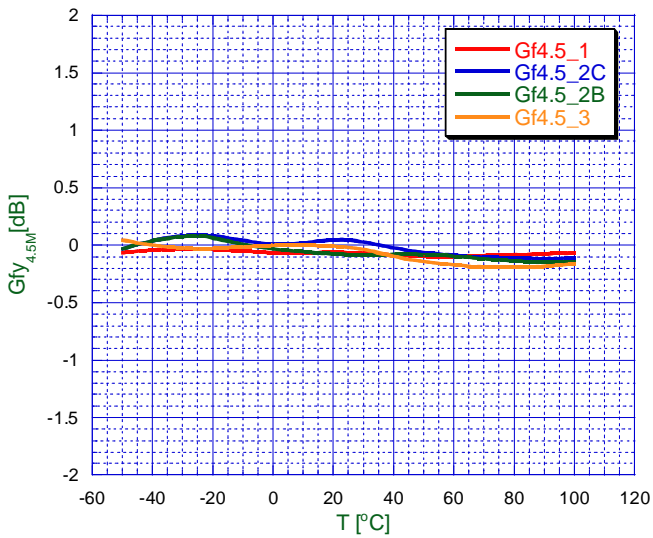
T vs Vomv



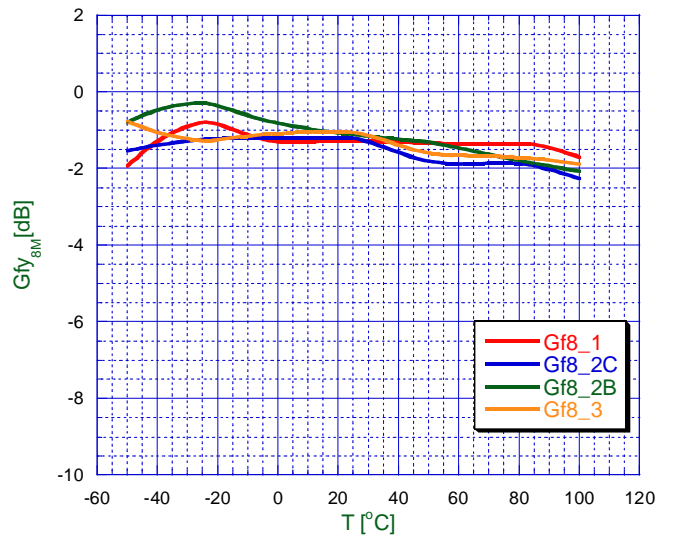
T vs Gv



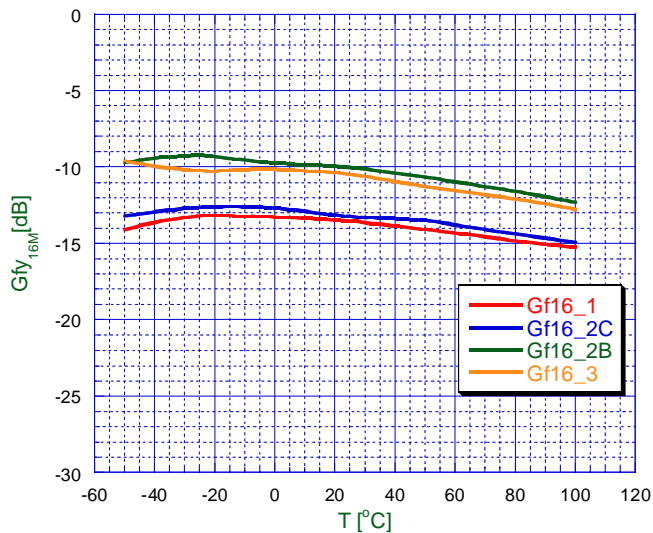
T vs Gfy_{4.5M}



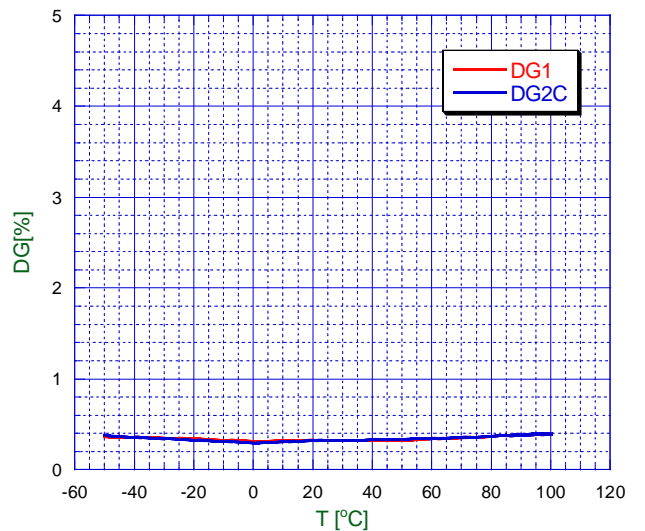
T vs Gfy_{8M}



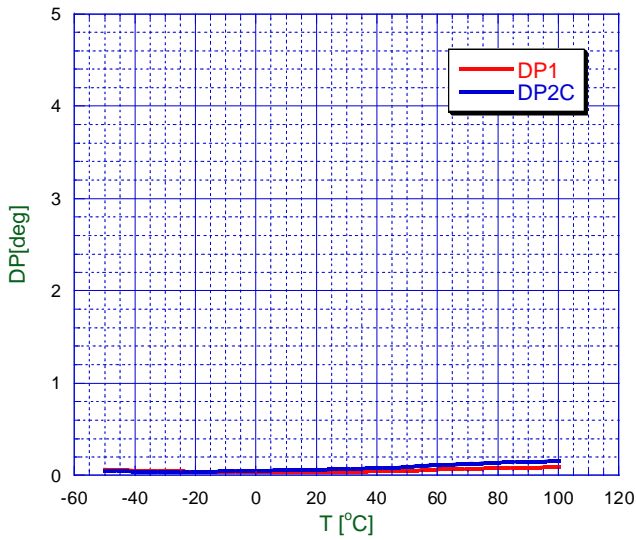
T vs Gfy_{16M}



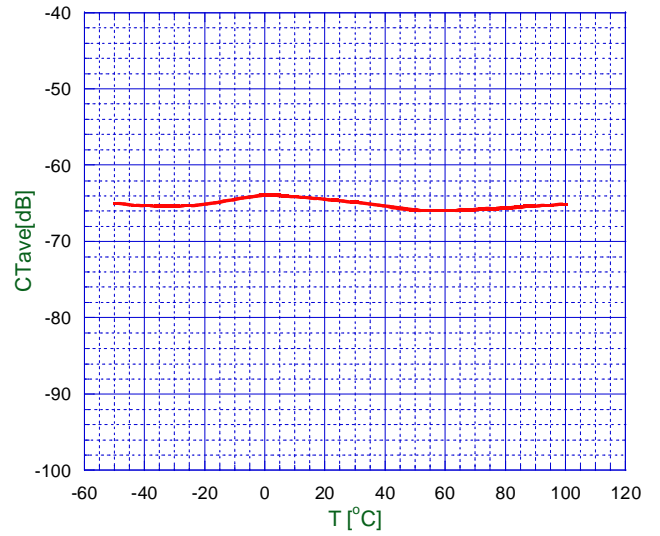
T vs DG



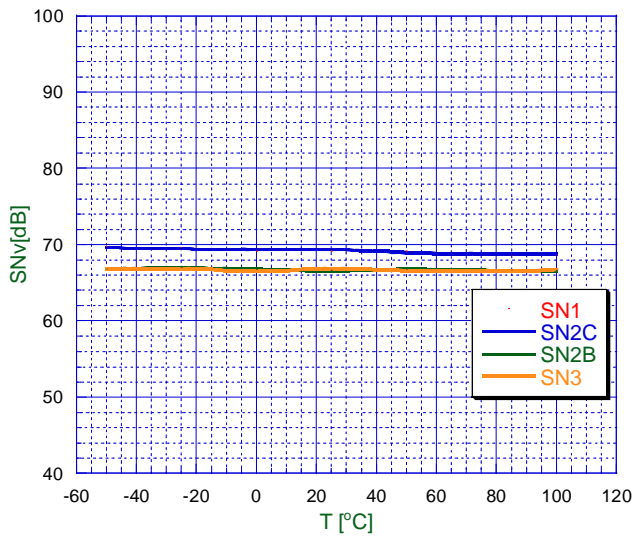
T vs DP



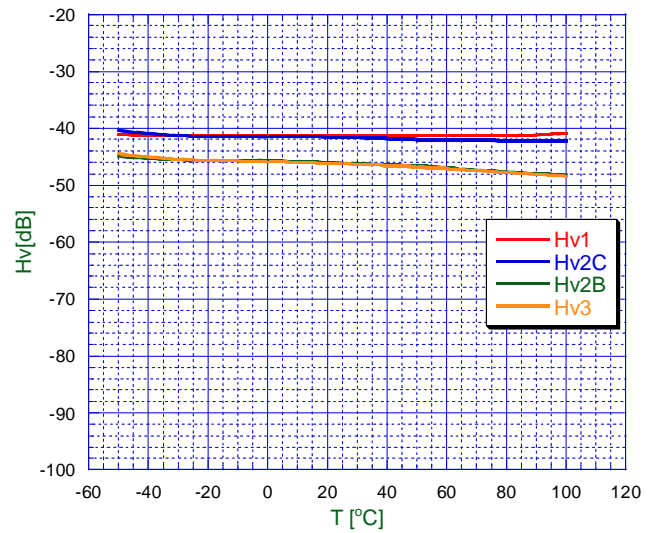
T vs CTave



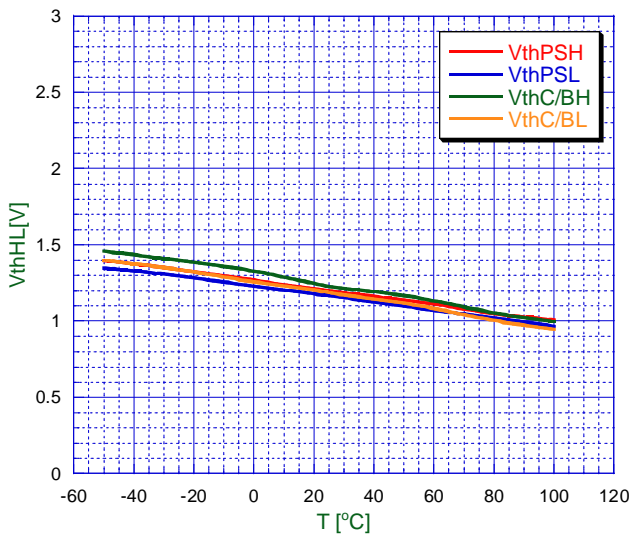
T vs SNv



T vs Hv



T vs VthHL



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