Freescale Semiconductor
Data Sheet

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Consumer Low Power Wireless Transmitter Controller

Features

- Low power (5 W) solution for Wireless Power Consortium (WPC) compliant transmitter design
- Conforms to the latest version low power WPC specifications
- Supports wide DC input voltage range starting from 4.2 V, typically 5 V, 12 V and 19 V
- Integrated digital demodulation on chip
- Supports all types of receiver modulation strategies (AC capacitor, AC resistor and DC resistor)
- Supports Foreign Object Detection (FOD)
- Super low standby power by Freescale Touch technology
- Supports any low power consumer power transmitter solutions using frequency and duty cycle control, or rail voltage control or phase shift control
- LED & buzzer for system status indication
- Over-voltage/current/temperature protection
- Supports CAN/IIC/SCI/SPI interfaces
- Software based solution to provide maximum design freedom and product differentiation
- FreeMASTER GUI tool to enable configuration, calibration and debugging

Applications

- Low Power Wireless Power Transmitter
  Any lower power consumer power transmitter solution with frequency & duty cycle control, or rail voltage control, or phase-shift control (WPC A/B types or customer properties)

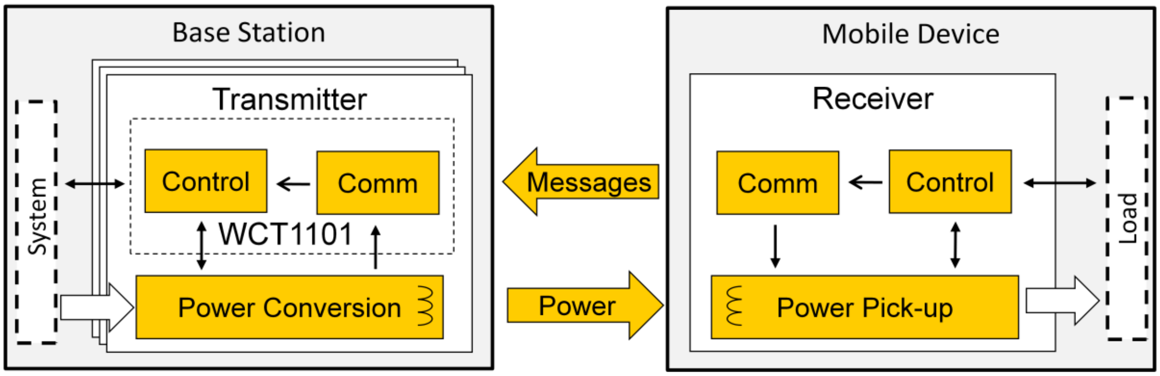
Overview Description

The WCT1101 is a wireless power transmitter controller that integrates all required functions for WPC “Qi” compliant wireless power transmitter design. It’s an intelligent device to work with Freescale touch sensing technology or use periodically analog PING (configurable by user) to detect a mobile device for charging while gaining super low standby power. Once the mobile device is detected, the WCT1101 controls the power transfer by adjusting the operation frequency and duty cycle, or rail voltage, or phase shift of power stage according to message packets sent by mobile device.

To maximize the design freedom and product differentiation, WCT1101 supports any low power consumer power transmitter design (WPC A/B types or customization) using frequency and duty cycle control, or rail voltage control or phase shift control by software based solution. Besides, easy-to-use FreeMASTER GUI tool with configuration, calibration and debugging functions provides user-friendly design experience and speed time-to-market.

The WCT1101 includes digital demodulation module to reduce external components, over-voltage/current/temperature protection, FOD method to protect from overheating by misplaced metallic foreign objects and general CAN/IIC/SCI/SPI interfaces for external communication purpose. It also handles any abnormal condition and operational status, and provides comprehensive indicator outputs for robust system design.

Wireless Charging System Functional Diagram



Contents

1 Absolute Maximum Ratings

1.1 Electrical Operating Ratings

Table 1. Absolute Maximum Electrical Ratings (V_{SS} = 0 V, V_{SSA} = 0 V)

Characteristic	Symbol	Notes[1]	Min.	Max.	Unit
Supply Voltage Range	V_{DD}		–0.3	4.0	V
Analog Supply Voltage Range	V_{DDA}		–0.3	4.0	V
ADC High Voltage Reference	V_{REFHx}		–0.3	4.0	V
Voltage difference V_{DD} to V_{DDA}	ΔV_{DD}		–0.3	0.3	V
Voltage difference V_{SS} to V_{SSA}	ΔV_{ss}		–0.3	0.3	V
Digital Input Voltage Range	V_{IN}	Pin Group 1	–0.3	5.5	V
$\overline{\text{RESET}}$ Input Voltage Range	V_{IN_RESET}	Pin Group 2	–0.3	4.0	V
Oscillator Input Voltage Range	V_{OSC}	Pin Group 4	–0.4	4.0	V
Analog Input Voltage Range	V_{INA}	Pin Group 3	–0.3	4.0	V
Input clamp current, per pin ($V_{IN} < V_{SS} – 0.3$ V)[2, 3]	V_{IC}		–	–5.0	mA
Output clamp current, per pin[4]	V_{OC}		–	±20.0	mA
Contiguous pin DC injection current—regional limit sum of 16 contiguous pins	I_{Icont}		–25	25	mA
Output Voltage Range (normal push-pull mode)	V_{OUT}	Pin Group 1,2	–0.3	4.0	V
Output Voltage Range (open drain mode)	V_{OUTOD}	Pin Group 1	–0.3	5.5	V
$\overline{\text{RESET}}$ Output Voltage Range	V_{OUTOD_RESET}	Pin Group 2	–0.3	4.0	V
DAC Output Voltage Range	V_{OUT_DAC}	Pin Group 5	–0.3	4.0	V
Ambient Temperature	T_A		–40	85	°C
Storage Temperature Range	T_{STG}		–55	150	°C

1. Default Mode:
   - Pin Group 1: GPIO, TDI, TDO, TMS, TCK
   - Pin Group 2: $\overline{\text{RESET}}$
   - Pin Group 3: ADC and Comparator Analog Inputs
   - Pin Group 4: XTAL, EXTAL
   - Pin Group 5: DAC analog output
2. Continuous clamp current.
3. All 5 volt tolerant digital I/O pins are internally clamped to V_{SS} through an ESD protection diode. There is no diode connection to V_{DD}. If VIN greater than VDIO_MIN (= V_{SS} –0.3 V) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed, then a current limiting resistor is required.
4. I/O is configured as push-pull mode.

1.2 Thermal Handling Ratings

Table 2. Thermal Handling Ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	–	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life.*
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.*

1.3 ESD Handling Ratings

Table 3. ESD Handling Ratings

Characteristic[1]	Min.	Max.	Unit
ESD for Human Body Model (HBM)	-2000	+2000	V
ESD for Machine Model (MM)	-200	+200	V
ESD for Charge Device Model (CDM)	-500	+500	V
Latch-up current at TA= 85°C (I_{LAT})	-100	+100	mA

1. Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

1.4 Moisture Handling Ratings

Table 4. Moisture Handling Ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	–	3	–	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.*

2 Electrical Characteristics

2.1 General Characteristics

Table 5. General Electrical Characteristics

Recommended Operating Conditions (V_{REFLx} = 0 V, V_{SSA} = 0 V, V_{SS} = 0 V)							
Characteristic	**Symbol**	**Notes**	**Min.**	**Typ.**	**Max.**	**Unit**	**Test Conditions**
Supply Voltage[2]	V_{DD} ,V_{DDA}		2.7	3.3	3.6	V	-

ADC (Cyclic) Reference Voltage High	V_{REFHA} V_{REFHB}		3.0		V_{DDA}	V	-
Voltage difference V_{DD} to V_{DDA}	ΔV_{DD}		-0.1	0	0.1	V	-
Voltage difference V_{SS} to V_{SSA}	ΔV_{ss}		-0.1	0	0.1	V	-
Input Voltage High (digital inputs)	V_{IH}	1 (Pin Group 1)	0.7×V_{DD}		5.5	V	-
$\overline{\text{RESET}}$ Voltage High	V_{IH_RESET}	1 (Pin Group 2)	0.7×V_{DD}	-	V_{DD}	V	-
Input Voltage Low (digital inputs)	V_{IL}	1 (Pin Group 1,2)			0.35×V_{DD}	V	-
Oscillator Input Voltage High XTAL driven by an external clock source	V_{IHOSC}	1 (Pin Group 4)	2.0		V_{DD} + 0.3	V	-
Oscillator Input Voltage Low	V_{ILOSC}	1 (Pin Group 4)	-0.3		0.8	V	-
Output Source Current High (at V_{OH} min.) [3,4] • Programmed for low drive strength • Programmed for high drive strength	I_{OH}	1 (Pin Group 1) 1 (Pin Group 1)	- -		-2 -9	mA	-
Output Source Current Low (at V_{OL} max.) [3,4] • Programmed for low drive strength • Programmed for high drive strength	I_{OL}	1 (Pin Group 1,2) 1 (Pin Group 1,2)	- -		2 9	mA	-
Output Voltage High	V_{OH}	1 (Pin Group 1)	V_{DD} - 0.5	-	-	V	$I_{OH} = I_{OHmax}$
Output Voltage Low	V_{OL}	1 (Pin Group 1,2)	-	-	0.5	V	$I_{OL} = I_{OLmax}$
Digital Input Current High pull-up enabled or disabled	I_{IH}	1 (Pin Group 1)	-	0	+/-2.5	µA	V_{IN} = 2.4 V to 5.5 V
		1 (Pin Group 2)					V_{IN} = 2.4 V to V_{DD}
Comparator Input Current High	I_{IHC}	1 (Pin Group 3)		0	+/-2	µA	$V_{IN} = V_{DDA}$
Oscillator Input Current High	I_{IHOSC}	1 (Pin Group 4)	-	0	+/-2	µA	$V_{IN} = V_{DDA}$
Internal Pull-Up Resistance	$R_{Pull\text{-}Up}$		20	-	50	kΩ	-
Internal Pull-Down Resistance	$R_{Pull\text{-}Down}$		20	-	50	kΩ	-

Comparator Input Current Low	I_{ILC}	1 (Pin Group 3)	-	0	+/-2	µA	V_{IN} = 0V
Oscillator Input Current Low	I_{ILOSC}	1 (Pin Group 4)	-	0	+/-2	µA	V_{IN} = 0V
DAC Output Voltage Range	V_{DAC}	1 (Pin Group 5)	V_{SSA} + 0.04	-	V_{DDA} - 0.04	V	R_{LD} = 3 kΩ, C_{LD} = 400 pF
Output Current[1] High Impedance State	I_{OZ}	1 (Pin Group 1,2)	-	0	+/-1	µA	-
Schmitt Trigger Input Hysteresis	V_{HYS}	1 (Pin Group 1,2)	0.06×V_{DD}	-	-	V	-
Input capacitance	C_{IN}		-	10	-	pF	-
Output capacitance	C_{OUT}		-	10	-	pF	-
GPIO pin interrupt pulse width[5]	T_{INT_Pulse}	6	1.5	-	-	Bus clock	-
Port rise and fall time (high drive strength). Slew disabled.	$T_{Port\_H\_DIS}$	7	5.5	-	15.1	ns	2.7 ≤ VDD ≤ 3.6 V
Port rise and fall time (high drive strength). Slew enabled.	$T_{Port\_H\_EN}$	7	1.5	-	6.8	ns	2.7 ≤ VDD ≤ 3.6 V
Port rise and fall time (low drive strength). Slew disabled.	$T_{Port\_L\_DIS}$	8	8.2	-	17.8	ns	2.7 ≤ VDD ≤ 3.6 V
Port rise and fall time (low drive strength). Slew enabled.	$T_{Port\_L\_EN}$	8	3.2	-	9.2	ns	2.7 ≤ VDD ≤ 3.6 V
Device (system and core) clock frequency	f_{SYSCLK}		0	-	100	MHz	-
Bus clock	f_{BUS}		-	-	50	MHz	-

1. Default Mode
    - Pin Group 1: GPIO, TDI, TDO, TMS, TCK
    - Pin Group 2: $\overline{\text{RESET}}$
    - Pin Group 3: ADC and Comparator Analog Inputs
    - Pin Group 4: XTAL, EXTAL
    - Pin Group 5: DAC analog output
2. ADC (Cyclic) specifications are not guaranteed when VDDA is below 3.0 V.
3. Total chip source or sink current cannot exceed 75 mA.
4. Contiguous pin DC injection current of regional limit—including sum of negative injection currents or sum of positive injection currents of 16 contiguous pins—is 25 mA.
5. Applies to a pin only when it is configured as GPIO and configured to cause an interrupt by appropriately programming GPIOn_IPOLR and GPIOn_IENR.
6. The greater synchronous and asynchronous timing must be met.
7. 75 pF load.
8. 15 pF load.

2.2 Device Characteristics

Table 6. General Device Characteristics

Power mode Transition Behavior					
Symbol	**Description**	**Min.**	**Max.**	**Unit**	**Notes**
T_{POR}	After a POR event, the amount of delay from when VDD reaches 2.7 V to when the first instruction executes (over the operating temperature range).	199	225	µs	
T_{S2R}	STOP mode to RUN mode	6.79	7.27	µs	1
$T_{LPS2LPR}$	LPS mode to LPRUN mode	240.9	551	µs	2
$T_{VLPS2VLPR}$	VLPS mode to VLPRUN mode	1424	1459	µs	4
T_{W2R}	WAIT mode to RUN mode	0.57	0.62	µs	3
$T_{LPW2LPR}$	LPWAIT mode to LPRUN mode	237.2	554	µs	2
$T_{VLPW2VLPR}$	VLPWAIT mode to VLPRUN mode	1413	1500	µs	4

Power Consumption Operating Behaviors					
Mode	**Conditions**	**Max. Frequency**	**Typical at 3.3 V, 25 °C**		**Notes**
			I_{DD}	**I_{DDA}**	
RUN1	100 MHz core clock, 50 MHz peripheral clock, regulators are in full regulation, relaxation oscillator on, PLL powered on, continuous MAC instructions with fetches from program Flash, all peripheral modules enabled, TMRs and SCIs using 1× peripheral clock, NanoEdge within eFlexPWM using 2× peripheral clock, ADC/DAC (only one 12-bit DAC and all 6-bit DACs) powered on and clocked, comparator powered on, all ports configured as inputs with input low and no DC loads	100 MHz	38.1 mA	9.9 mA	

RUN2	50 MHz core and peripheral clock, regulators are in full regulation, relaxation oscillator on, PLL powered on, continuous MAC instructions with fetches from program Flash, all peripheral modules enabled, TMRs and SCIs using 1× peripheral clock, NanoEdge within eFlexPWM using 2× peripheral clock, ADC/DAC (only one 12-bit DAC and all 6-bit DACs) powered on and clocked, comparator powered on, all ports configured as inputs with input low and no DC loads	50 MHz	27.6 mA	9.9 mA	
WAIT	50 MHz core and peripheral clock, regulators are in full regulation, relaxation oscillator on, PLL powered on, core in WAIT state, all peripheral modules enabled, TMRs and SCIs using 1× clock, NanoEdge within eFlexPWM using 2× clock, ADC/DAC (one 12-bit DAC, all 6-bit DACs)/comparator powered off, all ports configured as inputs with input low and no DC loads	50 MHz	24.0 mA	-	
STOP	4 MHz core and peripheral clock, regulators are in full regulation, relaxation oscillator on, PLL powered off, core in STOP state, all peripheral module and core clocks are off, ADC/DAC/Comparator powered off, all ports configured as inputs with input low and no DC loads	4 MHz	6.3 mA	-	
LPRUN	200 kHz core and peripheral clock from relaxation oscillator's low speed clock, relaxation oscillator in standby mode, regulators are in standby, PLL disabled, repeat NOP instructions, all peripheral modules enabled, except NanoEdge within eFlexPWM and cyclic ADCs, one 12-bit DAC and all 6-bit DACs enabled, simple loop with running from platform instruction buffer, all ports configured as inputs with input low and no DC loads	2 MHz	2.8 mA	3.1 mA	
LPWAIT	200 kHz core and peripheral clock from relaxation oscillator's low speed clock, relaxation oscillator in standby mode, regulators are in standby, PLL disabled, all peripheral modules enabled, except NanoEdge within eFlexPWM and cyclic ADCs, one 12-bit DAC and all 6-bit DACs enabled, core in WAIT mode, all ports configured as inputs with input low and no DC loads	2 MHz	2.7 mA	3.1 mA	

LPSTOP	200 kHz core and peripheral clock from relaxation oscillator's low speed clock, relaxation oscillator in standby mode, regulators are in standby, PLL disabled, only PITs and COP enabled, other peripheral modules disabled and clocks gated off, core in STOP mode, all ports configured as inputs with input low and no DC loads	2 MHz	1.2 mA	-	
VLPRUN	32 kHz core and peripheral clock from a 64 kHz external clock source, oscillator in power down, all relaxation oscillators disabled, large regulator is in standby, small regulator is disabled, PLL disabled, repeat NOP instructions, all peripheral modules, except COP and EWM, disabled and clocks gated off, simple loop running from platform instruction buffer, all ports configured as inputs with input low and no DC loads	200 kHz	0.7 mA	-	
VLPWAIT	32 kHz core and peripheral clock from a 64 kHz external clock source, oscillator in power down, all relaxation oscillators disabled, large regulator is in standby, small regulator is disabled, PLL disabled, all peripheral modules, except COP, disabled and clocks gated off, core in WAIT mode, all ports configured as inputs with input low and no DC loads	200 kHz	0.7 mA	-	
VLPSTOP	32 kHz core and peripheral clock from a 64 kHz external clock source, oscillator in power down, all relaxation oscillators disabled, large regulator is in standby, small regulator is disabled, PLL disabled, all peripheral modules, except COP, disabled and clocks gated off, core in STOP mode, all ports configured as inputs with input low and no DC loads	200 kHz	0.7 mA	-	

Reset and Interrupt Timing

Symbol	Characteristic	Min.	Max.	Unit	Notes
t_{RA}	Minimum $\overline{\text{RESET}}$ Assertion Duration	16	-	ns	5
t_{RDA}	$\overline{\text{RESET}}$ desertion to First Address Fetch	$865 \times T_{OSC} + 8 \times T_{SYSCLK}$	-	ns	6
t_{IF}	Delay from Interrupt Assertion to Fetch of first instruction (exiting STOP mode)	361.3	570.9	ns	

PMC Low-Voltage Detection (LVD) and Power-On Reset (POR) Parameters

Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{POR_A}	POR Assert Voltage[7]	-	2.0	-	V

V_{POR_R}	POR Release Voltage[8]	-	2.7	-	V
V_{LVI_2p7}	LVI_2p7 Threshold Voltage	-	2.73	-	V
V_{LVI_2p2}	LVI_2p2 Threshold Voltage	-	2.23	-	V

JTAG Timing

Symbol	Description	Min.	Max.	Unit	Notes
f_{OP}	TCK frequency of operation	DC	$f_{SYSCLK}/8$	MHz	
t_{PW}	TCK clock pulse width	50	-	ns	
t_{DS}	TMS, TDI data set-up time	5	-	ns	
t_{DH}	TMS, TDI data hold time	5	-	ns	
t_{DV}	TCK low to TDO data valid	-	30	ns	
t_{TS}	TCK low to TDO tri-state	-	30	ns	

Regulator 1.2 V Parameters

Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{CAP}	Output Voltage[9]	-	1.22	-	V
I_{SS}	Short Circuit Current[10]	-	600	-	mA
T_{RSC}	Short Circuit Tolerance (V_{CAP} shorted to ground)	-	-	30	Mins
V_{REF}	Reference Voltage (after trim)	-	1.21	-	V

External Clock Timing

Symbol	Characteristic	Min.	Typ.	Max.	Unit
f_{OSC}	Frequency of operation (external clock driver)	-	-	50	MHz
t_{PW}	Clock pulse width[11]	8			ns
t_{rise}	External clock input rise time[12]	-	-	1	ns
t_{fall}	External clock input fall time[13]	-	-	1	ns
V_{ih}	Input high voltage overdrive by an external clock	$0.85 \times V_{DD}$	-	-	V
V_{il}	Input low voltage overdrive by an external clock	-	-	$0.3 \times V_{DD}$	V

Phase-Locked Loop (PLL) Timing

Symbol	Characteristic	Min.	Typ.	Max.	Unit
f_{Ref_PLL}	PLL input reference frequency[14]	8	8	16	MHz
f_{OP_PLL}	PLL output frequency[15]	200	-	400	MHz
t_{Lock_PLL}	PLL lock time[16]	35.5	-	73.2	µs
t_{DC_PLL}	Allowed Duty Cycle of input reference	40	50	60	%

External Crystal or Resonator Specifications

Symbol	Characteristic	Min.	Typ.	Max.	Unit
f_{XOSC}	Frequency of operation	4	8	16	MHz

Relaxation Oscillator Electrical Specifications

Symbol	Characteristic	Min.	Typ.	Max.	Unit
f_{ROSC_8M}	8 MHz Output Frequency[17] RUN Mode • 0 °C to 85 °C • -40 °C to 85 °C Standby Mode (IRC trimmed @ 8 MHz) • -40 °C to 85 °C	7.84 7.76 -	8 8 405	8.16 8.24 -	MHz MHz kHz
$f_{ROSC\_8M\_Delta}$	8 MHz Frequency Variation over 25 °C RUN Mode Due to temperature • 0 °C to 85 °C • -40 °C to 85 °C	- -	+/-1.5 +/-1.5	+/-2 +/-3	% %
f_{ROSC_200k}[17]	200 kHz Output Frequency[18] RUN Mode • -40 °C to 85 °C	194	200	206	kHz
$f_{ROSC\_200k\_Delta}$[17]	200 kHz Output Frequency Variation over 25 °C[18] RUN Mode Due to temperature • 0 °C to 85 °C • -40 °C to 85 °C	- -	+/-1.5 +/-1.5	+/-2 +/-3	% %
t_{Stab}	Stabilization Time • 8 MHz output[19] • 200 kHz output[20]	- -	0.12 10	- -	µs µs
t_{DC_ROSC}	Output Duty Cycle	48	50	52	%

Flash Specifications

Symbol	Description	Min.	Typ.	Max.	Unit
t_{hvpgm4}	Longword Program high-voltage time	-	7.5	18	µs
$t_{hversscr}$	Sector Erase high-voltage time[21]	-	13	113	ms
$t_{hversall}$	Erase All high-voltage time[21]	-	52	452	ms
$t_{rd1sec1k}$	Read 1s Section execution time (flash sector)[22]	-	-	60	µs
t_{pgmchk}	Program Check execution time[22]	-	-	45	µs
t_{rdrsrc}	Read Resource execution time[22]	-	-	30	µs
t_{pgm4}	Program Longword execution time	-	65	145	µs
t_{ersscr}	Erase Flash Sector execution time[23]	-	14	114	ms

t_{rd1all}	Read 1s All Blocks execution time	-	-	0.9	ms
t_{rdonce}	Read Once execution time[22]	-	-	25	µs
$t_{pgmonce}$	Program Once execution time	-	65	-	µs
t_{ersall}	Erase All Blocks execution time[23]	-	70	575	ms
t_{vfykey}	Verify Backdoor Access Key execution time[22]	-	-	30	µs
$t_{flashret10k}$	Data retention after up to 10 K cycles	5	50[24]	-	years
$t_{flashret1k}$	Data retention after up to 1 K cycles	20	100[24]	-	years
$n_{flashcyc}$	Cycling endurance[25]	10 K	50 K[24]	-	cycles

12-bit Cyclic ADC Electrical Specifications

Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{DDA}	Supply voltage[26]	3.0	3.3	3.6	V
V_{REFHX}	V_{REFH} supply voltage[27]	V_{DDA} - 0.6		V_{DDA}	V
f_{ADCCLK}	ADC conversion clock[28]	0.1	-	10	MHz
R_{ADC}	Conversion range[29] • Fully differential • Single-ended/unipolar	 -(V_{REFH} - V_{REFL}) V_{REFL}	 - -	 V_{REFH} - V_{REFL} V_{REFH}	 V V
V_{ADCIN}	Input voltage range (per input)[30] • External Reference • Internal Reference	 V_{REFL} V_{SSA}	 - -	 V_{REFH} V_{DDA}	 V V
t_{ADC}	Conversion time	-	8	-	t_{ADCCLK}
t_{ADCPU}	ADC power-up time (from adc_pdn)	-	13	-	t_{ADCCLK}
I_{ADCRUN}	ADC RUN current (per ADC block)	-	1.8	-	mA
$I_{ADPWRDWN}$	ADC power down current (adc_pdn enabled)	-	0.1	-	µA
I_{VREFH}	V_{REFH} current (in external mode)	-	190	225	µA
INL_{ADC}	Integral non-linearity[31]	-	+/- 1.5	+/- 2.2	LSB[32]
DNL_{ADC}	Differential non-linearity[31]	-	+/- 0.5	+/- 0.8	LSB[32]
V_{OFFSET}	Offset[33] • Fully differential • Single ended/Unipolar	 - -	 +/- 8 +/- 12	 - -	 mV mV
E_{GAIN}	Gain Error	-	0.996 to 1.004	0.99 to 1.101	-
ENOB	Effective number of bits	-	10.6	-	bits
I_{INJ}	Input injection current[34]	-	-	+/-3	mA
C_{ADCI}	Input sampling capacitance	-	4.8	-	pF

12-bit DAC Electrical Specifications

Symbol	Characteristic	Min.	Typ.	Max.	Unit

t_{SETTLE}	Settling time[35] under R_{LD} = 3 kΩ, C_{LD} = 400 pF	-	1	-	µs
t_{DACPU}	DAC power-up time (from PWRDWN release to valid DACOUT)	-	-	11	µs
INL_{DAC}	Integral non-linearity[37]	-	+/- 3	+/- 4	LSB[36]
DNL_{DAC}	Differential non-linearity[37]	-	+/- 0.8	+/- 0.9	LSB[36]
MON_{DAC}	Monotonicity (> 6 sigma monotonicity, < 3.4 ppm non-monotonicity)	Guaranteed			-
V_{OFFSET}	Offset error[37] (5% to 95% of full range)	-	+/- 25	+/- 43	mV
E_{GAIN}	Gain error[37] (5% to 95% of full range)	-	+/- 0.5	+/- 1.5	%
V_{OUT}	Output voltage range	V_{SSA} + 0.04	-	V_{DDA} - 0.04	V
SNR	Signal-to-noise ratio	-	85	-	dB
ENOB	Effective number of bits	-	11	-	bits

Comparator and 6-bit DAC Electrical Specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	2.7	-	3.6	V
I_{DDHS}	Supply current, High-speed mode(EN=1, PMODE=1)	-	300	-	µA
I_{DDLS}	Supply current, Low-speed mode(EN=1, PMODE=0)	-	36	-	µA
V_{AIN}	Analog input voltage	V_{ss}	-	V_{DD}	V
V_{AIO}	Analog input offset voltage	-	-	20	mV
V_H	Analog comparator hysteresis[38]				
	• CR0[HYSTCTR]=00	-	5	13	mV
	• CR0[HYSTCTR]=01	-	25	48	mV
	• CR0[HYSTCTR]=10	-	55	105	mV
	• CR0[HYSTCTR]=11	-	80	148	mV
V_{CMPOh}	Output high	V_{DD} - 0.5	-	-	V
V_{CMPOl}	Output low	-	-	0.5	V
t_{DHS}	Propagation delay, high-speed mode(EN=1, PMODE=1)[39]	-	25	50	ns
t_{DLS}	Propagation delay, low-speed mode(EN=1, PMODE=0) [39]	-	60	200	ns
t_{DInit}	Analog comparator initialization delay[40]	-	40	-	µs
I_{DAC6b}	6-bit DAC current adder (enabled)	-	7	-	µA
R_{DAC6b}	6-bit DAC reference inputs	V_{DDA}	-	V_{DD}	V

INL_{DAC6b}	6-bit DAC integral non-linearity	-0.5	-	0.5	LSB[41]
DNL_{DAC6b}	6-bit DAC differential non-linearity	-0.3	-	0.3	LSB[41]

eFlexPWM Timing Parameters

Symbol	Characteristic	Min.	Typ.	Max.	Unit
f_{PWM}	PWM clock frequency	-	100	-	MHz
S_{PWMNEP}	NanoEdge Placement (NEP) step size[42,43]	-	312	-	ps
t_{DFLT}	Delay for fault input activating to PWM output deactivated	1	-	-	ns
t_{PWMPU}	Power-up time[44]	-	25	-	µs

Quad Timer Timing

Symbol	Characteristic	Min.	Max.	Unit	Notes
P_{IN}	Timer input period	$2T_{timer} + 6$	-	ns	45
P_{INHL}	Timer input high/low period	$1T_{timer} + 3$	-	ns	45
P_{OUT}	Timer output period	$2T_{timer} - 2$	-	ns	45
P_{OUTHL}	Timer output high/low period	$1T_{timer} - 2$	-	ns	45

QSPI Timing

Symbol	Characteristic	Min.		Max.		Unit
		Master	Slave	Master	Slave	
t_C	Cycle time	60	60	-	-	ns
t_{ELD}	Enable lead time	-	20	-	-	ns
t_{ELG}	Enable lag time	-	20	-	-	ns
t_{CH}	Clock (SCLK) high time	28	28	-	-	ns
t_{CL}	Clock (SCLK) low time	28	28	-	-	ns
t_{DS}	Data set-up time required for inputs	20	1	-	-	ns
t_{DH}	Data hold time required for inputs	1	3	-	-	ns
t_A	Access time (time to data active from high-impedance state)		5		-	ns
t_D	Disable time (hold time to high-impedance state)		5		-	ns
t_{DV}	Data valid for outputs	-	-			ns
t_{DI}	Data invalid	0	0	-	-	ns
t_R	Rise time	-	-	1	1	ns
t_F	Fall time	-	-	1	1	ns

QSCI Timing

Symbol	Characteristic	Min.	Max.	Unit	Notes
BR_{SCI}	Baud rate	-	$(f_{MAX\_SCI}/16)$	Mbit/s	46
PW_{RXD}	RXD pulse width	$0.965/BR_{SCI}$	$1.04/BR_{SCI}$	ns	

PW_{TXD}	TXD pulse width	$0.965/BR_{SCI}$	$1.04/BR_{SCI}$	ns	

CAN Timing

Symbol	Characteristic	Min.	Max.	Unit	Notes
BR_{CAN}	Baud rate	-	1	Mbit/s	
T_{WAKEUP}	CAN Wakeup dominant pulse filtered	-	1.5	µs	
T_{WAKEUP}	CAN Wakeup dominant pulse pass	5	-	µs	

IIC Timing

Symbol	Characteristic	Min.		Max.		Unit	Notes
		Min.	Max.	Min.	Max.		
f_{SCL}	SCL clock frequency	0	100	0	400	kHz	
t_{HD_STA}	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4	-	0.6	-	µs	
t_{SCL_LOW}	LOW period of the SCL clock	4.7	-	1.3	-	µs	
t_{SCL_HIGH}	HIGH period of the SCL clock	4	-	0.6	-	µs	
t_{SU_STA}	Set-up time for a repeated START condition	4.7	-	0.6	-	µs	
t_{HD_DAT}	Data hold time for IIC bus devices	0[47]	3.45[48]	0[49]	0.9[47]	µs	
t_{SU_DAT}	Data set-up time	250[50]	-	100[51]	-	ns	48
t_r	Rise time of SDA and SCL signals	-	1000	$20 + 0.1C_b$	300	ns	52
t_f	Fall time of SDA and SCL signals	-	300	$20 + 0.1C_b$	300	ns	51
t_{SU_STOP}	Set-up time for STOP condition	4	-	0.6	-	µs	
t_{BUS_Free}	Bus free time between STOP and START condition	4.7	-	1.3	-	µs	
t_{SP}	Pulse width of spikes that must be suppressed by the input filter	N/A	N/A	0	50	ns	

1. CPU clock = 4 MHz and System running from 8 MHz IRC Applicable to all wakeup times: Wakeup times (in 1,2,3,4) are measured from GPIO toggle for wakeup till GPIO toggle at the wakeup interrupt subroutine from respective stop/wait mode.
2. CPU clock = 200 kHz and 8 MHz IRC on standby. Exit via interrupt on Port C GPIO.
3. Clock configuration: CPU and system clocks= 100 MHz; Bus Clock = 50 MHz. Exit via an interrupt on PortC GPIO.
4. Using 64 KHz external clock; CPU Clock = 32 KHz. Exit via an interrupt on PortC GPIO.
5. If the $\overline{\text{RESET}}$ pin filter is enabled by setting the RST_FLT bit in the SIM_CTRL register to 1, the minimum pulse assertion must be greater than 21 ns.
6. TOSC means oscillator clock cycle; TSYSCLK means system clock cycle.
7. During 3.3 V VDD power supply ramp down.
8. During 3.3 V VDD power supply ramp up (gated by LVI_2p7).
9. Value is after trim.
10. Guaranteed by design.
11. The chip may not function if the high or low pulse width is smaller than 6.25 ns.
12. External clock input rise time is measured from 10% to 90%.
13. External clock input fall time is measured from 90% to 10%.
14. An externally supplied reference clock should be as free as possible from any phase jitter for the PLL to work correctly. The PLL is optimized for 8 MHz input.
15. The frequency of the core system clock cannot exceed 100 MHz. If the NanoEdge PWM is available, the PLL output must be set to 400 MHz.

16. This is the time required after the PLL is enabled to ensure reliable operation.
17. Frequency after application of 8 MHz trimmed.
18. Frequency after application of 200 kHz trimmed.
19. Standby to run mode transition.
20. Power down to run mode transition.
21. Maximum time based on expectations at cycling end-of-life.
22. Assumes 25 MHz flash clock frequency.
23. Maximum times for erase parameters based on expectations at cycling end-of-life.
24. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
25. Cycling endurance represents number of program/erase cycles at $-40^\circ C \le T_j \le 125^\circ C$.
26. The ADC functions up to VDDA = 2.7 V. When VDDA is below 3.0 V, ADC specifications are not guaranteed.
27. When the input is at the V_{REFL} level, the resulting output will be all zeros (hex 000), plus any error contribution due to offset and gain error. When the input is at the V_{REFH} level the output will be all ones (hex FFF), minus any error contribution due to offset and gain error.
28. ADC clock duty cycle is 45% ~ 55%.
29. Conversion range is defined for x1 gain setting. For x2 and x4 the range is 1/2 and 1/4, respectively.
30. In unipolar mode, positive input must be ensured to be always greater than negative input.
31. INL_{ADC}/DNL_{ADC} is measured from VADCIN = VREFL to VADCIN = VREFH using Histogram method at x1 gain setting.
32. Least Significant Bit = 0.806 mV at 3.3 V VDDA, x1 gain setting.
33. Any off-channel with 50 kHz full-scale input to the channel being sampled with DC input (isolation crosstalk).
34. The current that can be injected into or sourced from an unselected ADC input without affecting the performance of the ADC.
35. Settling time is swing range from VSSA to VDDA.
36. LSB = 0.806 mV.
37. No guaranteed specification within 5% of VDDA or VSSA.
38. Typical hysteresis is measured with input voltage range limited to 0.7 to VDD-0.7 V.
39. Signal swing is 100 mV.
40. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
41. 1 LSB = Vreference/64.
42. Reference IPbus clock of 100 MHz in NanoEdge Placement mode.
43. Temperature and voltage variations do not affect NanoEdge Placement step size.
44. Powerdown to NanoEdge mode transition.
45. Ttimer = Timer input clock cycle. For 100 MHz operation, Ttimer = 10 ns.
46. fMAX_SCI is the frequency of operation of the SCI clock in MHz, which can be selected as the bus clock or 2x bus clock for the device.
47. The master mode IIC deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
48. The maximum tHD_DAT must be met only if the device does not stretch the LOW period (tSCL_LOW) of the SCL signal.
49. Input signal Slew = 10 ns and Output Load = 50 pF
50. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
51. A Fast mode IIC bus device can be used in a Standard mode IIC bus system, but the requirement tSU_DAT ≥ 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line trmax + tSU_DAT = 1000 + 250 = 1250 ns (according to the Standard mode IIC bus specification) before the SCL line is released.
52. Cb = total capacitance of the one bus line in pF.

2.3 Thermal Operating Characteristics

Table 7. General Thermal Characteristics

Symbol	Description	Min.	Max.	Unit
T_J	Die junction temperature	-40	125	°C
T_A	Ambient temperature	-40	85	°C

3 Typical Performance Characteristics

3.1 System Efficiency

The typical maximum system efficiency (receiver output power vs. transmitter input power) on Freescale WCT1101 based transmitter solutions can usually reach 70 plus percentage. Of course, the detailed number depends on the specific solution type. For example, Freescale A11 reference solution has more than 75% system efficiency with bq51013AEVM-764 receiver module.

Note: Power components are the main factor to determine the system efficiency, such as drivers and MOSFETs.

3.2 Standby Power

The purpose of the standby mode of operation is to reduce the power consumption of a wireless power transfer system when power transfer is not required. There are two ways to enter standby mode. The first is when the transmitter doesn’t detect the presence of a valid receiver. The second is when the receiver sends only an End Power Transfer Packet. In standby mode, the transmitter only monitors if a receiver is placed on the active charging area of the transmitter or removed there from.

It is recommended that the transmitter’s power consumption in standby mode meets the relative regional regulations especially for “No-load power consumption”.

In Freescale A11 reference design solution:

- Transmitter power consumption in standby mode with Analog PING technology: < 12 mA (60 mW with 5 V DC input)
- Transmitter power consumption in standby mode with Touch Sensor technology: < 5 mA (25 mW with 5 V DC input)

3.3 Digital Demodulation

To optimize system BOM cost, WCT1101 solution employs digital demodulation algorithm to communicate with receiver. This method can achieve high performance, low cost, and very simple coil signal sensing circuit with less component number.

3.4 Foreign Object Detection

WCT1101 solution employs flexible, intelligent and easy-to-use FOD algorithm to ensure accurate foreign metal objects detection. With Freescale FreeMASTER GUI tool, FOD algorithm can be easily calibrated to get accurate power loss information especially for very sensitive foreign objects.

3.5 Dynamic Input Power Limit

When the transmitter is powered by a limited power supply, such as USB power, WCT1101 can limit the transmitter output power and provide necessary margin relative to the input power supply capability. By monitoring the input voltage and input current of the transmitter, when it drops to a specified level and still positive Control Error Packet (CEP) is received, WCT1101 will stop increasing power output and control transmitter operation in input power limit status. Users can know the system is in DIPL control mode by LED indication, LED1 and LED2 will be in fast blinking mode when input power is limited. WCT1101 will exit DIPL control mode and return to normal PID control mode if a negative Control Error Packet (CEP) is received to reduce output power. The input voltage level for DIPL control can be configured in the WCT1101 example project.

4 Device Information

4.1 Functional Block Diagram

This functional block diagram just shows the functional block pin assignment information of MWCT1101CLH. For the detailed pin multiplexing information, please see Section 4.4 of “Pin Function Description”.

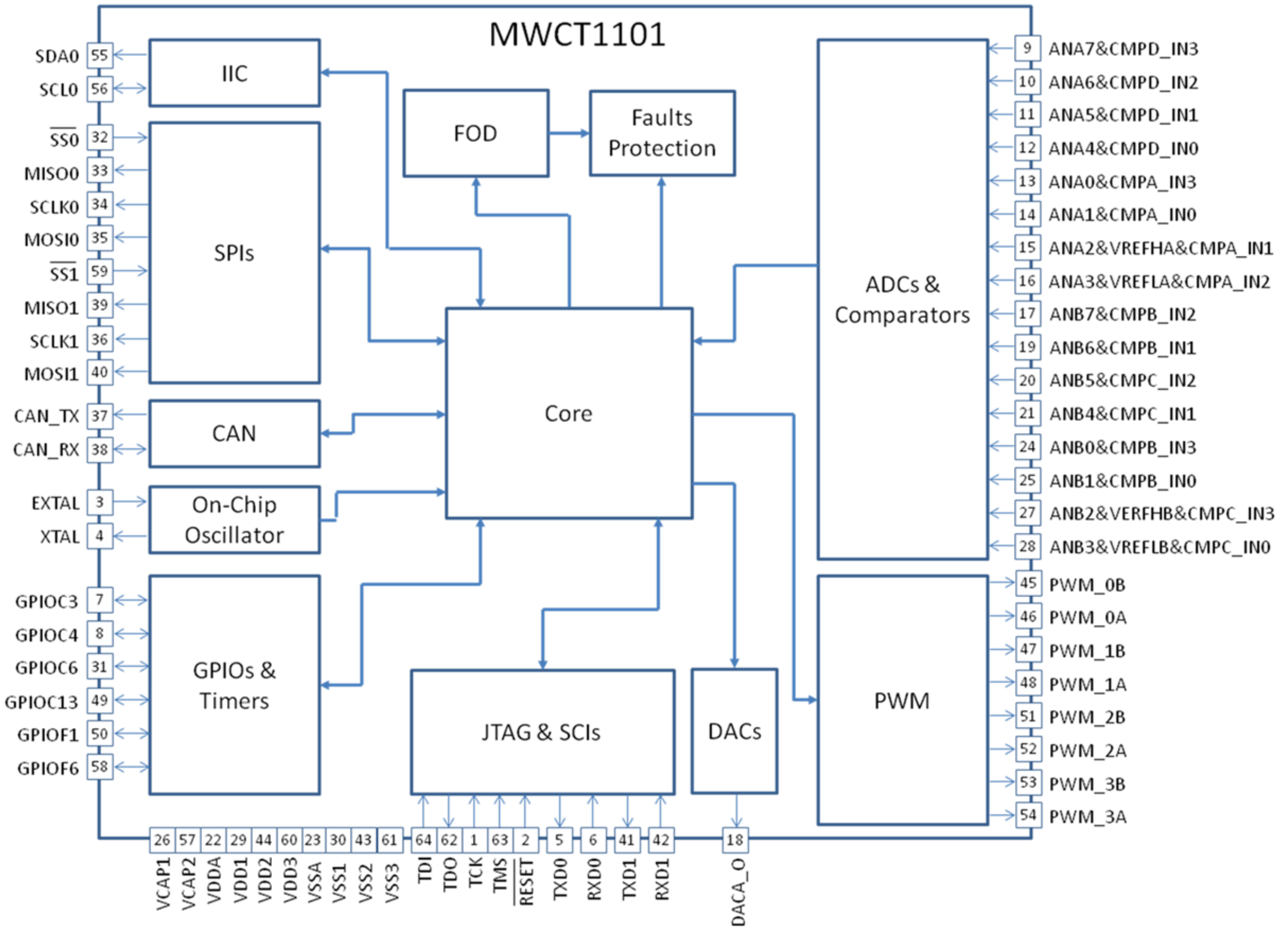


Figure 3. MWCT1101CLH Function Block Diagram

4.2 Product Features Overview

The following table highlights the main on-chip resource features of MWCT1101 device.

Table 8. Product Features Overview

Part	WCT1101
Maximum Core/Bus Clock (MHz)	100/50
Maximum Fully Run Current Consumption (mA)	38.1 (V_{DD}) + 9.9 (V_{DDA})
On-Chip Program Flash Memory Size (KB)	64
On-Chip SRAM Memory Size (KB)	8
Memory Resource Protection	Yes
Inter-Peripheral Crossbar Switches with AOI	Yes
On-Chip Relaxation Oscillator	1 (8 MHz) + 1 (200 kHz)
Windowed Computer Operating Properly	1
External Watchdog Monitor	1
Cyclic Redundancy Check	1

Periodic Interrupt Timer		2
Quad Timer		1 x 4
12-bit Cyclic ADC Channels		2 x 8
PWM Channels	High-Resolution	8
	Standard	4
12-bit DAC		2
Analog Comparator /w 6-bit REF DAC		4
DMA Channels		4
Queued Serial Communications Interface		2
Queued Serial Peripheral Interface		2
Inter-Integrated Circuit		1
Controller Area Network (MSCAN)		1
GPIO		54
Package		64 LQFP

4.3 Pinout Diagram

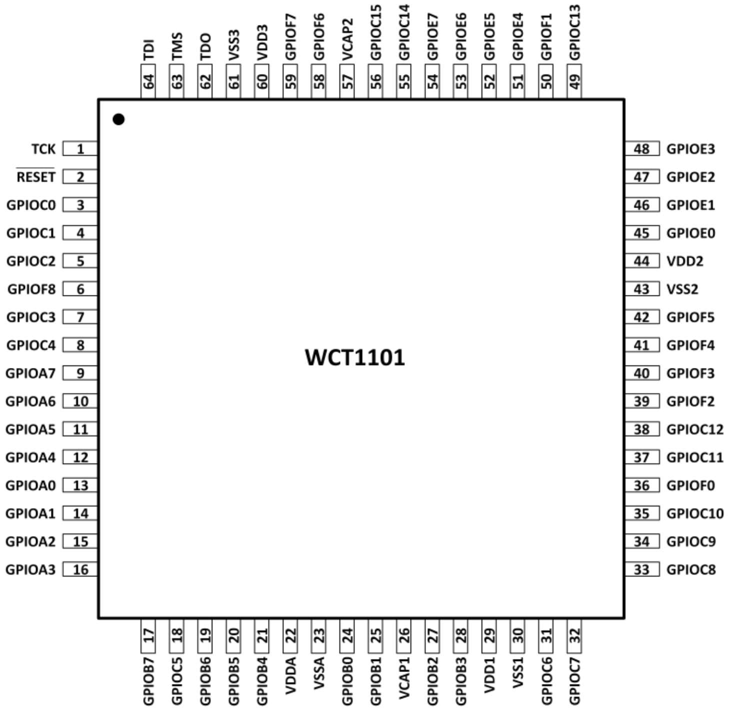


Figure 4. MWCT1101CLH Pinout Diagram

4.4 Pin Function Description

By default, each pin is configured for its primary function (listed first). Any alternative functionality, shown in parentheses, can be programmed through GPIO module peripheral enable registers and SIM module GPIO peripheral select registers.

Table 9. Pin Signal Descriptions

Signal Name	Pin No.	Multiplexing Signals	Function Description
TCK	1	GPIOD2	Test Clock Input — This input pin provides a gated clock to synchronize the test logic and shift serial data to the JTAG/EOnCE port. The pin is connected internally to a pull-up resistor. A Schmitt-trigger input is used for noise immunity. Port D GPIO — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is TCK.
$\overline{\text{RESET}}$	2	GPIOD4	$\overline{\text{RESET}}$ — This input is a direct hardware reset on the processor. When $\overline{\text{RESET}}$ is asserted low, the device is initialized and placed in the reset state. A Schmitt-trigger input is used for noise immunity. The internal reset signal is de-asserted synchronous with the internal clocks after a fixed number of internal clocks. Port D GPIO — This GPIO pin can be individually programmed as an input or output pin. If $\overline{\text{RESET}}$ functionality is disabled in this mode and the chip can be reset only via POR, COP reset, or software reset. After reset, the default state is $\overline{\text{RESET}}$.
GPIOC0	3	EXTAL/CLKIN0	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin. EXTAL — External Crystal Oscillator Input. This input connects the internal crystal oscillator input to an external crystal or ceramic resonator. CLKIN0 — This pin serves as an external clock input 0. After reset, the default state is GPIOC0.
GPIOC1	4	XTAL	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin. XTAL — External Crystal Oscillator Output. This output connects the internal crystal oscillator output to an external crystal or ceramic resonator. After reset, the default state is GPIOC1.
GPIOC2	5	TXD0/XB_OUT11/XB_IN2/CLKO0	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin. TXD0 — The SCI0 transmit data output or transmit/receive in single wire operation. XB_OUT11 — Crossbar module output 11. XB_IN2 — Crossbar module input 2. CLKO0 — This is a buffered clock output 0; the clock source is selected by clock out select (CLKOSEL) bits in the clock output select register (CLKOUT) of the SIM.

			After reset, the default state is GPIOC2.
GPIOF8	6	RXD0/XB_OUT10/CMPD_O/PWM_2X	Port F GPIO — This GPIO pin can be individually programmed as an input or output pin. RXD0 — The SCI0 receive data input. XB_OUT10 — Crossbar module output 10. CMPD_O — Analog comparator D output. PWM_2X — NanoEdge eFlexPWM sub-module 2 output X or input capture X. After reset, the default state is GPIOF8.
GPIOC3	7	TA0/CMPA_O/RXD0/CLKIN1	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin. TA0 — Quad timer module A channel 0 input/output. CMPA_O — Analog comparator A output. RXD0 — The SCI0 receive data input. CLKIN1 — This pin serves as an external clock input 1. After reset, the default state is GPIOC3.
GPIOC4	8	TA1/CMPB_O/XB_IN6/$\overline{\mathrm{EWM\_OUT}}$	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin. TA1 — Quad timer module A channel 1 input/output. CMPB_O — Analog comparator B output. XB_IN6 — Crossbar module input 6. $\overline{\mathrm{EWM\_OUT}}$ — External watchdog monitor output. After reset, the default state is GPIOC4.
GPIOA7	9	ANA7&CMPD_IN3	Port A GPIO — This GPIO pin can be individually programmed as an input or output pin. ANA7&CMPD_IN3 — Analog input to channel 7 of ADCA and input 3 of analog comparator D. When used as an analog input, the signal goes to the ANA7 and CMPD_IN3. After reset, the default state is GPIOA7.
GPIOA6	10	ANA6&CMPD_IN2	Port A GPIO — This GPIO pin can be individually programmed as an input or output pin. ANA6&CMPD_IN2 — Analog input to channel 6 of ADCA and input 2 of analog comparator D. When used as an analog input, the signal goes to the ANA6 and CMPD_IN2. After reset, the default state is GPIOA6.
GPIOA5	11	ANA5&CMPD_IN1	Port A GPIO — This GPIO pin can be individually programmed as an input or output pin. ANA5&CMPD_IN1 — Analog input to channel 5 of ADCA and input 1 of analog comparator D. When used as an analog input, the signal goes to the

			ANA5 and CMPD_IN1. After reset, the default state is GPIOA5.
GPIOA4	12	ANA4&CMPD_IN0	Port A GPIO — This GPIO pin can be individually programmed as an input or output pin. ANA4&CMPD_IN0 — Analog input to channel 4 of ADCA and input 0 of analog comparator D. When used as an analog input, the signal goes to the ANA4 and CMPD_IN0. After reset, the default state is GPIOA4.
GPIOA0	13	ANA0&CMPA_IN3/CMPC_O	Port A GPIO — This GPIO pin can be individually programmed as an input or output pin. ANA0&CMPA_IN3 — Analog input to channel 0 of ADCA and input 3 of analog comparator A. When used as an analog input, the signal goes to the ANA0 and CMPA_IN3. CMPC_O — Analog comparator C output. After reset, the default state is GPIOA0.
GPIOA1	14	ANA1&CMPA_IN0	Port A GPIO — This GPIO pin can be individually programmed as an input or output pin. ANA1 and CMPA_IN0 — Analog input to channel 1 of ADCA and input 0 of analog comparator A. When used as an analog input, the signal goes to the ANA1 and CMPA_IN0. After reset, the default state is GPIOA1.
GPIOA2	15	ANA2&VREFHA&CMPA_IN1	Port A GPIO — This GPIO pin can be individually programmed as an input or output pin. ANA2&VREFHA&CMPA_IN1 — Analog input to channel 2 of ADCA and analog references high of ADCA and input 1 of analog comparator A. When used as an analog input, the signal goes to ANA2 and VREFHA and CMPA_IN1. ADC control register configures this input as ANA2 or VREFHA. After reset, the default state is GPIOA2.
GPIOA3	16	ANA3&VREFLA&CMPA_IN2	Port A GPIO — This GPIO pin can be individually programmed as an input or output pin. ANA3&VREFLA&CMPA_IN2 — Analog input to channel 3 of ADCA and analog references low of ADCA and input 2 of analog comparator A. When used as an analog input, the signal goes to ANA3 and VREFLA and CMPA_IN2. ADC control register configures this input as ANA3 or VREFLA. After reset, the default state is GPIOA3.
GPIOB7	17	ANB7&CMPB_IN2	Port B GPIO — This GPIO pin can be individually programmed as an input or output pin. ANB7&CMPB_IN2 — Analog input to channel 7 of ADCB and input 2 of analog comparator B. When used as an analog input, the signal goes to the ANB7 and CMPB_IN2. After reset, the default state is GPIOB7.
GPIOC5	18	DACA_O/XB_IN7	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin. DACA_O — 12-bit Digital-to-Analog Converter A output.

			XB_IN7 — Crossbar module input 7. After reset, the default state is GPIOC5.
GPIOB6	19	ANB6&CMPB_IN1	Port B GPIO — This GPIO pin can be individually programmed as an input or output pin. ANB6&CMPB_IN1 — Analog input to channel 6 of ADCB and input 1 of analog comparator B. When used as an analog input, the signal goes to the ANB6 and CMPB_IN1. After reset, the default state is GPIOB6.
GPIOB5	20	ANB5&CMPC_IN2	Port B GPIO — This GPIO pin can be individually programmed as an input or output pin. ANB5&CMPC_IN2 — Analog input to channel 5 of ADCB and input 2 of analog comparator C. When used as an analog input, the signal goes to the ANB5 and CMPC_IN2. After reset, the default state is GPIOB5.
GPIOB4	21	ANB4&CMPC_IN1	Port B GPIO — This GPIO pin can be individually programmed as an input or output pin. ANB4&CMPC_IN1 — Analog input to channel 4 of ADCB and input 1 of analog comparator C. When used as an analog input, the signal goes to the ANB4 and CMPC_IN1. After reset, the default state is GPIOB4.
VDDA	22	-	Analog Power — This pin supplies 3.3 V power to the analog modules. It must be connected to a clean analog power supply.
VSSA	23	-	Analog Ground — This pin supplies an analog ground to the analog modules. It must be connected to a clean power supply.
GPIOB0	24	ANB0&CMPB_IN3	Port B GPIO — This GPIO pin can be individually programmed as an input or output pin. ANB0&CMPB_IN3 — Analog input to channel 0 of ADCB and input 3 of analog comparator B. When used as an analog input, the signal goes to ANB0 and CMPB_IN3. After reset, the default state is GPIOB0.
GPIOB1	25	ANB1&CMPB_IN0/DACB_O	Port B GPIO — This GPIO pin can be individually programmed as an input or output pin. ANB1&CMPB_IN0 — Analog input to channel 1 of ADCB and input 0 of analog comparator B. When used as an analog input, the signal goes to ANB1 and CMPB_IN0. DACB_O — 12-bit Digital-to-Analog Converter B output. After reset, the default state is GPIOB1.
VCAP1	26	-	Connect a 2.2 µF or greater bypass capacitor between this pin and VSS to stabilize the core voltage regulator output required for proper device operation.
GPIOB2	27	ANB2&VREFHB&CMPC_IN3	Port B GPIO — This GPIO pin can be individually programmed as an input or output pin. ANB2&VREFHB&CMPC_IN3 — Analog input to channel 2 of ADCB and analog references high of ADCB and input 3 of analog comparator C. When used as an analog input, the signal goes to ANB2 and VREFHB and CMPC_IN3. ADC control register configures this input as ANB2 or VREFHB.

			After reset, the default state is GPIOB2.
GPIOB3	28	ANB3&VREFLB&CMPC_IN0	Port B GPIO — This GPIO pin can be individually programmed as an input or output pin. ANB3&VREFLB&CMPC_IN0 — Analog input to channel 3 of ADCB and analog references low of ADCB and input 0 of analog comparator C. When used as an analog input, the signal goes to ANB3 and VREFLB and CMPC_IN0. ADC control register configures this input as ANB3 or VREFLB. After reset, the default state is GPIOB3.
VDD1	29	-	I/O Power — Supplies 3.3 V power to on-chip digital module.
VSS1	30	-	I/O Ground — Provides ground on-chip digital module.
GPIOC6	31	TA2/XB_IN3/CMP_REF/$\overline{SS0}$	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin. TA2 — Quad timer module A channel 2 input/output. XB_IN3 — Crossbar module input 3. CMP_REF — Input 5 of analog comparator A and B and C and D. $\overline{SS0}$ — $\overline{SS0}$ is used in slave mode to indicate to the SPI0 module that the current transfer is to be received. After reset, the default state is GPIOC6.
GPIOC7	32	$\overline{SS0}$/TXD0/XB_IN8	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin. $\overline{SS0}$ — $\overline{SS0}$ is used in slave mode to indicate to the SPI0 module that the current transfer is to be received. TXD0 — SCI0 transmit data output or transmit/receive in single wire operation. XB_IN8 — Crossbar module input 8. After reset, the default state is GPIOC7.
GPIOC8	33	MISO0/RXD0/XB_IN9/XB_OUT6	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin. MISO0 — Master in/slave out. In master mode, this pin serves as the data input. In slave mode, this pin serves as the data output. The MISO0 line of a slave device is placed in the high-impedance state if the slave device is not selected. RXD0 — SCI0 receive data input. XB_IN9 — Crossbar module input 9. XB_OUT6 — Crossbar module output 6. After reset, the default state is GPIOC8.
GPIOC9	34	SCLK0/XB_IN4/TXD0/XB_OUT8	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin. SCLK0 — The SPI0 serial clock. In master mode, this pin serves as an output, clocking slaved listeners. In slave mode, this pin serves as the data clock input.

			XB_IN4 — Crossbar module input 4. TXD0 — SCI0 transmit data output or transmit/receive in single wire operation. XB_OUT8 — Crossbar module output 8. After reset, the default state is GPIOC9.
GPIOC10	35	MOSI0 /XB_IN5/MISO0 /XB_OUT9	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin. MOSI0 — Master out/slave in. In master mode, this pin serves as the data output. In slave mode, this pin serves as the data input. XB_IN5 — Crossbar module input 5. MISO0 — Master in/slave out. In master mode, this pin serves as the data input. In slave mode, this pin serves as the data output. The MISO0 line of a slave device is placed in the high-impedance state if the slave device is not selected. XB_OUT9 — Crossbar module output 9. After reset, the default state is GPIOC10.
GPIOF0	36	XB_IN6/SCLK1	Port F GPIO — This GPIO pin can be individually programmed as an input or output pin. XB_IN6 — Crossbar module input 6. SCLK1 — The SPI1 serial clock. In master mode, this pin serves as an output, clocking slaved listeners. In slave mode, this pin serves as the data clock input. After reset, the default state is GPIOF0.
GPIOC11	37	CAN_TX/SCL0/ TXD1	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin. CANTX — CAN transmit data output. SCL0 — IIC0 serial clock. TXD1 — SCI1 transmit data output or transmit/receive in single wire operation. After reset, the default state is GPIOC11.
GPIOC12	38	CAN_RX/SDA0/ RXD1	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin. CANRX — CAN receive data input. SDA0 — IIC0 serial data line. RXD1 — SCI1 receive data input. After reset, the default state is GPIOC12.
GPIOF2	39	SCL0/XB_OUT 6/MISO1	Port F GPIO — This GPIO pin can be individually programmed as an input or output pin. SCL0 — IIC0 serial clock. XB_OUT6 — Crossbar module output 6.

			MISO1 — Master in/slave out. In master mode, this pin serves as the data input. In slave mode, this pin serves as the data output. The MISO1 line of a slave device is placed in the high-impedance state if the slave device is not selected. After reset, the default state is GPIOF2.
GPIOF3	40	SDA0/XB_OUT7/ MOSI1	Port F GPIO — This GPIO pin can be individually programmed as an input or output pin. SDA0 — IIC0 serial data line. XB_OUT7 — Crossbar module output 7. MOSI1 — Master out/slave in. In master mode, this pin serves as the data output. In slave mode, this pin serves as the data input. After reset, the default state is GPIOF3.
GPIOF4	41	TXD1/XB_OUT8/PWM_0X/PWM_FAULT6	Port F GPIO — This GPIO pin can be individually programmed as an input or output pin. TXD1 — The SCI1 transmit data output or transmit/receive in single wire operation. XB_OUT8 — Crossbar module output 8. PWM_0X — NanoEdge eFlexPWM sub-module 0 output X or input capture X. PWM_FAULT6 — NanoEdge eFlexPWM fault input 6. After reset, the default state is GPIOF4.
GPIOF5	42	RXD1/XB_OUT9/PWM_1X/PWM_FAULT7	Port F GPIO — This GPIO pin can be individually programmed as an input or output pin. RXD1 — The SCI1 receive data input. XB_OUT9 — Crossbar module output 9. PWM_1X — NanoEdge eFlexPWM sub-module 1 output X or input capture X. PWM_FAULT7 — NanoEdge eFlexPWM fault input 7. After reset, the default state is GPIOF5.
VSS2	43	-	I/O Ground — Provides ground to on-chip digital module.
VDD2	44	-	I/O Power — Supplies 3.3 V power to on-chip digital module.
GPIOE0	45	PWM_0B	Port E GPIO — This GPIO pin can be individually programmed as an input or output pin. PWM_0B — NanoEdge eFlexPWM sub-module 0 output B or input capture B. After reset, the default state is GPIOE0.
GPIOE1	46	PWM_0A	Port E GPIO — This GPIO pin can be individually programmed as an input or output pin. PWM_0A — NanoEdge eFlexPWM sub-module 0 output A or input capture A.

			After reset, the default state is GPIOE1.
GPIOE2	47	PWM_1B	Port E GPIO — This GPIO pin can be individually programmed as an input or output pin. PWM_1B — NanoEdge eFlexPWM sub-module 1 output B or input capture B. After reset, the default state is GPIOE2.
GPIOE3	48	PWM_1A	Port E GPIO — This GPIO pin can be individually programmed as an input or output pin. PWM_1A — NanoEdge eFlexPWM sub-module 1 output A or input capture A. After reset, the default state is GPIOE3.
GPIOC13	49	TA3/XB_IN6/ $\overline{\text{EWM\_OUT}}$	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin. TA3 — Quad timer module A channel 3 input/output. XB_IN6 — Crossbar module input 6. $\overline{\text{EWM\_OUT}}$ — External watchdog monitor output. After reset, the default state is GPIOC13.
GPIOF1	50	CLKO1/XB_IN7/ CMPD_O	Port F GPIO — This GPIO pin can be individually programmed as an input or output pin. CLKO1 — This is a buffered clock output 1; the clock source is selected by clock out select (CLKOSEL) bits in the clock output select register (CLKOUT) of the SIM. XB_IN7 — Crossbar module input 7. CMPD_O — Analog comparator D output. After reset, the default state is GPIOF1.
GPIOE4	51	PWM_2B/XB_IN2	Port E GPIO — This GPIO pin can be individually programmed as an input or output pin. PWM_2B — NanoEdge eFlexPWM sub-module 2 output B or input capture B. XB_IN2 — Crossbar module input 2. After reset, the default state is GPIOE4.
GPIOE5	52	PWM_2A/XB_IN3	Port E GPIO — This GPIO pin can be individually programmed as an input or output pin. PWM_2A — NanoEdge eFlexPWM sub-module 2 output A or input capture A. XB_IN3 — Crossbar module input 3. After reset, the default state is GPIOE5.
GPIOE6	53	PWM_3B/XB_IN4	Port E GPIO — This GPIO pin can be individually programmed as an input or output pin. PWM_3B — NanoEdge eFlexPWM sub-module 3 output B or input capture B.

			XB_IN4 — Crossbar module input 4. After reset, the default state is GPIOE6.
GPIOE7	54	PWM_3A/XB_IN5	Port E GPIO — This GPIO pin can be individually programmed as an input or output pin. PWM_3A — NanoEdge eFlexPWM sub-module 3 output A or input capture A. XB_IN5 — Crossbar module input 5. After reset, the default state is GPIOE7.
GPIOC14	55	SDA0/XB_OUT4/PWM_FAULT4	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin. SDA0 — IIC0 serial data line. XB_OUT4 — Crossbar module output 4. PWM_FAULT4 — NanoEdge eFlexPWM fault input 4. After reset, the default state is GPIOC14.
GPIOC15	56	SCL0/XB_OUT5/PWM_FAULT5	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin. SCL0 — IIC0 serial clock. XB_OUT5 — Crossbar module output 5. PWM_FAULT5 — NanoEdge eFlexPWM fault input 5. After reset, the default state is GPIOC15.
VCAP2	57	-	Connect a 2.2 µF or greater bypass capacitor between this pin and VSS to stabilize the core voltage regulator output required for proper device operation.
GPIOF6	58	PWM_3X/XB_IN2	Port F GPIO — This GPIO pin can be individually programmed as an input or output pin. PWM_3X — NanoEdge eFlexPWM sub-module 3 output X or input capture X. XB_IN2 — Crossbar module input 2. After reset, the default state is GPIOF6.
GPIOF7	59	CMPC_O/$\overline{SS1}$/XB_IN3	Port F GPIO — This GPIO pin can be individually programmed as an input or output pin. CMPC_O— Analog comparator C output. $\overline{SS1}$ — $\overline{SS1}$ is used in slave mode to indicate to the SPI1 module that the current transfer is to be received. XB_IN3 — Crossbar module input 3. After reset, the default state is GPIOF7.
VDD3	60	-	I/O Power — Supplies 3.3 V power to on-chip digital module.
VSS3	61	-	I/O Ground — Provides ground to on-chip digital module.
TDO	62	GPIOD1	Test Data Output — This tri-stateable output pin provides a serial output data stream from the JTAG/EOnCE port. It is driven in the shift-IR and

			shift-DR controller states, and changes on the falling edge of TCK. Port D GPIO — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is TDO.
TMS	63	GPIOD3	Test Mode Select Input — This input pin is used to sequence the JTAG TAP controller's state machine. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor. Port D GPIO — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is TMS. NOTE: Always tie the TMS pin to VDD through a 2.2 kΩ resistor if need to keep on-board debug capability. Otherwise, directly tie to VDD.
TDI	64	GPIOD0	Test Data Input — This input pin provides a serial input data stream to the JTAG/EOnCE port. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor. Port D GPIO — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is TDI.

4.5 Ordering Information

Table 1 lists the pertinent information needed to place an order. Consult a Freescale Semiconductor sales office to determine availability and to order this device.

Table 10 MWCT1101CLH Ordering Information

Device	Supply Voltage	Package Type	Pin Count	Ambient Temp.	Order Number
MWCT1101CLH	3.0 to 3.6V	LQFP	64	-40 to +85℃	MWCT1101CLH

4.6 Package Outline Drawing

To find a package drawing, go to freescale.com and perform a keyword search for the drawing's document number of 98ASS23234W.

5 Software Library

WCT1101 can not only run the core wireless charging function, but also allow user to add user application functions. Freescale provides two Wireless Charging Transmitter (WCT) software libraries (WCT1000 TX library and WCT1200 TX library) for different solutions design on WCT1101. In these libraries, low level drivers of HAL (Hardware Abstract Layer), callback functions for library access are open to user. For the software API and library details, see *WCT1000 TX Library User Guide.pdf* (WCT1000LIBUG).

5.1 Memory Map

WCT1101 has large on-chip Flash memory and RAM for user design. Besides for wireless charging transmitter library code, the user can develop private functions and link it to library through predefined APIs.

Table 11. WCT1101 Memory Footprint

Part	Memory	Total Size	Library Size	FreeMASTER Size	EEPROM Size	Free Size
WCT1101	Flash	64 Kbytes	19 Kbytes	1.5 Kbytes	1 Kbytes	42.5 Kbytes
	RAM	8 Kbytes	5.8 Kbytes	0.1 Kbytes	0 Kbytes	2.1 Kbytes

5.2 Software Library and API Description

For more and detailed information about WCT software library and API definition, see *WCT1000 TX Library User Guide.pdf* (WCT1000LIBUG).

6 Design Considerations

6.1 Electrical Design Considerations

Use the following list of considerations to assure correct operation of the device and system:

- The minimum bypass requirement is to place 0.01 - 0.1 µ F capacitors positioned as near as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the VDD/VSS pairs, including VDDA/VSSA. Ceramic and tantalum capacitors tend to provide better tolerances.
- Bypass the VDD and VSS with approximately 10 µ F, plus the number of 0.1 µ F ceramic capacitors.
- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the VDD and VSS circuits.
- Take special care to minimize noise levels on the VDDA, and VSSA pins.
- Using separate power planes for VDD and VDDA and separate ground planes for VSS and VSSA are recommended. Connect the separate analog and digital power and ground planes as near as possible to power supply outputs. If an analog circuit and digital circuit are powered by the same power supply, you should connect a small inductor or ferrite bead in serial with VDDA trace.
- If desired, connect an external RC circuit to the RESET pin. The resistor value should be in the range of 4.7 kΩ – 10 kΩ; and the capacitor value should be in the range of 0.1 µ F – 4.7 µ F.

- Add a 2.2 kΩ external pull-up on the TMS pin of the JTAG port to keep device in a restate during normal operation if JTAG converter is not present.
- During reset and after reset but before I/O initialization, all I/O pins are at input mode with internal weak pull-up.
- To eliminate PCB trace impedance effect, each ADC input should have a no less than 33pF/10 Ω RC filter.
- To assure chip reliable operation, please reserve enough margin for chip electrical design. The figure 6 shows the relationship between electrical ratings and electrical operating characteristics for correct chip operation.

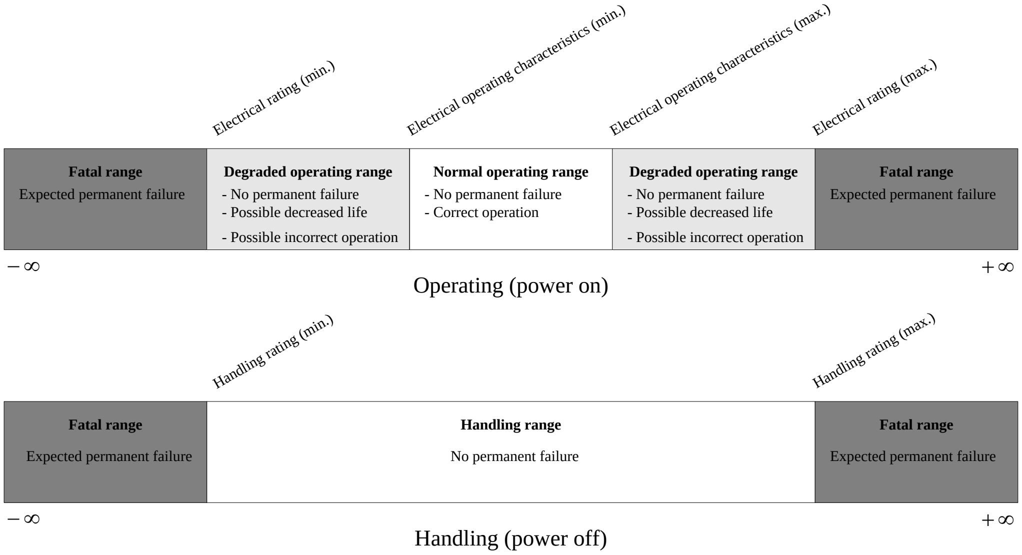


Figure 6. Relationship between Ratings and Operating Characteristics

6.2 PCB Layout Considerations

- Provide a low-impedance path from the board power supply to each VDD pin on the device and from the board ground to each VSS pin.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip VDD and VSS pins are as short as possible.
- PCB trace lengths should be minimal for high-frequency signals.
- Physically separate analog components from noisy digital components by ground planes. Do not place an analog trace in parallel with digital traces. Place an analog ground trace around an analog signal trace to isolate it from digital traces.
- The decoupling capacitors of 0.1 μ F must be placed on the VDD pins as close as possible, and place those ceramic capacitors on the same PCB layer with WCT1101 device. VIA is not recommend between the VDD pins and decoupling capacitors.

- The WCT1101 bottom EP pad should be soldered to the ground plane, which will make the system more stable, and VIA matrix method can be used to connect this pad to the ground plane.
- As the Wireless Charging system functions as a switching-mode power supply, the power components layout is very important for the whole system power transfer efficiency and EMI performance. The power routing loop should be small and short as can as possible, especially for the resonant network, the traces of this circuit should be short and wide, and the current loop should be optimized smaller for the MOSFETs, resonant capacitor and primary coil. Another important thing is that the control circuit and power circuit should be separated.

6.3 Thermal Design Considerations

WCT1101 power consumption is not so critical, so there is not additional part needed for power dissipation. However, the power inverter needs the additional PCB Cu copper to dissipate the heat, so good thermal package MOSFET is recommended to select, such as DFN package, and for the resonant capacitor, COG material, and 1206 or 1210 package are recommended to meet the thermal requirement. And the worst thermal case is on the inverter, so the user should make some special actions to dissipate the heat for good transmitter system thermal performance.

7 References and Links

7.1 References

- *WCT1000 A11 Reference Design System User Guide* (WCT1000SYSUG)
- *WCT1000 TX Library User Guide* (WCT1000LIBUG)
- *WCT Runtime Debug User Guide* (WCT1XXXRTDUG)
- *WCT1000 A11 Reference Design Calibration User Guide* (WCT1000CALUG)
- *WPC Low Power Wireless Transfer System Description* Part 1: Interface Definition Version 1.1

7.2 Useful Links

- freescale.com
- freescale.com\wirelesscharging
- www.wirelesspowerconsortium.com

How to Reach Us:

Home Page:
freescale.com

Web Support:
freescale.com/support

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