Revision History

256K x16 bit Low Power CMOS Static RAM

Revision No	History	Date	Remark
1.0	Initial Issue	January 2011	Preliminary
2.0	updated DC operating character table	May 2016	

256K X 16 BIT LOW POWER CMOS SRAM

FEATURES

- Process Technology : 0.18µm Full CMOS
- Organization : 256K x 16 bit
- Power Supply Voltage : 2.7V ~ 3.6V
- Low Data Retention Voltage : 1.5V(Min.)
- Three state output and TTL Compatible
- Package Type : VFBGA-48, 44-TSOP2

GENERAL DESCRIPTION

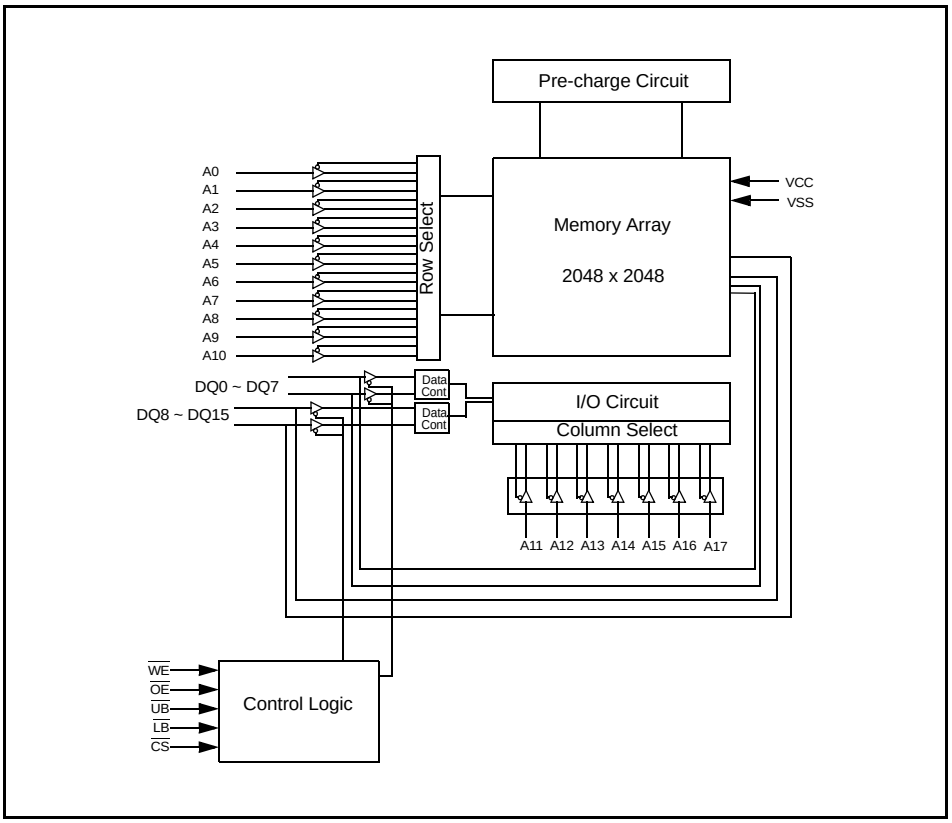
The AS6C4016A families are fabricated by Alliance Memory advanced full CMOS process technology. The families support industrial temperature range and Chip Scale Package for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (I_{SB1}, Typ.)	Operating (I_{SB1}.Max.)	
AS6C4016A	Industrial (-40 ~ 85°C)	2.7 ~ 3.6V	45 ns	0.25 µA[2)]	3 mA	KGD VFBGA-48 44-TSOP2

2. Typical values are measured at Vcc=3.3V, TA=25°C and not 100% tested.

FUNCTIONAL BLOCK DIAGRAM

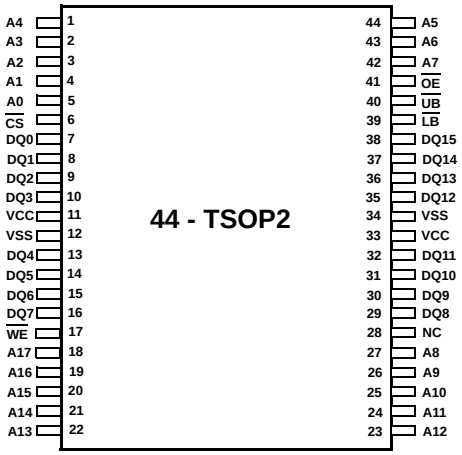


PIN CONFIGURATIONS

VFBGA-48 : Top view(ball down)

	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A0	A1	A2	NC
B	DQ8	$\overline{UB}$	A3	A4	$\overline{CS}$	DQ0
C	DQ9	DQ10	A5	A6	DQ1	DQ2
D	VSS	DQ11	A17	A7	DQ3	VCC
E	VCC	DQ12	NC	A16	DQ4	VSS
F	DQ14	DQ13	A14	A15	DQ5	DQ6
G	DQ15	NC	A12	A13	$\overline{WE}$	DQ7
H	NC	A8	A9	A10	A11	NC

44 - TSOP2 : Top view



PIN DESCRIPTION

Name	Function	Name	Function
$\overline{CS}$	Chip Select input	VCC	Power Supply
$\overline{OE}$	Output Enable input	VSS	Ground
$\overline{WE}$	Write Enable input	$\overline{UB}$	Upper Byte (DQ8~DQ15)
A0~A17	Address inputs	$\overline{LB}$	Lower Byte (DQ0~DQ7)
DQ0~DQ15	Data inputs/outputs	NC	No Connection

ABSOLUTE MAXIMUM RATINGS[1)]

Parameter	Symbol	Ratings	Unit
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-0.2 to 4.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-0.2 to 4.0	V
Power Dissipation	P_D	1.0	W
Operating Temperature	T_A	-40 to 85	^oC

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	DQ0~7	DQ8~15	Mode	Power
H	X	X	X	X	High-Z	High-Z	Deselected	Stand by
X	X	X	H	H	High-Z	High-Z	Deselected	Stand by
L	H	H	L	X	High-Z	High-Z	Output Disabled	Active
L	H	H	X	L	High-Z	High-Z	Output Disabled	Active
L	L	H	L	H	Data Out	High-Z	Lower Byte Read	Active
L	L	H	H	L	High-Z	Data Out	Upper Byte Read	Active
L	L	H	L	L	Data Out	Data Out	Word Read	Active
L	X	L	L	H	Data In	High-Z	Lower Byte Write	Active
L	X	L	H	L	High-Z	Data In	Upper Byte Write	Active
L	X	L	L	L	Data In	Data In	Word Write	Active

NOTE : X means don't care. (Must be low or high state)

RECOMMENDED DC OPERATING CONDITIONS [1)]

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	2.7	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input high voltage	V_{IH}	2.2	-	V_{CC} + 0.2[2)]	V
Input low voltage	V_{IL}	-0.2[3)]	-	0.6	V

1. TA= -40 to 85°C, otherwise specified
2. Overshoot: VCC +2.0 V in case of pulse width ≤ 20ns
3. Undershoot: -2.0 V in case of pulse width ≤ 20ns
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE[1)] (f =1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	8	pF
Input/Ouput capacitance	C_{IO}	V_{IO}=0V	-	10	pF

1. Capacitance is sampled, not 100% tested.

DC AND OPERATING CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Input leakage current	I_{LI}	V_{IN}=V_{SS} to V_{CC}		-1	-	1	μA
Output leakage current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} or $\overline{LB}$=$\overline{UB}$=V_{IH} V_{IO}=V_{SS} to V_{CC}		-1	-	1	μA
Operating power supply	I_{CC}	I_{IO}=0mA, $\overline{CS}$=V_{IL}, V_{IN}=V_{IH} or V_{IL}		-	-	3	mA
Average operating current	I_{CC1}	Cycle time=1μs, 100% duty, I_{IO}=0mA, $\overline{CS}$≤0.2V, $\overline{LB}$≤0.2V or/and $\overline{UB}$≤0.2V, V_{IN}≤0.2V or V_{IN}≥V_{CC}-0.2V		-	-	3	mA
	I_{CC2}	Cycle time = Min, I_{IO}=0mA, 100% duty, $\overline{CS}$=V_{IL}, $\overline{LB}$=V_{IL} or/and $\overline{UB}$=V_{IL} , V_{IN}=V_{IL} or V_{IH}	45ns	-	-	35	mA
Output low voltage	V_{OL}	I_{OL} = 2.1mA		-	-	0.4	V
Output high voltage	V_{OH}	I_{OH} = -1.0mA		2.4	-	-	V
Standby Current (TTL)	I_{SB}	$\overline{CS}$=V_{IH}, Other inputs=V_{IH} or V_{IL}		-	-	0.3	mA
Standby Current (CMOS)	I_{SB1}	$\overline{CS}$≥V_{CC}-0.2V, Other inputs = 0~V_{CC} (Typ. condition : V_{CC}=3.3V @ 25°C) (Max. condition : V_{CC}=3.6V @ 85°C)	LL LF	-	0.25 [1)]	4	μA

1. Typical values are measured at Vcc=3.3V, T_A=25°C and not 100% tested.

AC OPERATING CONDITIONS

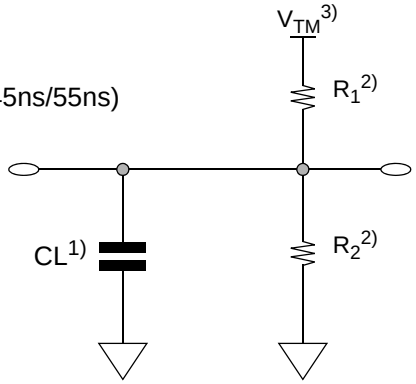
Test Conditions (Test Load and Test Input/Output Reference)

Input Pulse Level : 0.4 to 2.2V

Input Rise and Fall Time : 5ns

Input and Output reference Voltage : 1.5V

Output Load (See right) : $CL^{1)}$ = 100pF+ 1 TTL(70ns), $CL^{1)}$ = 30pF + 1 TTL(45ns/55ns)



1. Inc ding scope and Jig capacitance
2. $_1$=3070Ω, R_2=3150Ω
3. $_{TM}$=2.8V
4. L = 5pF + 1 TTL (measurement with tLZ, tOLZ, tHZ, tOHZ, tWHZ)

READ CYCLE (V_{cc} =2.7 to 3.6V, Gnd = 0V, T_A = -40°C to +85°C)

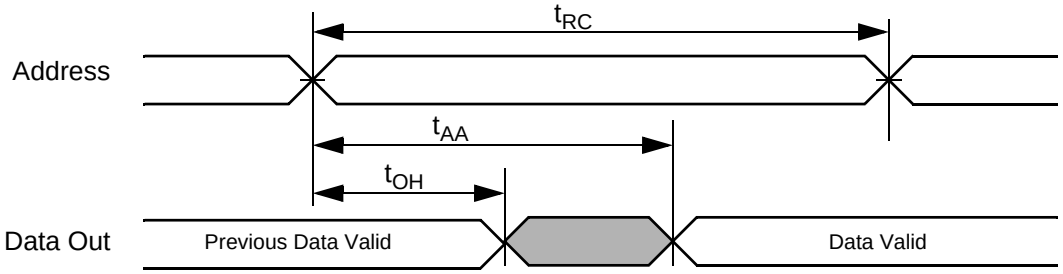
Parameter	Symbol	45ns		Unit
		Min	Max	
Read cycle time	t_{RC}	45	-	ns
Address access time	t_{AA}	-	45	ns
Chip select to output	t_{CO}	-	45	ns
Output enable to valid output	t_{OE}	-	20	ns
$\overline{UB}$, $\overline{LB}$ acess time	t_{BA}		20	ns
Chip select to low-Z output	t_{LZ}	10	-	ns
$\overline{UB}$, $\overline{LB}$ enable to low-Z output	t_{BLZ}	5	-	ns
Output enable to low-Z output	t_{OLZ}	5	-	ns
Chip disable to high-Z output	t_{HZ}	0	20	ns
$\overline{UB}$, $\overline{LB}$ disable to high-Z output	t_{BHZ}	0	20	ns
Output disable to high-Z output	t_{OHZ}	0	20	ns
Output hold from address change	t_{OH}	10	-	ns

WRITE CYCLE (V_{cc} =2.7 to 3.6V, Gnd = 0V, T_A = -40°C to +85°C)

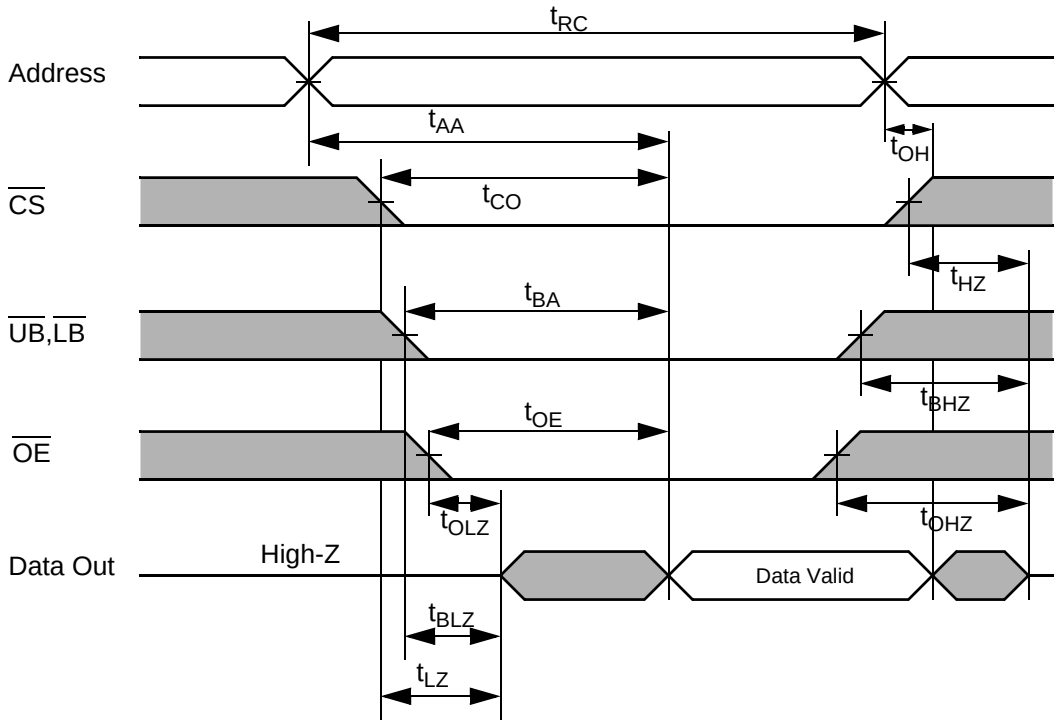
Parameter	Symbol	45ns		Unit
		Min	Max	
Write cycle time	t_{WC}	45	-	ns
Chip select to end of write	t_{CW}	35	-	ns
Address setup time	t_{AS}	0	-	ns
Address valid to end of write	t_{AW}	35	-	ns
$\overline{UB}$, $\overline{LB}$ valid to end of write	t_{BW}	35	-	ns
Write pulse width	t_{WP}	35	-	ns
Write recovery time	t_{WR}	0	-	ns
Write to ouput high-Z	t_{WHZ}	0	20	ns
Data to write time overlap	t_{DW}	25	25	ns
Data hold from write time	t_{DH}	0	-	ns
End write to output low-Z	t_{OW}	5	-	ns

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH}, $\overline{UB}$ or/and $\overline{LB}$=V_{IL})



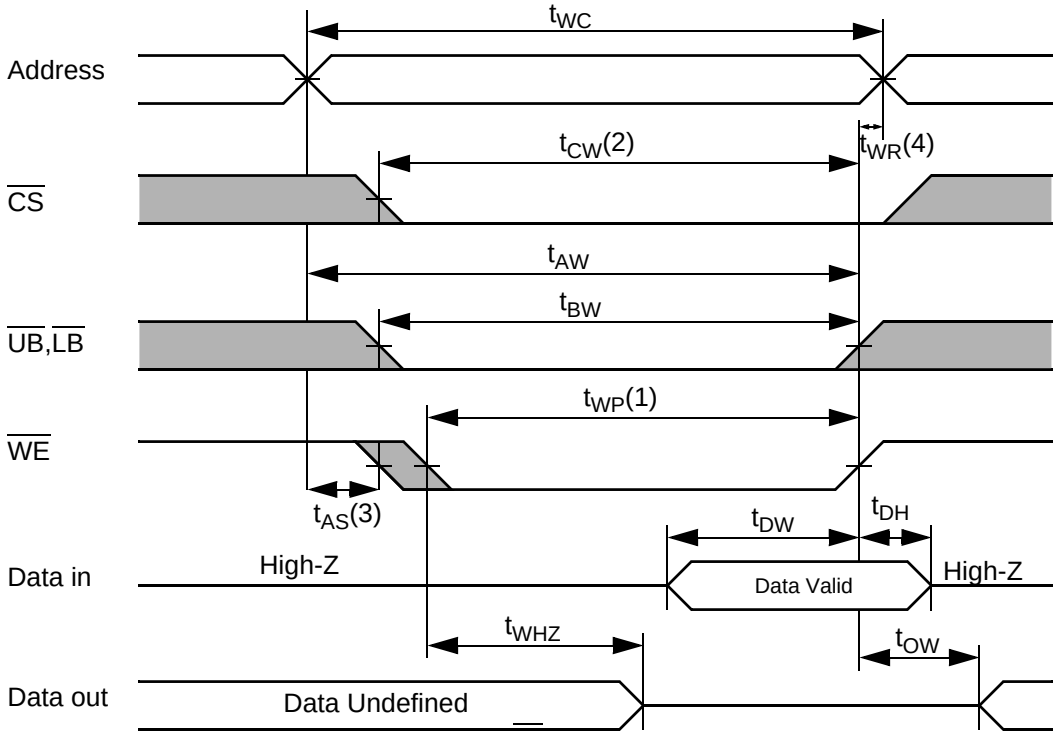
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$ = V_{IH})



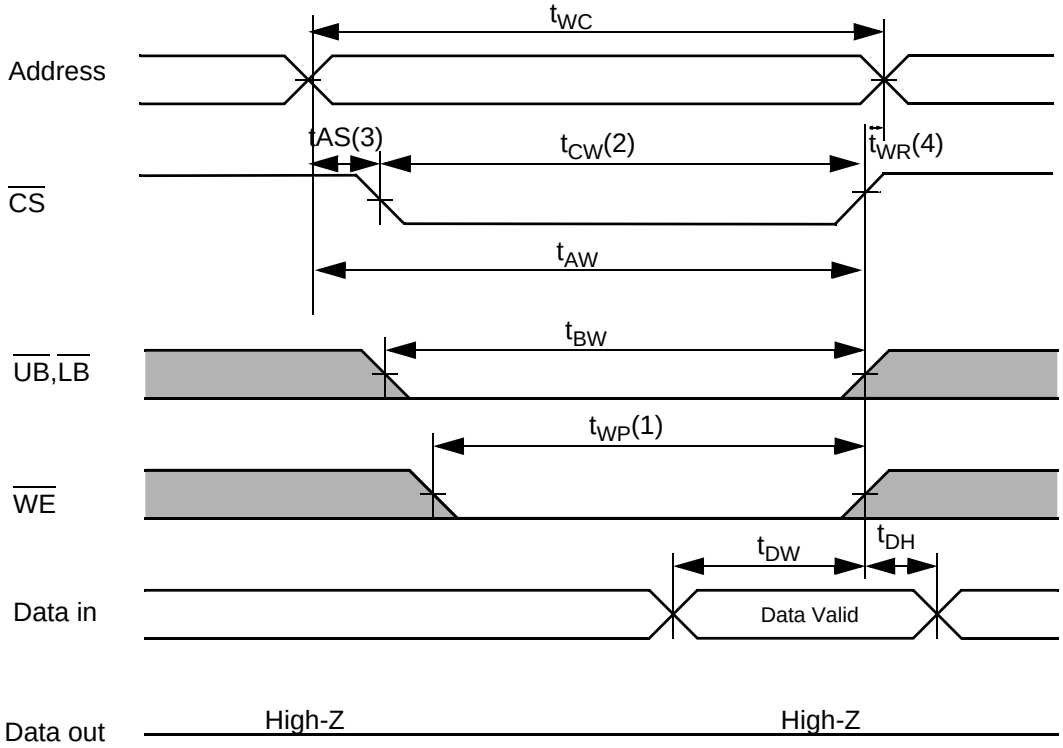
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device interconnection.

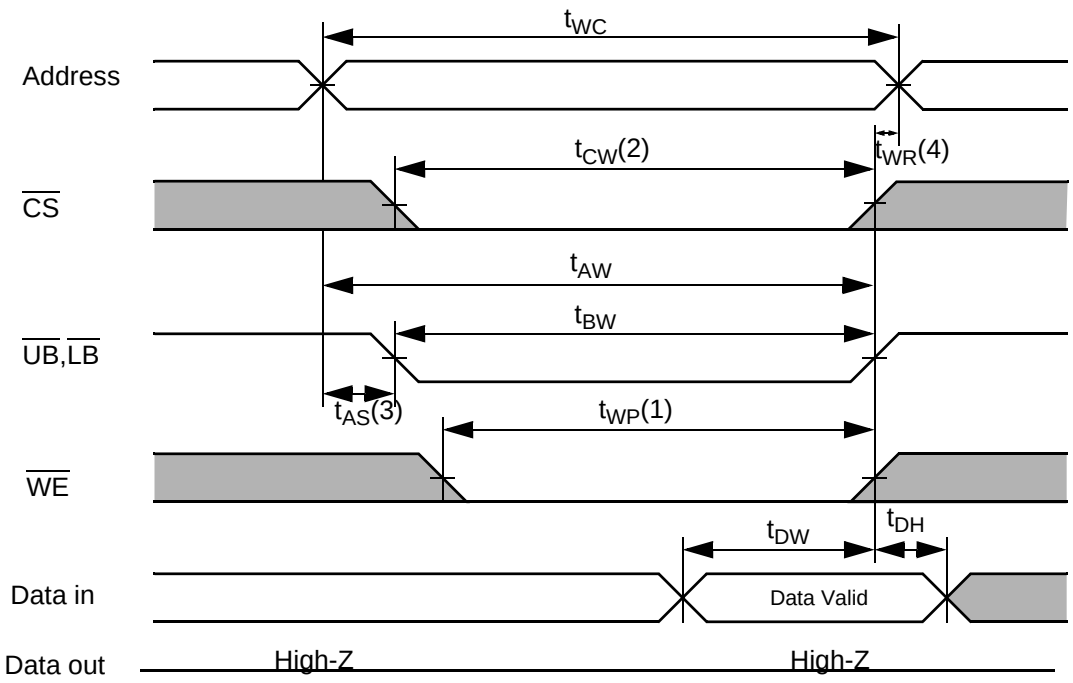
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) (CS Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{UB}$, $\overline{LB}$ Controlled)



NOTES (WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of low $\overline{CS}$ and low $\overline{WE}$. A write begins when $\overline{CS}$ goes low and $\overline{WE}$ goes low with asserting $\overline{UB}$ or $\overline{LB}$ for single byte operation or simultaneously asserting $\overline{UB}$ and $\overline{LB}$ for double byte operation. A write ends at the earliest transition when $\overline{CS}$ goes high and $\overline{WE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS}$ going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end or write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.

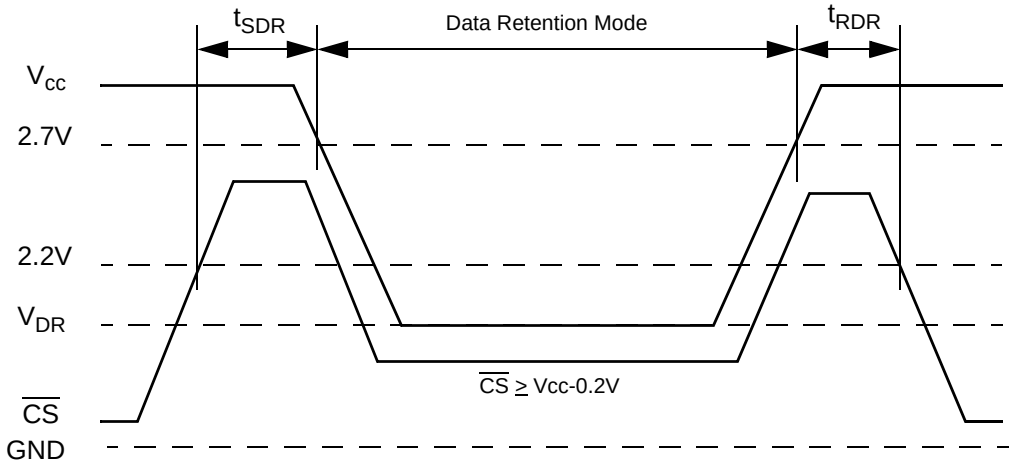
DATA RETENTION CHARACTERISTICS

Parameter	Symbol	Test Condition	Min	Typ[2)]	Max	Unit
V_{CC} for Data Retention	V_{DR}	I_{SB1} Test Condition (Chip Disabled) [1)]	1.5	-	3.6	V
Data Retention Current	I_{DR}	V_{CC}=1.5V, I_{SB1} Test Condition (Chip Disabled) [1)]	-	0.5	-	µA
Chip Deselect to Data Retention Time	t_{SDR}	See data retention wave form	0	-	-	ns
Operation Recovery Time	t_{RDR}		t_{RC}	-	-	

NOTES

1. See the I_{SB1} measurement condition of datasheet page 5.
2. Typical values are measured at T_A=25°C and not 100% tested.

DATA RETENTION WAVE FORM

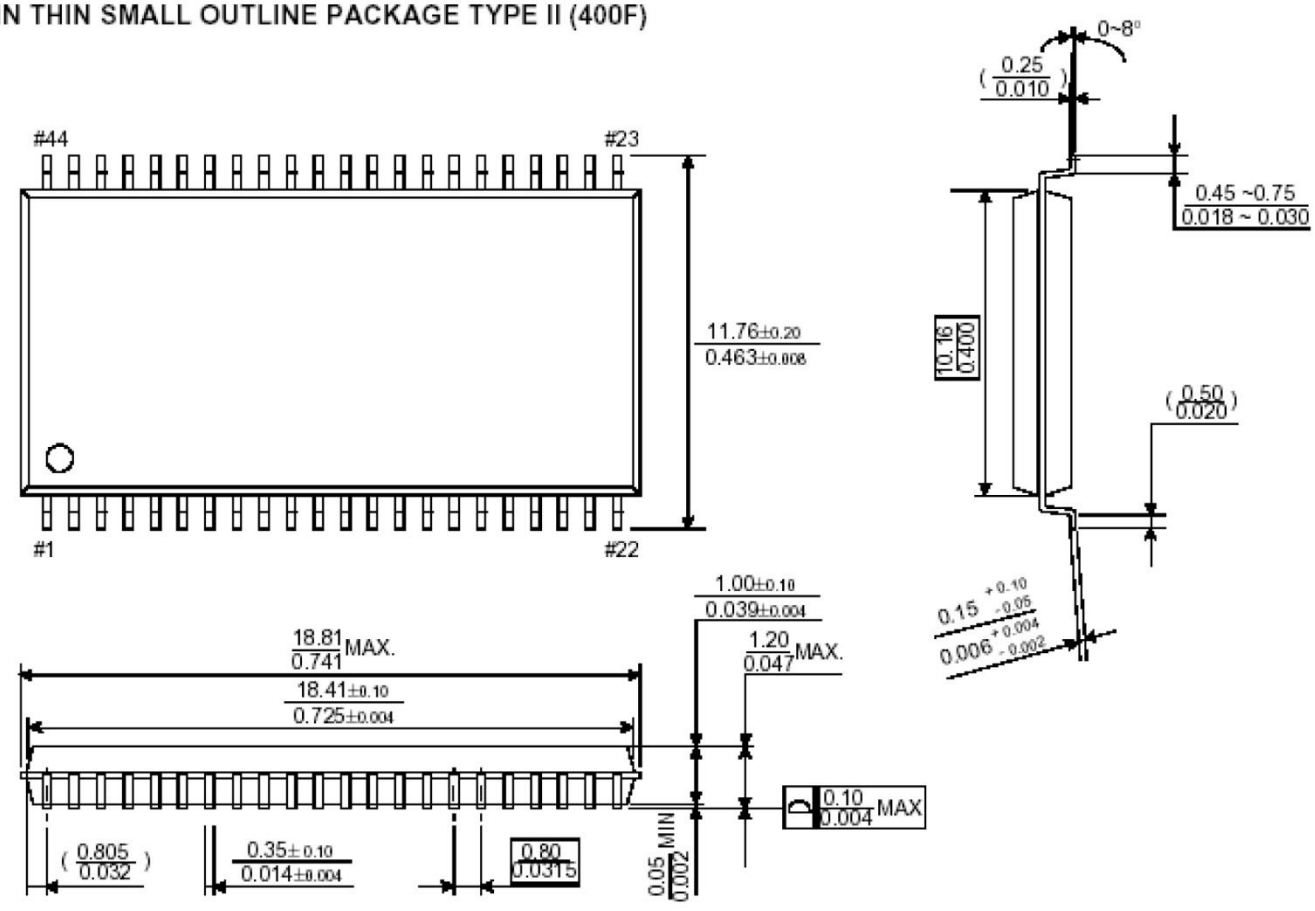


PACKAGE DIMENSION

44 - TSOP2 (0.8mm pin pitch)

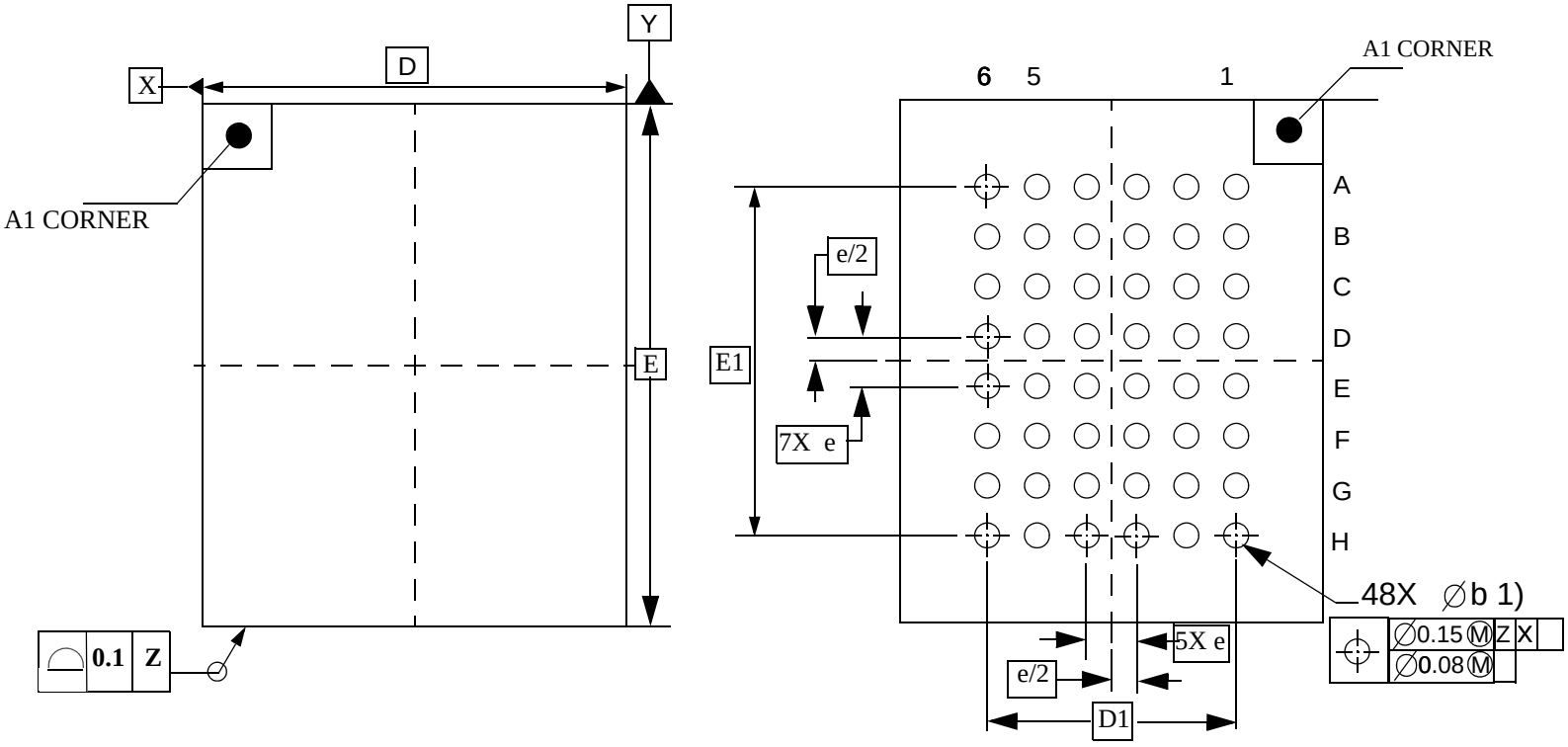
Unit : millimeters / inches

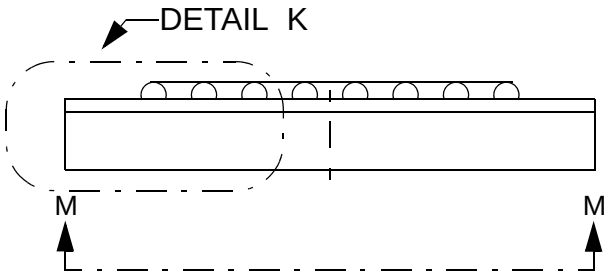
44 PIN THIN SMALL OUTLINE PACKAGE TYPE II (400F)

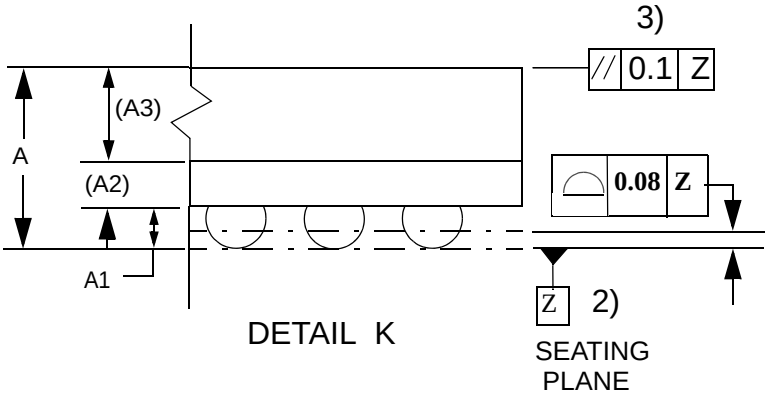


Unit: millimeters

VFBGA 48 BALLS (6X7X1 0.75mm ball pitch)







	Min.	NOR.	Max.
A	---		1
A1	0.22		0.32
A2		0.21 REF	
A3		0.45 REF	
b	0.32	5.25	0.42
D		6 BSC	
E		7 BSC	
e		0.75 BSC	
D1		0.35 BSC	
E1		5.25 BSC	

NOTES.

1). DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
2). DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3). PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

Ordering Information

Alliance	Organization	VCC Range	Package	Operating Temp	Speed ns
AS6C4016A-45ZIN	256K x 16	2.7 ~ 3.6V	44-TSOP2	Industrial (-40 ~ 85°C)	45
AS6C4016A-45BIN	256K x 16	2.7 ~ 3.6V	VFBGA-48	Industrial (-40 ~ 85°C)	45

Part Numbering System

AS6C	4016A	-45	X	X	N
low power SRAM prefix	Device Number 40 = 4M 16 = x16	Access Time	Package Option 44pin TSOP II 48ball TFBGA	Temperature Range I = Industrial (-40 to + 85°C)	N = Lead Free RoHS compliant part