MOSFET

Metal Oxide Semiconductor Field Effect Transistor

OptiMOS^{TM}

OptiMOS^{TM} Power-MOSFET, 25 V
BSB012NE2LXI

Data Sheet

Rev. 2.1
Final

Power Management & Multimarket

1   Description

Features

- Optimized SyncFET for high performance Buck converter
- Integrated monolithic Schottky like diode
- Low profile (<0.7 mm)
- 100% avalanche tested
- 100% R_G Tested
- Double-sided cooling
- Compatible with DirectFET® package MX footprint and outline [1]
- Qualified according to JEDEC[2] for target applications
- Pb-free lead plating; RoHS compliant

CanPAK M-size
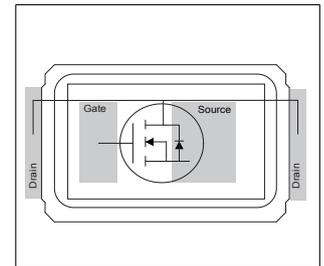
Table 1   Key Performance Parameters

Parameter	Value	Unit
V_{DS}	25	V
$R_{DS(on),max}$	1.2	mΩ
I_D	170	A
Q_{oss}	39	nC
$Q_g(0V..10V)$	62	nC

Type / Ordering Code	Package	Marking	Related Links
BSB012NE2LXI	MG-WDSON-2	05E2	-

[1] CanPAK^{TM} uses DirectFET ® technology licensed from International Rectifier Corporation. DirectFET® is a registered trademark of International Rectifier Corporation.
[2] J-STD20 and JESD22

Table of Contents

2 Maximum ratings

at T_j = 25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	- - -	- - -	170 107 37	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=100 °C V_{GS}=10 V, T_A=25 °C, R_{thJA}=45 K/W[1]
Pulsed drain current[2]	$I_{D,pulse}$	-	-	400	A	T_C=25 °C
Avalanche current, single pulse[3]	I_{AS}	-	-	40	A	T_C=25 °C
Avalanche energy, single pulse	E_{AS}	-	-	130	mJ	I_D=40 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	- -	- -	57 2.8	W	T_C=25 °C T_A=25 °C, R_{thJA}=45 K/W
Operating and storage temperature	T_j, T_{stg}	-40	-	150	°C	IEC climatic category; DIN IEC 68-1: 40/150/56

3 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	1.0	-	K/W	-
Thermal resistance, junction - case, top	R_{thJC}	-	-	2.2	K/W	-
Device on PCB, 6 cm² cooling area[1]	R_{thJA}	-	-	45	K/W	-

[1] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm2 (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.
[2] See figure 3 for more detailed information
[3] See figure 13 for more detailed information

4 Electrical characteristics

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	25	-	-	V	V_{GS}=0 V, I_D=10 mA
Breakdown voltage temperature coefficient	$dV_{(BR)DSS}/dT_j$	-	15	-	mV/K	I_D=10 mA, referenced to 25 °C
Gate threshold voltage	$V_{GS(th)}$	1.2	-	2	V	V_{DS}=V_{GS}, I_D=250 µA
Zero gate voltage drain current, T_j=25 °C	I_{DSS}	-	25	500	µA	V_{DS}=20 V, V_{GS}=0 V
Zero gate voltage drain current, T_j=125 °C	I_{DSS}	-	4	-	mA	V_{DS}=20 V, V_{GS}=0 V
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	- -	1.3 1.0	1.6 1.2	mΩ	V_{GS}=4.5 V, I_D=30 A V_{GS}=10 V, I_D=30 A
Gate resistance	R_G	0.3	0.6	1.2	Ω	-
Transconductance	g_{fs}	95	190	-	S	$|V_{DS}|$>2$|I_D|R_{DS(on)max}$, I_D=30 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	4400	5900	pF	V_{GS}=0 V, V_{DS}=12 V, f=1 MHz
Output capacitance	C_{oss}	-	1900	2600	pF	V_{GS}=0 V, V_{DS}=12 V, f=1 MHz
Reverse transfer capacitance	C_{rss}	-	190	-	pF	V_{GS}=0 V, V_{DS}=12 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	5.4	-	ns	V_{DD}=12 V, V_{GS}=10 V, I_D=30 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r	-	6.4	-	ns	V_{DD}=12 V, V_{GS}=10 V, I_D=30 A, $R_{G,ext}$=1.6 Ω
Turn-off delay time	$t_{d(off)}$	-	32	-	ns	V_{DD}=12 V, V_{GS}=10 V, I_D=30 A, $R_{G,ext}$=1.6 Ω
Fall time	t_f	-	4.8	-	ns	V_{DD}=12 V, V_{GS}=10 V, I_D=30 A, $R_{G,ext}$=1.6 Ω

Table 6 Gate charge characteristics[1]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	10.5	14	nC	V_{DD}=12 V, I_D=30 A, V_{GS}=0 to 4.5 V
Gate charge at threshold	$Q_{g(th)}$	-	7.1	-	nC	V_{DD}=12 V, I_D=30 A, V_{GS}=0 to 4.5 V
Gate to drain charge	Q_{gd}	-	7.3	11	nC	V_{DD}=12 V, I_D=30 A, V_{GS}=0 to 4.5 V
Switching charge	Q_{sw}	-	10.7	-	nC	V_{DD}=12 V, I_D=30 A, V_{GS}=0 to 4.5 V
Gate charge total	Q_g	-	30	40	nC	V_{DD}=12 V, I_D=30 A, V_{GS}=0 to 4.5 V
Gate plateau voltage	$V_{plateau}$	-	2.4	-	V	V_{DD}=12 V, I_D=30 A, V_{GS}=0 to 4.5 V
Gate charge total	Q_g	-	62	82	nC	V_{DD}=12 V, I_D=30 A, V_{GS}=0 to 10 V
Gate charge total, sync. FET	$Q_{g(sync)}$	-	26	-	nC	V_{DS}=0.1 V, V_{GS}=0 to 4.5 V
Output charge	Q_{oss}	-	39	52	nC	V_{DD}=12 V, V_{GS}=0 V

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	57	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	227	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	0.56	-	V	V_{GS}=0 V, I_F=12 A, T_j=25 °C
Reverse recovery charge	Q_{rr}	-	5	-	nC	V_R=15 V, I_F=I_S, di_F/dt=400 A/μs

[1] See ″Gate charge waveforms″ for parameter definition

5   Electrical characteristics diagrams

Diagram 1: Power dissipation

P_{tot}=f(T_C)

Diagram 2: Drain current

I_D=f(T_C); V_{GS}≥10 V

Diagram 3: Safe operating area

I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p
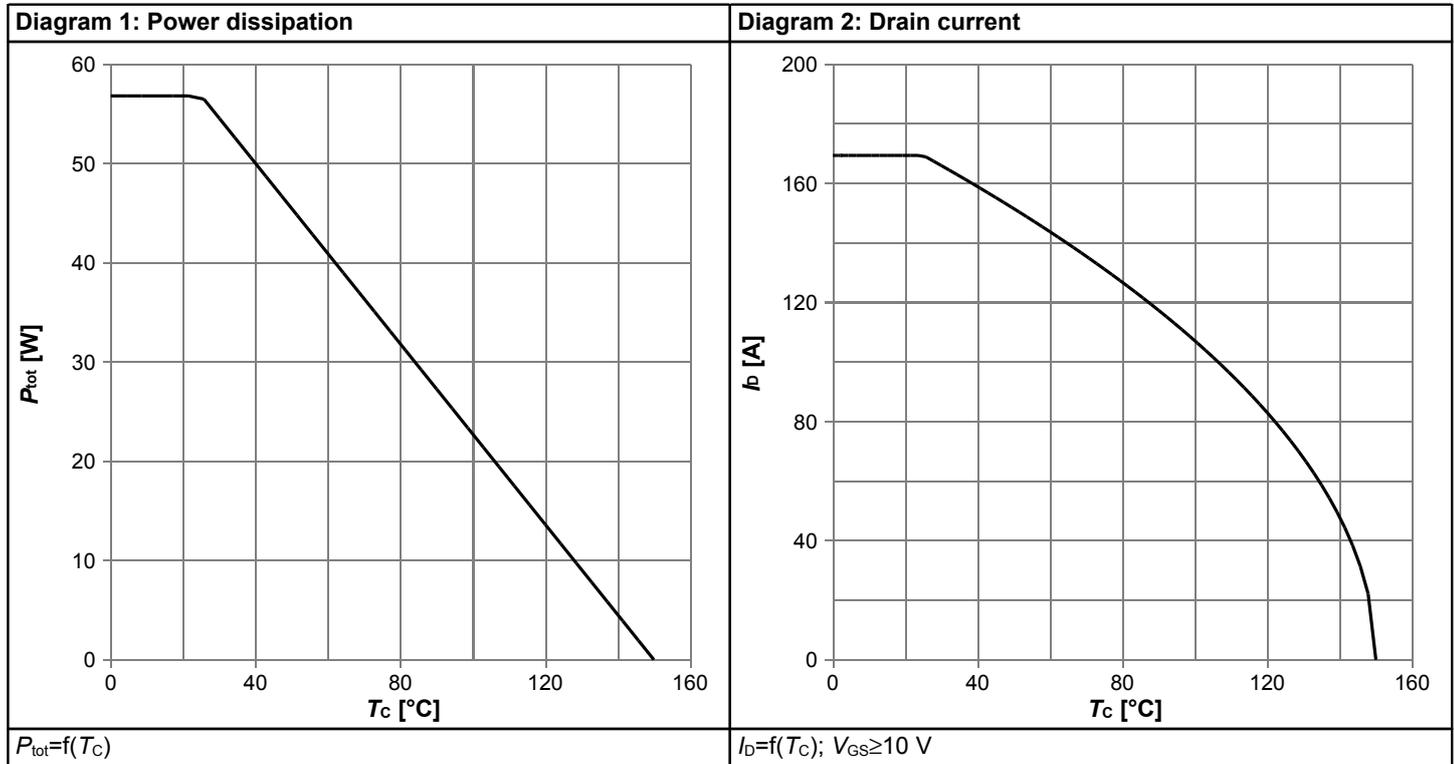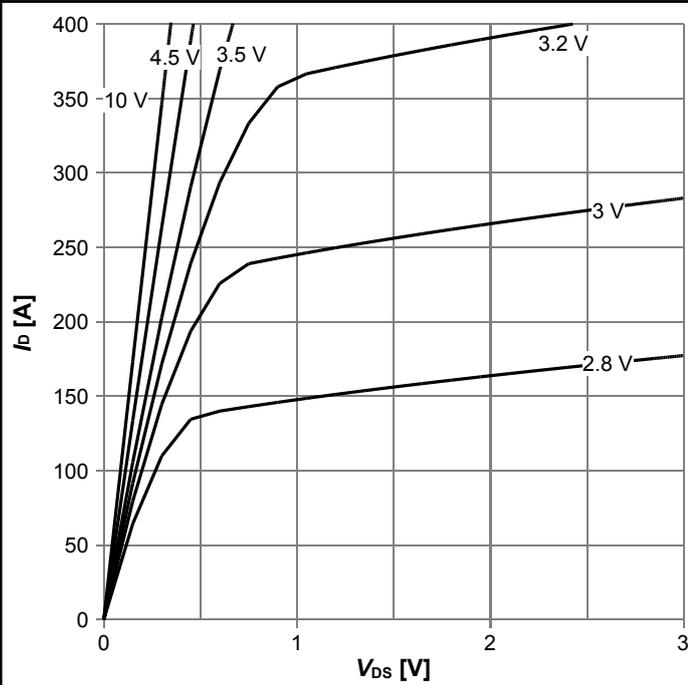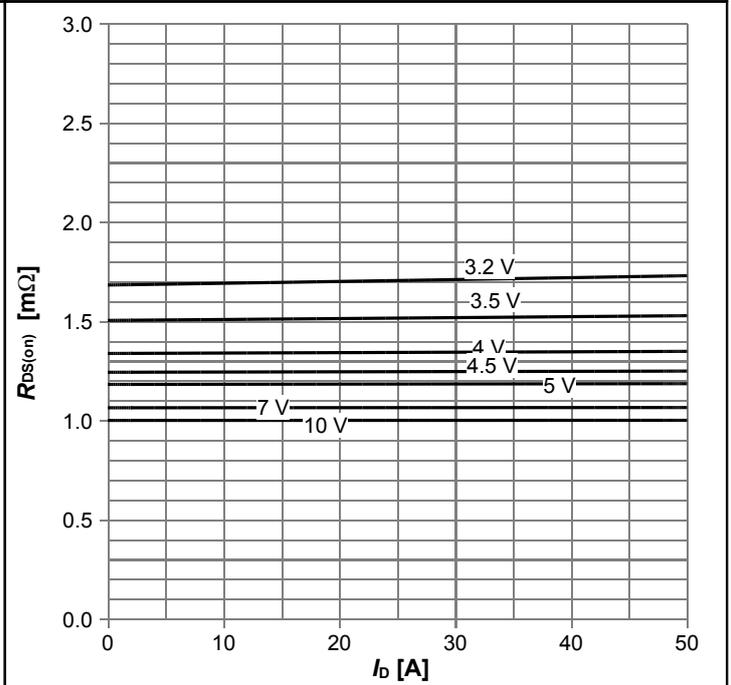
Diagram 4: Max. transient thermal impedance
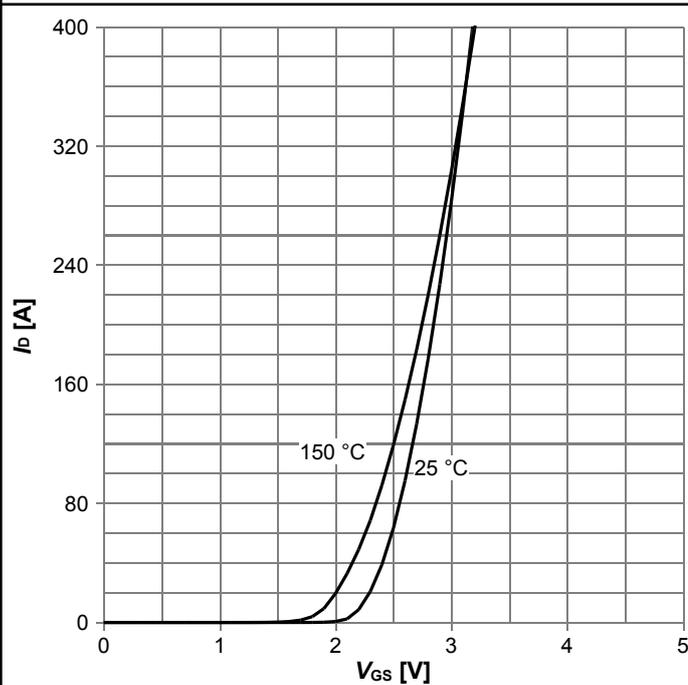

Z_{thJC}=f(t_p); parameter: D=t_p/T
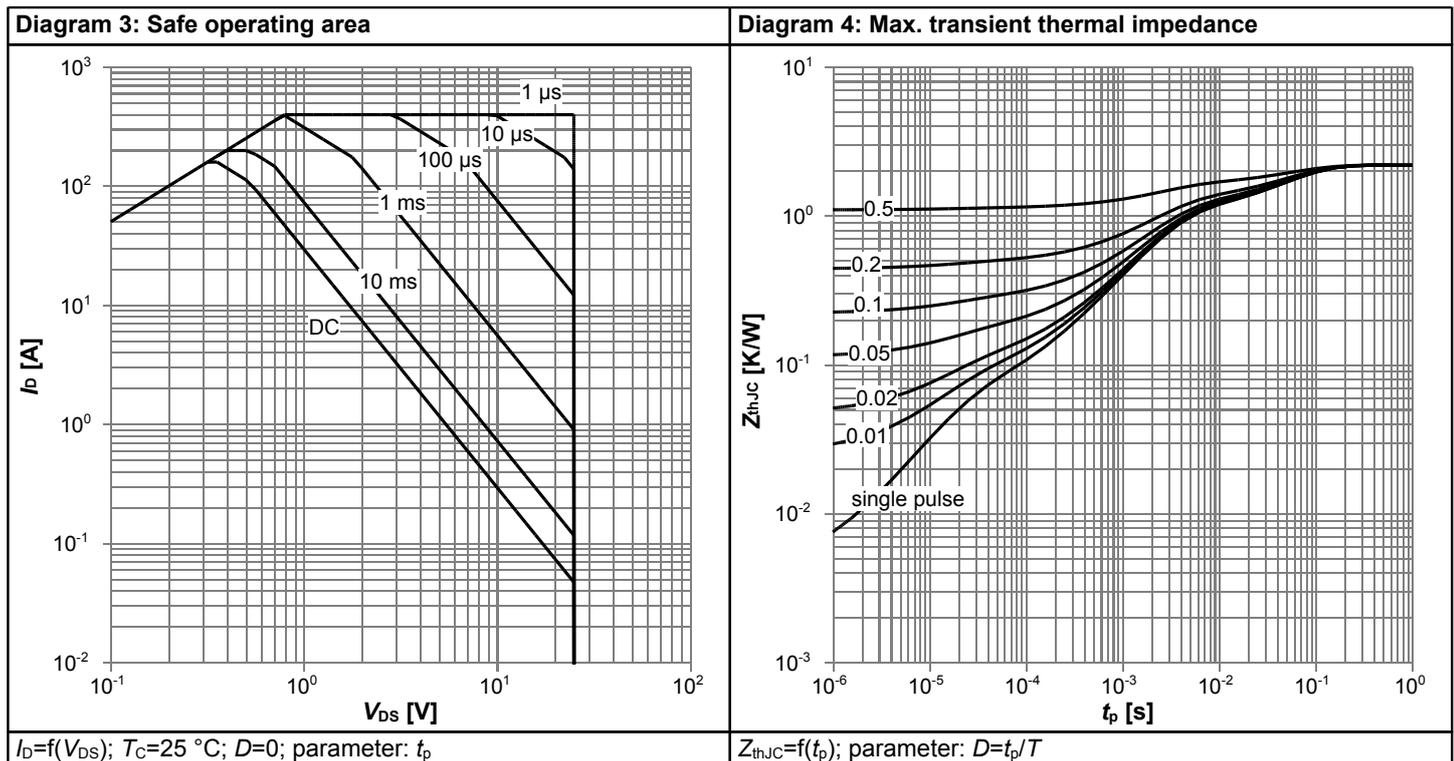
Diagram 5: Typ. output characteristics

I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance

$R_{DS(on)}$=f(I_D); T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics

I_D=f(V_{GS}); |V_{DS}|>2|I_D|$R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. forward transconductance
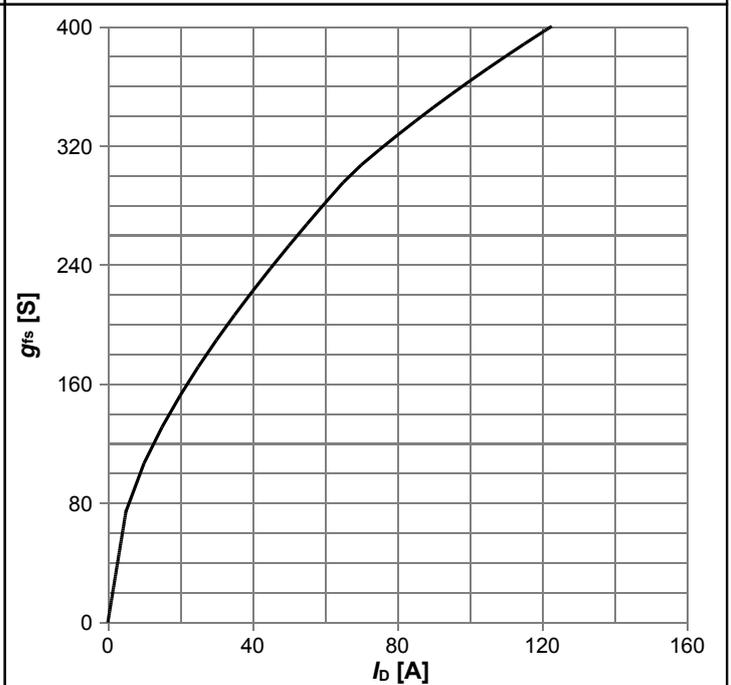
g_{fs}=f(I_D); T_j=25 °C

Diagram 9: Drain-source on-state resistance
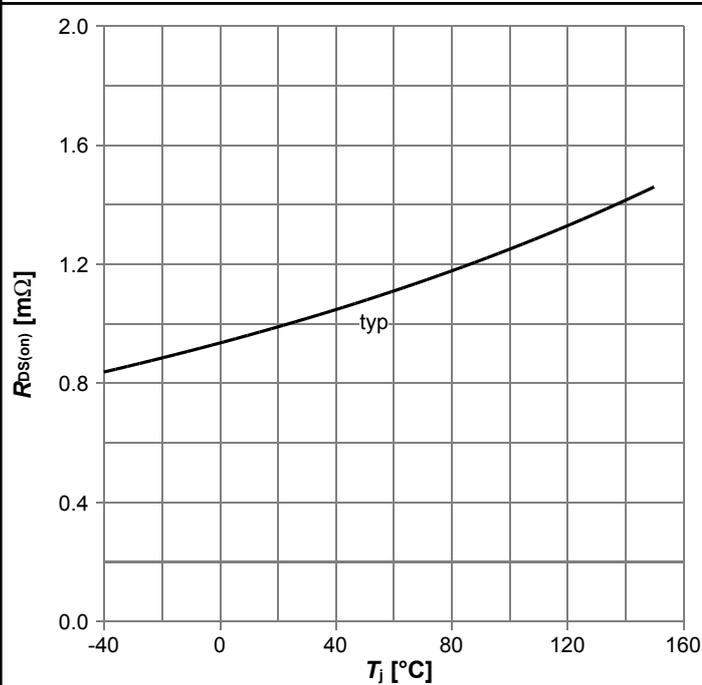
$R_{DS(on)}$=f(T_j); I_D=30 A; V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage
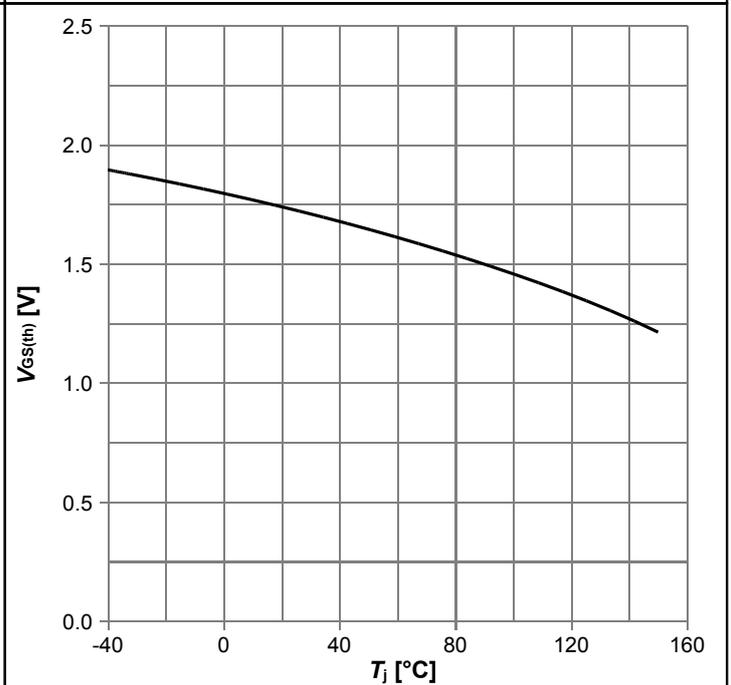
$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}; I_D=10 mA

Diagram 11: Typ. capacitances
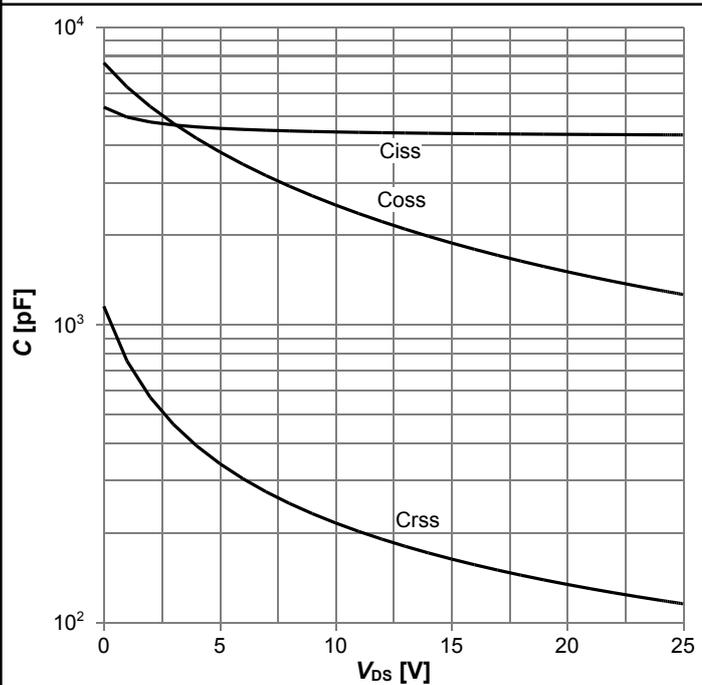
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode
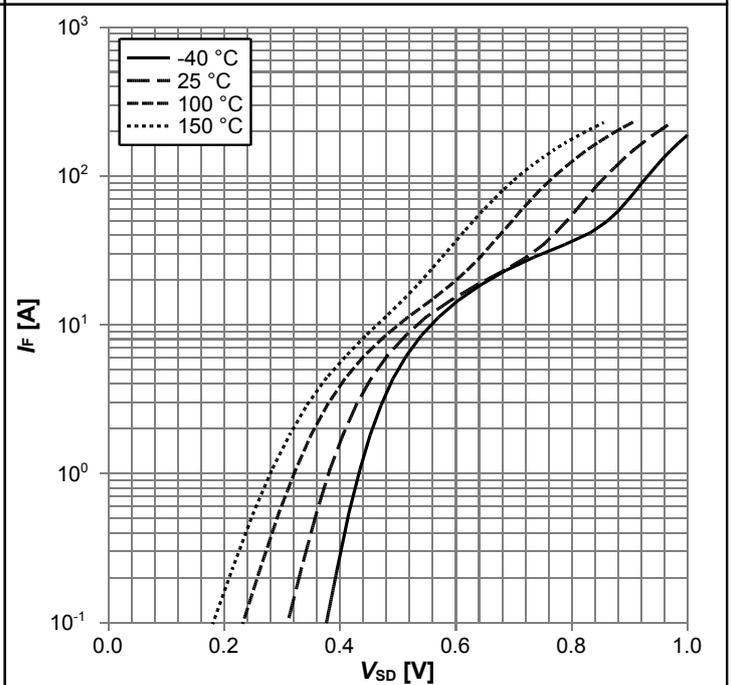
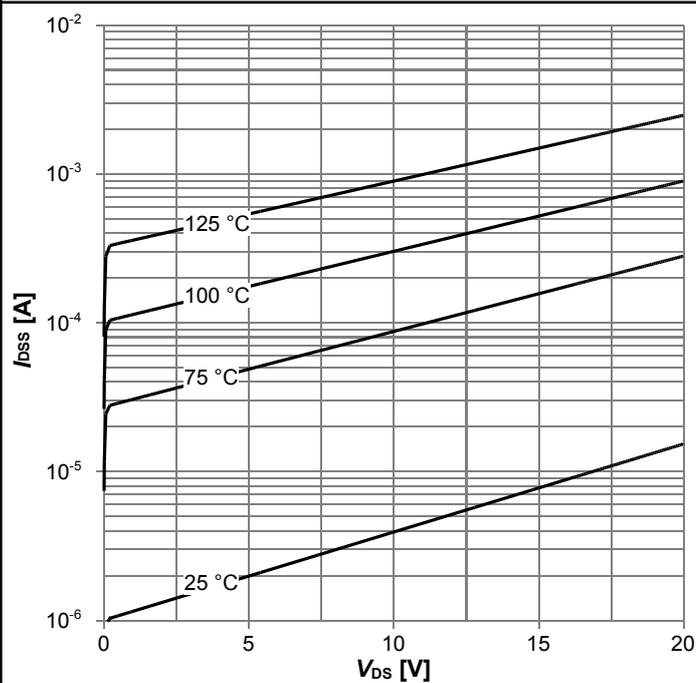I_F=f(V_{SD}); parameter: T_j

Diagram 13: Avalanche characteristics
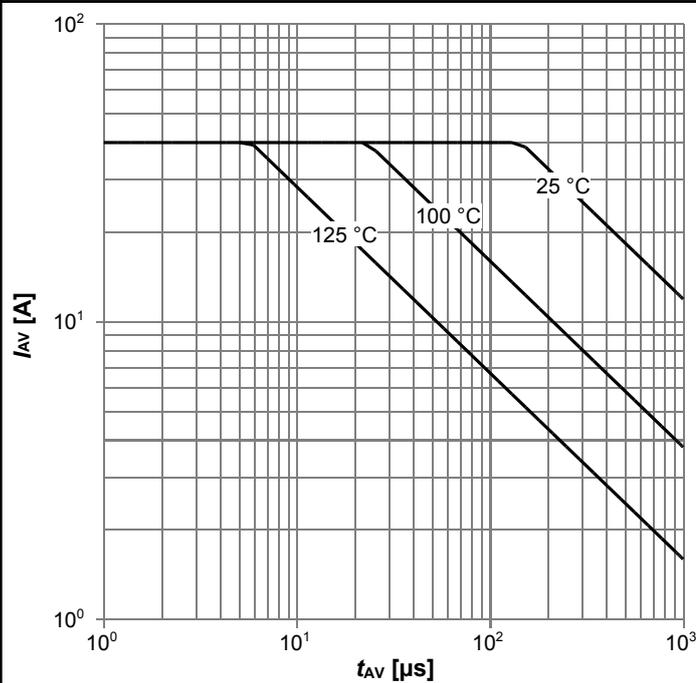
$I_{AS}=f(t_{AV})$; $R_{GS}=25\ \Omega$; parameter: $T_{j(start)}$

Diagram 14: Typ. gate charge
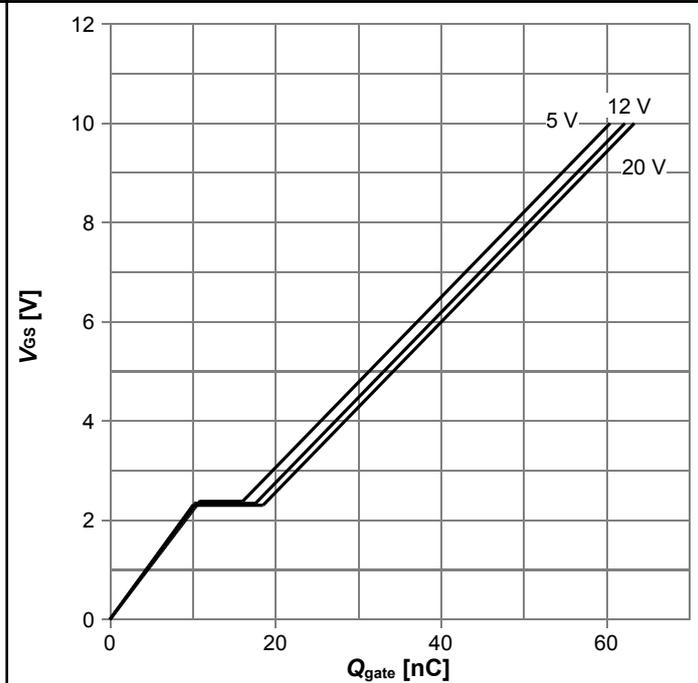
$V_{GS}=f(Q_{gate})$; $I_D=30$ A pulsed; parameter: V_{DD}

Diagram 15: Typ. Drain-source leakage current

$I_{DSS}=f(V_{DS})$; $V_{GS}=0$ V; parameter: T_j
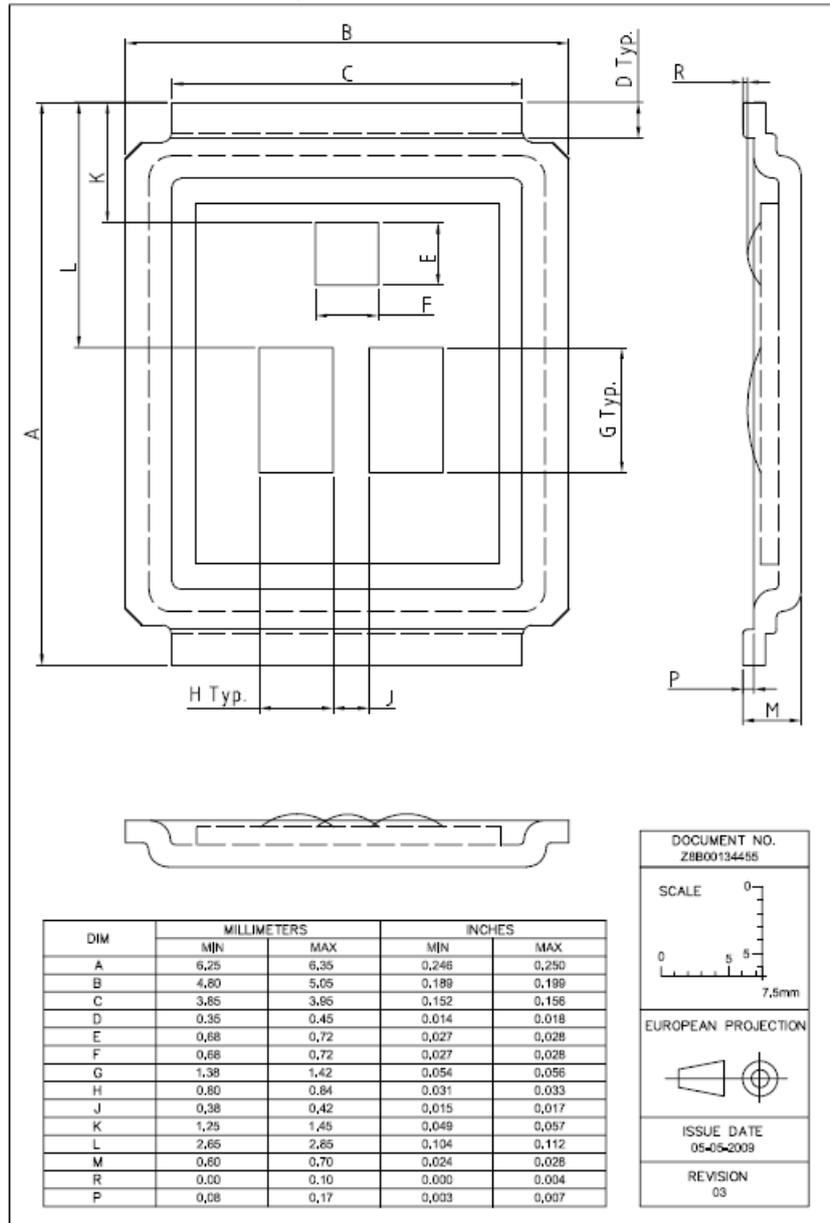
Gate charge waveforms

6 Package Outlines

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6,25	6,35	0,246	0,250
B	4,80	5,05	0,189	0,199
C	3,85	3,95	0,152	0,156
D	0,35	0,45	0,014	0,018
E	0,68	0,72	0,027	0,028
F	0,68	0,72	0,027	0,028
G	1,38	1,42	0,054	0,056
H	0,80	0,84	0,031	0,033
J	0,38	0,42	0,015	0,017
K	1,25	1,45	0,049	0,057
L	2,65	2,85	0,104	0,112
M	0,60	0,70	0,024	0,028
R	0,00	0,10	0,000	0,004
P	0,08	0,17	0,003	0,007

DOCUMENT NO.
Z8B00134455

SCALE

7,5mm

EUROPEAN PROJECTION

ISSUE DATE
05-05-2009

REVISION
03
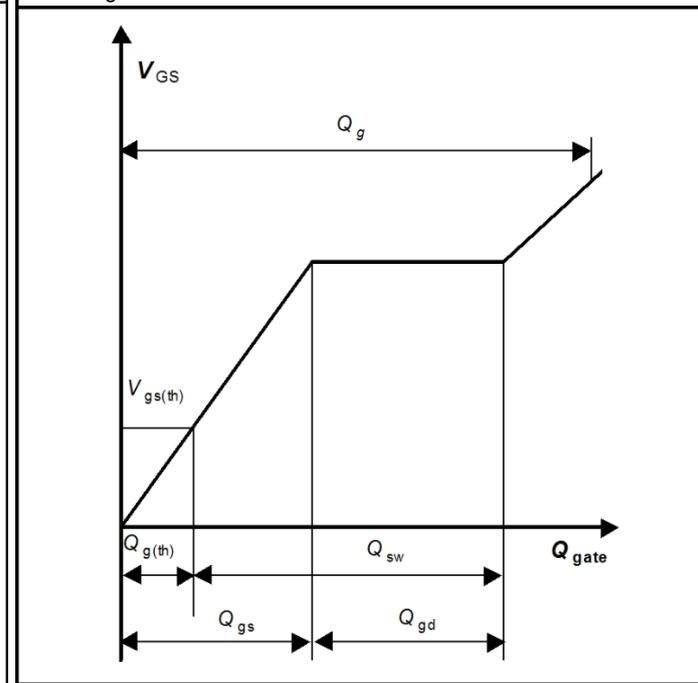
Figure 1   Outline MG-WDSON-2, dimensions in mm/inches
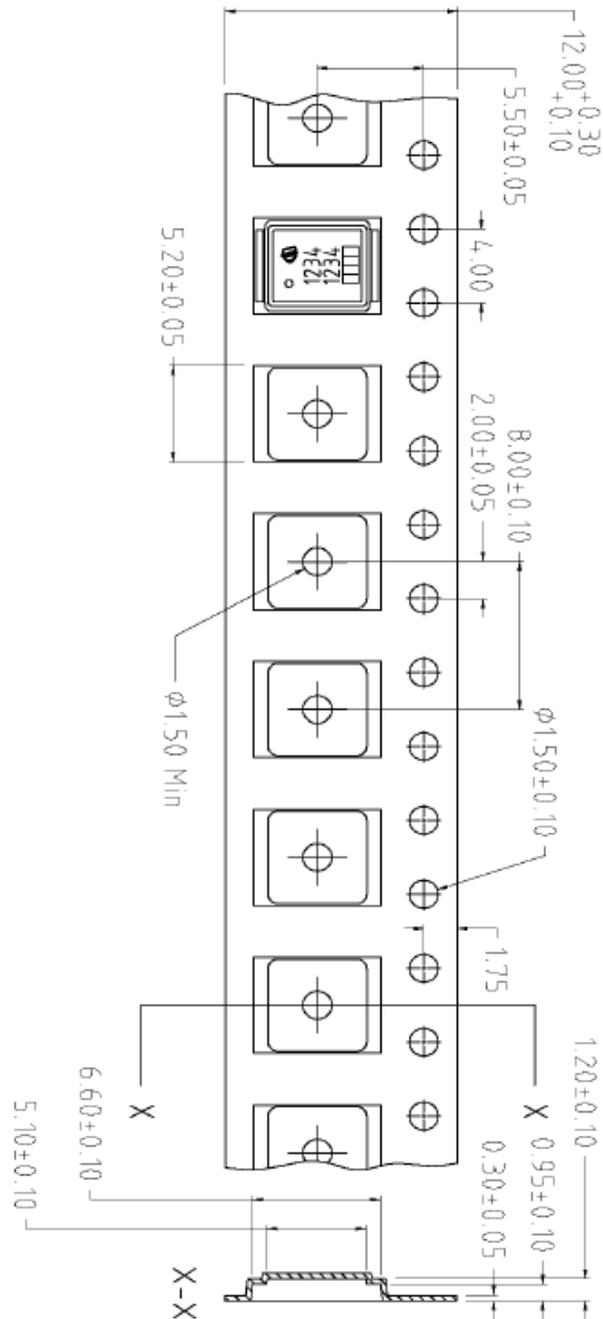
Figure 2   Outline Tape CanPAK MX, dimensions in mm

SMD

copper   solder mask   stencil apertures
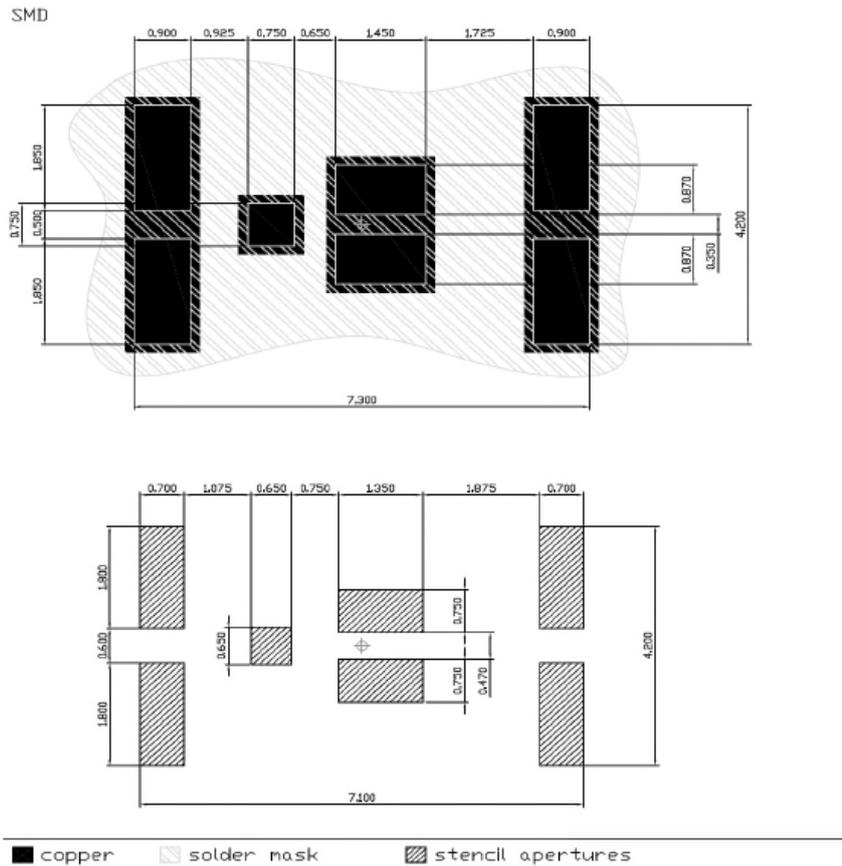
Dimensions in mm

Recommended stencil thickness 150 μm

Marking Layout

Gate Marking

G = Green Product / RoHS compliant
H = Halogen-free + RoHS compliant

Manufacturer
Type code
Lot code
Date code (YYWW)

1234
1234
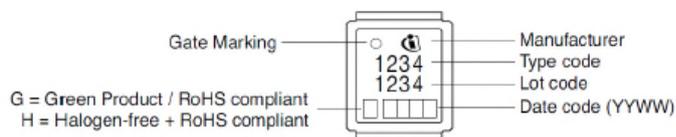
Figure 3   Outline Boardpads and apertures CanPAK MX, dimensions in mm

Revision History

BSB012NE2LXI

Revision: 2015-09-09, Rev. 2.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2015-01-20	Release of final version
2.1	2015-09-09	Rev. 2.0

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