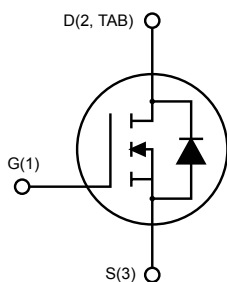
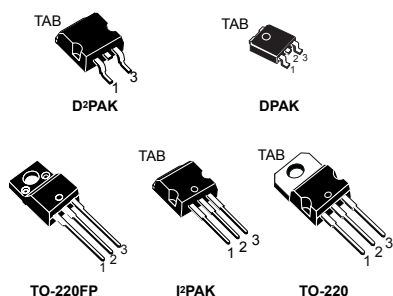


N-channel 100 V, 6.8 mΩ typ., 80 A STripFET™ F7 Power MOSFETs
in D²PAK, DPAK, TO-220FP, I²PAK and TO-220 packages



AM01475v1_noZen

Features

Order codes	V _{DS}	R _{DS(on)} max.	I _D	Package
STB100N10F7	100 V	8.0 mΩ	80 A	D ² PAK
STD100N10F7			80 A	DPAK
STF100N10F7			45 A	TO-220FP
STI100N10F7			80 A	I ² PAK
STP100N10F7			80 A	TO-220

- Among the lowest R_{DS(on)} on the market
- Excellent FoM (figure of merit)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

These N-channel Power MOSFETs utilize STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Product status links

[STB100N10F7](#)
[STD100N10F7](#)
[STF100N10F7](#)
[STI100N10F7](#)
[STP100N10F7](#)

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value			Unit
		DPAK	TO-220FP	TO-220 D ² PAK I ² PAK	
V _{DS}	Drain-source voltage	100			V
V _{GS}	Gate-source voltage	±20			V
I _D	Drain current (continuous) at T _C = 25 °C	80	45 ⁽¹⁾	80	A
	Drain current (continuous) at T _C = 100 °C	62	32 ⁽¹⁾	70	A
I _{DM} ⁽²⁾	Drain current (pulsed)	320	180	320	A
P _{TOT} ⁽¹⁾	Total dissipation at T _C = 25 °C	120	30	150	W
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heatsink (t = 1 s, T _C = 25 °C)		2.5		kV
T _J	Operating junction temperature	-55 to 175			°C
T _{stg}	Storage temperature range				°C

1. This value is limited by package.
2. Pulse width is limited by safe operating area.

Table 2. Thermal resistance

Symbol	Parameter	Value				Unit
		D ² PAK	DPAK	TO-220FP	TO-220 I ² PAK	
R _{thj-case}	Thermal resistance junction-case	1	1.25	5	1	°C/W
R _{thj-amb}	Thermal resistance junction-ambient			62.5		°C/W
R _{thj-pcb} ⁽¹⁾	Thermal resistance junction-pcb	30	50			°C/W

1. When mounted on an 1-inch² FR-4 board, 2oz CU, t < 10 s.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
E _{AS}	Single pulse avalanche energy (T _J = 25 °C, L = 3.5 mH, I _{AS} = 15 A, V _{DD} = 50 V, V _{GS} = 10 V)	400	mJ

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On-/off-states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 250 µA, V _{GS} = 0 V	100			V
I _{DSS}	Zero gate voltage drain current	V _{DS} = 100 V, V _{GS} = 0 V			1	µA
		V _{DS} = 100 V, V _{GS} = 0 V, T _C = 125 °C ⁽¹⁾			100	µA
I _{GSS}	Gate-body leakage current	V _{GS} = 20 V, V _{DS} = 0 V			100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 µA	2.5		4.5	V
R _{DS(on)}	Static drain-source on-resistance	For D²PAK, DPAK, I²PAK and TO-220: V _{GS} = 10 V, I _D = 40 A For TO-220FP: V _{GS} = 10 V, I _D = 22.5 A		6.8	8.0	mΩ

1. Defined by design, not subject to production test.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 50 V, f = 1 MHz, V _{GS} = 0 V	-	4369	-	pF
C _{oss}	Output capacitance		-	823	-	pF
C _{rss}	Reverse transfer capacitance		-	36	-	pF
Q _g	Total gate charge	V _{DD} = 50 V, I _D = 80 A,	-	61	-	nC
Q _{gs}	Gate-source charge	V _{GS} = 0 to 10 V	-	26	-	nC
Q _{gd}	Gate-drain charge	(see Figure 17. Test circuit for gate charge behavior)	-	13	-	nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 50 V, I _D = 40 A, R _G = 4.7 Ω, V _{GS} = 10 V	-	27	-	ns
t _r	Rise time		-	40	-	ns
t _{d(off)}	Turn-off delay time	(see Figure 16. Test circuit for resistive load switching times and Figure 21. Switching time waveform)	-	46	-	ns
t _f	Fall time		-	15	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		80	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		320	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 80\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.2	V
t_{rr}	Reverse recovery time	$I_{SD} = 80\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 80\text{ V}$, $T_J = 150\text{ }^{\circ}\text{C}$ (see Figure 18. Test circuit for inductive load switching and diode recovery times)	-	77		ns
Q_{rr}	Reverse recovery charge		-	146		nC
I_{RRM}	Reverse recovery current		-	4		A

1. Pulse width is limited by safe operating area.

2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

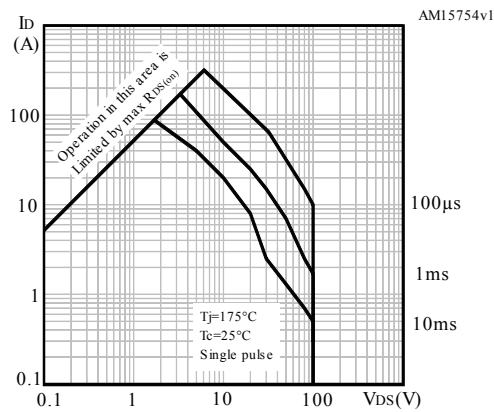
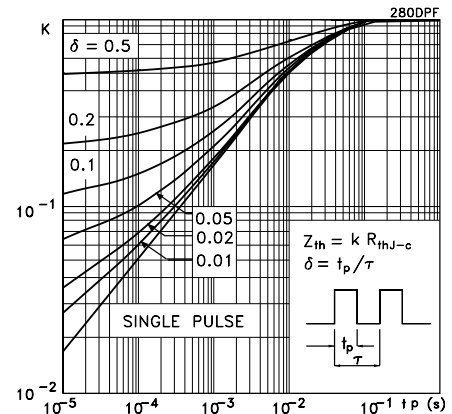
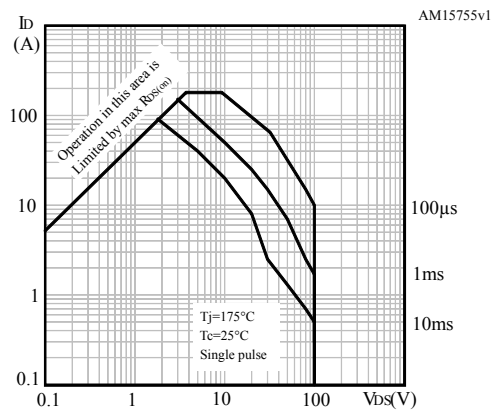
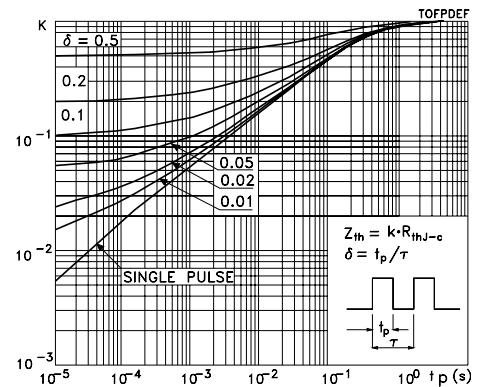
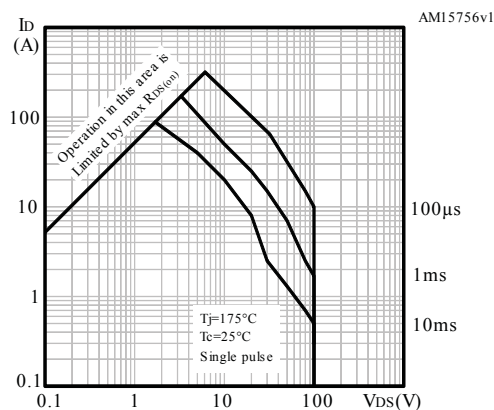
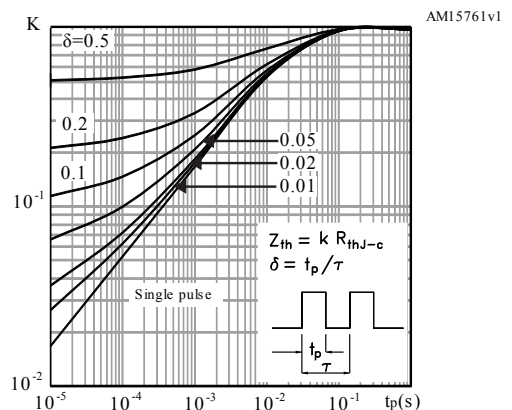
Figure 1. Safe operating area for DPAK

Figure 2. Thermal impedance for DPAK

Figure 3. Safe operating area for TO-220FP

Figure 4. Thermal impedance for TO-220FP

Figure 5. Safe operating area for D²PAK, I²PAK and TO-220

Figure 6. Thermal impedance for D²PAK, I²PAK and TO-220


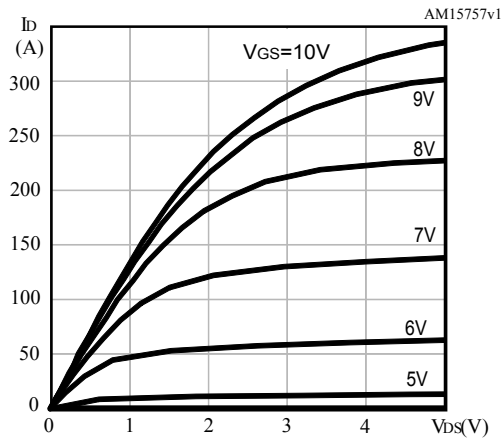
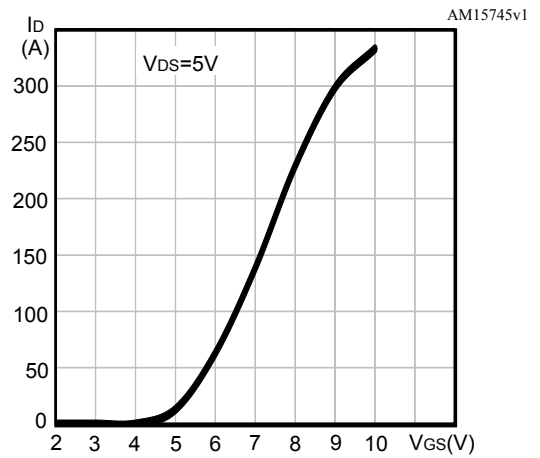
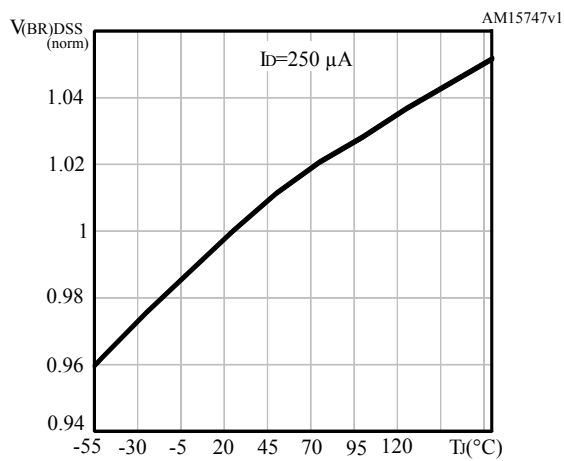
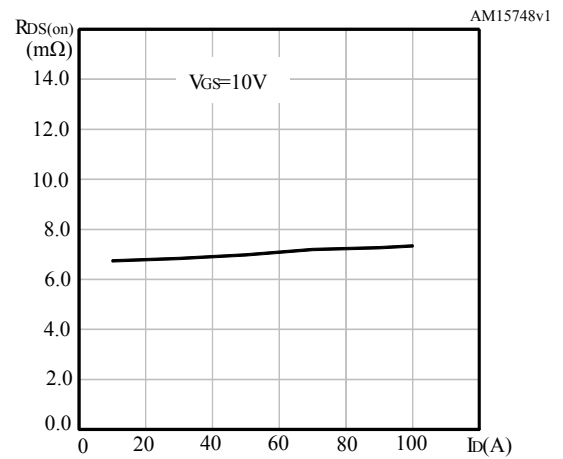
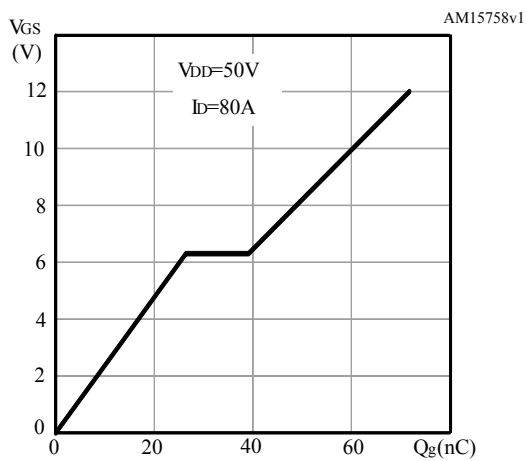
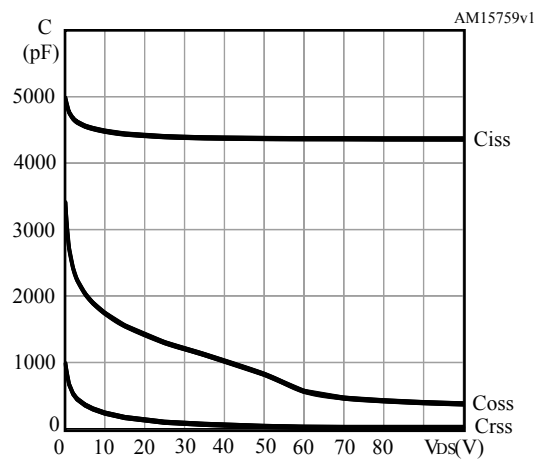
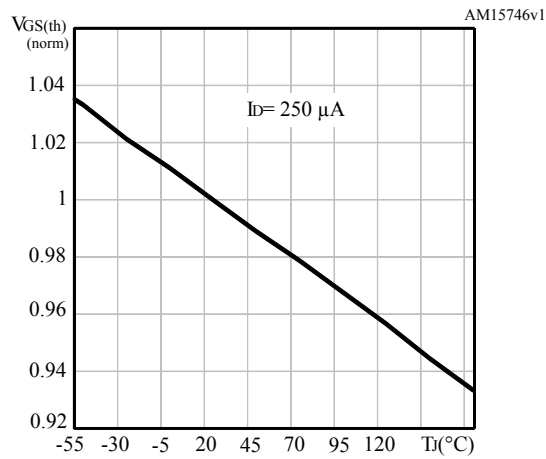
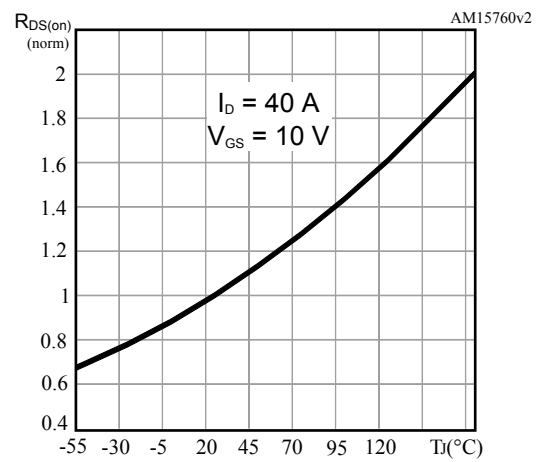
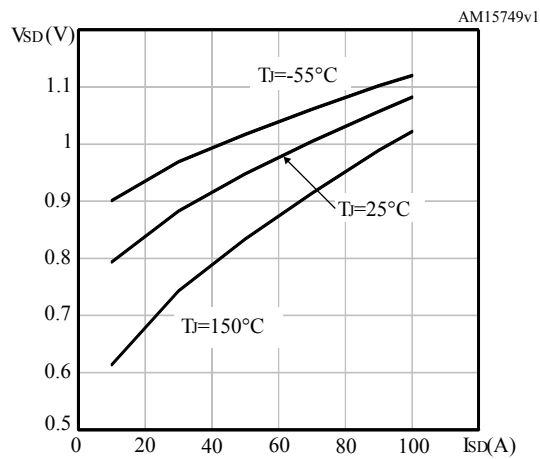
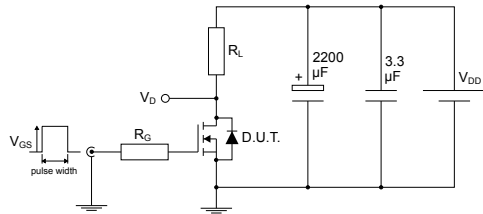
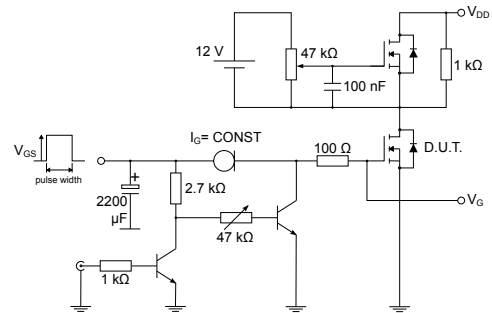
Figure 7. Output characteristics

Figure 8. Transfer characteristics

Figure 9. Normalized $V_{(BR)DSS}$ vs temperature

Figure 10. Static drain-source on-resistance

Figure 11. Gate charge vs gate-source voltage

Figure 12. Capacitance variations


Figure 13. Normalized gate threshold voltage vs temperature

Figure 14. Normalized on-resistance vs temperature

Figure 15. Source-drain diode forward characteristics


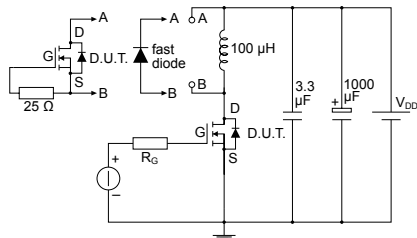
3 Test circuits

Figure 16. Test circuit for resistive load switching times


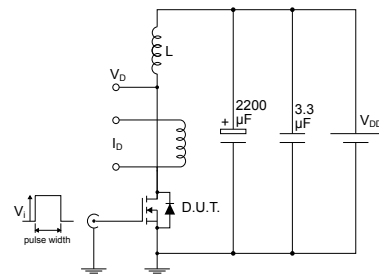
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Figure 17. Test circuit for gate charge behavior


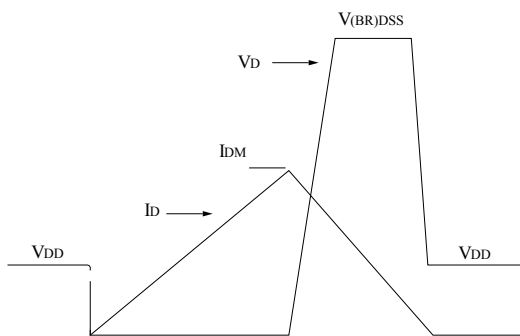
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Figure 18. Test circuit for inductive load switching and diode recovery times


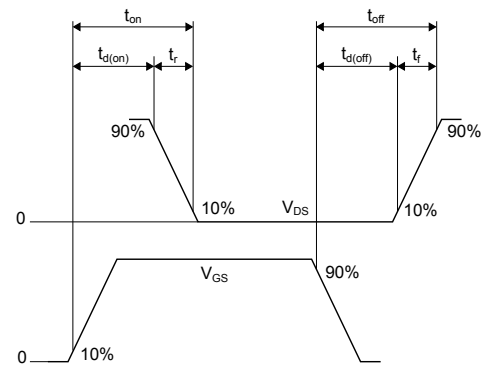
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Figure 19. Unclamped inductive load test circuit


AM01471v1

Figure 20. Unclamped inductive waveform


AM01472v1

Figure 21. Switching time waveform


AM01473v1

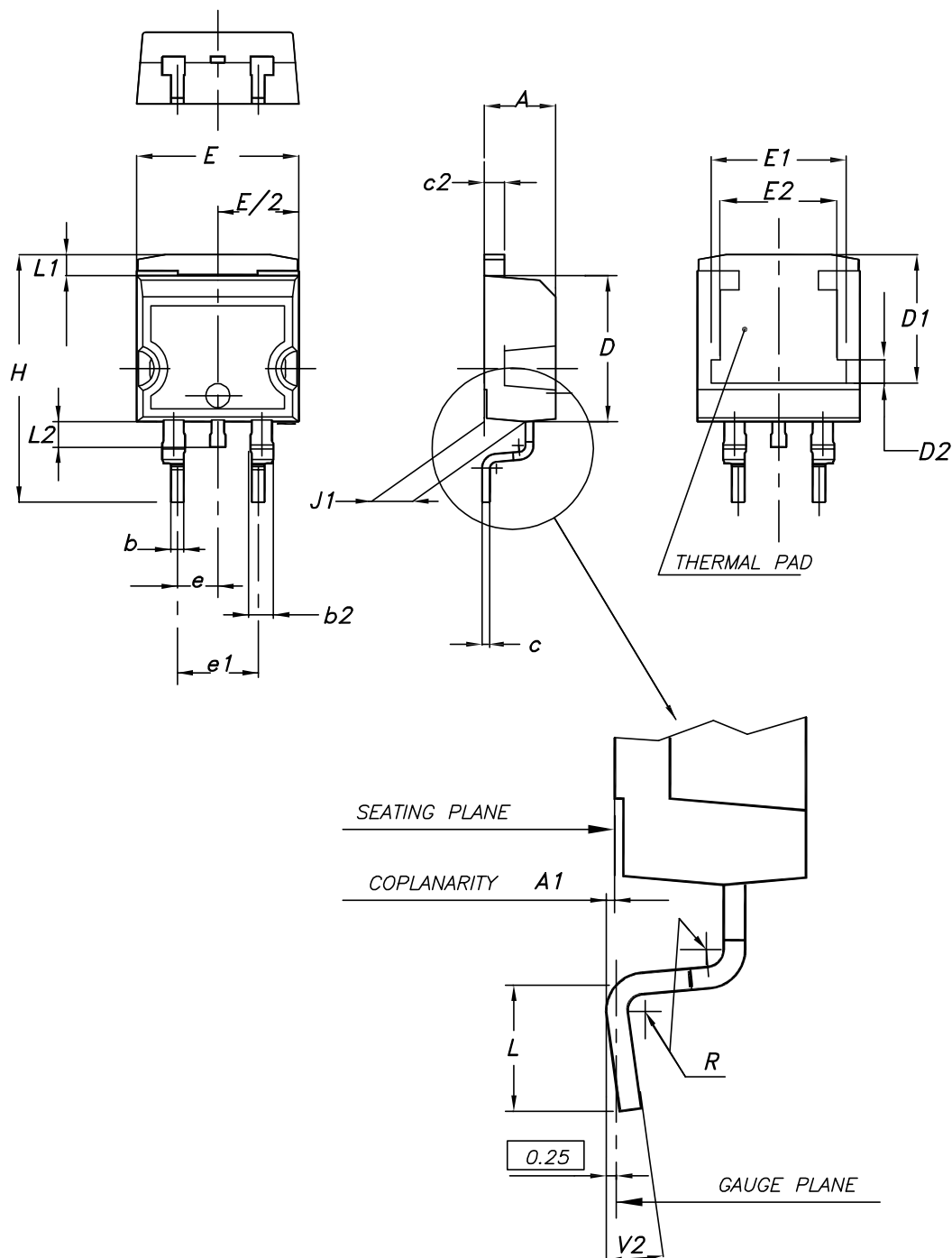


4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 D²PAK (TO-263) type A package information

Figure 22. D²PAK (TO-263) type A package outline

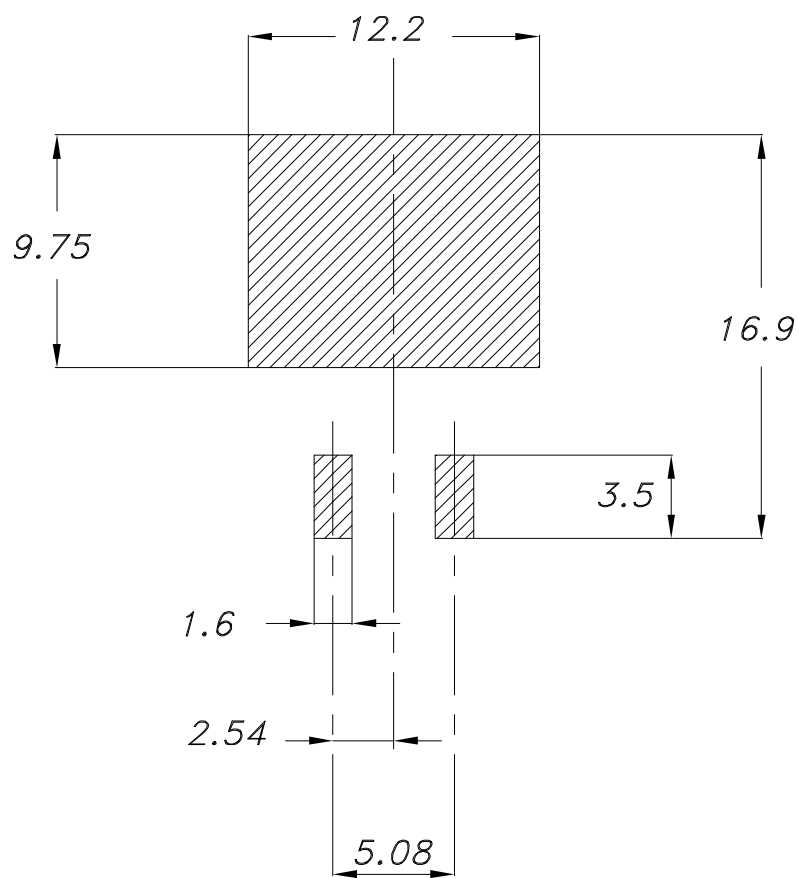


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Table 8. D²PAK (TO-263) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.30	8.50	8.70
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

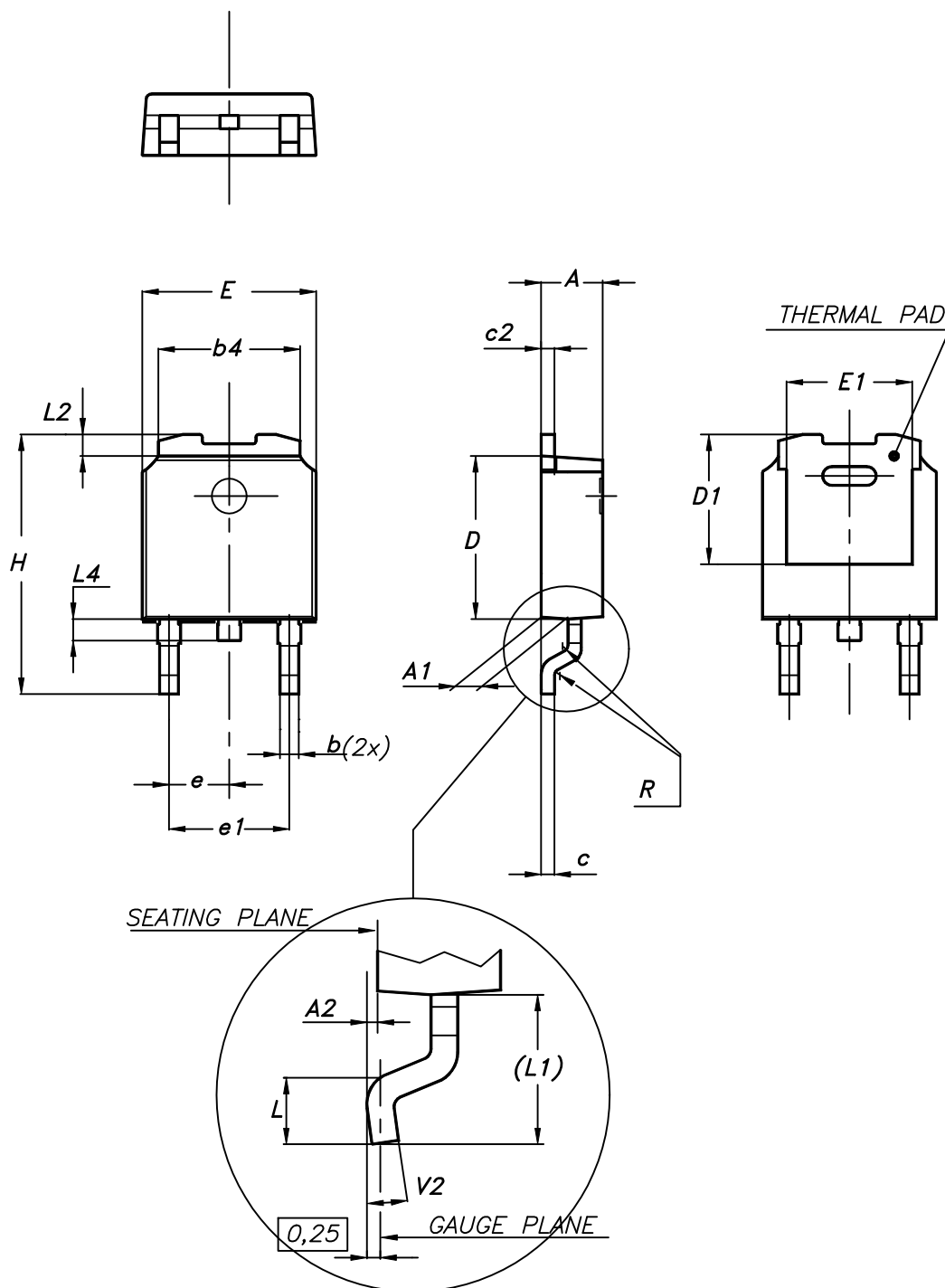
Figure 23. D²PAK (TO-263) recommended footprint (dimensions are in mm)



Footprint

4.2 DPAK (TO-252) type A2 package information

Figure 24. DPAK (TO-252) type A2 package outline

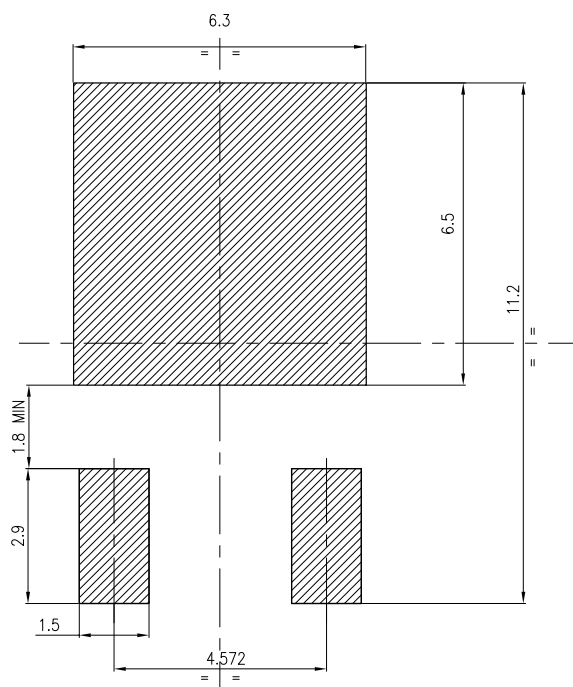


0068772_type-A2_rev25

Table 9. DPAK (TO-252) type A2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

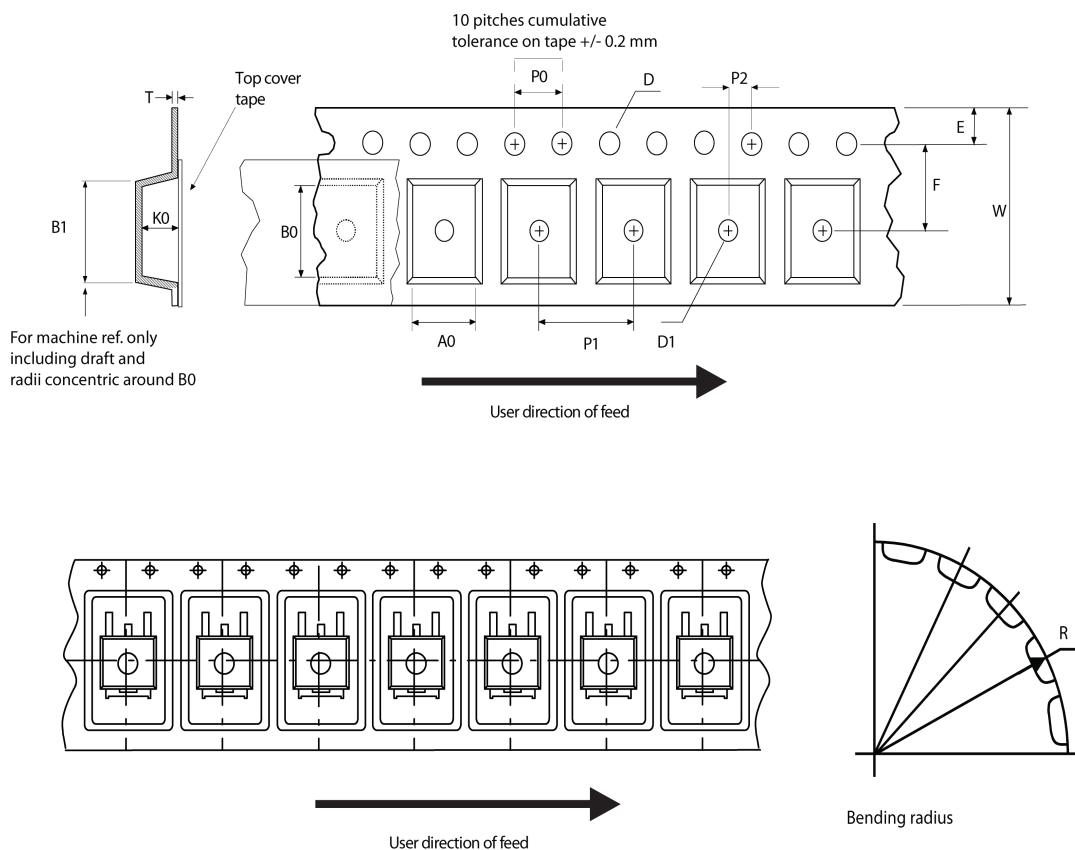
Figure 25. DPAK (TO-252) recommended footprint (dimensions are in mm)



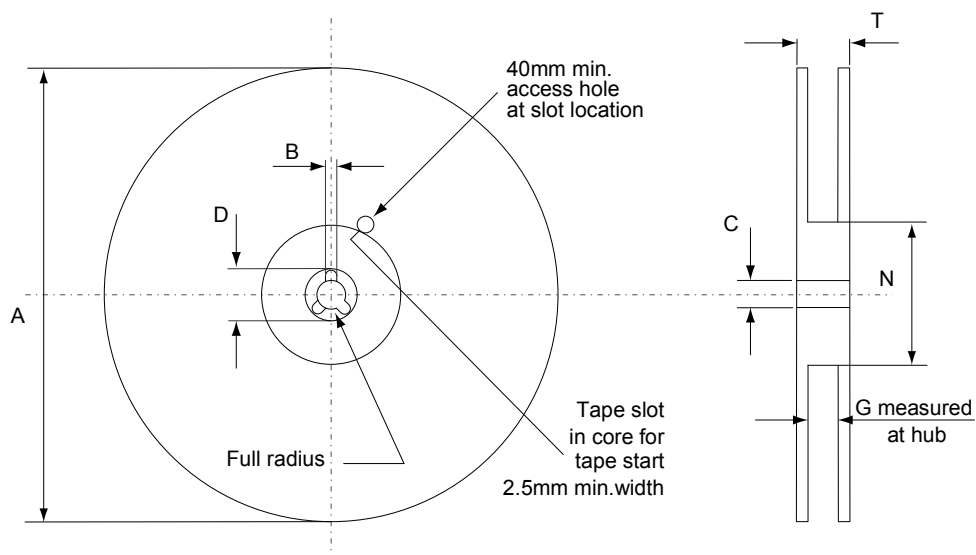
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4.3 D²PAK and DPAK packing information

Figure 26. Tape outline



AM08852v1

Figure 27. Reel outline


AM06038v1

Table 10. D²PAK tape and reel mechanical data

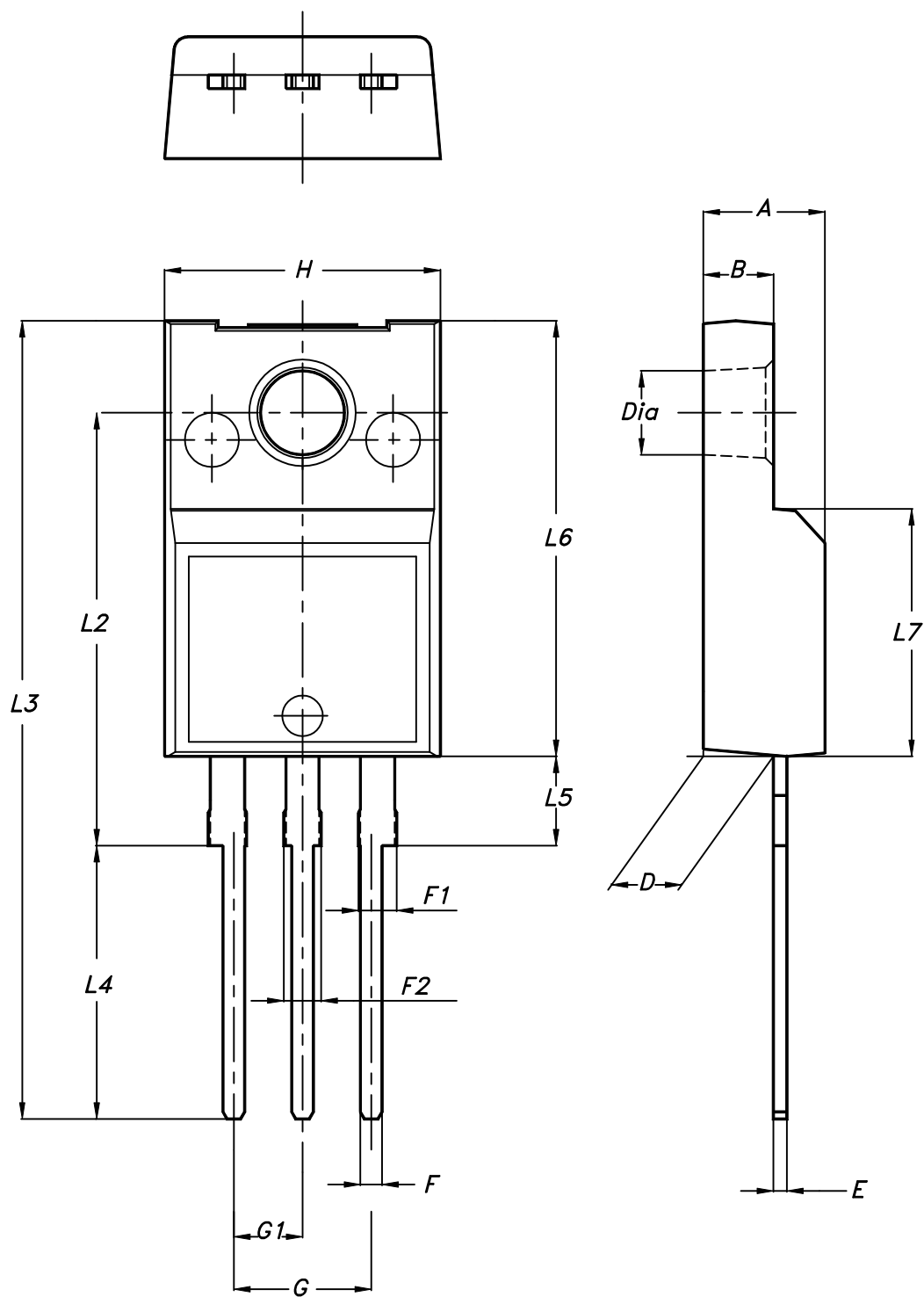
Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Table 11. DPAK tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

4.4 TO-220FP package information

Figure 28. TO-220FP package outline



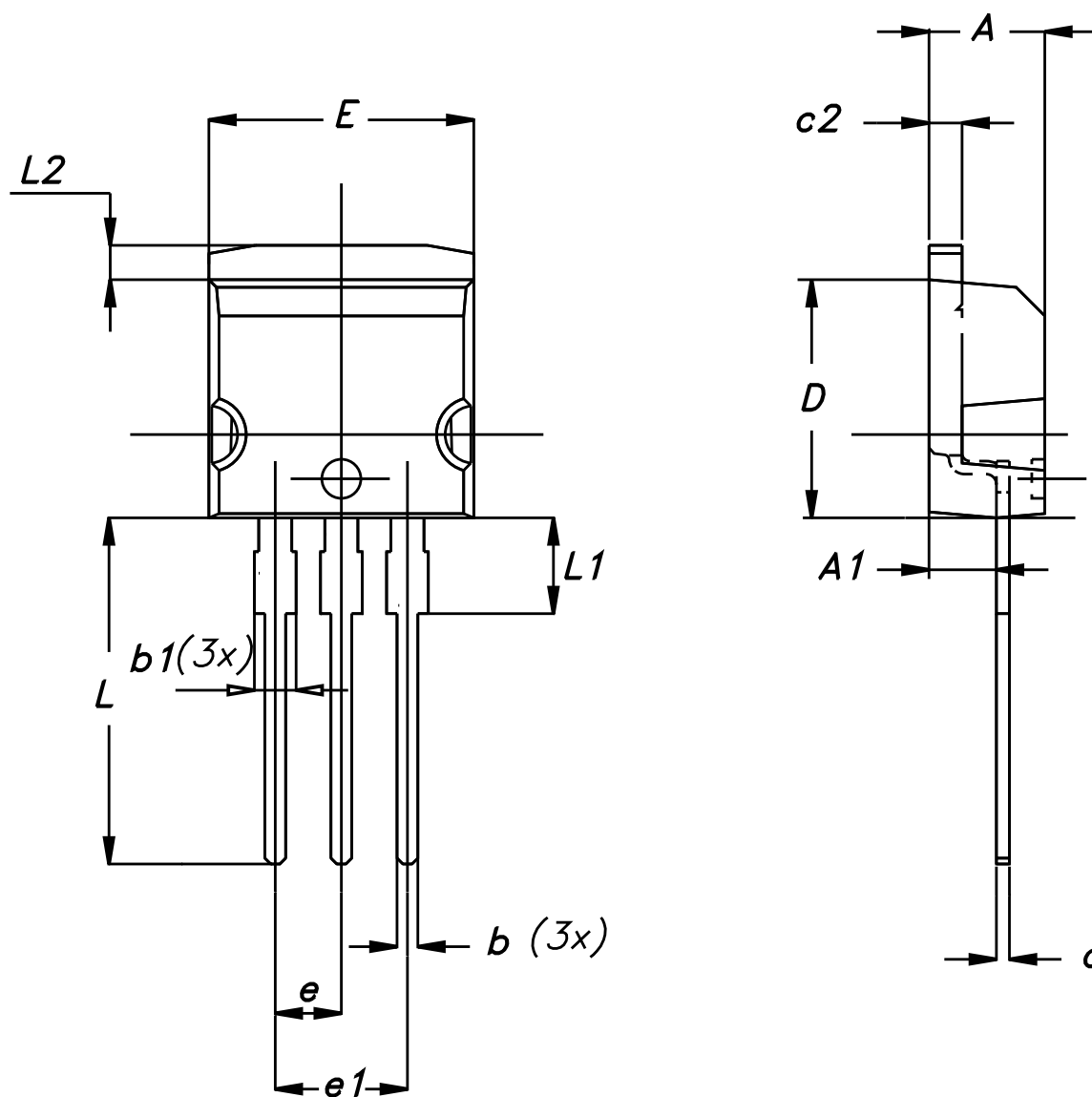
7012510_Rev_12_B

Table 12. TO-220FP package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

4.5 I²PAK package information

Figure 29. I²PAK package outline



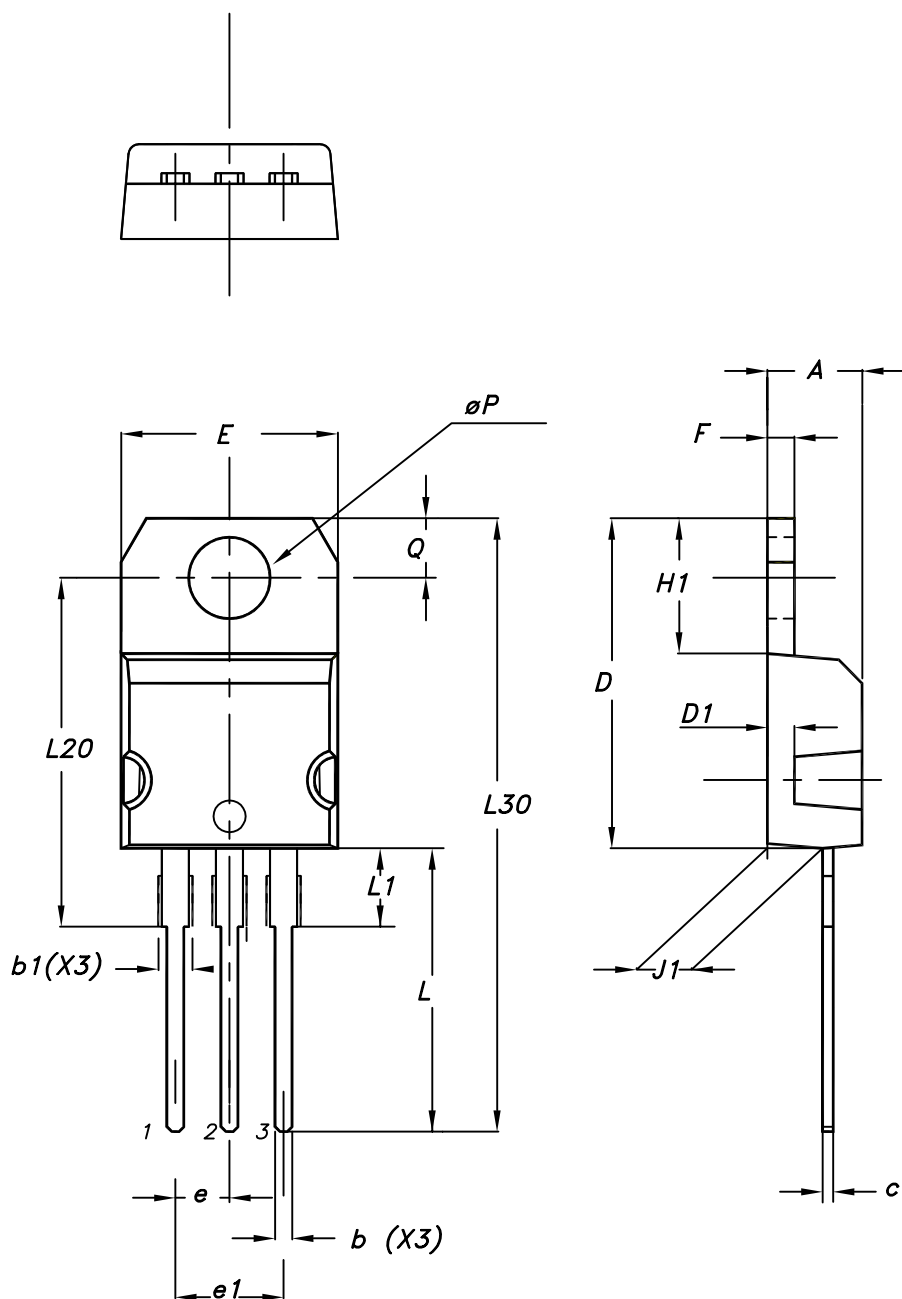
0004982_Rev_H

Table 13. I²PAK package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40	-	4.60
A1	2.40	-	2.72
b	0.61	-	0.88
b1	1.14	-	1.70
c	0.49	-	0.70
c2	1.23	-	1.32
D	8.95	-	9.35
e	2.40	-	2.70
e1	4.95	-	5.15
E	10	-	10.40
L	13	-	14
L1	3.50	-	3.93
L2	1.27	-	1.40

4.6 TO-220 type A package information

Figure 30. TO-220 type A package outline



0015988_typeA_Rev_21

Table 14. TO-220 type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

5 Ordering information

Table 15. Order codes

Order code	Marking	Package	Packing
STB100N10F7	100N10F7	D ² PAK	Tape and reel
STD100N10F7		DPAK	Tape and reel
STF100N10F7		TO-220FP	Tube
STI100N10F7		I ² PAK	Tube
STP100N10F7		TO-220	Tube

Revision history

Table 16. Document revision history

Date	Version	Changes
05-Oct-2012	1	Initial release.
07-Feb-2013	2	Inserted device in TO-220FP. Updated title and features on the cover page, <i>Table 1: Device summary</i>, <i>Table 2: Absolute maximum ratings</i>, <i>Table 3: Thermal resistance</i> and <i>Table 5: On/off states</i> accordingly. Updated <i>Table 6: Dynamic</i>, <i>Table 7: Switching times</i>, <i>Table 8: Source drain diode</i> and <i>Section 4: Package mechanical data</i>. Added <i>Section 5: Packaging mechanical data</i>.
29-Apr-2013	3	Modified: the entire typical values in <i>Table 6</i>, <i>t_f</i> typical value in <i>Table 7</i>, VSD and typical values for <i>t_{rr}</i>, <i>q_{rr}</i>, IRRM Inserted: <i>Table 4: Avalanche characteristics</i> and <i>Section 2.1: Electrical characteristics (curves)</i> Minor text changes
25-Nov-2013	4	Inserted device in D²PAK. Updated title and features on the cover page, <i>Table 1: Device summary</i>, <i>Table 2: Absolute maximum ratings</i>, <i>Table 3: Thermal resistance</i> and <i>Table 5: On/off states</i> accordingly. Updated <i>Table 6: Dynamic</i>, <i>Section 4: Package mechanical data</i> and <i>Section 5: Packaging mechanical data</i>.
18-Jun-2018	5	Added STI100N10F7 device and updated the document accordingly. Removed maturity status indication, updated title, features and description on cover page. Updated Table 1. Absolute maximum ratings. Updated Section 4 Package information. Minor text changes

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