9 kHz to 7 GHz, Bidirectional RMS and VSWR Detector

Data Sheet **ADL5920**

FEATURES

Wideband matched 9 kHz to 7 GHz operation
Forward and reverse power and return loss measurement
49 dB ±1.0 dB input range with −19 dBm minimum input level, ±1.0 dB at 1 GHz
Linear in dB rms (crest factor insensitive) outputs
Insertion loss: 1.1 dB at 1 GHz and 1.9 dB at 6 GHz
Input and output return loss and VSWR
- **1 GHz: 22 dB/1.16:1**
- **3 GHz: 14 dB/1.5:1**
- **6 GHz: 12 dB/1.7:1**

Output IP3: 70.5 dBm at 1 GHz
Directivity
- **20 dB at 1 GHz**
- **13 dB at 3 GHz**
- **5 dB at 6 GHz**

Maximum input power
- **30 dBm for open or shorted termination**
- **33 dBm for matched termination**

APPLICATIONS

Industrial metering
Broadband inline power and return loss measurement
Transmit power control and automatic level control in wireless transmitters, signal generators, network analyzers, and wireless communications testers
Condition based monitoring of system modules, cables, and connectors

FUNCTIONAL BLOCK DIAGRAM

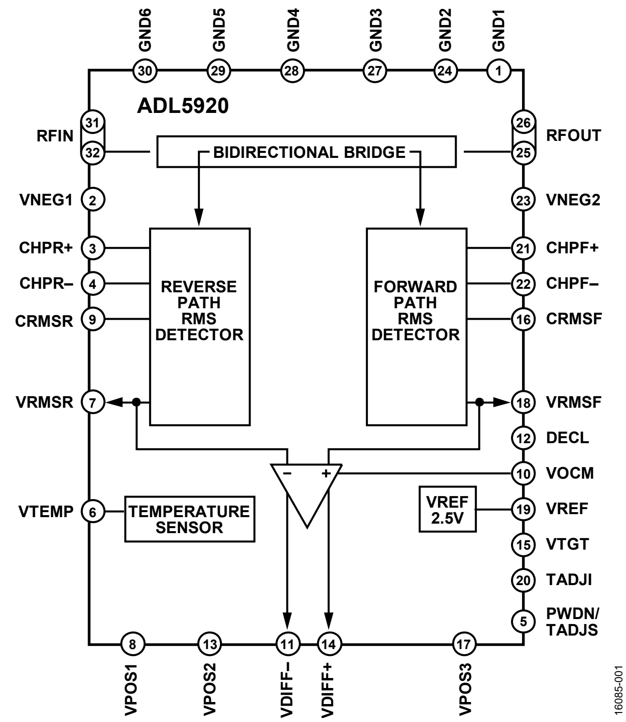

Figure 1.

GENERAL DESCRIPTION

The ADL5920 is an ultrawideband, bidirectional detector that simultaneously measures forward and reverse rms power levels in a signal path, along with the return loss.

The forward and reverse power traveling through the integrated bidirectional bridge is measured using two 50 dB linear in dB rms detectors. The detector output voltages, available at the VRMSF and VRMSR pins, are proportional to the forward and reflected power in dBm. A third, differential, output produces a voltage proportional to the return loss (reflection coefficient) in dB, closely related to the voltage standing wave ratio (VSWR). The common-mode level of this output is externally adjustable through the VOCM pin.

The primary transmission line of the bidirectional bridge, from RFIN to RFOUT (or vice versa) is dc-coupled and allows small amounts of dc bias current through the bridge. When dc-coupled to source and load, the positive and negative supply pins of the ADL5920 must be connected to +5 V and −2.5 V, respectively (relative to the dc voltage at RFIN and RFOUT). The internal detector circuitry is also dc-coupled to the bidirectional bridge to support measurements down to 9 kHz.

The maximum input signal on each of the RF ports (RFIN and RFOOUT) is 30 dBm for open and shorted terminations and 33 dBm for a matched termination.

The ADL5920 draws 160 mA from a 5 V supply and has a low power, power-down mode controlled through the PWDN/TADJS pin.

The device is supplied in a 32-lead, 5 mm × 5 mm LFCSP and is specified for ambient operating temperatures in the −40°C to +85°C range.

Multifunction pin names may be referenced by their relevant function only.

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REVISION HISTORY

12/2019—Rev. A to Rev. B

3/2019—Rev. 0 to Rev. A

1/2019—Revision 0: Initial Version

SPECIFICATIONS

VPOS1, VPOS2, VPOS3 = 5 V, VNEG = 0 V, T_A = 25°C, output impedance (Z_O) = 50 Ω, unless otherwise noted (see Figure 38).

Table 1.

Parameter[1]	Test Conditions/Comments	Min	Typ	Max	Unit
OVERALL FUNCTION					
Frequency Range		0.009		7000	MHz
Input and Output Impedance	RFIN, RFOUT require 50 Ω terminations		50		Ω
Maximum Input Power (P_{IN})	Open or short termination		30		dBm
	Matched termination		33		dBm
10 MHz	VRMSF, VRMSR, TADJI voltage (V_{TADJI}) = 0 V, TADJS voltage (V_{TADJS}) = 0 V				
Insertion Loss			0.9		dB
Return Loss (RFIN, RFOUT)	50 Ω load on RFOUT		43		dB
VSWR (RFIN, RFOUT)			1.02:1		
Directivity	0.1 µF capacitors on CHPR+/CHPR− and CHPF+/CHPF−		43		dB
±1.0 dB Input Range	VRMSF, VRMSR, continuous wave (CW) input		50		dB
Maximum Input Level, ±1.0 dB	Slope and intercept calculated using linear regression from +30 dBm to −15 dBm		30		dBm
Minimum Input Level, ±1.0 dB			−20		dBm
Deviation vs. Temperature	Deviation from output at T_A = 25°C				
	−40°C, P_{IN} = −10 dBm		−0.46		dB
	−40°C, P_{IN} = 20 dBm		−0.4		dB
	85°C, P_{IN} = −10 dBm		−0.02		dB
	85°C, P_{IN} = 20 dBm		0.18		dB
	70°C, P_{IN} = −10 dBm		−0.03		dB
	70°C, P_{IN} = 20 dBm		0.2		dB
Logarithmic Slope	VRMSF, VRMSR		61		mV/dB
Logarithmic Intercept	VRMSF, VRMSR		−29.7		dBm
100 MHz	VRMSF, VRMSR, V_{TADJI} = 0 V, V_{TADJS} = 0 V				
Insertion Loss			0.9		dB
Return Loss (RFIN, RFOUT)	50 Ω load on RFOUT		37		dB
VSWR (RFIN, RFOUT)			1.03:1		
Directivity	0.1 µF capacitors on CHPR+/CHPR− and CHPF+/CHPF−		43		dB
±1.0 dB Input Range	VRMSF, VRMSR, CW input		49		dB
Maximum Input Level, ±1.0 dB	Slope and intercept calculated using linear regression from +30 dBm to −15 dBm		30		dBm
Minimum Input Level, ±1.0 dB			−19		dBm
Deviation vs. Temperature	Deviation from output at T_A = 25°C				
	−40°C, P_{IN} = −10 dBm		−0.43		dB
	−40°C, P_{IN} = 20 dBm		−0.46		dB
	85°C, P_{IN} = −10 dBm		0.04		dB
	85°C, P_{IN} = 20 dBm		0.26		dB
	70°C, P_{IN} = −10 dBm		0.04		dB
	70°C, P_{IN} = 20 dBm		0.28		dB
Logarithmic Slope	VRMSF, VRMSR		61		mV/dB
Logarithmic Intercept	VRMSF, VRMSR		−29.8		dBm

Parameter[1]	Test Conditions/Comments	Min	Typ	Max	Unit
1 GHz	VRMSF, VRMSR, V_{TADJI} = 0 V, V_{TADJS} = 0 V				
Insertion Loss			1.1		dB
Return Loss (RFIN, RFOUT)	50 Ω load on RFOUT		22		dB
VSWR (RFIN, RFOUT)			1.16:1		
Directivity	0.1 µF capacitors on CHPR+/CHPR− and CHPF+/CHPF−		20		dB
Output Third-Order Intercept (IP3)	27 dBm per tone at RFIN, RFOUT terminated with 50 Ω, 1 MHz tone spacing		70.5		dBm
±1.0 dB Input Range	VRMSF, VRMSR, CW input		49		dB
Maximum Input Level, ±1.0 dB	Slope and intercept calculated using linear regression from +30 dBm to −15 dBm		30		dBm
Minimum Input Level, ±1.0 dB			−19		dBm
Deviation vs. Temperature	Deviation from output at T_A = 25°C				
	−40°C, P_{IN} = −10 dBm		−0.41		dB
	−40°C, P_{IN} = 20 dBm		−0.32		dB
	85°C, P_{IN} = −10 dBm		−0.5		dB
	85°C, P_{IN} = 20 dBm		−0.11		dB
	70°C, P_{IN} = −10 dBm		−0.24		dB
	70°C, P_{IN} = 20 dBm		0.15		dB
Logarithmic Slope	VRMSF, VRMSR		61		mV/dB
Logarithmic Intercept	VRMSF, VRMSR		−27		dBm
2 GHz	VRMSF, VRMSR, V_{TADJI} = 0 V, V_{TADJS} = 0.2 V				
Insertion Loss			1.3		dB
Return Loss (RFIN, RFOUT)	50 Ω load on RFOUT		17		dB
VSWR (RFIN, RFOUT)			1.30:1		
Directivity	No capacitors on CHPR+/CHPR− and CHPF+/CHPF−		16		dB
±1.0 dB Input Range	VRMSF, VRMSR, CW input		45		dB
Maximum Input Level, ±1.0 dB	Slope and intercept calculated using linear regression from +30 dBm to −15 dBm		28		dBm
Minimum Input Level, ±1.0 dB			−17		dBm
Deviation vs. Temperature	Deviation from output at T_A = 25°C				
	−40°C, P_{IN} = −10 dBm		−0.44		dB
	−40°C, P_{IN} = 20 dBm		−0.73		dB
	85°C, P_{IN} = −10 dBm		−0.98		dB
	85°C, P_{IN} = 20 dBm		−0.58		dB
	70°C, P_{IN} = −10 dBm		−0.36		dB
	70°C, P_{IN} = 20 dBm		0.04		dB
Logarithmic Slope	VRMSF, VRMSR		60.6		mV/dB
Logarithmic Intercept	VRMSF, VRMSR		−26		dBm
3 GHz	VRMSF, VRMSR, V_{TADJI} = 0 V, V_{TADJS} = 0.2 V				
Insertion Loss			1.5		dB
Return Loss (RFIN, RFOUT)	50 Ω load on RFOUT		14		dB
VSWR (RFIN, RFOUT)			1.5:1		
Directivity	No capacitors on CHPR+/CHPR− and CHPF+/CHPF−		13		dB
±1.0 dB Input Range	VRMSF, VRMSR, CW input		43		dB
Maximum Input Level, ±1.0 dB	Slope and intercept calculated using linear regression from +30 dBm to −15 dBm		26		dBm
Minimum Input Level, ±1.0 dB			−17		dBm

Parameter[1]	Test Conditions/Comments	Min	Typ	Max	Unit
Deviation vs. Temperature	Deviation from output at T_A = 25°C				
	−40°C, P_{IN} = −10 dBm		−0.38		dB
	−40°C, P_{IN} = 20 dBm		−0.71		dB
	85°C, P_{IN} = −10 dBm		−1.83		dB
	85°C, P_{IN} = 20 dBm		−1.48		dB
	70°C, P_{IN} = −10 dBm		−0.85		dB
	70°C, P_{IN} = 20 dBm		−0.37		dB
Logarithmic Slope	VRMSF, VRMSR		59.4		mV/dB
Logarithmic Intercept	VRMSF, VRMSR		−25.5		dBm
4 GHz	VRMSF, VRMSR, V_{TADJI} = 0 V, V_{TADJS} = 0.2 V				
Insertion Loss			1.7		dB
Return Loss (RFIN, RFOUT)	50 Ω load on RFOUT		12.5		dB
VSWR (RFIN, RFOUT)			1.7:1		
Directivity	No capacitors on CHPR+/CHPR− and CHPF+/CHPF−		7		dB
±1.0 dB Input Range	VRMSF, VRMSR, CW input		41		dB
Maximum Input Level, ±1.0 dB	Slope and intercept calculated using linear regression from +30 dBm to −15 dBm		25		dBm
Minimum Input Level, ±1.0 dB			−16		dBm
Deviation vs. Temperature	Deviation from output at T_A = 25°C				
	−40°C, P_{IN} = 0 dBm		−0.07		dB
	−40°C, P_{IN} = 20 dBm		−0.53		dB
	85°C, P_{IN} = 0 dBm		−1.95		dB
	85°C, P_{IN} = 20 dBm		−2.9		dB
	70°C, P_{IN} = 0 dBm		−0.81		dB
	70°C, P_{IN} = 20 dBm		−1.0		dB
Logarithmic Slope	VRMSF, VRMSR		59		mV/dB
Logarithmic Intercept	VRMSF, VRMSR		−24.6		dBm
5 GHz	VRMSF, VRMSR, V_{TADJI} = 0.2 V, V_{TADJS} = 0.2 V				
Insertion Loss			1.7		dB
Return Loss (RFIN, RFOUT)	50 Ω load on RFOUT		11		dB
VSWR (RFIN, RFOUT)			1.9:1		
Directivity	No capacitors on CHPR+/CHPR− and CHPF+/CHPF−		6		dB
±1.0 dB Input Range	VRMSF, VRMSR, CW input		37		dB
Maximum Input Level, ±1.0 dB	Slope and intercept calculated using linear regression from +15 dBm to −10 dBm		24		dBm
Minimum Input Level, ±1.0 dB			−13		dBm
Deviation vs. Temperature	Deviation from output at T_A = 25°C				
	−40°C, P_{IN} = 0 dBm		−0.86		dB
	−40°C, P_{IN} = 20 dBm		−1.46		dB
	85°C, P_{IN} = 0 dBm		−1.9		dB
	85°C, P_{IN} = 20 dBm		−2.94		dB
	70°C, P_{IN} = 0 dBm		−0.5		dB
	70°C, P_{IN} = 20 dBm		−1.09		dB
Logarithmic Slope	VRMSF, VRMSR		59.2		mV/dB
Logarithmic Intercept	VRMSF, VRMSR		−22.3		dBm

Parameter[1]	Test Conditions/Comments	Min	Typ	Max	Unit
6 GHz	VRMSF, VRMSR, V_{TADJI} = 0.2 V, V_{TADJS} = 0 V				
Insertion Loss			1.9		dB
Return Loss (RFIN, RFOUT)	50 Ω load on RFOUT		12		dB
VSWR (RFIN, RFOUT)			1.7:1		
Directivity	No capacitors on CHPR+/CHPR− and CHPF+/CHPF−		5		dB
±1.0 dB Input Range	VRMSF, VRMSR, CW input		33		dB
Maximum Input Level, ±1.0 dB	Slope and intercept calculated using linear regression from +20 dBm to −5 dBm		22		dBm
Minimum Input Level, ±1.0 dB			−11		dBm
Deviation vs. Temperature	Deviation from output at T_A = 25°C				
	−40°C, P_{IN} = 0 dBm		−0.74		dB
	−40°C, P_{IN} = 20 dBm		−1.45		dB
	85°C, P_{IN} = 0 dBm		−3.36		dB
	85°C, P_{IN} = 20 dBm		−3.57		dB
	70°C, P_{IN} = 0 dBm		−1.14		dB
	70°C, P_{IN} = 20 dBm		−1.72		dB
Logarithmic Slope	VRMSF, VRMSR		57.7		mV/dB
Logarithmic Intercept	VRMSF, VRMSR		−19.7		dBm
7 GHz	VRMSF, VRMSR, V_{TADJI} = 0.2 V, V_{TADJS} = 0.8 V				
Insertion Loss			2		dB
Return Loss (RFIN, RFOUT)	50 Ω load on RFOUT		14		dB
VSWR (RFIN, RFOUT)			1.5:1		
Directivity	No capacitors on CHPR+/CHPR− and CHPF+/CHPF−		7		dB
±1.0 dB Input Range	VRMSF, VRMSR, CW input		31		dB
Maximum Input Level, ±1.0 dB	Slope and intercept calculated using linear regression from 20 dBm to 0 dBm		21		dBm
Minimum Input Level, ±1.0 dB			−10		dBm
Deviation vs. Temperature	Deviation from output at T_A = 25°C				
	−40°C, P_{IN} = 0 dBm		−1.39		dB
	−40°C, P_{IN} = 20 dBm		−2.75		dB
	85°C, P_{IN} = 0 dBm		−3.77		dB
	85°C, P_{IN} = 20 dBm		−3.11		dB
	70°C, P_{IN} = 0 dBm		−1.55		dB
	70°C, P_{IN} = 20 dBm		−1.15		dB
Logarithmic Slope	VRMSF, VRMSR		57.4		mV/dB
Logarithmic Intercept	VRMSF, VRMSR		−17.7		dBm
OUTPUT INTERFACE	VRMSF, VRMSR				
Short-Circuit Current					
Sourcing	VRMSF and VRMSR = 3.5 V		73		mA
Sinking	VRMSR and VRMSR = 100 mV, no RF Input		71		mA
Small Signal Output Impedance			0.4		Ω
Rise Time	P_{IN} = off to −10 dBm, 10% to 90%, 10 nF on CRMSF and CRMSR		18		µs
Fall Time	P_{IN} = −10 dBm to off, 10% to 90%, 10 nF on CRMSF and CRMSR		75		µs
OUTPUT INTERFACE	VDIFF+, VDIFF−				
Common-Mode Output Voltage	VOCM		2.5		V
Small Signal Output Impedance			0.4		Ω
Current Capability					
Source			69		mA
Sink			69		mA

Parameter[1]	Test Conditions/Comments	Min	Typ	Max	Unit
TEMPERATURE COMPENSATION	TADJI				
Input Voltage Range		0		1	V
Input Bias Current	V_{TADJI} = 1 V		14		µA
Input Resistance			70		kΩ
VOLTAGE REFERENCE	VREF				
Output Voltage	T_A = 25°C, load resistance (R_L) = 10 kΩ		2.5		V
Small Signal Output Impedance			3.1		Ω
Current Capability					
Source			9.8		mA
Sink			4.6		mA
TEMPERATURE REFERENCE	VTEMP				
Output Voltage	T_A = 25°C, R_L ≥ 10 kΩ		1.38		V
Temperature Coefficient	−40°C ≤ T_A ≤ +85°C, R_L ≥ 10 kΩ		4.5		mV/°C
POWER-DOWN INTERFACE AND TEMPERATURE COMPENSATION	Pin PWDN/TADJS				
Voltage Level					
To Enable				1.2	V
To Disable		1.5			V
Enable Time	P_{IN} = 10 dBm, PWDN/TADJS at 50% to output voltage at 90%, 10 nF on CRMSF and CRMSR		10		µs
Disable Time	P_{IN} = 10 dBm, PWDN/TADJS at 50% to output voltage at 10%, 10 nF on CRMSF and CRMSR		5		µs
Input Bias Current	V_{TADJS} = 2.5 V		36		µA
Input Resistance			70		kΩ
POWER SUPPLY	VPOS1, VPOS2, VPOS3				
Supply Voltage		4.9	5	5.1	V
Quiescent Current	PWDN/TADJS low	130	160	200	mA
	PWDN/TADJS high		1	3	mA

[1] When referring to a single function of a multifunction pin in the parameters, only the portion of the pin name that is relevant to the specification is listed. For full pin names of multifunction pins, refer to the Pin Configuration and Function Descriptions section.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage (VPOS1, VPOS2, and VPOS3)	5.5 V
Negative Supply Voltage (VNEG1 and VNEG2)	−3 V
Input Average Radio Frequency (RF) Power[1]	
50 Ω Load	33 dBm
Open or Shorted Load	30 dBm
Equivalent Voltage, Sine Wave Input	28.25 V p-p
PWDN/TADJS, TADJI, VOCM	0 V, VPOSx
VTGT	4 V
Maximum Junction Temperature	150°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

[1] Guaranteed by design based on extended duration bench testing at 85°C case temperature

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is junction to ambient thermal impedance, and θ_{JC} is junction to case (exposed pad) thermal impedance.

Table 3. Thermal Resistance

Package Type[1]	θ_{JA}	θ_{JC}	Unit
CP-32-7	44.05	1.08	°C/W

[1] No airflow with the exposed pad soldered to a 4-layer JEDEC board.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

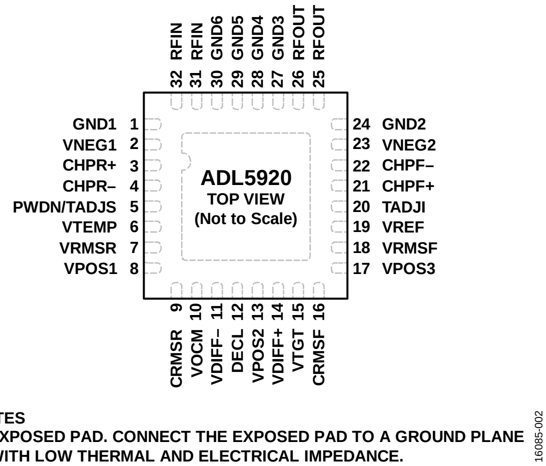

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 24, 27 to 30	GND1, GND2, GND3, GND4, GND5, GND6	RF Ground. Connect all ground pins to a low impedance ground plane.
2, 23	VNEG1, VNEG2	Negative Supply Pins. For normal single-supply operation, connect these pins to ground. In applications where the RF input and output are dc-coupled, apply a −2.5 V supply voltage to these pins along with a +5 V power supply on VPOS1, VPOS2, and VPOS3. In this dc-coupled operating mode, Pin 12 (DECL) must be connected to ground.
8, 13, 17	VPOS1, VPOS2, VPOS3	Power Supply. Separately decouple each power supply pin using 100 pF and 0.1 μF capacitors. The nominal supply voltage on these pins is 5 V.
3, 4, 21, 22	CHPR+, CHPR−, CHPF+, CHPF−	Offset Compensation Loop Control. The capacitances on these pin pairs set the high-pass corner frequency of the internal offset compensation loops, which in turn sets the minimum operating frequency of the rms detectors in the forward and reverse paths. For normal operation, add a capacitor from each pin to ground along with a capacitor across the pins. To operate at input frequencies down to 9 kHz, capacitances in the 1 μF range are required. To maintain the specified directivity, leave these pins open when operating at frequencies above 2 GHz.
5	PWDN/TADJS	Temperature Compensation and Shutdown. This pin is a dual function pin that controls temperature slope compensation at voltages <1.0 V and/or shuts down the device at voltages >1.4 V. The temperature compensation voltage is set by connecting this pin to VREF through a resistor divider.
6	VTEMP	Temperature Sensor Output of 1.38 V at T_A = 25°C with a Coefficient of 4.5 mV/°C.
7, 18	VRMSR, VRMSF	Reverse and Forward RMS Voltage Measurement. The voltages on these pins are proportional to the decibel power of the incident signal to the RFOUT and RFIN pins.
9, 16	CRMSR, CRMSF	RMS Averaging Capacitor for Reverse and Forward Path Detectors. Connect rms averaging capacitors between CRMSR and ground and between CRMSF and ground to set the averaging time constant of the forward and reverse rms detectors. For normal operation, the values of these two capacitors must be equal.
10	VOCM	Common-Mode Input Voltage for VDIFF+ and VDIFF−. The input voltage applied to VOCM sets the common-mode voltage for the VDIFF+ and VDIFF− differential pair. The nominal voltage on this pin is 2.5 V. However, this value can be reduced to as low as 1.5 V to accommodate the common-mode requirements of the ADC, which is driven by VDIFF+ and VDIFF−. The VOCM input requires a bias current of ±1 mA and must be driven from a low impedance source. VOCM can be driven from the VREF pin but the connection must include a 1 kΩ resistor to ground.
11, 14	VDIFF−, VDIFF+	Return Loss and VSWR Output. The differential voltage on these pins is proportional to the dB return loss of the load connected to the RFOUT port when the device is driven through the RFIN port. This differential voltage has a bias level equal to the voltage applied to VOCM, nominally 2.5 V.

Pin No.	Mnemonic	Description
12	DECL	Internal Decoupling Node. Decouple this pin with a 0.1 µF capacitor to ground. Do not use the voltage on this pin, nominally 3.2 V, externally to set any bias levels. In dc-coupled applications where VNEGx is connected to −2.5 V, this pin must be connected directly to ground.
15	VTGT	RMS Target Voltage. The voltage applied to this pin sets the target RF level at the output of the internal voltage controlled amplifiers that drive the internal squaring cells of the rms detectors. The recommended voltage for VTGT is 1 V. Increasing VTGT above 1 V degrades the rms accuracy of the ADL5920. Reducing VTGT below 1 V can improve the rms accuracy for signals with high crest factors. The voltage on this pin can be derived from a resistor divider circuit that is driven by the VREF pin (Pin 19).
19	VREF	Reference Voltage Output. This voltage reference has a nominal value of 2.5 V. This reference output voltage can set the voltage to the TADJI, TADJS, VTGT, and VOCM pins.
20	TADJI	RMS Detector Temperature Compensation. Use this pin to fine tune the temperature intercept stability of the rms detectors. The voltage applied to this pin can be derived from VREF using a simple resistor divider.
25, 26, 31, 32	RFOUT, RFIN	RF Inputs and Outputs. The two RFIN pins are common inputs that must always be connected to each other. Likewise, the two RFOUT pins must always be connected to each other. The power of the incident signal on RFIN is measured on the VRMSF pin, and the power on the incident signal into RFOUT is measured on the VRMSR pin. The ratio of the incident signals on RFIN and RFOUT is measured on the VDIFF+ and VDIFF− pins. The RFIN and RFOUT pins are interchangeable, allowing the source signal to drive into RFOUT with the load connected to RFIN. RFIN and RFOUT are normally ac-coupled to the source and load. RFIN and RFOUT can be dc-coupled by connecting a −2.5 V supply to the two VNEGx pins and by connecting the DECL pin to ground.
	EPAD	Exposed Pad. Connect the exposed pad to a ground plane with low thermal and electrical impedance.

TYPICAL PERFORMANCE CHARACTERISTICS

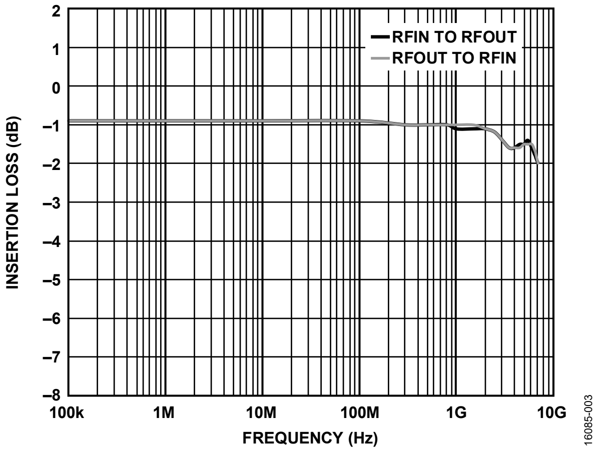

Figure 3. Forward and Reverse Insertion Loss vs. Frequency

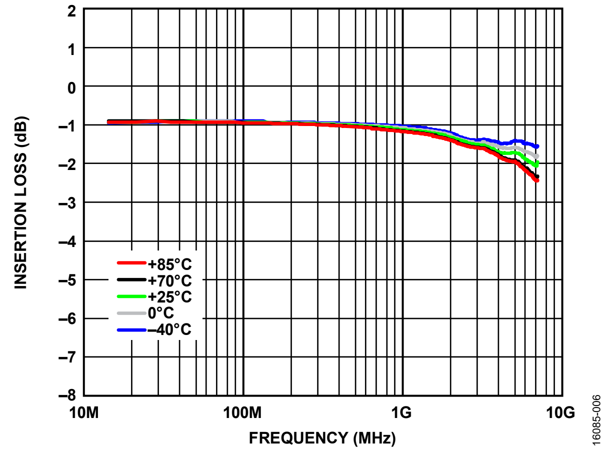

Figure 6. Forward Insertion Loss vs. Frequency at Various Temperatures

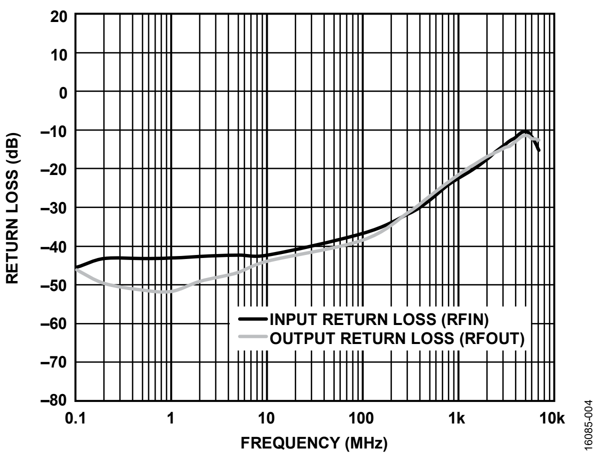

Figure 4. Return Loss vs. Frequency

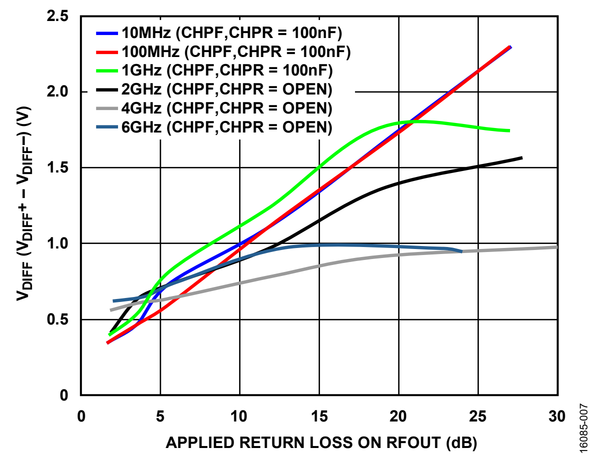

Figure 7. V_{DIFF} ($V_{DIFF+} - V_{DIFF-}$) vs. Applied Return Loss on RFOUT, Bridge Driven from RFIN at 15 dBm and Variable Return Loss at RFOUT

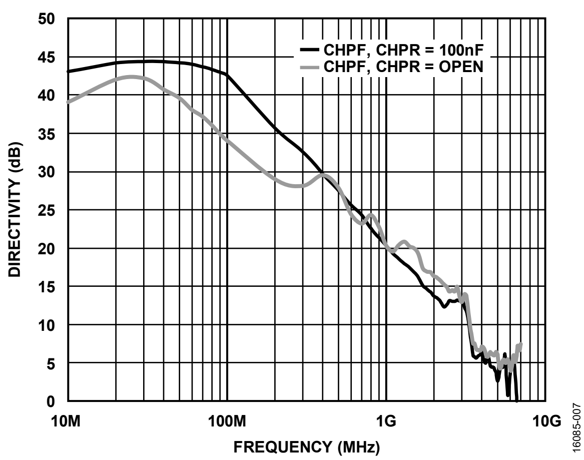

Figure 5. Directivity vs. Frequency with Bridge Driven from RFIN at 20 dBm and RFOUT Terminated with 50 Ω

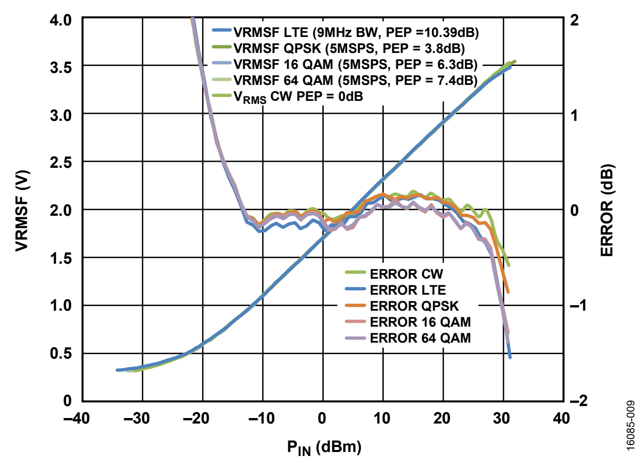

Figure 8. VRMSF Error from CW Linear Reference vs. Signal Modulation, Frequency = 1 GHz, CRMSF = 0.1 µF, Error Calculated Using Linear Regression of Data From –15 dBm to +30 dBm (BW Stands for Bandwidth and PEP Stands for Peak Envelope Power)

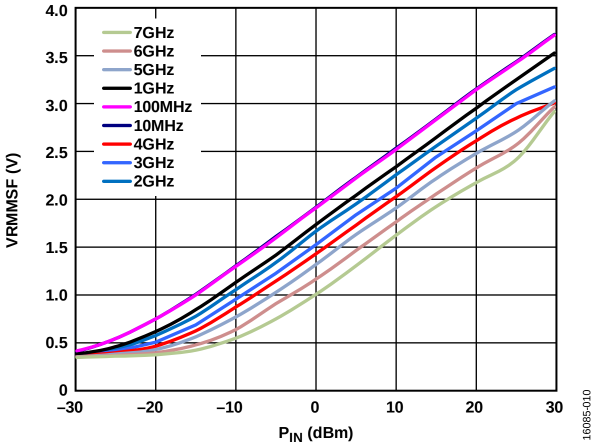

Figure 9. VRMSF Output Voltage vs. P_{IN} at Various Frequencies, Forward Drive

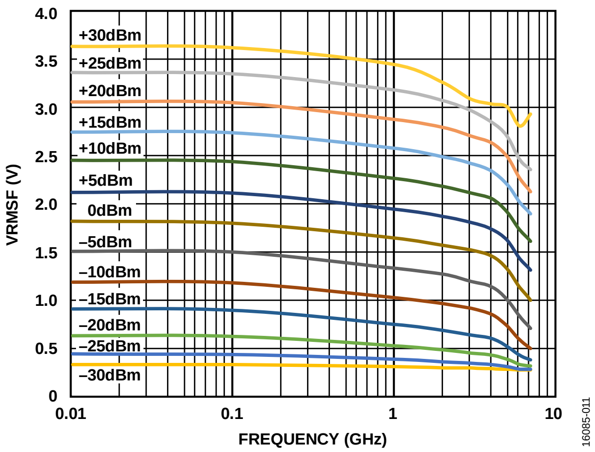

Figure 10. VRMSF vs. Frequency at Various Input Power Levels, Forward Drive

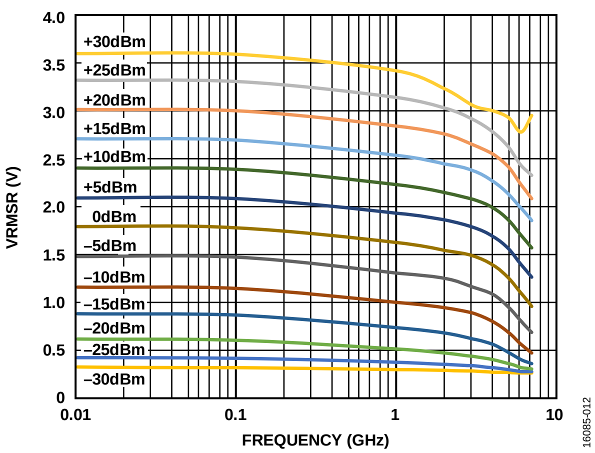

Figure 11. VRMSR vs. Frequency at Various Input Power Levels, Reverse Drive

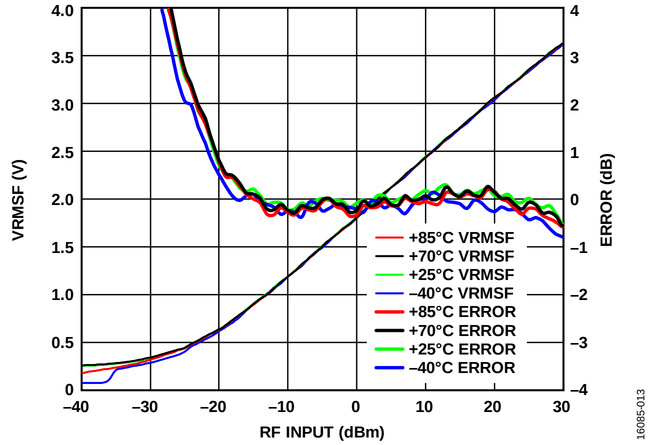

Figure 12. VRMSF Output Voltage and Error vs. RF Input and Temperature at 10 MHz, Error Calculated Using Linear Regression of Data Between +30 dBm and −15 dBm, TADJS = 0 V, TADJI = 0 V, 0.1 μF Across CHPF+, CHPF−

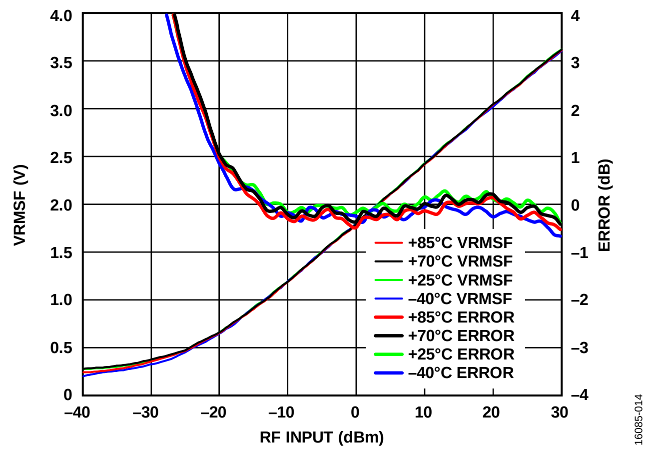

Figure 13. VRMSF and Error vs. RF Input and Temperature at 100 MHz, Error Calculated Using Linear Regression of Data Between +30 dBm and −15 dBm, TADJS = 0 V, TADJI = 0 V, 0.1 μF Across CHPF+, CHPF−

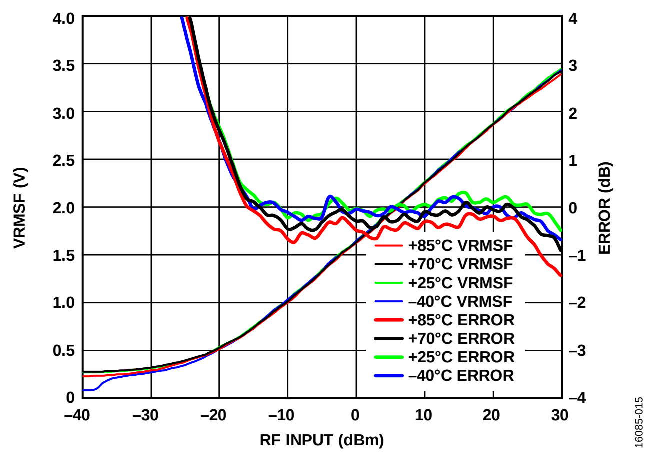

Figure 14. VRMSF and Error vs. RF Input and Temperature at 1 GHz, Error Calculated Using Linear Regression of Data Between +30 dBm and −15 dBm, TADJS = 0 V, TADJI = 0 V, 0.1 μF Across CHPF+, CHPF−

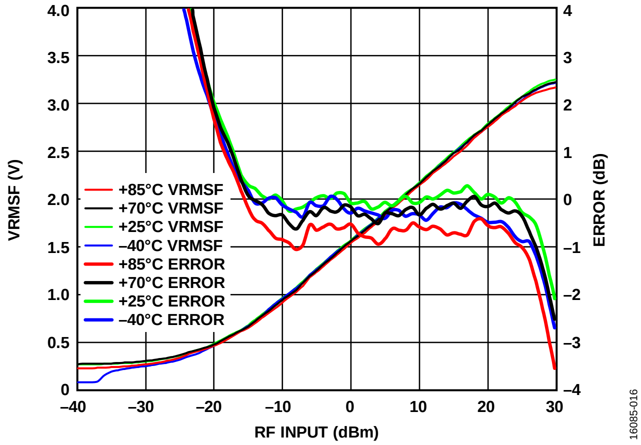

Figure 15. VRMSF and Error vs. RF Input and Temperature at 2 GHz, Error Calculated Using Linear Regression of Data Between +25 dBm and −15 dBm, TADJS = 0.2 V, TADJI = 0 V, CHPF+/CHPF− Open

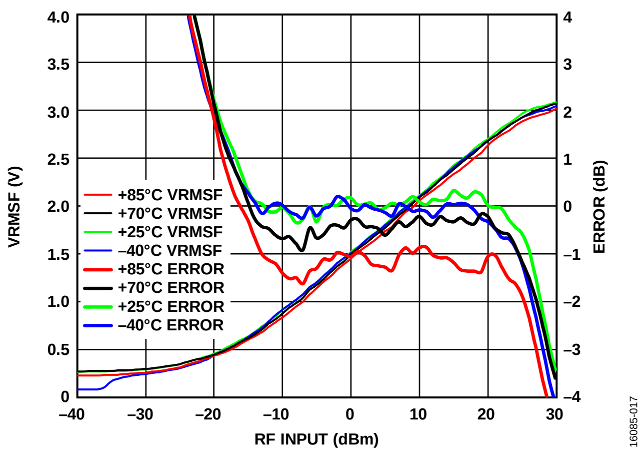

Figure 16. VRMSF and Error vs. RF Input and Temperature at 3 GHz, Error Calculated Using Linear Regression of Data Between +25 dBm and −15 dBm, TADJS = 0.2 V, TADJI = 0 V, CHPF+/CHPF− Open

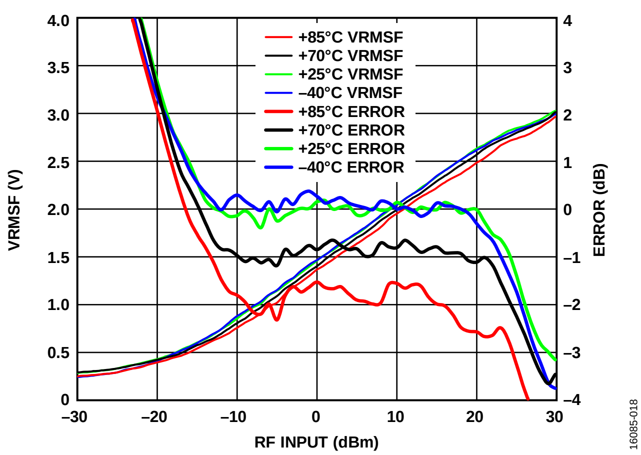

Figure 17. VRMSF and Error vs. RF Input Level and Temperature at 4 GHz, Error Calculated Using Linear Regression of Data Between +20 dBm and −15 dBm, TADJS = 0.2 V, TADJI = 0 V, CHPF+/CHPF− Open

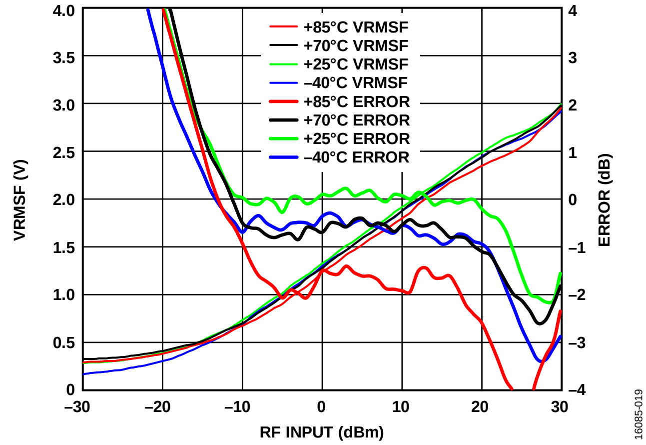

Figure 18. VRMSF and Error vs. RF Input Level and Temperature at 5 GHz, Error Calculated Using Linear Regression of Data Between 15 dBm and −10 dBm, TADJS = 0.2 V, TADJI = 0.2 V, CHPF+/CHPF− Open

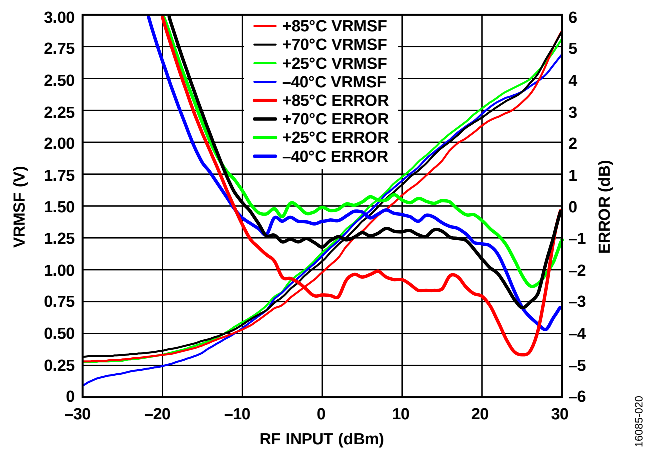

Figure 19. VRMSF and Error vs. RF Input Level and Temperature at 6 GHz, Error Calculated Using Linear Regression of Data Between 20 dBm and −5 dBm, TADJS = 0 V, TADJI = 0.2 V, CHPF+/CHPF− Open

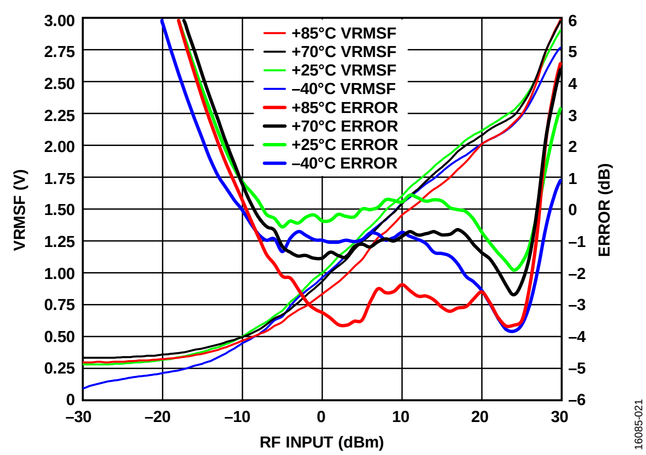

Figure 20. VRMSF and Error vs. RF Input and Temperature at 7 GHz, Error Calculated Using Linear Regression of Data Between 20 dBm and 0 dBm, TADJS = 0.8 V, TADJI = 0.2 V, CHPF+/CHPF− Open

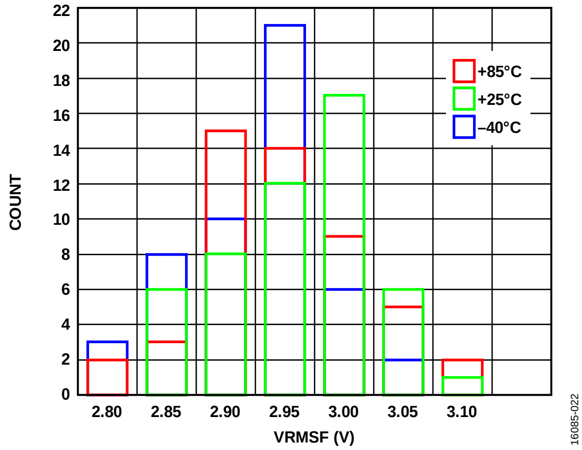

Figure 21. Distribution of VRMSF, P_{IN} = 20 dBm, 1 GHz

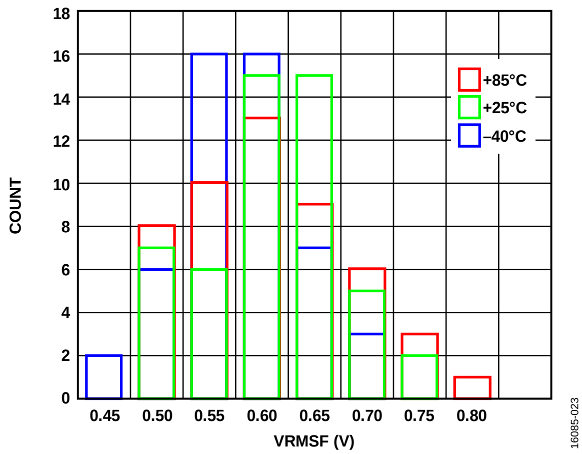

Figure 22. Distribution of VRMSF, P_{IN} = −20 dBm, 1 GHz

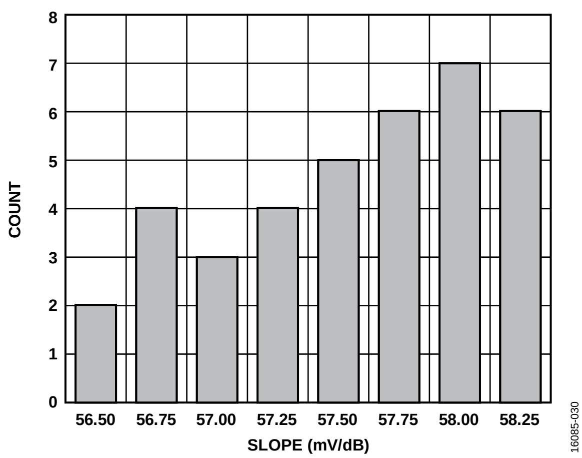

Figure 23. Distribution of Slope at 6 GHz

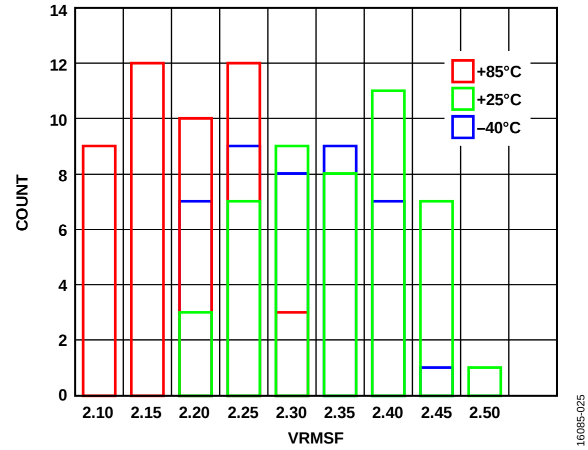

Figure 24. Distribution of VRMSF, P_{IN} = 20 dBm, 6 GHz

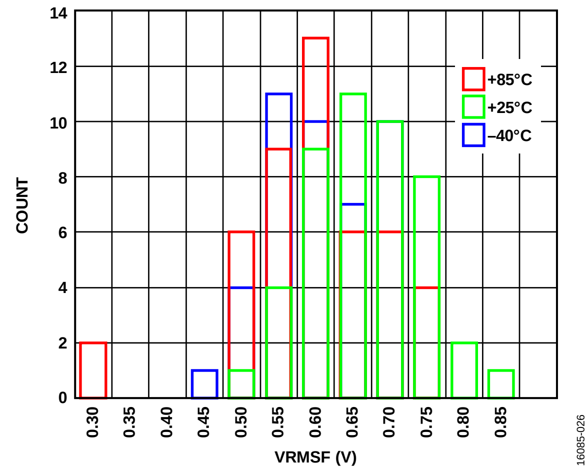

Figure 25. Distribution of VRMSF, P_{IN} = −10 dBm, 6 GHz

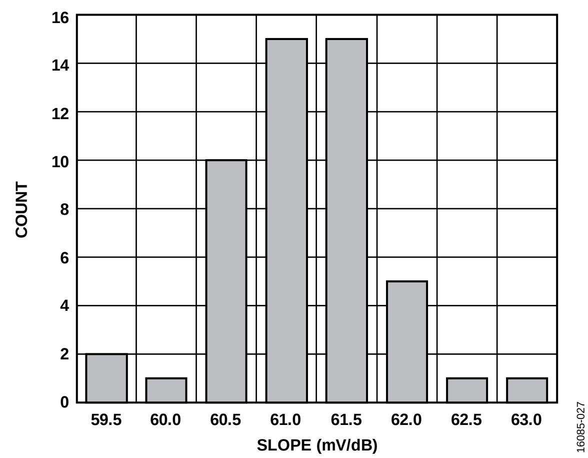

Figure 26. Distribution of Slope at 1 GHz

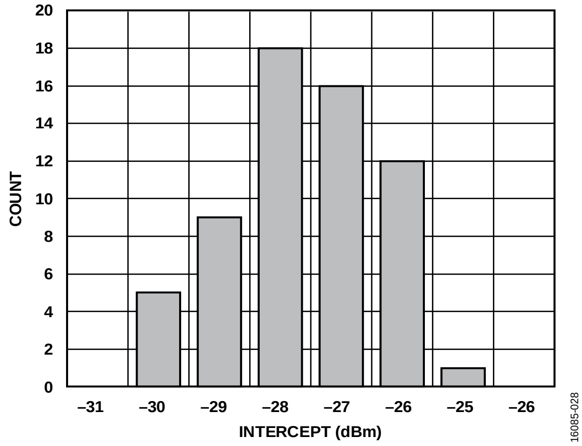

Figure 27. Distribution of Intercept at 1 GHz

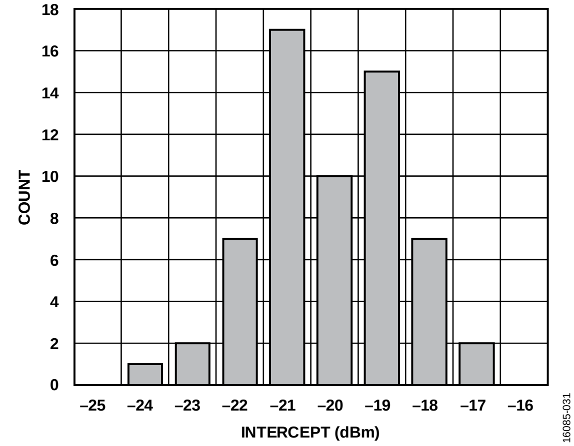

Figure 30. Distribution of Intercept at 6 GHz

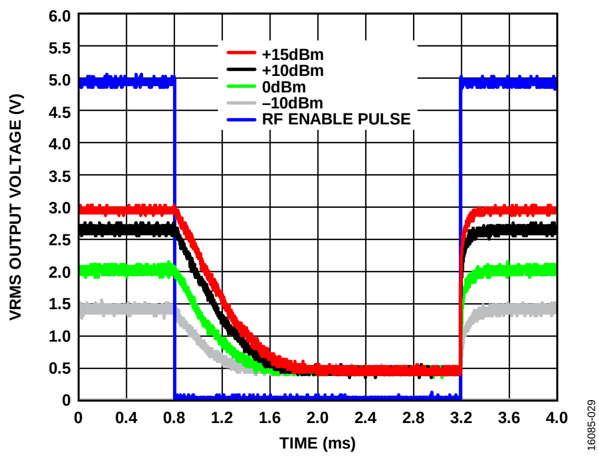

Figure 28. VRMSF Response to Various RF Input Burst Levels, Carrier Frequency = 1 GHz, CRMSF = 0.1 µF

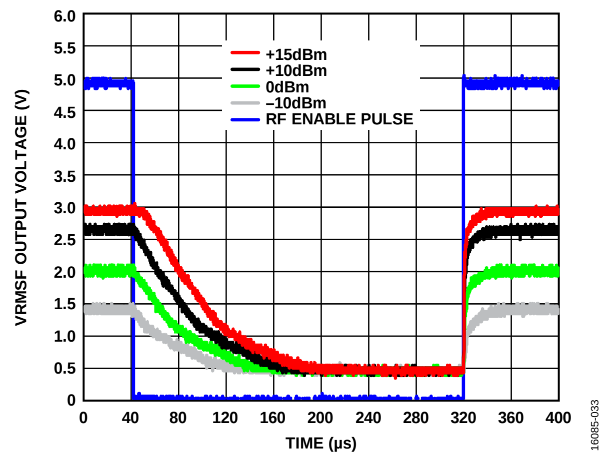

Figure 31. VRMSF Response to Various RF Input Burst Levels, Carrier Frequency = 1 GHz, CRMSF = 0.01 µF

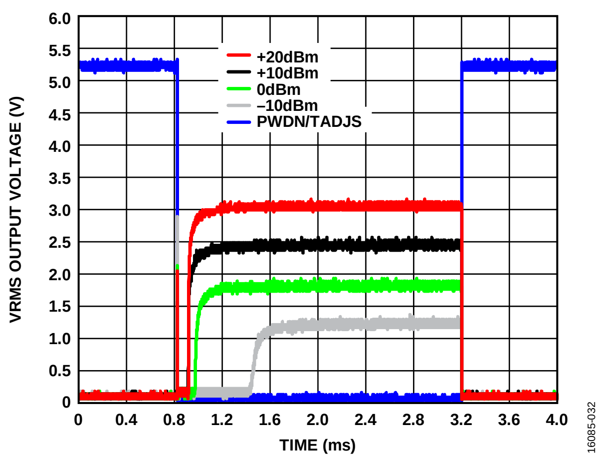

Figure 29. VRMSF Response to PWDN/TADJS for Various RF Input Levels, Carrier Frequency = 1 GHz, CRMSF = 0.1 µF

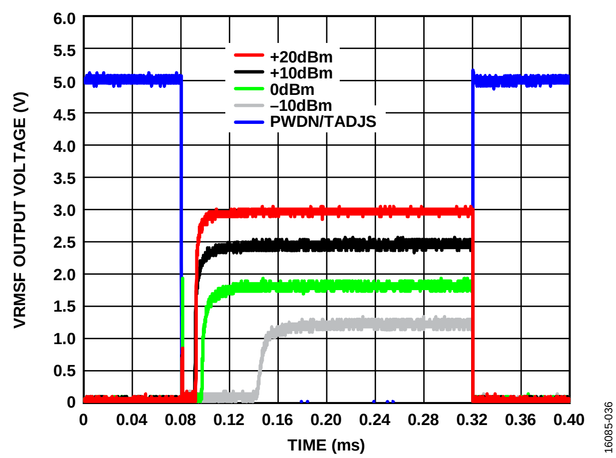

Figure 32. VRMSF Response to PWDN/TADJS for Various RF Input Levels, Carrier Frequency = 1 GHz, CRMSF = 0.01 µF

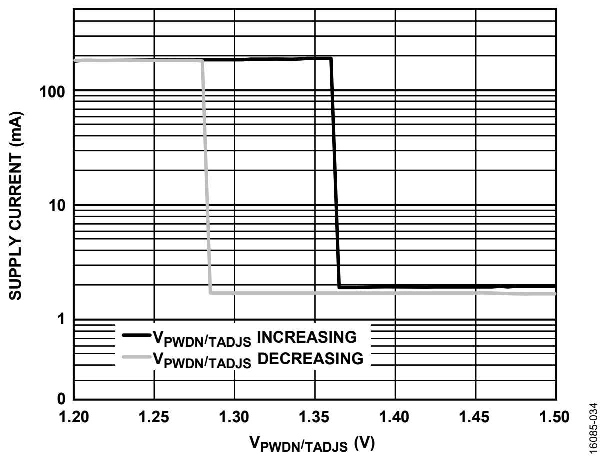

Figure 33. Supply Current vs. PWDN/TADJS Voltage ($V_{PWDN/TADJS}$)

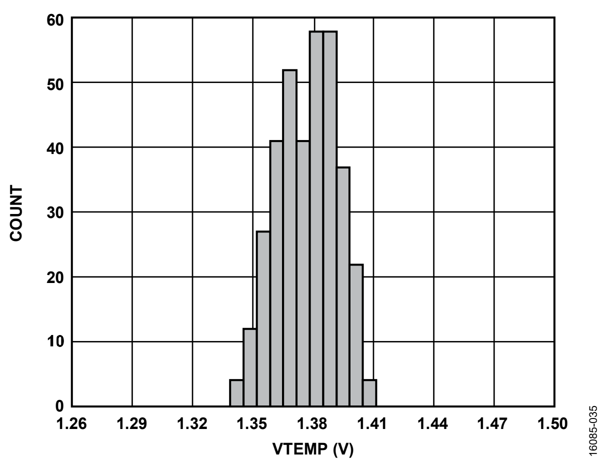

Figure 34. Distribution of VTEMP Voltage at T_A = 25°C, No RF Input

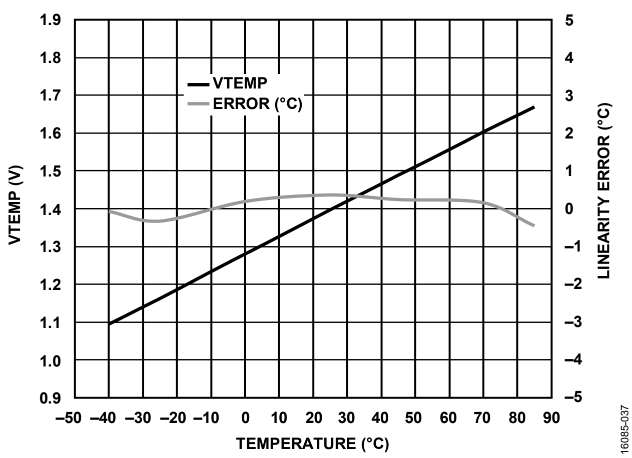

Figure 35. VTEMP and Linearity Error vs. Temperature

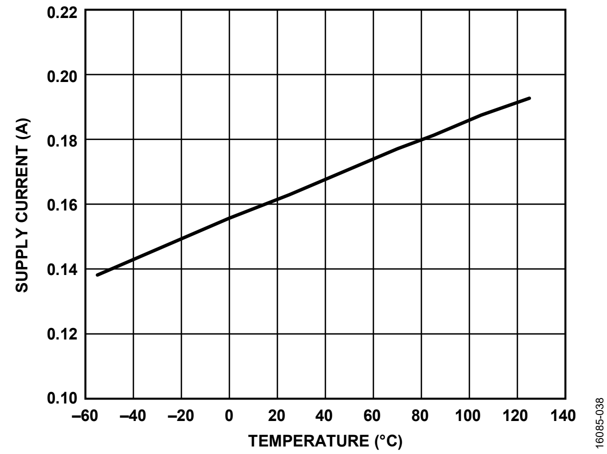

Figure 36. Supply Current vs. Temperature

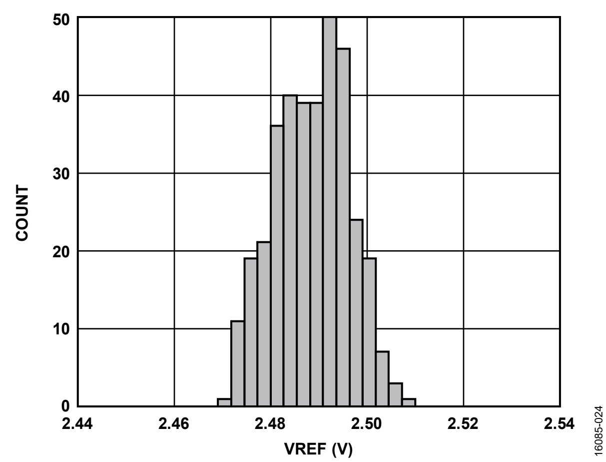

Figure 37. Distribution of VREF Voltage

THEORY OF OPERATION

The ADL5920 contains a symmetric and bidirectional resistive bridge plus two identical rms detectors that provide both forward and reverse power indications at the VRMSF and VRMSR pins, respectively. A detailed description of the theory of operation can be found in the Analog Dialogue article, An Integrated Bidirectional Bridge with Dual RMS Detectors for RF Power and Return Loss Measurement.

The device provides return loss and VSWR indication at the V_{DIFF+} and V_{DIFF-} outputs, where

$$V_{DIFF} = (V_{DIFF+}) - (V_{DIFF-}) = VRMSF - VRMSR \quad (1)$$

The bridge has an insertion loss (IL) of 0.9 dB below about 1 GHz when the source and load impedances are 50 Ω (the ADL5920 is only intended to be used in 50 Ω systems). The insertion loss increases with increasing frequency to 1.9 dB at 6 GHz. Note that insertion loss in dB is

$$IL = -20\log_{10}|S21| = -20\log_{10}|V_{RFOUT}/V_{RFIN}| \quad (2)$$

where:
V_{RFOUT} is the RFOUT voltage.
V_{RFIN} is the RFIN voltage.

As the source or load impedance deviates from 50 Ω, the VRMSF and VRMSR outputs indicate this deviation via a reduction in the separation of these two voltages. For example, with a fixed signal level applied to the RFIN port, as the load resistance on the RFOUT port varies from a short-circuit condition to an open circuit condition, only the VRMSR signal changes. The VRMSF output stays constant. The voltage difference indicates the return loss and reflection coefficient of the load and indicates the directivity of the structure when $R_{LOAD} = R_{SOURCE} = 50\ \Omega$.

The two rms detectors are architecturally similar to the ADL5906 but are internally dc-coupled to operate down to dc. The detectors provide linear in dB outputs and thereby give a direct indication in dBm of the applied forward and reverse signals. Due to their linear in dB response, the output voltages represent the coupled and isolated port voltages in dB and thereby their difference directly indicates directivity or return loss, which is an advantage over simple diode detectors that produce a linear in volt output. The detector slope of each detector output voltage vs. P_{IN} is approximately 60 mV/dB. Because both detectors are identical, the difference in output voltage with a perfectly matched source and load (50 Ω R_{SOURCE} and R_{LOAD}) is the directivity of the bidirectional bridge and is calculated as follows:

$$Directivity = ((VRMSF - VRMSR)/Slope)\ (\text{dB}) \quad (3)$$

Directivity is defined as follows:

$$Directivity\ (\text{dB}) = Coupling\ (\text{dB}) - Isolation\ (\text{dB}) = 20\log10(C/I) \quad (4)$$

Where the isolation (I) and coupling (C) factors are positive numbers, and isolation is a smaller value than C.

In the default, single-supply and ac-coupled connection (see Figure 38), the ADL5920 device directivity is greater than 30 dB for frequencies below 400 MHz, as shown in Figure 5, which shows as a constant difference voltage for the largest input powers. When the signal is applied to the RFIN port (by definition in the forward direction), the resulting V_{DIFF}, VRMSF − VRMSR, is approximately constant at frequencies less than 100 MHz. However, as the input signal level reduces, eventually, the rejected side limits at the noise and offset floor, and the VRMSR output stays constant while the VRMSF output keeps decreasing until this output also reaches the noise and offset floor. To determine the inherent directivity of the ADL5920 measurement system, apply a large enough input signal level to reliably determine the isolated port voltage, which is best achieved through a P_{IN} sweep of around 100 MHz.

APPLICATIONS INFORMATION

BASIC CONNECTIONS

For ac-coupled operation, the ADL5920 requires a single supply of 5 V. The supply is connected to the VPOS1, VPOS2, and VPOS3 supply pins. Decouple each of these pins using two capacitors with values equal or similar to those shown in Figure 38. Place these capacitors as close as possible to the VPOS pins.

The RF input and output pins are ac-coupled using broadband 0.01 µF capacitors, which allow operation down to approximately 600 kHz. Larger value capacitors can reduce the minimum input frequency further.

CHPR± AND CHPF± CAPACITORS

Each rms detector contains an offset compensation loop that eliminates internal offset voltages and ensures optimal detector sensitivity. The offset compensation loop works like a high-pass filter so that all input frequencies (and dc) below a certain corner frequency are nulled by the servo action of the loop. An internal 190 pF capacitor and an internal 2 kΩ resistor sets the nominal corner frequency of this loop. This configuration results in a high-pass corner frequency of approximately 400 kHz. For operation at a specific input frequency, the high-pass corner must be set two to three decades lower than this corner frequency. For example, for a minimum input frequency of 1 MHz, the high-pass corner frequency must be set to 1 kHz to ensure that the offset compensation loop does not interfere with the input signal being measured.

Capacitors connected between CHPF+ and CHPF− and between CHPR+ and CHPR− can reduce the corner frequency (f_{3dB}) of the offset compensation loops for each detector. The following equation sets the corner frequency of the offset compensation loop:

$$f_{3dB} = 1/(2\pi \times 2000 \times (190\text{ pF} + CHPx\pm)) \quad (5)$$

For example, setting the CHPx± capacitors values to 0.1 µF results in a high-pass corner of approximately 800 Hz, ensuring reliable operation for input frequencies down to 800 kHz.

At input frequencies above 2 GHz, the presence of capacitors or stray capacitance on the CHPx± nodes adversely affects directivity. As a result, it is recommended to leave these nodes open with no stray capacitance present for operation from 2 GHz to 7 GHz. For broadband operation (for example, from 1 MHz to 7 GHz), it is recommended to use 0201 size capacitors and to mount the capacitors as close the pins as possible.

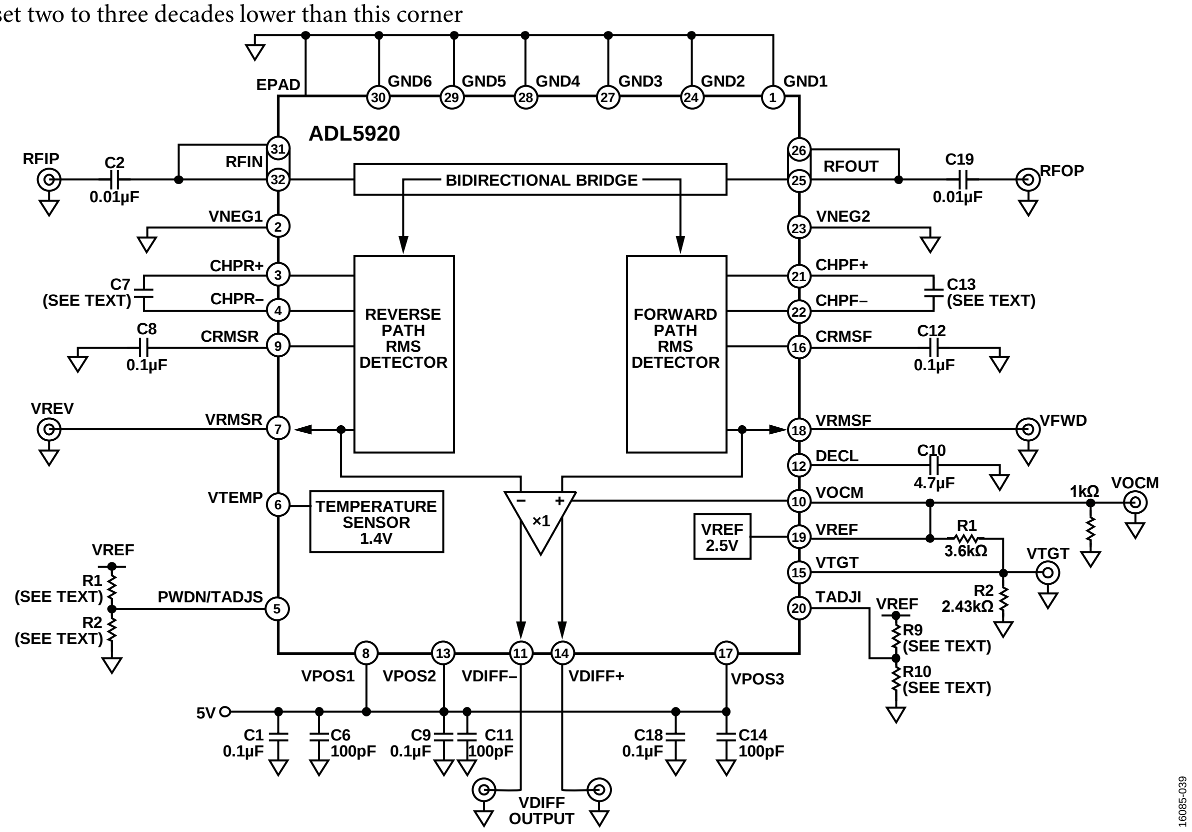

Figure 38. Basic Connections for Single-Supply AC-Coupled Operation

VREF INTERFACE

The VREF pin provides an internally generated voltage reference for the user. The VREF voltage is temperature stable and is capable of sourcing 4 mA and sinking 50 µA maximum. To provide additional current sink capability, connect an external resistor from VREF to GNDx. The voltage on this pin can drive the PWDN/TADJS, TADJI, VTGT, and VOCM pins.

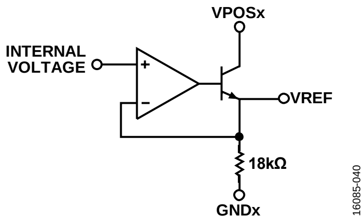

Figure 39. VREF Interface Simplified Schematic

V_{DIFF} OUTPUT INTERFACE

The ADL5920 contains a differential output stage (see Figure 40) that converts the detector output voltages of VRMSF and VRMSR to a differential voltage ($V_{DIFF+} − V_{DIFF−}$) with two differential amplifiers that each have a gain of one half. The differential gain from VRMSF minus VRMSR to $V_{DIFF+} − V_{DIFF−}$ is therefore equal to one, that is,

$$V_{DIFF+} - V_{DIFF-} = VRMSF - VRMSR \quad (6)$$

The VOCM pin sets the output common-mode voltage of V_{DIFF}. Because the difference voltage can be as large as 2 V to 2.5 V depending on directivity and frequency, VOCM must be high enough (at least 1.25 V for |VRMSF − VRMSR| = 2.5 V) such that the negative swinging output voltage is not limited at ground. A voltage of midsupply (2.5 V) is optimal for VOCM. The VOCM pin must be driven by a low impedance because the current flowing in and out of this pin can be up to ±2 mA, depending on the voltage applied to the VOCM pin and the voltages present on VRMSF and VRMSR. VOCM can connect directly to VREF. However, the connection must include a 1 kΩ resistor to ground, as shown in Figure 38.

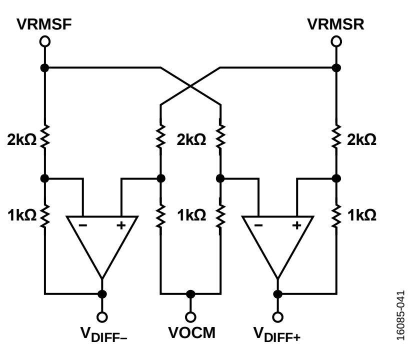

Figure 40. Differential Output Stage

TEMPERATURE DRIFT COMPENSATION

The TADJI and TADJS pins provide the option to optimize the temperature drift of the output voltages of ADL5920. The voltage on TADJI provides compensation of intercept temperature drift and the voltage on TADJS compensates for temperature drift of the slope.

Table 5 shows the recommended voltages for V_{TADJI} and V_{TADJS} to minimize temperature drift over the intended temperature range (−40°C < T_A < +85°C).

Table 5. Recommended V_{TADJI} and V_{TADJS} Values for Selected Frequencies

Frequency (GHz)	V_{TADJI} (V)	V_{TADJS} (V)
0.01	0	0
0.1	0	0
1	0	0
2	0	0.2
3	0	0.2
4	0	0.2
5	0.2	0.2
6	0.2	0
7	0.2	0.8

The TADI and TADJS pins have a high input impedance and can be conveniently driven from an external source or from an attenuated value of V_{REF} using a resistor divider.

SETTING VTGT

The voltage on the VTGT pin determines the settling point of internal automatic level control (ALC) loops that are part of the rms computation core. The recommended value for VTGT is 1 V, which represents a compromise between achieving excellent rms accuracy and maximizing dynamic range. The voltage on VTGT can be derived from the VREF pin using a resistor divider, as shown in Figure 38. Like the resistors chosen to set the voltage on TADJI and TADJS, the resistors setting VTGT must have reasonable values that do not pull too much current from VREF or cause bias current errors. In addition, note the combined current that VREF must deliver to generate the voltages on TADJI, TADJS and VTGT (which cannot exceed 4 mA).

CHOOSING VALUES FOR CRMSF AND CRMSR

CRMSF and CRMSR provide the averaging function for the rms computation in the forward path and reverse path rms detectors, respectively. Using the minimum value for these capacitances allows the quickest response time to a pulsed waveform but leaves significant output noise on the output voltage signal, especially with input signals that are modulated. Similarly, a large filter capacitor reduces output noise at the expense of response time.

In applications where response time is not critical, place a relatively large capacitor on the CRMSF and CRMSR pins. In Figure 38, a 0.1 μF capacitor was used on these pins. For most signal modulation schemes, this value ensures excellent rms measurement compliance and low residual output noise. There is no maximum capacitance limit for CRMSF and CRMSR.

Figure 41 shows how output noise varies with CRMSF when the ADL5920 is driven by a single-carrier W-CDMA signal (Test Model TM1-64, peak envelope power = 10.56 dB, bandwidth = 3.84 MHz). The response for the reverse path is identical.

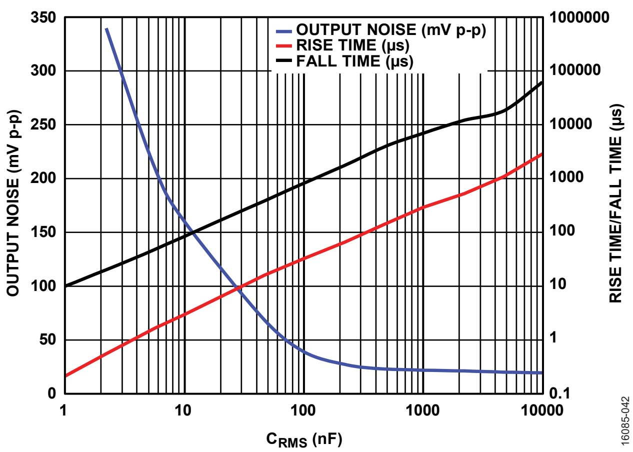

Figure 41. Output Noise, Rise and Fall Times vs. C_{RMS} Capacitance, Single-Carrier W-CDMA (TM1-64) at 2.14 GHz with P_{IN} = 0 dBm

Figure 41 also shows how the response time is affected by the value of CRMSF and CRMSR. To measure this response time, an RF burst at 2.14 GHz at 0 dBm is applied to the ADL5920. The 10% to 90% rise time and 90% to 10% fall time are then measured.

Table 6 shows the recommended minimum values of CRMSF and CRMSR for popular modulation schemes. Using lower capacitor values results in rms measurement errors. Output response time is also shown. If the output noise shown in Table 6 is too high, increase the CRMSF and CRMSR values to reduce the noise. However, increasing the CRMSF and CRMSR values results in slower rise and fall times.

The values in Table 6 are experimentally determined as the minimum capacitance that ensures achieving the specified rms accuracy for that particular signal type. This test is carried out by starting out with a large capacitance value on the CRMSF pin (for example, 10 μF). The VRMSF value is noted for a fixed input power level (for example, 10 dBm). The CRMSF value is then progressively reduced (with press down capacitors) until the value of VRMSF starts to deviate from its original value. This deviation indicates that the accuracy of the rms computation is degrading and that CRMSF is becoming too small).

In general, the minimum required rms averaging capacitance increases as the peak to average ratio of the carrier increases. The minimum required CRMSF and CRMSR values also tend to increase as the bandwidth of the carrier decreases. With narrow-band carriers, the noise spectrum of the VRMSF and VRMSR outputs tend to have a correspondingly narrow profile. The relatively narrow spectral profile demands larger CRMSF and CRMSR values to reduce the low-pass corner frequency of the averaging function and to ensure a valid rms computation.

Table 6. Recommended Minimum Capacitor Values on CRMSF and CRMSR for Various Modulation Schemes

Modulation/Standard	Peak Envelope Power Ratio (dB)	Carrier Bandwidth (MHz)	CRMSF and CRMSR (nF)	Output Noise (mV p-p)	Rise/Fall Time (μs)
QPSK, 5 MSPS (SQR COS Filter, α = 0.35)	3.8	5	1	84	0.2/10
QPSK ,15 MSPS (SQR COS Filter, α = 0.35)	3.8	15	1	42	0.2/10
64 QAM, 1 MSPS (SQR COS Filter, α = 0.35)	7.4	1	10	265	3/85
64 QAM, 5 MSPS (SQR COS Filter, α = 0.35)	7.4	5	1	380	0.2/10
64 QAM, 13 MSPS (SQR COS Filter, α = 0.35)	7.4	13	1	205	0.2/10
W-CDMA, One Carrier, TM1-64	10.56	3.84	1	820	0.2/10
W-CDMA Four Carrier, TM1-64, TM1-32, TM1-16, TM1-8	12.08	18.84	1	640	0.2/10
LTE, TM1, One Carrier, 20 MHz (2048 QPSK Subcarriers)	11.58	20	1	140	0.2/10

RF POWER AND RETURN LOSS CALCULATION

Figure 42 shows the voltage measured on VRMSF and VRMSR when RFIN is swept across its power range at various frequencies with a 50 Ω termination on RFOUT.

The VRMSR output ideally only responds to power reflected from the load. However, because of the finite directivity of the bridge circuit of the ADL5920, the VRMSR voltage starts to increase as the RF power at RFIN increases. Thereafter, the VRMSR voltage follows a similar linear in dB response as VRMSF, although at a much lower level. At a particular frequency, the difference in output voltage between VRMSF and VRMSR, where both voltages are following this linear in dB characteristic, is proportional to the directivity in dB of the bridge circuit when the load is 50 Ω. As frequency increases, the vertical difference between the VRMSF and VRMSR traces decreases, indicating a decrease in directivity.

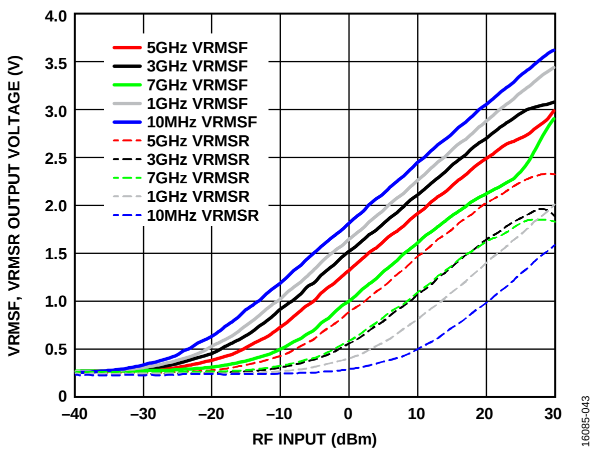

Figure 42. VRMSF, VRMSR Output Voltage vs. RF Input at Various Frequencies When Bridge Driven from RFIN and RFOUT Terminated with 50 Ω

Use the following equation to calculate the idealized output voltage on VRMSF ($V_{RMSF(IDEAL)}$):

$$V_{RMSF(IDEAL)} = Slope \times (P_{INF} - Intercept) \quad (7)$$

where:
Slope is the change in output voltage divided by the dB change in input power.
P_{INF} is the power level in dBm applied to the RFIN pin.
Intercept is the calculated input power level (in dBm) at which the output voltage is equal to 0 V. Note that *Intercept* is an extrapolated theoretical value, not a measured value.

The equation for $V_{RMSR(IDEAL)}$ is similar with the exception that P_{INR} substitutes in for P_{INF}.

$$V_{RMSR(IDEAL)} = Slope \times (P_{INR} - Intercept) \quad (8)$$

Where P_{INR} is the power level in dBm applied to the RFOUT pin with the RFIN pin terminated with 50 Ω.

Because slope and intercept vary from device to device and vs. frequency, calibration must be performed to achieve high accuracy.

In general, calibration is performed by applying two or more known signal levels (P_{IN1} and P_{IN2} in this case) to the input of the ADL5920 and measuring the corresponding output voltages (V_{RMSF1} and V_{RMSF2}). The calibration points must be within the linear operating range of the device.

With a two-point calibration, calculate the slope and intercept as follows:

$$Slope = (V_{RMSF1} - V_{RMSF2})/(P_{RFIN1} - P_{RFIN2}) \quad (9)$$

$$Intercept = P_{RFIN1} - (V_{RMSF1}/Slope) \quad (10)$$

After the slope and intercept are calculated and stored in nonvolatile memory during equipment calibration, use the following equation to calculate the unknown input power based on the output voltage of the detector:

$$P_{RFIN}\ (Unknown) = (V_{RMSF(MEASURED)}/Slope) + Intercept \quad (11)$$

Perform a separate calibration to establish the slope and intercept of the reverse path. Alternatively, because the forward and reverse path bridge circuits and rms detectors are matched closely, use the slope and intercept from the forward path calibration to convert the VRMSR voltage to the equivalent dBm RF power. Using this methodology, use the following equations to calculate forward power (P_{FWD}), reverse power (P_{REV}), and return loss.

$$P_{FWD}\ (\text{dBm}) = (VRMSF/Slope) + Intercept \quad (12)$$

$$P_{REV}\ (\text{dBm}) = (VRMSR/Slope) + Intercept \quad (13)$$

$$Return\ Loss\ (\text{dB}) = (P_{FWD} - P_{REV}) + Insertion\ Loss\ (\text{dB}) \quad (14)$$

Note that insertion loss has a negative sign for a passive load.

Return loss can also be calculated by using the V_{DIFF+} and V_{DIFF-} differential outputs.

$$Return\ Loss\ (\text{dB}) = (V_{DIFF+} - V_{DIFF-})/Slope + Insertion\ Loss\ (\text{dB}) \quad (15)$$

To calculate the directivity of the bridge circuit, place a 50 Ω load on RFOUT and measure V_{DIFF+} and V_{DIFF-}. Directivity in dB is then given by the following equation:

$$Directivity\ (\text{dB}) = (V_{DIFF+} - V_{DIFF-})/Slope \quad (16)$$

DC-COUPLED OPERATION

The ADL5920 RFIN and RFOUT pins can be dc-coupled as shown in Figure 43. However, to drive the inputs with signals that are biased at 0 V, apply a negative supply of −2.5 V to the two VNEG pins as shown in Figure 43. If dc-coupled operation is required for the sake of applying low input frequencies, connect capacitors to the CHPF and CHPR pins to reduce the corner frequency of the offset compensation loops as previously detailed. In addition, connect the DECL pin (Pin 12) to ground to ensure that the specified directivity is achieved at low frequencies.

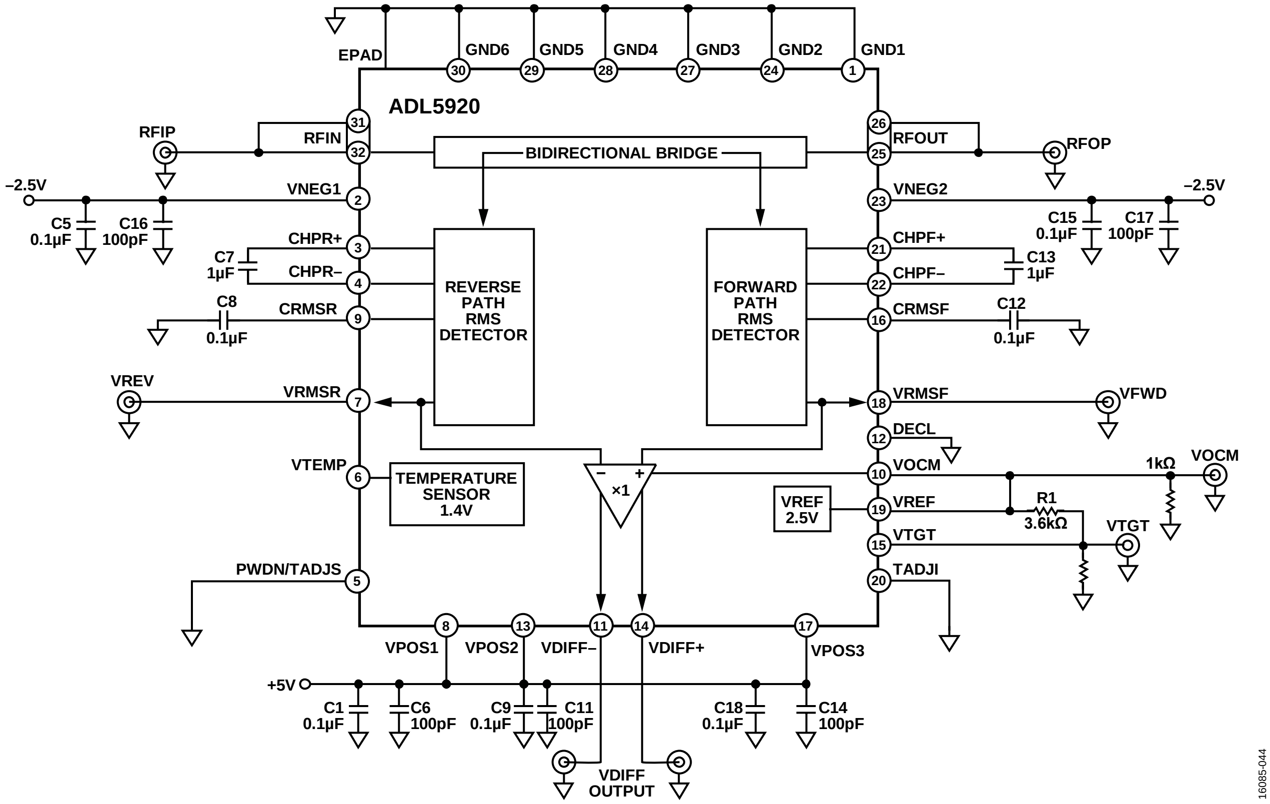

Figure 43. Basic Connections for DC-Coupled Operation

EVALUATION BOARD

The ADL5920-EVALZ is a fully populated, 4-layer, FR4-based evaluation board. For normal operation, the board requires a 5 V, 200 mA power supply. The 5 V power supply must be connected to the VPOS and GND test loops. The RF input and load must be applied to the RFIN and RFOUT 2.92 mm connectors, respectively (because the ADL5920 is fully bidirectional, the input signal can also be applied to RFOUT with the load on RFIN). The output voltages are available on the VRMSR, VRMSF, VDIFF+, and VDIFF− SMA connectors or on the adjacent test loops. Configuration options for the evaluation board are listed in Table 7. Note that an Arduino/Linduino based evaluation platform for the ADL5920 is also available (Part Number DC2847A-Kit). For more information, go to www.analog.com/ADL5920.

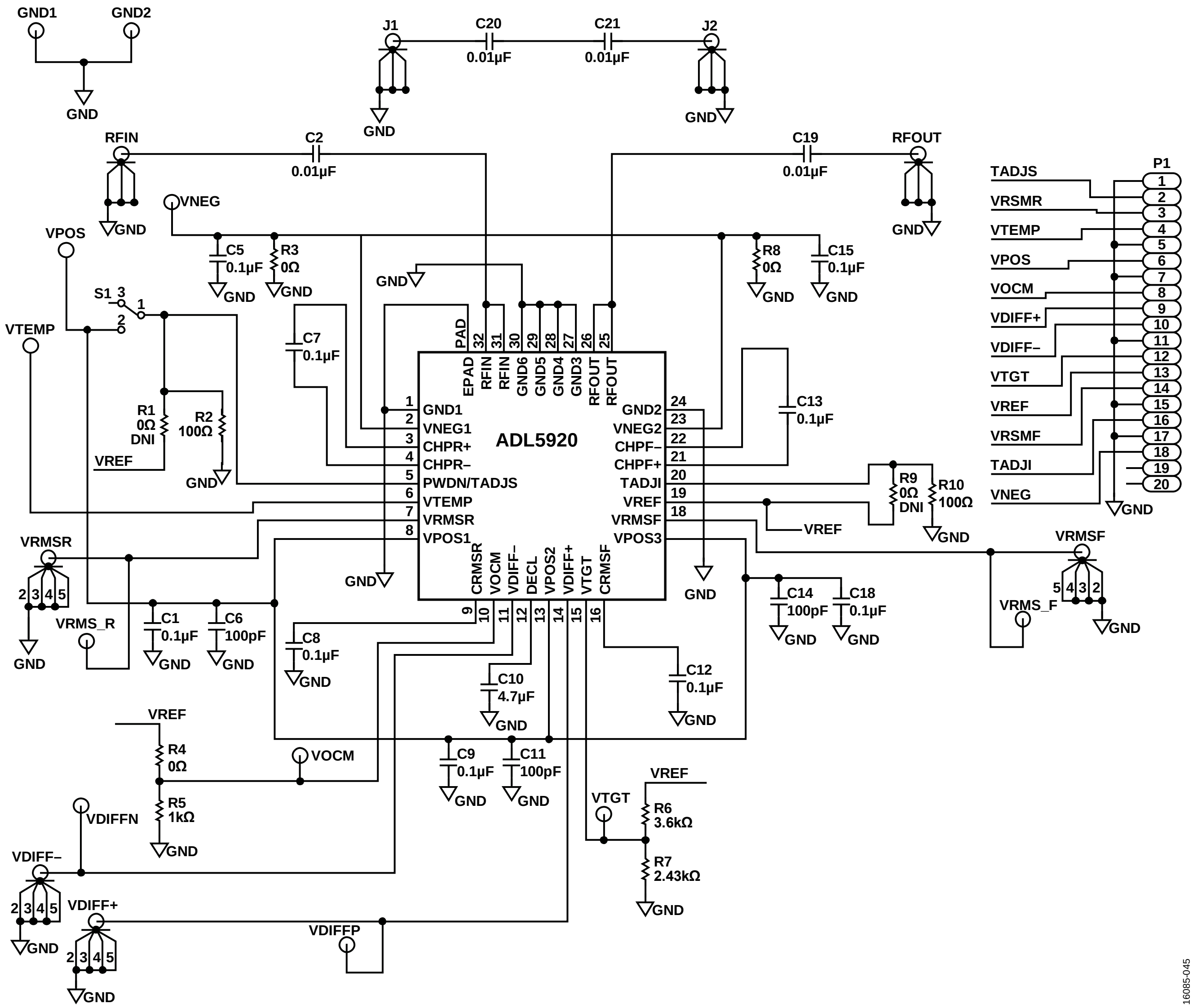

Figure 44. Evaluation Board Schematic

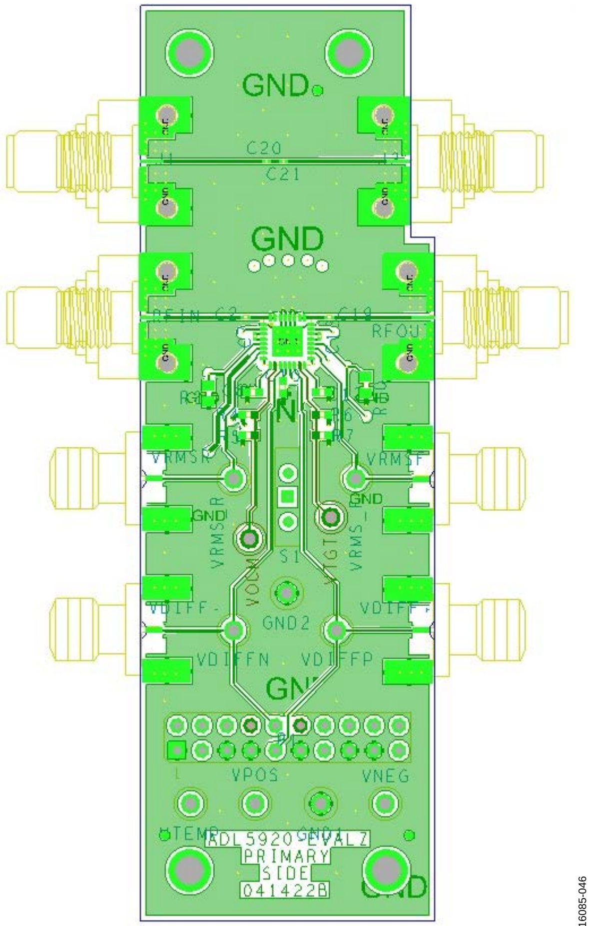

Figure 45. Evaluation Board Layout, Component Side

Table 7. Evaluation Board Configuration and Operation

Component	Function Description/Comments	Default Value
VPOS, GND1, GND2, C1, C6, C9, C11, C14, C18	Power supply interface and decoupling. Apply a 5 V power supply from the evaluation board to the VPOS and GND1/GND2 test loops (GND1 and GND2 are connected to a common ground). The nominal supply decoupling on the VPOS1, VPOS2, and VPOS3 pins consist of a 100 pF capacitor and a 0.1 µF capacitor on each power supply pin, with the 100 pF capacitor placed closer to the pin.	VPOS = 5 V, GND1 = GND2 = 0 V, C1, C9, C18 = 0.1 µF (0402), C6, C11, C14 = 100 pF (0402)
RFIN, RFOUT, C2, C19	RF inputs and outputs to bridge circuit. The main signal path is ac-coupled by 0.01 µF, 0201 capacitors, setting the input corner frequency to approximately 600 kHz. For operation at lower frequencies, larger capacitor values can be installed. The RFIN and RFOUT connectors are interchangeable, allowing the source signal driven into RFOUT with the load connected to RFIN. The RFIN and RFOUT connectors are 2.92 mm. Take care when attaching to these connectors because of mechanical fragility.	C2 = C19 = 0.01 µF (0201), RFIN, RFOUT = 2.92 mm end launch connector
J1, J2, C20, C21	Calibration path. This path can calibrate out the insertion loss of the RFIN and RFOUT traces. This signal path is ac-coupled by 0.01 µF, 0201 capacitors. The J1 and J2 connectors are 2.92 mm. Take care when connecting to these connectors because of mechanical fragility.	C20 = C21 = 0.01 µF (0201), J1, J2 = 2.92 mm end launch connector

Component	Function Description/Comments	Default Value
VNEG, C5, C15, R3, R8, C10	Negative supply. The main signal path from RFIN and RFOUT can be dc-coupled by connecting a −2.5 V supply to the VNEG test loop and replacing ac coupling capacitors, C2 and C19, with 0 Ω resistors. R3 and R8 must be removed and replaced with 100 pF capacitors pins. Connect the DECL pin to ground by removing C10 and replacing it with a 0 Ω resistor. In this mode, the voltage on VPOS must remain at 5 V.	VNEG = 0 V, R3 = R8 = 0 Ω (0603), C15 = C5 = 0.1 μF (0402), C10 = 4.7 μF (0402)
R6, R7	VTGT interface. R7 and R6 are driven from VREF (2.5 V) and provide 1 V to VTGT. If R6 and R7 are removed, an external voltage can be applied on the VTGT test point.	R7 = 2.43 kΩ, R6 = 3.6 kΩ, VTGT = 1 V
C7, C13	RMS detector offset compensation loop. The capacitances on these pins set the corner frequency of internal offset compensation loops of the two rms detectors. These loops limit the minimum input frequency that can be sensed by the ADL5920. The default values for these capacitors set minimum input frequencies that are well below the frequency corner set by the ac-coupling capacitors in the main signal path. These capacitors are deliberately located as close as possible to Pin 3 and Pin 4 and Pin 21 and Pin 22. To achieve the specified directivity when operating above 2 GHz, remove these capacitors (see Figure 5).	C7, C13 = 0.1 μF (0201)
S1, R1, R2, PWDN/TADJS	Device enable and slope temperature compensation. S1 is used to disable the ADL5920 by connecting the PWDN/TADJS pin to VPOS. In its other position, S1 is open and the voltage on PWDN/TADJS is set by VREF (2.5 V) and the R1, R2 resistor divider. This voltage is used to fine tune the temperature stability of the slope of the rms detectors.	S1 = open position, R1 = 0 Ω DNI, R2 = 100 Ω, PWDN/TADJS = 0 V
VTEMP	Temperature sensor output. This yellow test loop is connected directly to Pin 6 of the ADL5920 (VTEMP).	Not applicable
VRMSF, RMSR, VRMS_F, RMS_R	Reverse and forward rms voltage measurement. The voltages on these connectors are proportional to the dB power of the forward and reverse signals in the bridge circuit.	VRMSF, VRMSR = SMA end launch connector, VRMS_F, VRMS_R = yellow test loops
C8, C12	RMS averaging capacitors. The value of the rms averaging capacitor must be set based on the peak to average ratio of the input signal and based on the desired output response time and residual output noise on the rms detector outputs.	C8 = C12 = 0.1 μF (0402)
VOCM, R4, R5	Common-mode voltage for VDIFF+ and VDIFF−. The voltage on VOCM pin (Pin 10) sets the common-mode level for the VDIFF+ and VDIFF− differential pair. The nominal voltage on this pin must be 2.5 V. This input requires a bias current of ±1 mA and must be driven from a low impedance source. The nominal biasing method for VOCM is to connect it to VREF and connecting a 1 kΩ resistor from VOCM to ground. An external voltage can be applied VOCM through Pin 8 of the P1 connector.	R4 = 0 Ω (0402), R5 = 1 kΩ (0402), VOCM = 2.5 V
VDIFF+, VDIFF−, VDIFFN, VDIFFP	Return loss measurement. The output voltage from this differential pair is proportion to the ratio of the forward and reverse power in the bridge circuit. The common-mode level is set by the voltage on VOCM.	VDIFF+, VDIFF− = SMA end launch connector, VDIFFN, VDIFFP = yellow test loops
R9, R10, TADJI	TADJI interface. R9 and R10 set the voltage on the TADJI pin that is derived from VREF. This voltage is used to fine tune the temperature stability of the Intercept of the rms detectors.	R9 = 0 Ω DNI, R10 = 100 Ω (0402), TADJI = 0 V
P1	P1 header. The P1 header can access all of the dc levels on the evaluation board.	Not applicable

OUTLINE DIMENSIONS

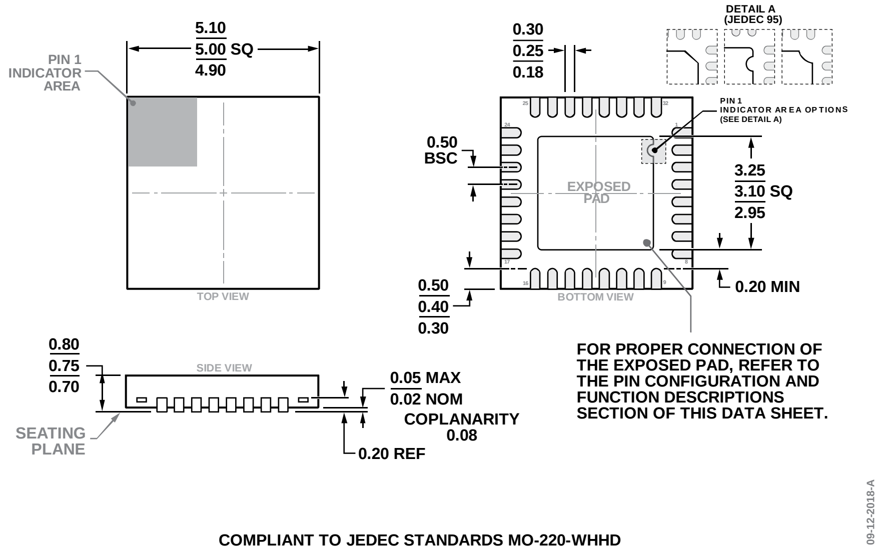

*Figure 46. 32-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm × 5 mm Body and 0.75 mm Package Height
(CP-32-7)
Dimensions shown in millimeters*

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Ordering Quantity
ADL5920ACPZ	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-7	490
ADL5920ACPZ-R2	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-7	250
ADL5920ACPZ-R7	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-7	1500
ADL5920-EVALZ		Evaluation Board with Voltage Outputs		
DC2847A-Kit		ADL5920 Linduino Demo Kit		

[1] Z = RoHS Compliant Part.

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