**Product data sheet** 

# 1. General description

Planar passivated sensitive gate four quadrant triac in a SOT54 (TO-92) plastic package intended for use in applications requiring direct interfacing to logic ICs and low power gate drivers.

## 2. Features and benefits

- Direct interfacing to logic level ICs
- · Direct interfacing to low power gate drive circuits
- · High blocking voltage capability
- · Planar passivated for voltage ruggedness and reliability
- Sensitive gate in four quadrants
- Triggering in all four quadrants

## 3. Applications

- General purpose low power motor control
- Home appliances
- · Industrial process control
- Low power AC Fan controllers

### 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$V_{DRM}$	repetitive peak off- state voltage		-	-	600	V
I <sub>T(RMS)</sub>	RMS on-state current	full sine wave; T <sub>lead</sub> ≤ 45 °C; <u>Fig. 1;</u> <u>Fig. 2; Fig. 3</u>	-	-	1	A
I <sub>TSM</sub>	non-repetitive peak on- state current	full sine wave; $T_{j(init)} = 25$ °C; $t_p = 20$ ms; Fig. 4; Fig. 5	-	-	8	Α
		full sine wave; $T_{j(init)}$ = 25 °C; $t_p$ = 16.7 ms	-	-	8.5	Α
Tj	junction temperature		-	-	125	°C
Static chara	acteristics					
I <sub>GT</sub>	gate trigger current	$V_D = 12 \text{ V; } I_T = 0.1 \text{ A; } T2+ G+;$ $T_j = 25 \text{ °C; } Fig. 7$	-	-	10	mA
		$V_D = 12 \text{ V; } I_T = 0.1 \text{ A; } T2 + G-;$ $T_j = 25 \text{ °C; } \frac{\text{Fig. 7}}{}$	-	-	10	mA
		V <sub>D</sub> = 12 V; I <sub>T</sub> = 0.1 A; T2- G-; T <sub>i</sub> = 25 °C; <u>Fig. 7</u>	-	-	10	mA

**4Q Triac** 

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
		V <sub>D</sub> = 12 V; I <sub>T</sub> = 0.1 A; T2- G+; T <sub>j</sub> = 25 °C; <u>Fig. 7</u>	-	-	10	mA
I <sub>H</sub>	holding current	V <sub>D</sub> = 12 V; T <sub>j</sub> = 25 °C; <u>Fig. 9</u>	-	-	10	mA
$V_{T}$	on-state voltage	I <sub>T</sub> = 1 A; T <sub>j</sub> = 25 °C; <u>Fig. 10</u>	-	1.3	1.6	V
Dynamic cha	racteristics					
dV <sub>D</sub> /dt	rate of rise of off-state voltage	$V_{DM}$ = 402 V; $T_j$ = 110 °C; ( $V_{DM}$ = 67% of $V_{DRM}$ ); exponential waveform; gate open circuit; Fig. 12	50	-	-	V/µs
dV <sub>com</sub> /dt	rate of change of commutating voltage	$V_D$ = 400 V; $T_j$ = 110 °C; $dI_{com}/dt$ = 0.44 A/ms; $I_T$ = 1 A; gate open circuit	2	-	-	V/µs

# 5. Pinning information

### **Table 2. Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T2	main terminal 2		T2
2	G	gate		G sym051
3	T1	main terminal 1	TO-92 (SOT54)	symosi

# 6. Ordering information

**Table 3. Ordering information** 

Type number		Package	ge				
		Name	Description	Version			
	Z0109MA	TO-92	plastic single-ended leaded (through hole) package; 3 leads	SOT54			

**4Q Triac** 

# 7. Limiting values

#### **Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DRM}$	repetitive peak off-state voltage		-	600	V
I <sub>T(RMS)</sub>	RMS on-state current	full sine wave; T <sub>lead</sub> ≤ 45 °C; <u>Fig. 1</u> ; <u>Fig. 2</u> ; <u>Fig. 3</u>	-	1	Α
I <sub>TSM</sub>	non-repetitive peak on- state current	full sine wave; $T_{j(init)}$ = 25 °C; $t_p$ = 20 ms; Fig. 4; Fig. 5	-	8	Α
		full sine wave; T <sub>j(init)</sub> = 25 °C; t <sub>p</sub> = 16.7 ms	-	8.5	Α
l <sup>2</sup> t	I <sup>2</sup> t for fusing	t <sub>p</sub> = 10 ms; SIN	-	0.32	A²s
dl <sub>T</sub> /dt	rate of rise of on-state	I <sub>G</sub> = 20 mA; T2+ G+	-	50	A/µs
	current	I <sub>G</sub> = 20 mA; T2+ G-	-	50	A/µs
		I <sub>G</sub> = 20 mA; T2- G-	-	50	A/µs
		I <sub>G</sub> = 20 mA; T2- G+	-	20	A/µs
I <sub>GM</sub>	peak gate current		-	1	Α
$P_{GM}$	peak gate power		-	2	W
P <sub>G(AV)</sub>	average gate power	over any 20 ms period	-	0.1	W
T <sub>stg</sub>	storage temperature		-40	150	°C
Tj	junction temperature		-	125	°C

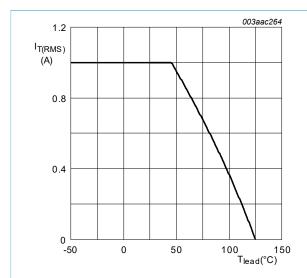


Fig. 1. RMS on-state current as a function of lead temperature; maximum values

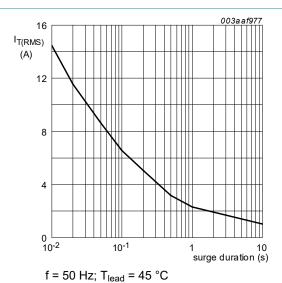


Fig. 2. RMS on-state current as a function of surge duration; maximum values

**4Q Triac** 

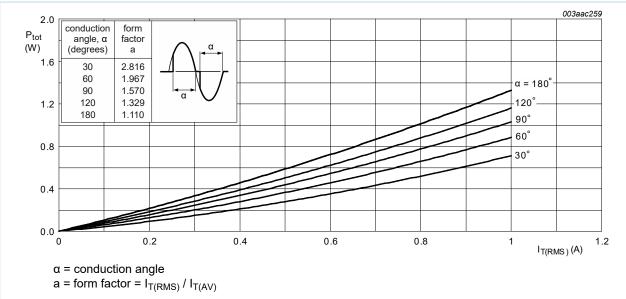


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

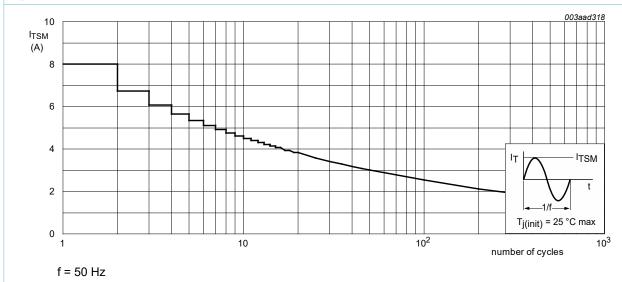
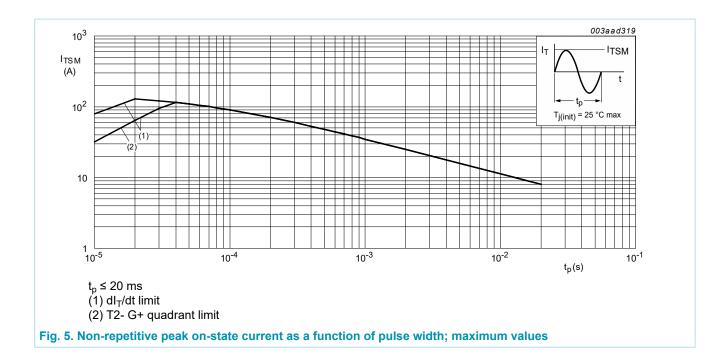


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

**4Q Triac** 



5 / 13

**4Q Triac** 

### 8. Thermal characteristics

**Table 5. Thermal characteristics** 

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R <sub>th(j-lead)</sub>	thermal resistance from junction to lead	full cycle; Fig. 6	-	-	60	K/W
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient free air	full cycle; printed-circuit board mounted; lead length = 4 mm	-	150	-	K/W

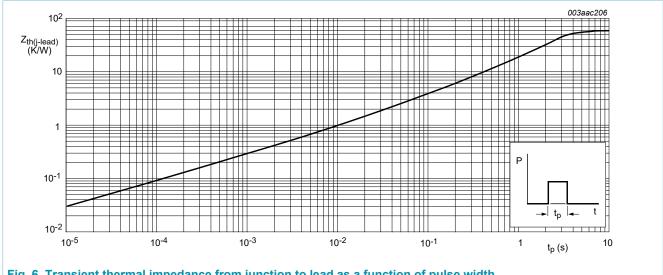


Fig. 6. Transient thermal impedance from junction to lead as a function of pulse width

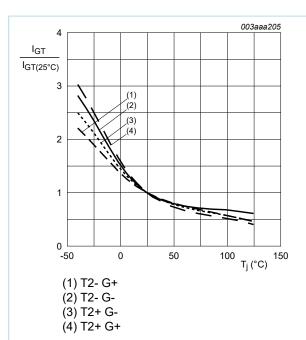
**4Q Triac** 

## 9. Characteristics

#### Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics		'			,
I <sub>GT</sub>	gate trigger current	$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T2+ G+;$ $T_j = 25 \text{ °C}; Fig. 7$	-	-	10	mA
		V <sub>D</sub> = 12 V; I <sub>T</sub> = 0.1 A; T2+ G-; T <sub>j</sub> = 25 °C; <u>Fig. 7</u>	-	-	10	mA
		V <sub>D</sub> = 12 V; I <sub>T</sub> = 0.1 A; T2- G-; T <sub>j</sub> = 25 °C; <u>Fig. 7</u>	-	-	10	mA
		V <sub>D</sub> = 12 V; I <sub>T</sub> = 0.1 A; T2- G+; T <sub>j</sub> = 25 °C; <u>Fig. 7</u>	-	-	10	mA
l <sub>L</sub>	latching current	V <sub>D</sub> = 12 V; I <sub>G</sub> = 0.1 A; T2+ G+; T <sub>j</sub> = 25 °C; <u>Fig. 8</u>	-	-	15	mA
		$V_D = 12 \text{ V}; I_G = 0.1 \text{ A}; T2+ G-;$ $T_j = 25 \text{ °C}; Fig. 8$	-	-	25	mA
		$V_D = 12 \text{ V}; I_G = 0.1 \text{ A}; T2- G-;$ $T_j = 25 \text{ °C}; Fig. 8$	-	-	15	mA
		$V_D = 12 \text{ V}; I_G = 0.1 \text{ A}; T2- G+;$ $T_j = 25 \text{ °C}; Fig. 8$	-	-	15	mA
I <sub>H</sub>	holding current	V <sub>D</sub> = 12 V; T <sub>j</sub> = 25 °C; <u>Fig. 9</u>	-	-	10	mA
V <sub>T</sub>	on-state voltage	I <sub>T</sub> = 1 A; T <sub>j</sub> = 25 °C; <u>Fig. 10</u>	-	1.3	1.6	V
V <sub>GT</sub>	gate trigger voltage	V <sub>D</sub> = 12 V; I <sub>T</sub> = 0.1 A; T <sub>j</sub> = 25 °C	-	-	1	V
		V <sub>D</sub> = 600 V; I <sub>T</sub> = 0.1 A; T <sub>j</sub> = 125 °C; Fig. 11	0.2	-	-	V
I <sub>D</sub>	off-state current	V <sub>D</sub> = 600 V; T <sub>j</sub> = 125 °C	-	-	0.5	mA
Dynamic ch	naracteristics					
dV <sub>D</sub> /dt	rate of rise of off-state voltage	$V_{DM}$ = 402 V; $T_j$ = 110 °C; ( $V_{DM}$ = 67% of $V_{DRM}$ ); exponential waveform; gate open circuit; Fig. 12	50	-	-	V/µs
dV <sub>com</sub> /dt	rate of change of commutating voltage	$V_D$ = 400 V; $T_j$ = 110 °C; $dI_{com}$ / dt = 0.44 A/ms; $I_T$ = 1 A; gate open circuit	2	-	-	V/µs

**4Q Triac** 



003aaa203 3 I<sub>L(25°C)</sub> 2 0 -50 0 50 100 150 T<sub>i</sub> (°C)

Fig. 8. Normalized latching current as a function of junction temperature

Fig. 7. Normalized gate trigger current as a function of junction temperature

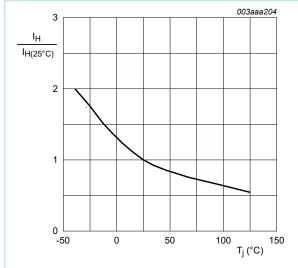
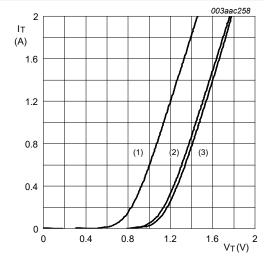


Fig. 9. Normalized holding current as a function of junction temperature



 $V_0 = 1.13 \text{ V}$  $R_s = 0.31 \Omega$ 

(1)  $T_j$  = 125 °C; typical values (2)  $T_j$  = 125 °C; maximum values

(3) T<sub>i</sub> = 25 °C; maximum values

Fig. 10. On-state current as a function of on-state voltage

**4Q Triac** 

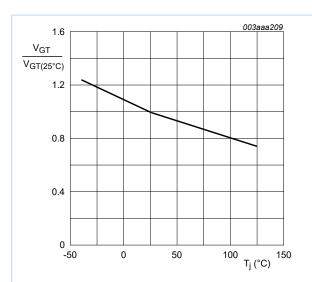


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

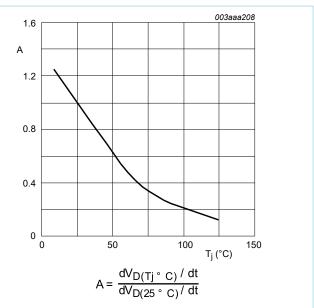
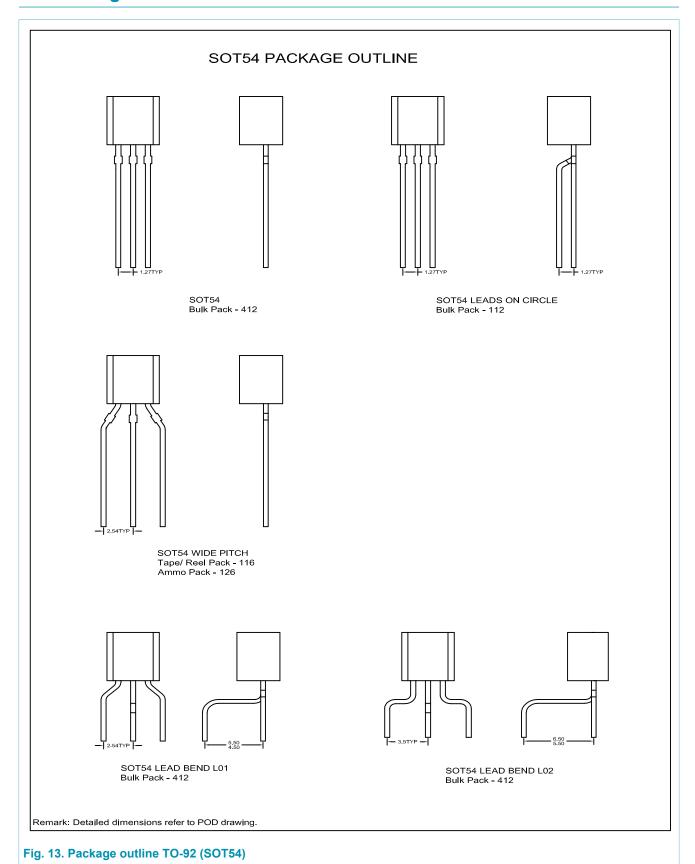


Fig. 12. Normalized critical rate of rise of off-state voltage as a function of junction temperature; typical values

9 / 13

# 10. Package outline



**4Q Triac** 

## 11. Legal information

#### **Data sheet status**

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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**4Q Triac** 

## 12. Contents

1.	General description	1
2.	Features and benefits	1
3.	Applications	1
4.	Quick reference data	1
5.	Pinning information	2
6.	Ordering information	2
7.	Limiting values	3
8.	Thermal characteristics	<del>6</del>
9.	Characteristics	7
10.	. Package outline	10
11.	Legal information	11

For more information, please visit: http://www.ween-semi.com
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