Intelligent Power Module (IPM)

600 V, 15 A

STK531U394C-E

The STK531U394C−E is a fully−integrated inverter power stage consisting of a high−voltage driver, six IGBT's and a thermistor, suitable for driving permanent magnet synchronous (PMSM) motors, brushless−DC (BLDC) motors and AC asynchronous motors. The IGBT's are configured in a 3−phase bridge with separate emitter connections for the lower legs for maximum flexibility in the choice of control algorithm.

The power stage has a full range of protection functions including cross−conduction protection, external shutdown and under−voltage lockout functions. Output stage uses IGBT/FRD technology and implements Under Voltage Protection (UVP) and Over Current Protection (OCP: Shunt Resistor internal) with a Fault Detection output flag. Internal Boost diodes are provided for high side gate boost drive.

Features

- Three−phase 15 A / 600 V IGBT Module with Integrated Drivers
- Typical Values (Upper Side at 15 A) : $V_{CE}(sat)$ = 1.8 V, V_F = 2.0 V
- 44.0 mm × 26.5 mm Single In−line Package with Vertical LF Type
- Cross−conduction Protection
- Adjustable Over−current Protection Level
- Integrated Bootstrap Diodes and Resistors
- These Devices are Pb−Free and are RoHS Compliant

Certification

- UL1557 (File number : E339285)

Typical Applications

- Industrial Pumps
- Industrial Fans
- Industrial Automation
- Heat Pumps, Home Appliances

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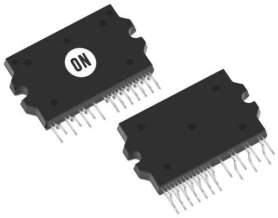


SIP29 44x26.5
CASE 127ET

MARKING DIAGRAM

STK531U394C = Specific Device Code
A = Year
B = Month
C = Production Site
DD = Factory Lot code
Device marking is on package underside

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.

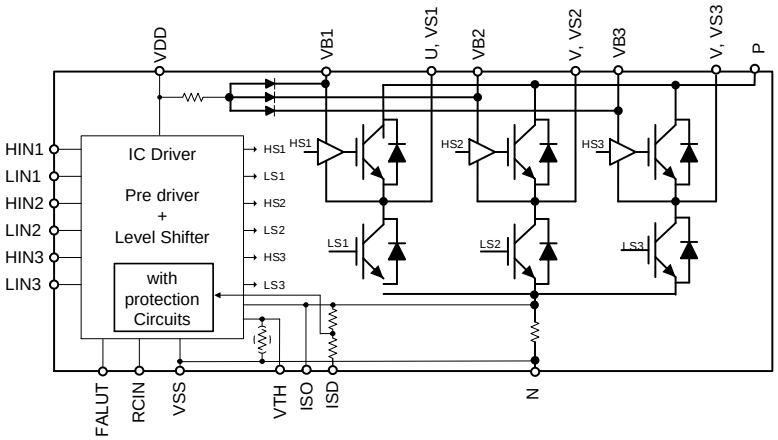


Figure 1. Functional Diagram

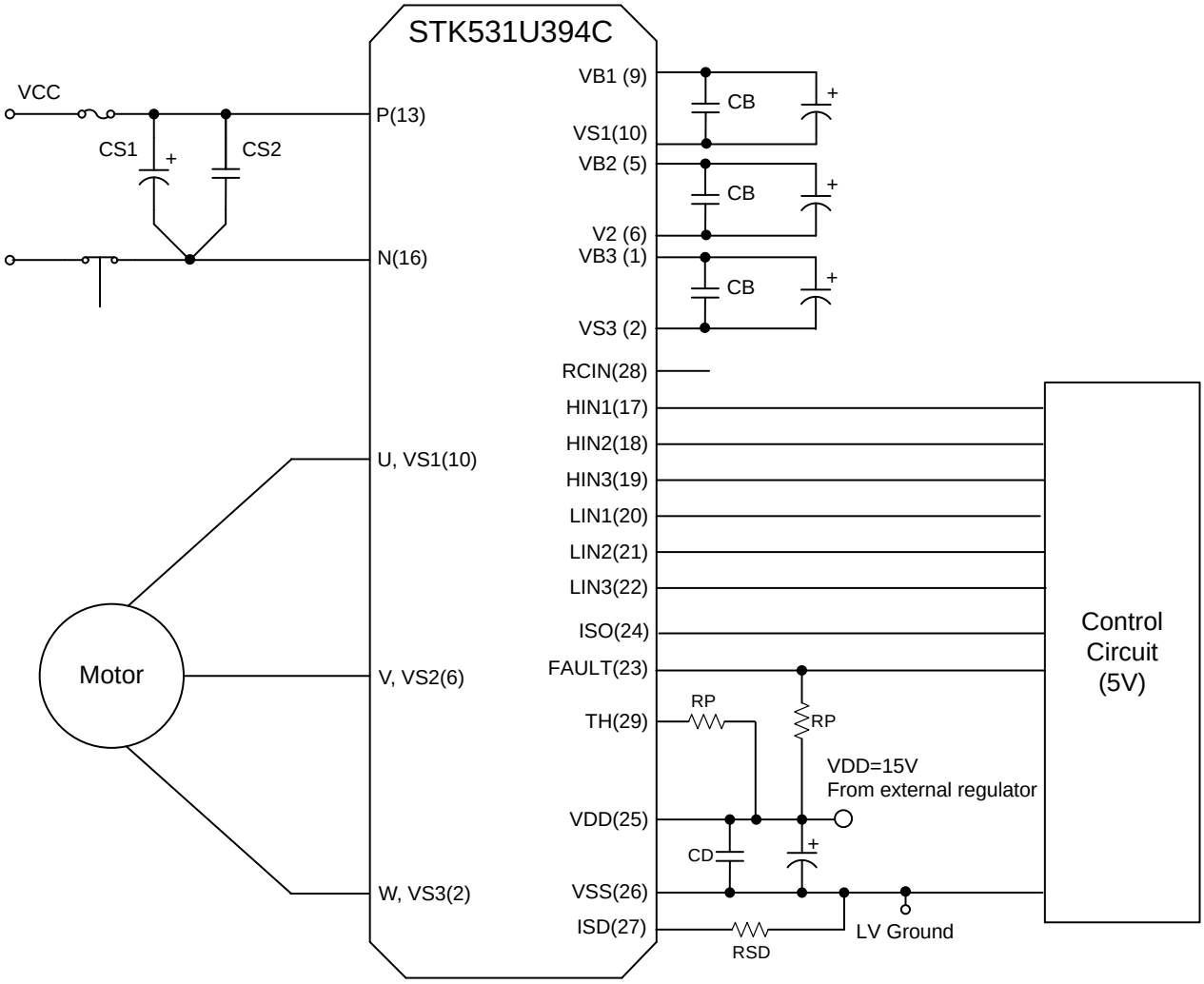


Figure 2. Application Schematic

Usage Precaution

1. It is essential that wiring length between terminals in the snubber circuit be kept as short as possible to reduce the effect of surge voltages. Recommended value of “CS” is in the range of 0.1 to 10 μF.
2. “ISO” (pin24) is terminal for current monitor. High current may flow into that course when short−circuiting the “ISO” terminal and “VSS” terminal. Please do not connect them.
3. Inside the IPM, a thermistor used as the temperature monitor for internal substrate is connected between VSS terminal and TH terminal therefore, an external pull up resistor connected between the TH terminal and an external power supply should be used.
   The temperature monitor example application is as follows, please refer the Fig.5, and Fig.6 below.
4. Pull down resistor of 33 kΩ is provided internally at the signal input terminals. An external resistor of 2.2 k to 3.3 kΩ should be added to reduce the influence of external wiring noise.
5. The level of the over current protection might be changed from IPM design value when “ISD” terminal and “VSS” terminal are shorted at external. Be confirm with actual application (“N” terminal and “VSS” terminal are shorted at internal).
6. The level of the over current protection is adjustable with the external resistor “RSD” between “ISD” terminal and “VSS” terminal.

This data shows the example of the application circuit, does not guarantee a design as the mass production set.

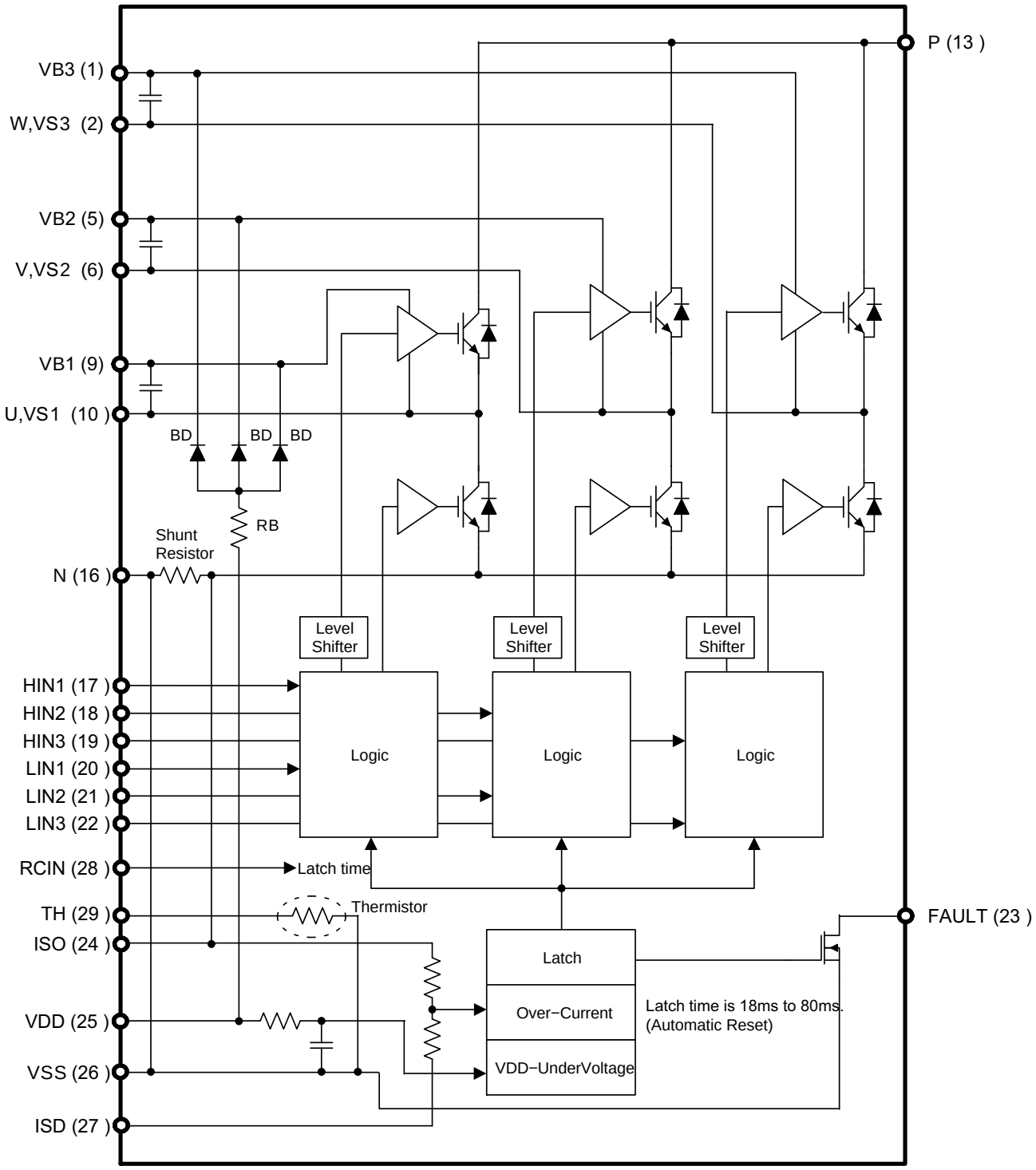


Figure 3. Simplified Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin	Name	Description
1	VB3	High Side Floating Supply Voltage 3
2	W, VS3	Output 3 − High Side Floating Supply Offset Voltage
5	VB2	High Side Floating Supply voltage 2
6	V,VS2	Output 2 − High Side Floating Supply Offset Voltage

Table 1. PIN FUNCTION DESCRIPTION (continued)

Pin	Name	Description
9	VB1	High Side Floating Supply voltage 1
10	U,VS1	Output 1 − High Side Floating Supply Offset Voltage
13	P	Positive Bus Input Voltage
16	N	Negative Bus Input Voltage
17	HIN1	Logic Input High Side Gate Driver − Phase U
18	HIN2	Logic Input High Side Gate Driver − Phase V
19	HIN3	Logic Input High Side Gate Driver − Phase W
20	LIN1	Logic Input Low Side Gate Driver − Phase U
21	LIN2	Logic Input Low Side Gate Driver − Phase V
22	LIN3	Logic Input Low Side Gate Driver − Phase W
23	FAULT	Fault output
24	ISO	Current monitor output
25	VDD	+15V Main Supply
26	VSS	Negative Main Supply
27	ISD	Over current detection and setting
28	RCIN	Fault clear time setting output
29	TH	Thermistor output

NOTE: Pins 3, 4, 7, 8, 11, 12, 14, 15 are not present.

Table 2. ABSOLUTE MAXIMUM RATINGS at T_C = 25°C (Note 1)

Rating	Symbol	Conditions	Value	Unit
Supply voltage	V_{CC}	P to N, surge < 500 V (Note 2)	450	V
Collector−emitter voltage	V_{CE}	P to U,V,W or U, V, W, to N	600	V
Output current	Io	P, N, U, V, W terminal current	±15	A
		P, N, U, V, W terminal current at Tc = 100°C	±7	A
Output peak current	Iop	P, N, U, V, W terminal current, PW=1ms	±30	A
Pre−driver supply voltages	VD1,2,3,4	VB1 to U, VB2 to V, VB3 to W, V_{DD} to V_{SS} (Note 3)	+20	V
Input signal voltage	VIN	HIN1, 2, 3, LIN1, 2, 3	−0.3 to V_{DD}	V
FAULT terminal voltage	VFAULT	FAULT terminal	−0.3 to V_{DD}	V
Maximum power dissipation	Pd	IGBT per 1 channel	35	W
Junction temperature	Tj	IGBT, FRD	150	°C
Storage temperature	Tstg		−40 to +125	°C
Operating case temperature	Tc	IPM case temperature	−20 to +100	°C
Package mounting torque		Case mounting screw	0.9	Nm
Isolation voltage	Vis	50 Hz sine wave AC 1 minute (Note 4)	2000	Vrms

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters
2. This surge voltage developed by the switching operation due to the wiring inductance between P and N terminals.
3. VD1=VB1 to U, VD2 = VB2 to V, VD3 = VB3 to W, VD4 = VDD to VSS terminal voltage.
4. Test conditions: AC 2500 V, 1 s.

Table 3. RECOMMENDED OPERATING RANGES (Note 5)

Rating	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{CC}	P to N	0	280	450	V
Pre−driver supply voltage	VD1, 2, 3	VB1 to U, VB2 to V, VB3 to W	12.5	15	17.5	V
	VD4	V_{DD} to V_{SS} (Note 5)	13.5	15	16.5	V
PWM frequency	f_{PWM}		1	−	20	kHz
Dead time	DT	Turn−off to turn−on (external)	2	−	−	μs
Allowable input pulse width	PWIN	ON and OFF	1	−	−	μs
Package mounting torque		'M3' type screw	0.6	−	0.9	Nm

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

5. Pre−drive power supply (VD4 = 15 ±1.5 V) must have the capacity of Io = 20 mA (DC), 0.5 A (Peak).

Table 4. ELECTRICAL CHARACTERISTICS at Tc = 25°C, VD1, VD2, VD3, VD4 = 15 V

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
Power Output Section							
Collector−emitter leakage current	V_{CE} = 600 V		I_{CE}	−	−	100	μA
Bootstrap diode reverse current	VR(BD) = 600 V		IR(BD)	−	−	100	μA
Collector to emitter saturation voltage	Ic = 15 A, Tj = 25°C	Upper side	V_{CE}(sat)	−	1.8	2.3	V
		Lower side (Note 6)		−	2.2	2.7	V
	Ic = 7 A, Tj = 100°C	Upper side		−	1.5	–	V
		Lower side (Note 6)		−	1.7	–	V
Diode forward voltage	IF = 15 A, Tj = 25°C	Upper side	VF	−	2.0	3.2	V
		Lower side (Note 6)		−	2.2	3.4	V
	IF = 7 A, Tj = 100°C	Upper side		−	1.6	–	V
		Lower side (Note 6)		−	1.8	–	V
Junction to case thermal resistance	IGBT		θj−c(T)	–	–	3.8	°C/W
	FRD		θj−c(D)	–	–	6.0	
Switching time	Io = 15 A, V_{CC} = 300 V, L = 3.9 mH,		t_{ON}	0.3	0.5	1.2	μs
			t_{OFF}	–	0.6	1.5	μs
Turn−on switching loss	Io = 7 A, V_{CC} = 300 V, L = 3.9 mH		E_{ON}	–	160	–	μJ
Turn−off switching loss			E_{OFF}	–	200	–	μJ
Total switching loss			E_{TOT}	–	360	–	μJ
Turn−on switching loss	Io = 7 A, V_{CC} = 300 V, Tc = 100°C		E_{ON}	–	200	–	μJ
Turn−off switching loss			E_{OFF}	–	250	–	μJ
Total switching loss			E_{TOT}	–	450	–	μJ
Diode reverse recovery energy	Io = 7 A, V_{CC} = 400 V, TC = 100°C (di/dt set by internal driver)		E_{REC}	–	25	–	μJ
Diode reverse recovery time			trr	–	80	–	ns
Reverse bias safe operating area	Io = 30 A, V_{CE} = 450 V		RBSOA	Full Square			
Short circuit safe operating area	V_{CE} = 400 V, Tc = 100°C		SCSOA	4	–	–	μs
Driver Section							
Pre−driver consumption current	VD1,2,3 = 15 V (Note 4)		ID	–	0.08	0.4	mA
	VD4 = 15 V			–	1.6	4.0	mA
High level Input voltage	HIN1, HIN2, HIN3, LIN1, LIN2, LIN3 to VSS		Vin H	2.5	–	–	V
Low level Input voltage			Vin L	–	–	0.8	V
Input threshold voltage hysteresis (Note 7)			Vinth(hys)	0.5	0.8	−	V

Table 4. ELECTRICAL CHARACTERISTICS at Tc = 25°C, VD1, VD2, VD3, VD4 = 15 V (continued)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Logic 1 input current	VIN = +3.3 V	I_{IN+}	–	100	143	μA
Logic 0 input current	VIN = 0 V	I_{IN-}	–	–	2	μA
FAULT terminal sink current	FAULT : ON / VFAULT = 0.1 V	IoSD	–	2	–	mA
FAULT clearance delay time	Fault output latch time	FLTCLR	18	–	80	ms
VCC and VS undervoltage positive going threshold		V_{CCUV+} V_{SUV+}	10.5	11.1	11.7	V
VCC and VS undervoltage negative going threshold		V_{CCUV-} V_{SUV-}	10.3	10.9	11.5	V
VCC and VS undervoltage hysteresis		V_{CCUVH} V_{SUVH-}	0.14	0.2	−	V
Over current protection level	PW=100 μs, RSD = 0 Ω	ISD	22.0	−	27.8	A
Electric current output signal level	Io = 15 A	ISO	0.36	0.38	0.40	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. The lower side's VCE(SAT) and VF include a loss by the shunt resistance.
7. Input threshold voltage hysteresis indicates a reference value based on the design value of built−in pre−driver IC.

APPLICATIONS INFORMATION

Input / Output Timing Chart

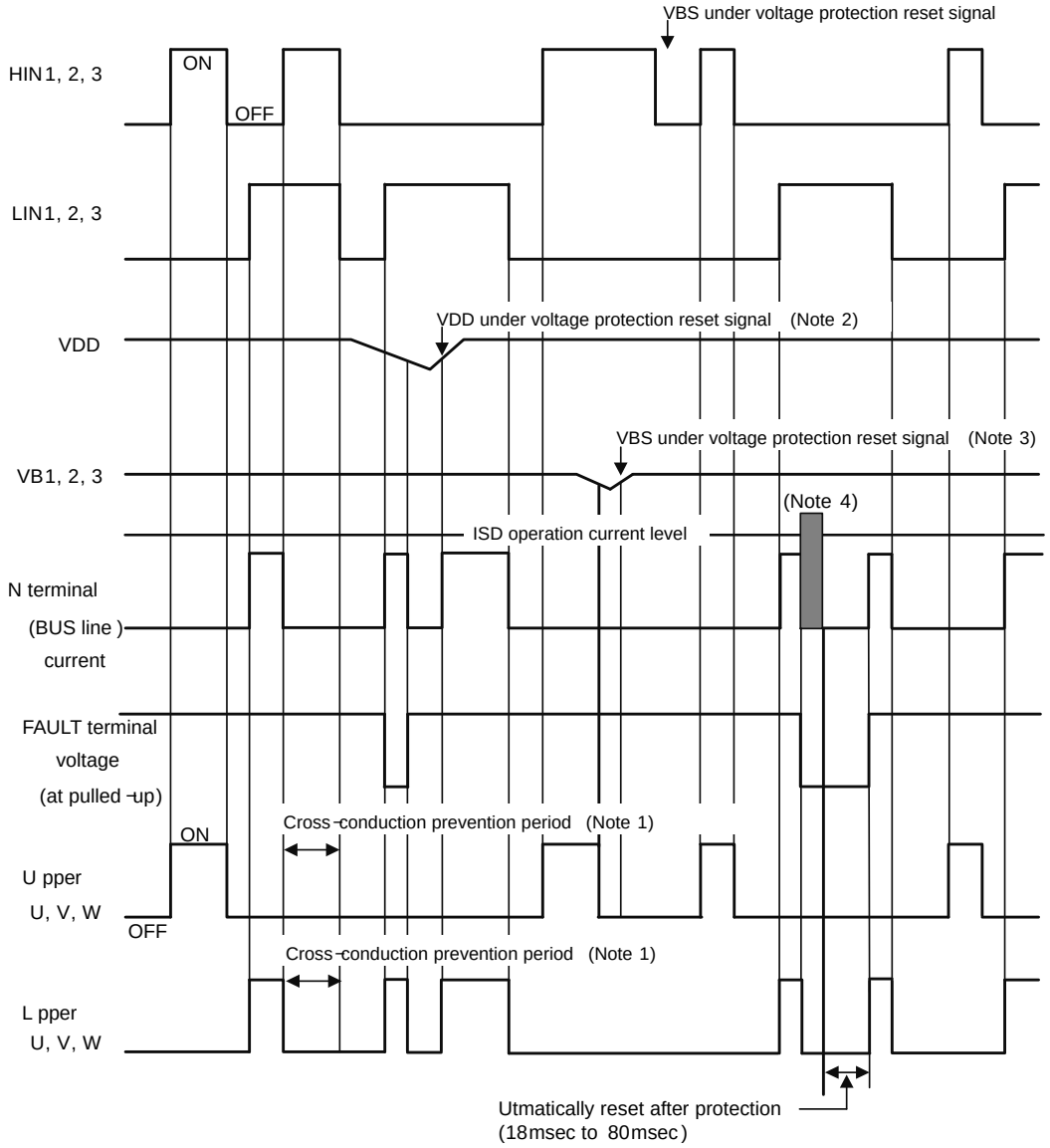


Figure 4. Input / Output Timing Chart

Notes:

1. Diagram shows the prevention of shoot−through via control logic. More dead time to account for switching delay needs to be added externally.
2. When VDD decreases all gate output signals will go low and cut off all of 6 IGBT outputs. When VDD rises the operation will resume immediately.
3. When the upper side gate voltage at VB1, VB2 and VB3 drops only, the corresponding upper side output is turned off.
   The outputs return to normal operation immediately after the upper side gate voltage rises.
4. In case of over current detection, all IGBT's are turned off and the FAULT output is asserted. Normal operation resumes in 18 to 80 ms after the over current condition is removed.

Table 5. INPUT / OUTPUT LOGIC TABLE

INPUT			OUTPUT			
HIN	**LIN**	**OCP**	**Upper side IGBT**	**Lower side IGBT**	**U,V,W**	**FAULT**
H	L	OFF	ON	OFF	P	OFF
L	H	OFF	OFF	ON	N	OFF
L	L	OFF	OFF	OFF	High Impedance	OFF
H	H	OFF	OFF	OFF	High Impedance	OFF
X	X	ON	OFF	OFF	High Impedance	ON

Table 6. THERMISTOR CHARACTERISTICS

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Resistance	R_{25}	Tc = 25°C	99	100	101	kΩ
	R_{100}	Tc = 100°C	5.18	5.38	5.60	kΩ
B−Constant (25 to 50°C)	B		4208	4250	4293	K
Temperature Range			–40	−	+125	°C

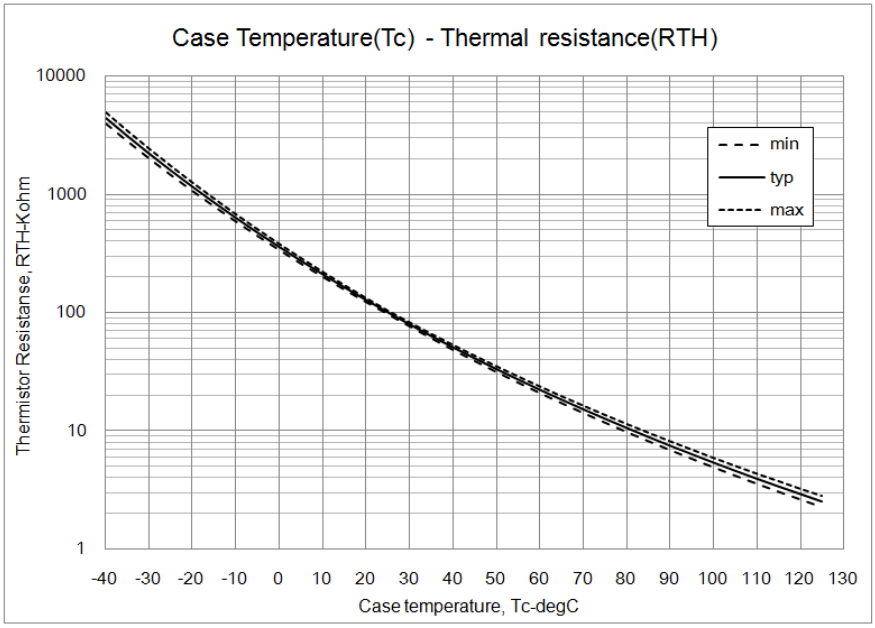
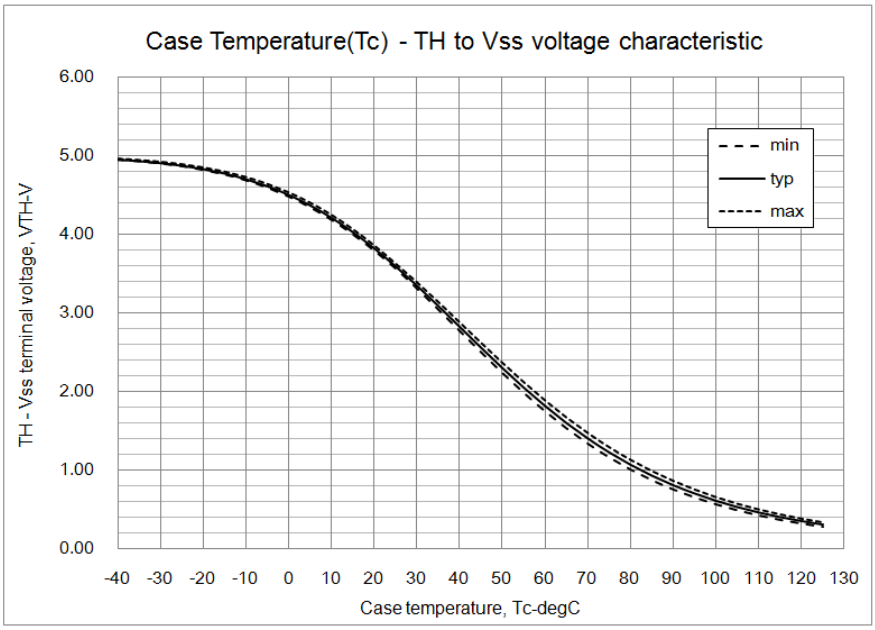


Figure 5. Thermistor Resistance versus Case Temperature



Conditions: RTH = 39 kΩ, pull−up voltage 5.0 V

Figure 6. Thermistor Voltage versus Case Temperature

FAULT Output

The FAULT terminal is an open drain output requiring a pull−up resistor. If the pull−up voltage is 5 V, use a pull−up resistor with a value of 6.8 kΩ or higher. If the pull−up voltage is 15 V, use a pull−up resistor with a value of 20 kΩ or higher. The FAULT output is triggered if there is a V_{DD} undervoltage or an overcurrent condition.

The terminal has a function of enable output, this pin is used to enable or shut down the built−in driver. If the voltage on the FAULT pin rises above the ENABLE ON−state voltage, the output drivers are enabled. If the voltage on the ELTEN pin falls below the ENABLE OFF−state voltage, the drivers are disabled.

Undervoltage Lockout Protection

If V_{DD} goes below the V_{DD} supply undervoltage lockout falling threshold, the FAULT output is switched on. The FAULT output stays on until V_{DD} rises above the V_{DD} supply undervoltage lockout rising threshold. After V_{DD} has risen above the threshold to enable normal operation, the driver waits to receive an input signal on the LIN input before enabling the driver for the HIN signal.

Overcurrent protection

The over current protection feature is not intended to protect in exceptional fault condition. An external fuse is recommended for safety.

An additional fuse is recommended to protect against system level or abnormal over−current fault conditions.

Capacitors on High Voltage and V_{DD} Supplies

Both the high voltage and V_{DD} supplies require an electrolytic capacitor and an additional high frequency capacitor.

Minimum Input Pulse Width

When input pulse width is less than 1.0 μs, an output may not react to the pulse. (Both ON signal and OFF signal)

Calculation of Bootstrap Capacitor Value

The bootstrap capacitor value CB is calculated using the following approach. The following parameters influence the choice of bootstrap capacitor:

- VBS: Bootstrap power supply.
  15 V is recommended.
- QG: Total gate charge of IGBT at VBS = 15 V.
  132 nC
- UVLO: Falling threshold for UVLO.
  Specified as 12 V.
- ID_{MAX}: High side drive consumption current.
  Specified as 0.4 mA
- t_{ONMAX}: Maximum ON pulse width of high side IGBT.

Capacitance calculation formula:

$$CB = (QG + ID_{MAX} * t_{ONMAX}) / (VBS - UVLO)$$

CB is recommended to be approximately 3 times the value calculated above. The recommended value of CB is in the

range of 1 to 47 μF, however, the value needs to be verified prior to production. When not using the bootstrap circuit, each high side driver power supply requires an external independent power supply.

The internal bootstrap circuit uses a MOSFET. The turn on time of this MOSFET is synchronized with the turn on of the low side IGBT. The bootstrap capacitor is charged by turning on the low side IGBT.

If the low side IGBT is held on for a long period of time (more than one second for example), the bootstrap voltage on the high side MOSFET will slowly discharge.

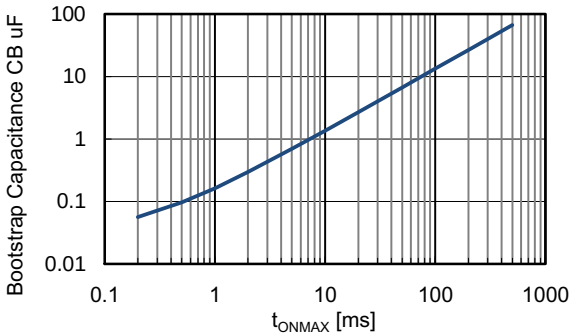


Figure 7. Bootstrap Capacitance versus t_{ONMAX}

Table 7. MOUNTING INSTRUCTIONS

Item	Recommended Condition
Pitch	40.6 ±0.1 mm (Please refer to Package Outline Diagram)
Screw	Diameter: M3 Screw head types: pan head, truss head, binding head
Washer	Plane washer The size is D = 7 mm, d = 3.2 mm and t = 0.5 mm JIS B 1256
Heat sink	Material: Aluminum or Copper Warpage (the surface that contacts IPM): −50 to 100 μm Screw holes must be countersunk. No contamination on the heat sink surface that contacts IPM.
Torque	Temporary tightening: 20 to 30 % of final tightening on first screw Temporary tightening: 20 to 30 % of final tightening on second screw Final tightening: 0.6 to 0.9 Nm on first screw Final tightening: 0.6 to 0.9 Nm on second screw
Grease	Silicone grease. Thickness: 100 to 200 μm Uniformly apply silicone grease to whole back. Thermal foils are only recommended after careful evaluation. Thickness, stiffness and compressibility parameters have a strong influence on performance.

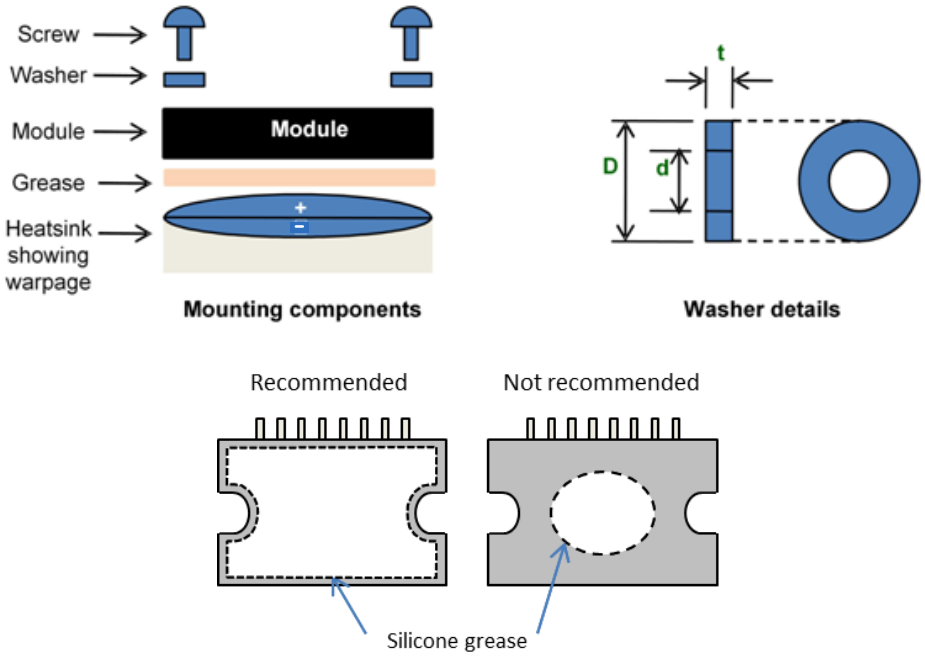


Figure 8. Module Mounting Details: Components; Washer Drawing; Need for Even Spreading of Thermal Grease

TEST CIRCUITS

- I_{CE}

	U+	V+	W+	U−	V−	W−
M	13	13	13	10	6	2
N	10	6	2	16	16	16

	U(DB)	V(DB)	W(DB)
M	9	5	1
N	26	26	26

NOTE: U+,V+,W+ : High side phase
U−, V−, W− : Low side phase

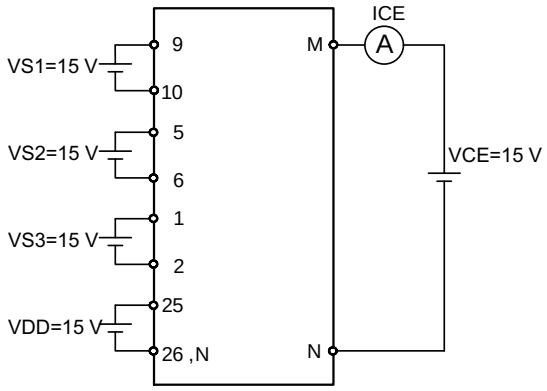


Figure 9. Test Circuit for I_{CE}

- V_{CE}(sat) (Test by pulse)

	U+	V+	W+	U−	V−	W−
M	13	13	13	10	6	2
N	10	6	2	16	16	16
m	17	18	19	20	21	22

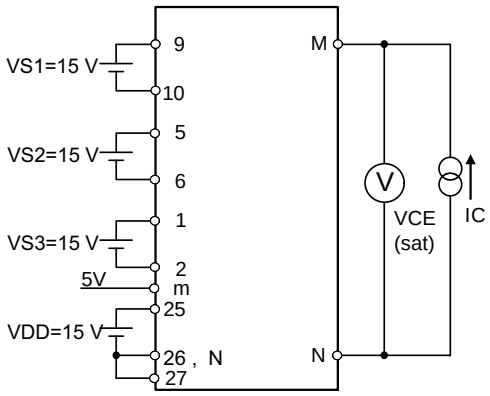


Figure 10. Test Circuit for V_{CE}(sat)

- V_F (Test by pulse)

	U+	V+	W+	U−	V−	W−
M	13	13	13	10	6	2
N	10	6	2	16	16	16

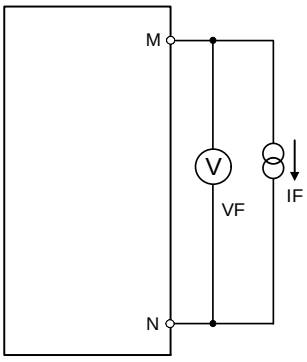


Figure 11. Test Circuit for V_F

- ID

	VD1	VD2	VD3	VD4
M	9	5	1	25
N	10	6	2	26

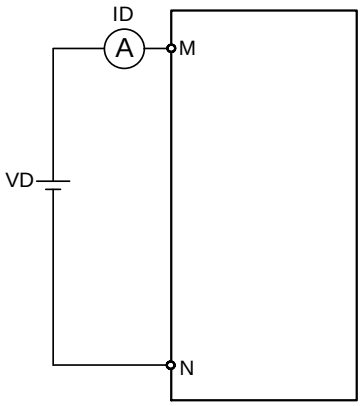
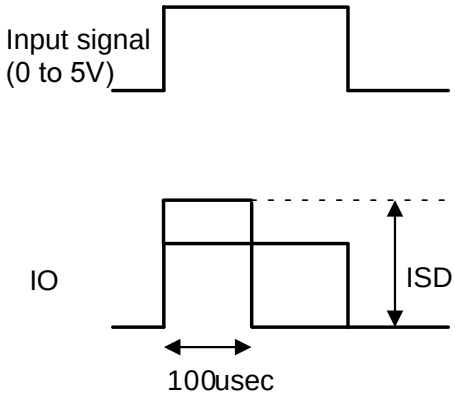


Figure 12. Test Circuit for ID

- ISD



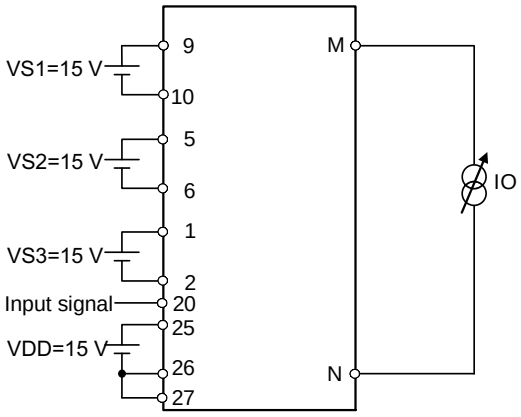
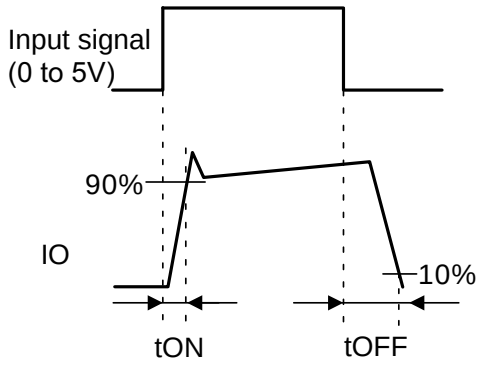


Figure 13. Test Circuit for ISD

- Switching time
  (The circuit is a representative example of the low side U phase.)



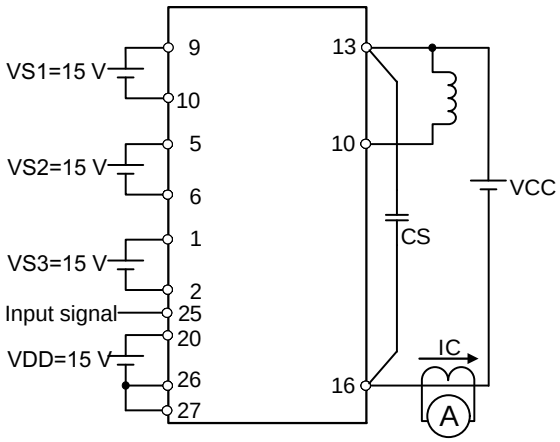


Figure 14. Switching Time Test Circuit

ORDERING INFORMATION

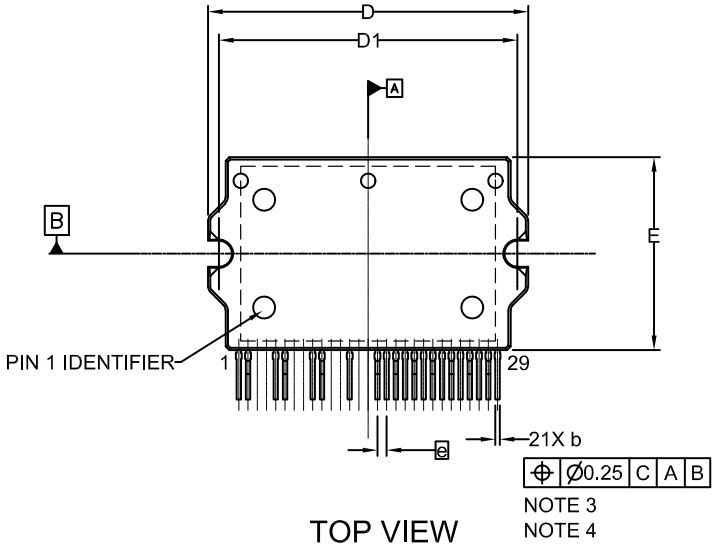
Device	Marking	Package	Shipping
STK531U394C−E	STK531U394C	SIP29 44x26.5 (Pb−Free)	11 Units / Tube

SIP29 44x26.5
CASE 127ET
ISSUE O

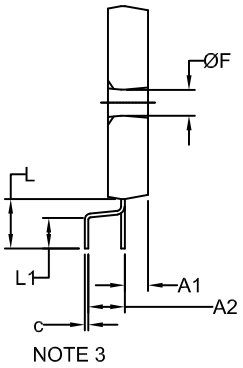
DATE 18 AUG 2017

NOTES:
1. DIMENSIONING AND TOLERANCING PER. ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b and c APPLY TO THE PLATED LEADS AND ARE MEASURED BETWEEN 1.00 AND 2.00 FROM THE LEAD TIP.
4. POSITION OF THE LEAD IS DETERMINED AT THE ROOT OF THE LEAD WHERE IT EXITS THE PACKAGE BODY.
5. PIN 1 IDENTIFICATION IS A MIRRORED SURFACE INDENT.
6. MISSING PINS ARE 3,4,7,8,11,12,14 AND 15.

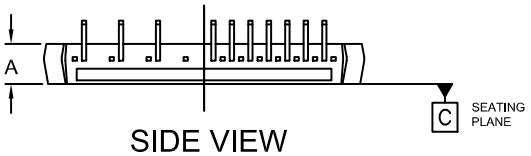
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	5.00	5.50	6.00
A1	2.70	3.20	3.70
A2	4.50	5.00	5.50
b	0.55	0.60	0.65
c	0.45	0.50	0.55
D	43.50	44.00	44.50
D1	40.50	41.00	41.50
E	26.00	26.50	27.00
e	1.27 BSC		
F	3.10	3.60	4.10
L	6.30	6.80	7.30
L1	3.80	4.30	4.80



TOP VIEW



END VIEW



SIDE VIEW

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