VNS14NV04P-E

"OMNIFET II"
fully autoprotected Power MOSFET

Features

Type	$R_{DS(on)}$	I_{lim}	V_{clamp}
VNS14NV04P-E	35 mΩ	12 A	40 V

- Linear current limitation
- Thermal shutdown
- Short circuit protection
- Integrated clamp
- Low current drawn from input pin
- Diagnostic feedback through input pin
- ESD protection
- Direct access to the gate of the Power MOSFET (analog driving)
- Compatible with standard Power MOSFET

SO-8

Description

The VNS14NV04P-E is monolithic device made using STMicroelectronics™ VIPower™ M0 Technology, intended for replacement of standard Power MOSFETs in DC to 50 KHz applications. Built-in thermal shutdown, linear current limitation and overvoltage clamp protect the chip in harsh environments.

Fault feedback can be detected by monitoring the voltage at the input pin.

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
SO-8	VNS14NV04P-E	VNS14NV04PTR-E

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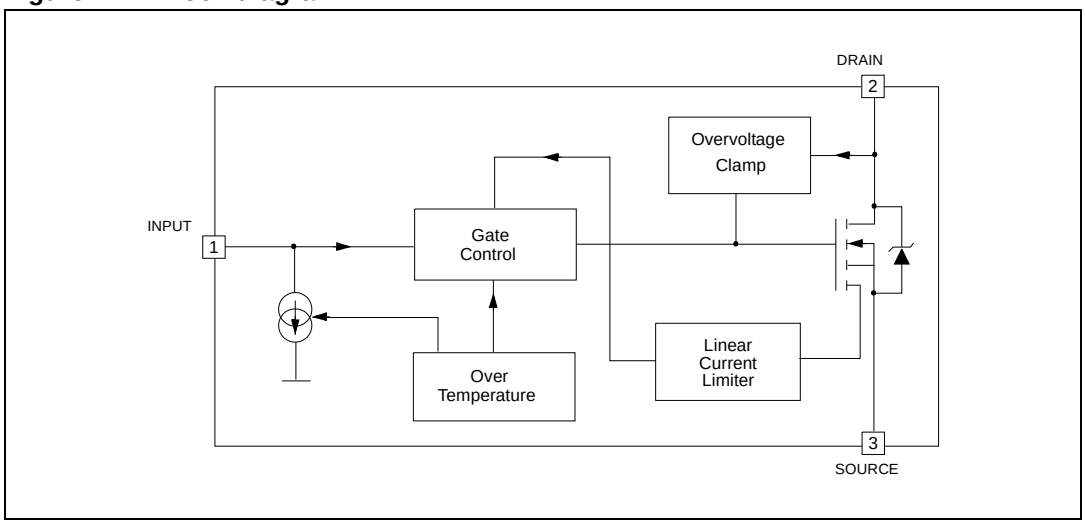
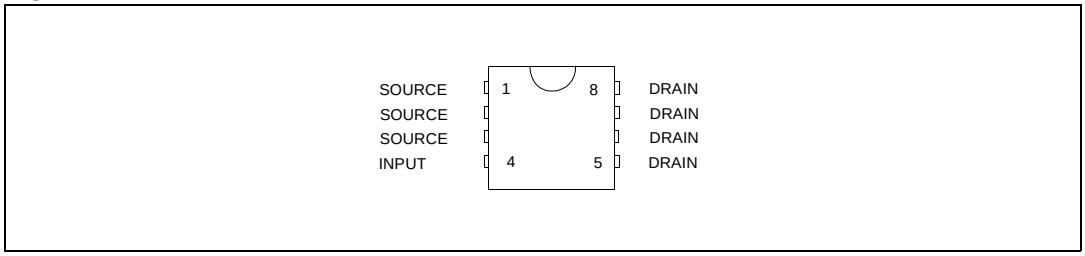
1 Block diagram

Figure 1. Block diagram



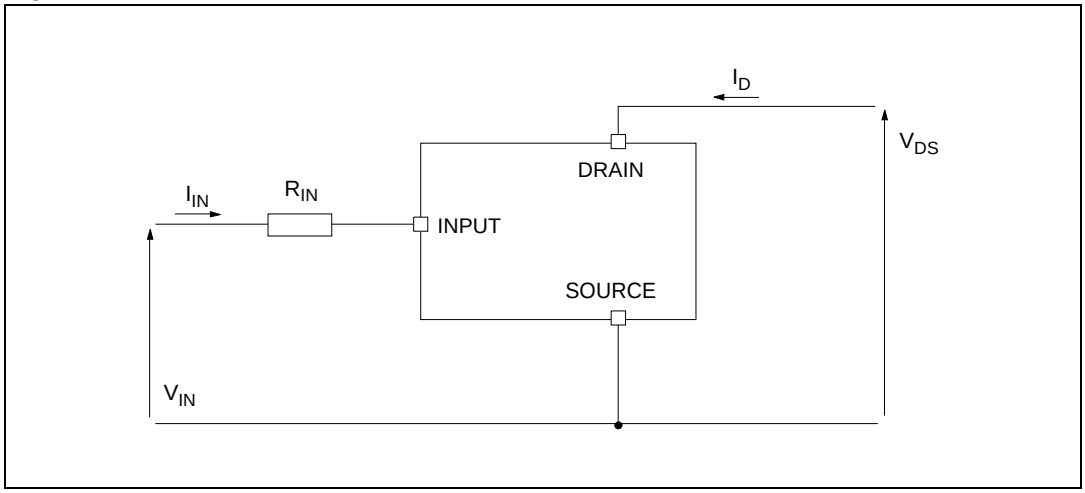
2 Pin description

Figure 2. Connection diagram SO-8 package (top view)



3 Electrical specification

Figure 3. Current and voltage conventions



3.1 Absolute maximum rating

Table 2. Absolute maximum rating

Symbol	Parameter	Value	Unit
		SO-8	
V_{DS}	Drain-source voltage (V_{IN}=0 V)	Internally clamped	V
V_{IN}	Input voltage	Internally clamped	V
I_{IN}	Input current	+/-20	mA
$R_{IN\ MIN}$	Minimum input series impedance	10	Ω
I_D	Drain current	Internally limited	A
I_R	Reverse DC output current	-15	A
V_{ESD1}	Electrostatic discharge (R=1.5 KΩ, C=100 pF)	4000	V
V_{ESD2}	Electrostatic discharge on output pin only (R=330 Ω, C=150 pF)	16500	V
P_{tot}	Total dissipation at T_c=25 °C	4.6	W
E_{MAX}	Maximum switching energy (L=0.4 mH; RL=0 Ω; V_{bat}=13.5 V; T_{jstart}=150 °C; I_L=18 A)		mJ
T_j	Operating junction temperature	Internally limited	°C
T_c	Case operating temperature	Internally limited	°C
T_{stg}	Storage temperature	-55 to 150	°C

3.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
		SO-8	
$R_{thj\text{-}case}$	Thermal resistance junction-case max		°C/W
$R_{thj\text{-}lead}$	Thermal resistance junction-lead max	27	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max	90(1)	°C/W

1. When mounted on a standard single-sided FR4 board with 0.5 cm^2 of Cu (at least 35 µm thick) connected to all DRAIN pins. Horizontal mounting and no artificial air flow.

3.3 Electrical characteristics

-40 < T_j < 150 °C unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Off						
V_{CLAMP}	Drain-source clamp voltage	V_{IN}=0 V; I_D=7 A	40	45	55	V
V_{CLTH}	Drain-source clamp threshold voltage	V_{IN}=0 V; I_D=2 mA	36			V
V_{INTH}	Input threshold voltage	V_{DS}=V_{IN}; I_D=1 mA	0.5		2.5	V
I_{ISS}	Supply current from input pin	V_{DS}=0 V; V_{IN}=5 V		100	150	µA
V_{INCL}	Input-source clamp voltage	I_{IN}=1 mA I_{IN}=-1 mA	6 -1.0	6.8	8 -0.3	V
I_{DSS}	Zero input voltage drain current (V_{IN}=0 V)	V_{DS}=13 V; V_{IN}=0 V; T_j=25 °C V_{DS}=25 V; V_{IN}=0 V			30 75	µA
On						
$R_{DS(on)}$	Static drain-source on resistance	V_{in} = 5 V I_D = 7 A T_j = 25 °C V_{in} = 5 V I_D = 7 A			35 70	mΩ
Dynamic (T_j=25 °C, unless otherwise specified)						
g_{fs} (1)	Forward transconductance	V_{DD} = 13 V I_D = 7 A		18		S
C_{oss}	Output capacitance	V_{DS} = 13 V f = 1 MHz V_{IN} = 0 V		400		pF
Switching						
$t_{d(on)}$	Turn-on delay time	V_{DD} = 15 V I_D = 7 A V_{gen} = 5 V R_{gen} = $R_{IN\ MIN}$ =10 Ω (see *Figure 4*)		80	250	ns
t_r	Rise time			350	1000	ns
$t_{d(off)}$	Turn-off delay time			450	1350	ns
t_f	Fall time			150	500	ns

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 15 V I_d = 7 A V_{gen} = 5 V R_{gen} = 2.2 KΩ (see *Figure 4*)		1.5	4.5	µs
t_r	Rise time			9.7	30.0	µs
$t_{d(off)}$	Turn-off delay time				25.0	µs
t_f	Fall time			10.2	30.0	µs
$(di/dt)_{on}$	Turn-on current slope	V_{DD} = 15 V I_D = 7 A V_{gen} = 5 V R_{gen} = $R_{IN\ MIN}$ =10 Ω		16		A/µs
Q_i	Total input charge	V_{DD} = 12 V I_D = 7 A V_{in} = 5 V; I_{gen} = 2.13 mA (see *Figure 8*)		36.8		nC
Source drain diode						
V_{SD} (1)	Forward on voltage	I_{SD} = 7 A V_{in} = 0 V		0.8		V
t_{rr}	Reverse recovery time	I_{SD} = 7 A; di/dt = 40 A/µs V_{DD} = 30 V L = 200 µH (see test circuit, *Figure 5*)		300		ns
Q_{rr}	Reverse recovery charge			0.8		µC
I_{RRM}	Reverse recovery current			5		A
Protection						
I_{lim}	Drain current limit	V_{IN} = 5 V; V_{DS} = 13 V	12	18	24	A
t_{dlim}	Step response current limit	V_{IN} = 5 V; V_{DS} = 13 V		45		µs
T_{jsh}	Over temperature shutdown		150	175	200	°C
T_{jrs}	Over temperature reset		135			°C
I_{gf}	Fault sink current	V_{IN} = 5 V; V_{DS} = 13 V; T_j = T_{jsh}	10	15	20	mA
E_{as}	Single pulse avalanche energy	starting T_j = 25 °C; V_{DD} = 24 V V_{IN} = 5 V; R_{gen} = $R_{IN\ MIN}$ = 10 Ω; L = 24 mH (see *Figure 6* and *Figure 7*)	400			mJ

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

4 Protection features

During normal operation, the input pin is electrically connected to the gate of the internal power MOSFET through a low impedance path.

The device then behaves like a standard power MOSFET and can be used as a switch from DC up to 50 KHz. The only difference from the user's standpoint is that a small DC current I_{ISS} (typ. 100 µA) flows into the input pin in order to supply the internal circuitry.

The device integrates:

- Overvoltage clamp protection: internally set at 45 V, along with the rugged avalanche characteristics of the Power MOSFET stage give this device unrivalled ruggedness and energy handling capability. This feature is mainly important when driving inductive loads.
- Linear current limiter circuit: limits the drain current I_D to I_{lim} whatever the input pin voltages. When the current limiter is active, the device operates in the linear region, so power dissipation may exceed the capability of the heatsink. Both case and junction temperatures increase, and if this phase lasts long enough, junction temperature may reach the over temperature threshold T_{jsh}.
- Over temperature and short circuit protection: these are based on sensing the chip temperature and are not dependent on the input voltage. The location of the sensing element on the chip in the power stage area ensures fast, accurate detection of the junction temperature. Over temperature cutout occurs in the range 150 to 190 °C, a typical value being 170 °C. The device is automatically restarted when the chip temperature falls of about 15 °C below shutdown temperature.
- Status feedback: in the case of an over temperature fault condition ($T_j > T_{jsh}$), the device tries to sink a diagnostic current I_{gf} through the input pin in order to indicate fault condition. If driven from a low impedance source, this current may be used in order to warn the control circuit of a device shutdown. If the drive impedance is high enough so that the input pin driver is not able to supply the current I_{gf}, the input pin will fall to 0 V. This will not however affect the device operation: no requirement is put on the current capability of the input pin driver except to be able to supply the normal operation drive current I_{ISS}.

Additional features of this device are ESD protection according to the Human Body model and the ability to be driven from a TTL logic circuit.

Figure 4. Switching time test circuit for resistive load

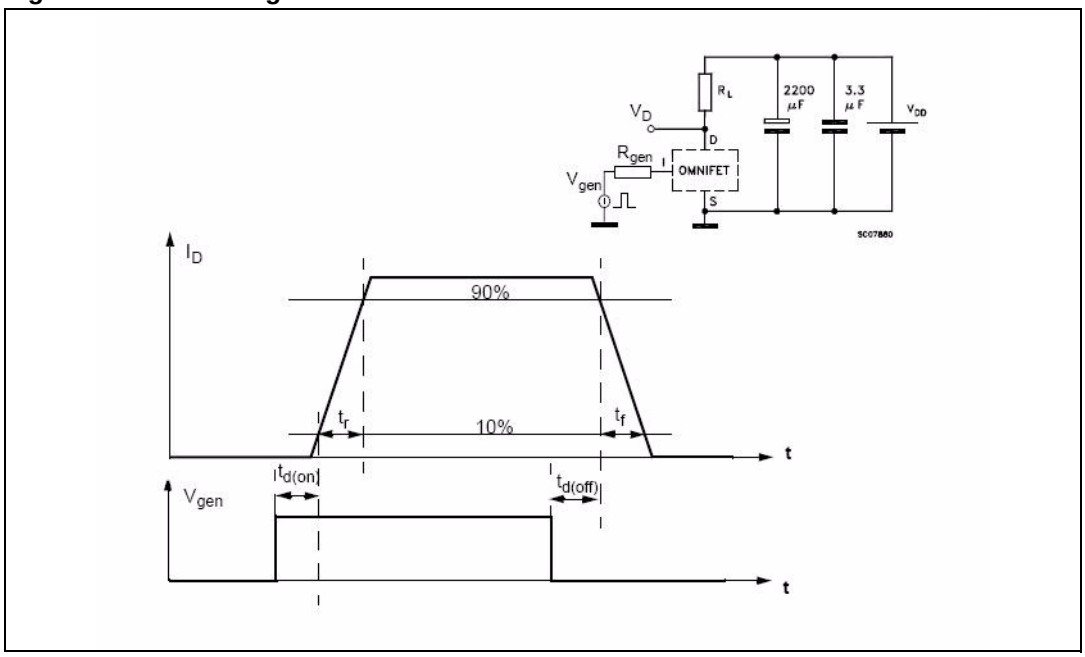


Figure 5. Test circuit for diode recovery times

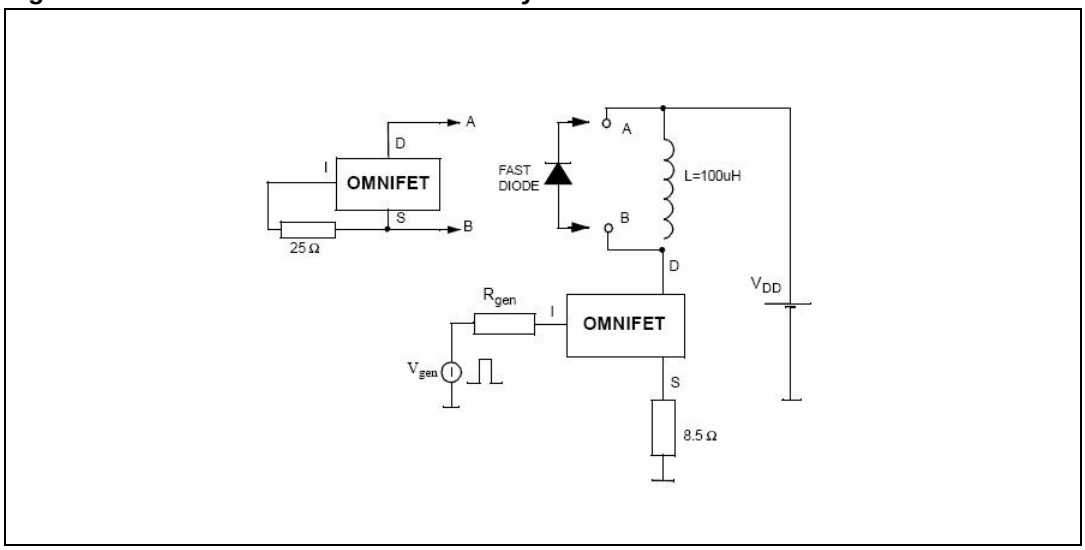


Figure 6. Unclamped inductive load test circuits

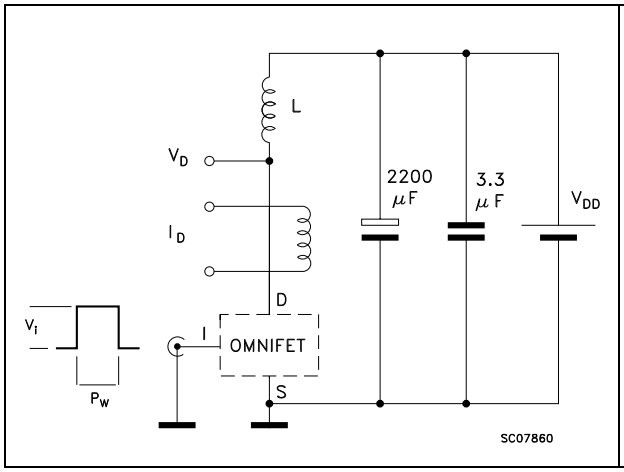


Figure 7. Unclamped inductive waveforms

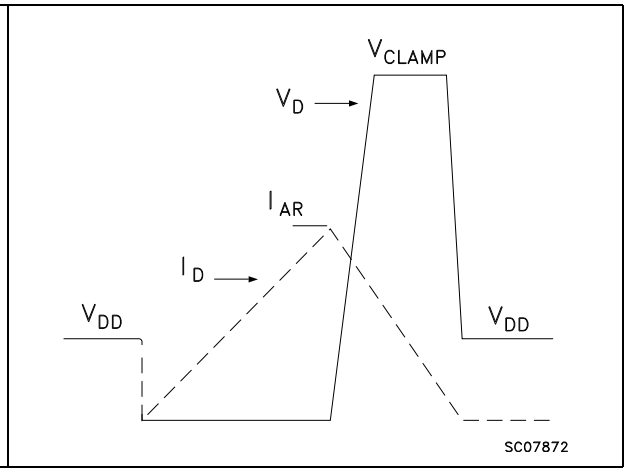


Figure 8. Input charge test circuit

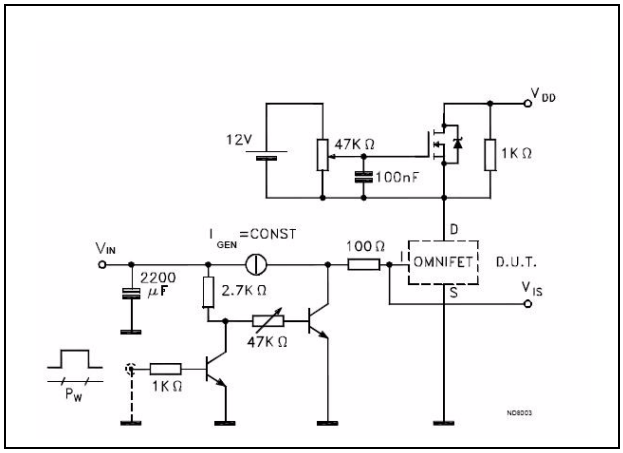


Figure 9. Source-drain diode forward characteristics

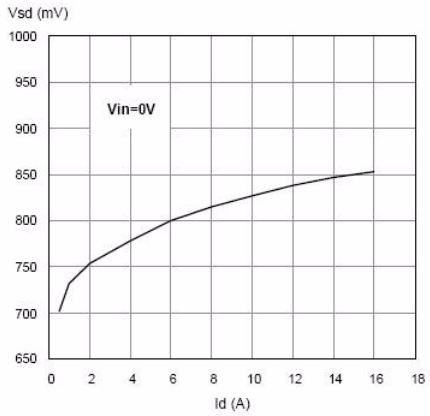


Figure 10. Static drain source on resistance

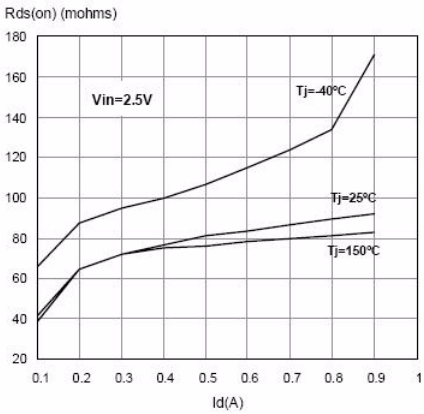


Figure 11. Derating curve

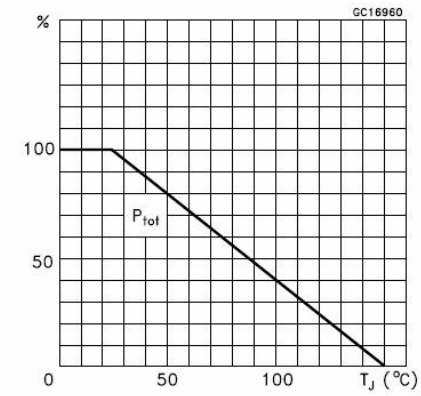


Figure 12. Static drain-source on resistance vs. input voltage (part 1/2)

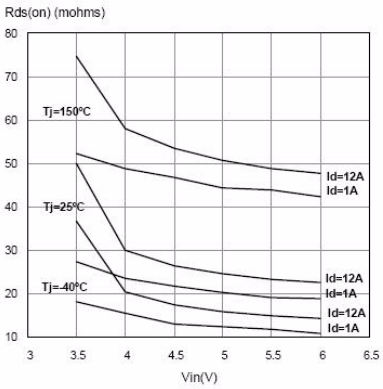


Figure 13. Static drain-source on resistance vs. input voltage (part 2/2)

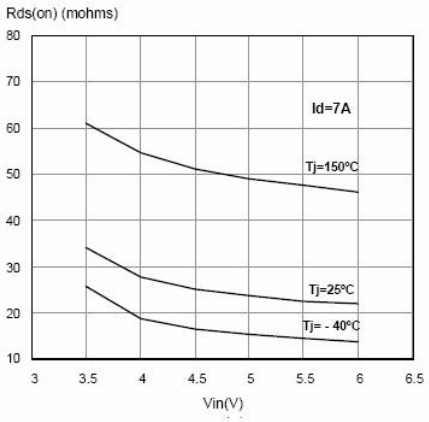


Figure 14. Transconductance

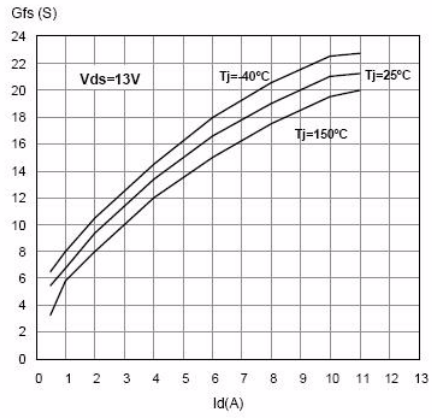


Figure 15. Static drain-source on resistance vs. Id

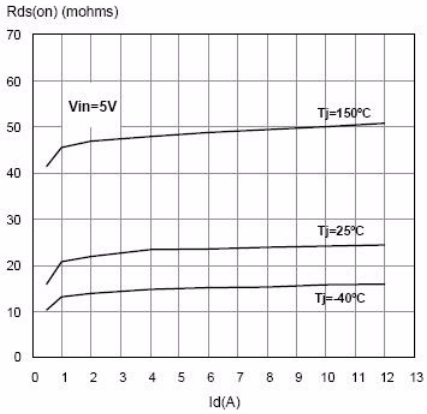


Figure 16. Transfer characteristics

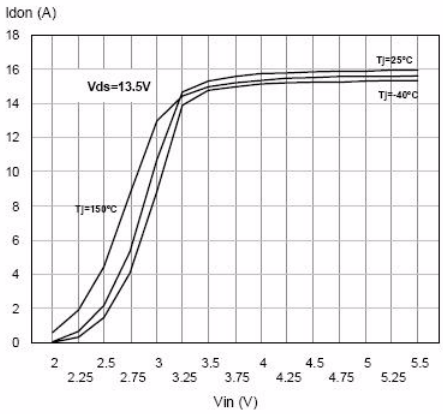


Figure 17. Turn-on current slope (part 1/2)

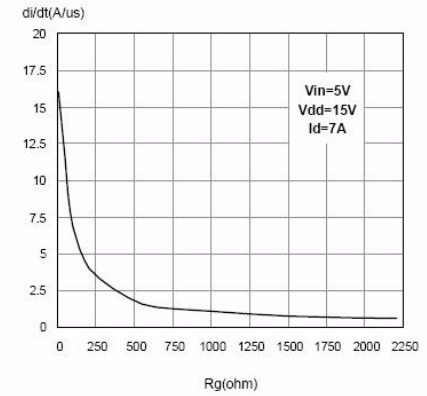


Figure 18. Turn-on current slope (part 2/2)

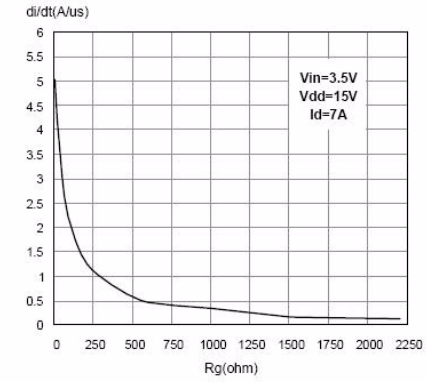


Figure 19. Input voltage vs. input charge

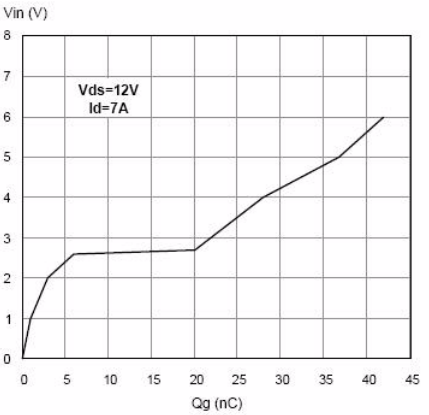


Figure 20. Turn-off drain source voltage slope (part 1/2)

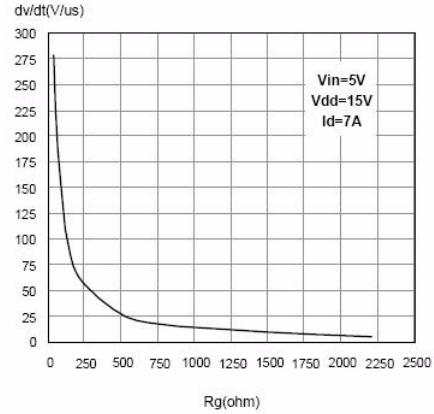


Figure 21. Turn-off drain source voltage slope (part 2/2)

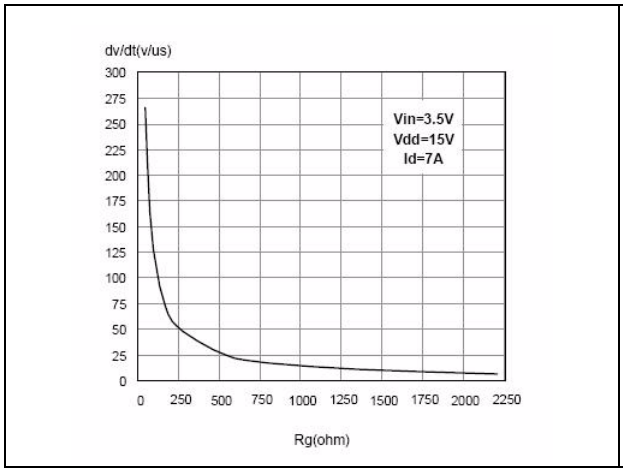


Figure 22. Capacitance variations

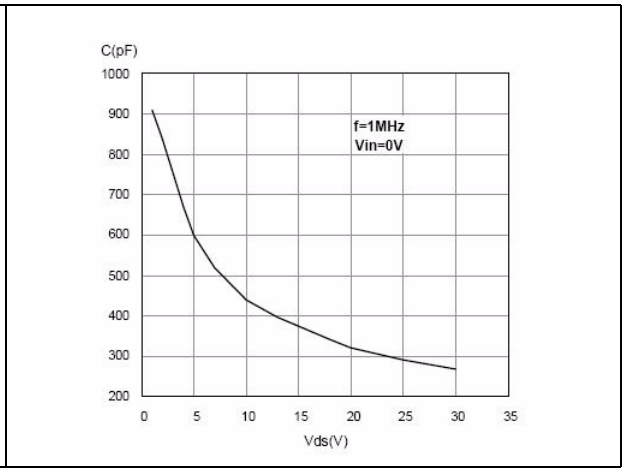


Figure 23. Switching time resistive load (part 1/2)

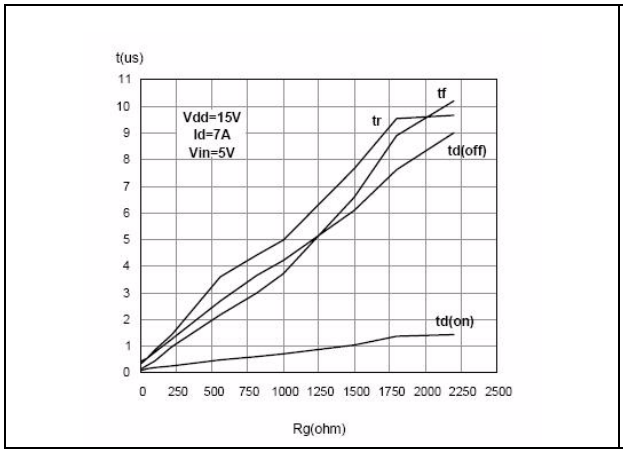


Figure 24. Switching time resistive load (part 2/2)

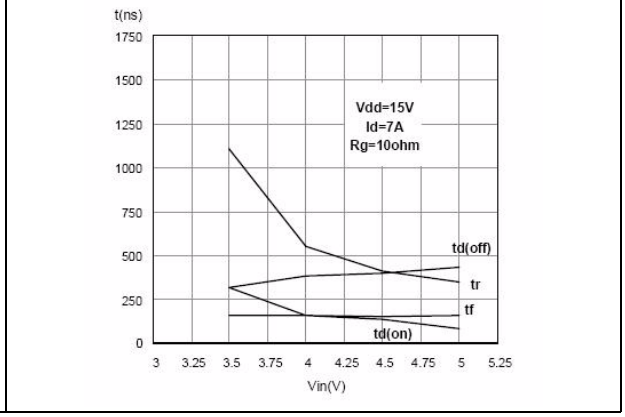
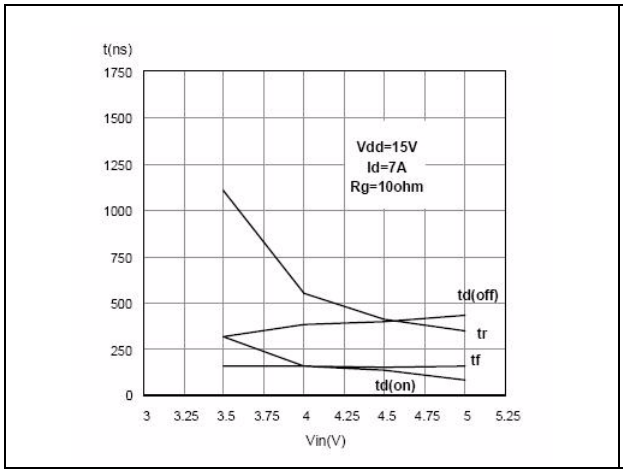


Figure 25. Output characteristics

Figure 26. Normalized on resistance vs. temperature



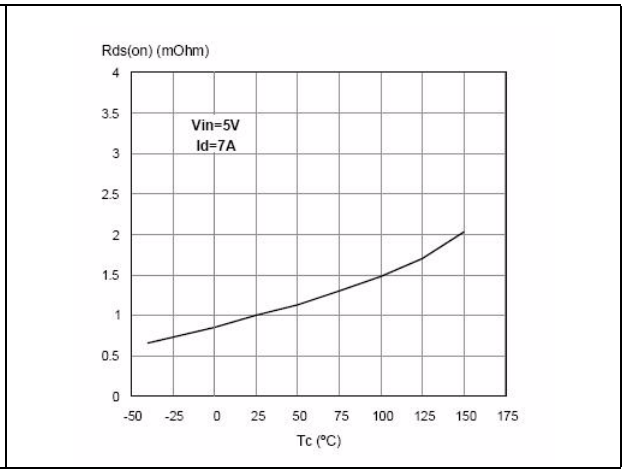


Figure 27. Normalized input threshold voltage vs. temperature

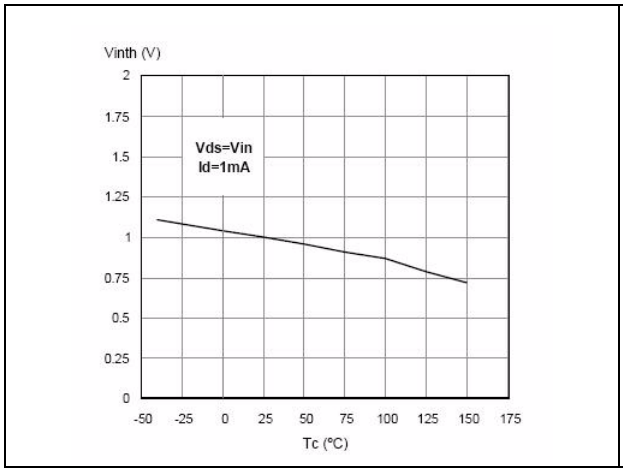


Figure 28. Current limit vs. junction temperatures

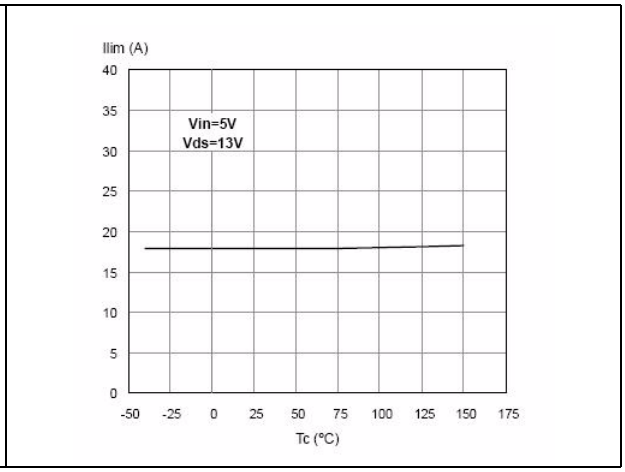
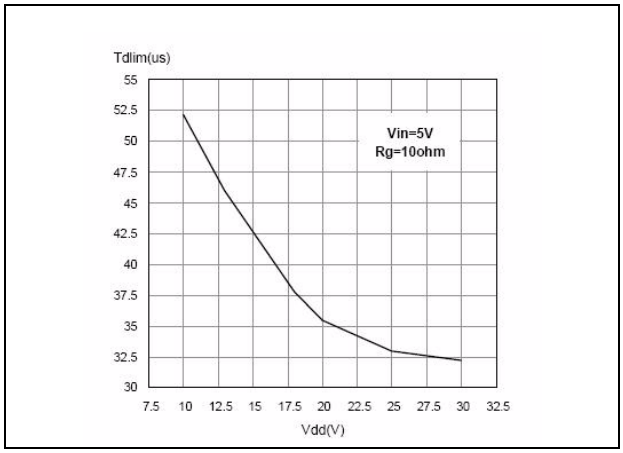


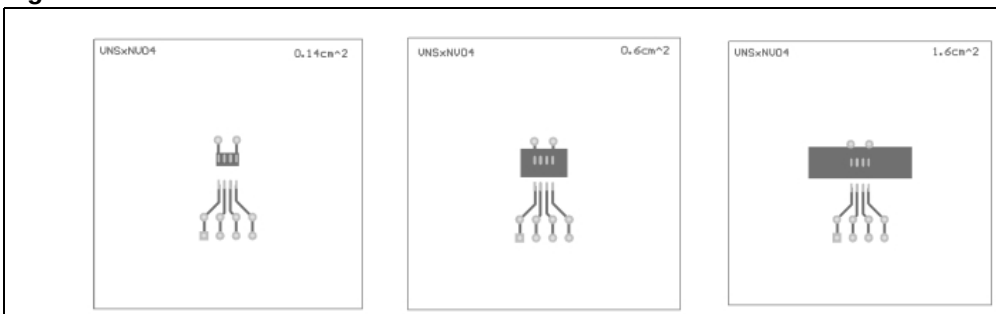
Figure 29. Step response current limit



5 Package thermal data

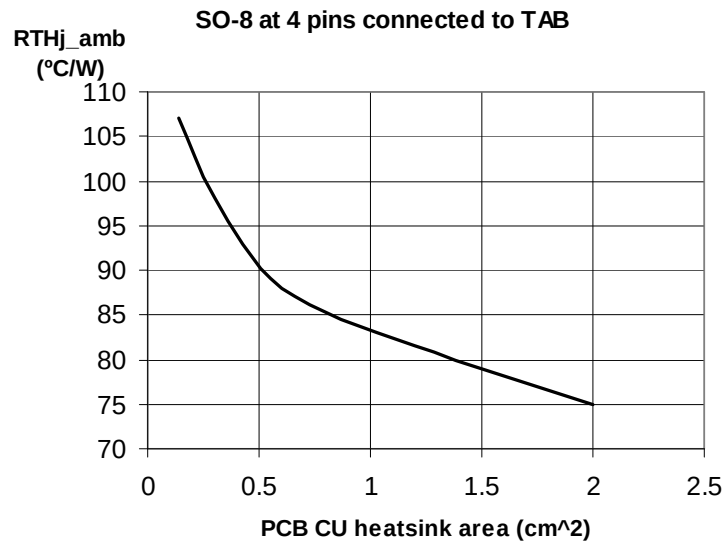
5.1 SO-8 thermal data

Figure 30. SO-8 PC board



1. Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area=58 mm x 58 mm, PCB thickness=2 mm, Cu thickness=35 µm, Copper areas: 0.14 cm^2, 0.6 cm^2, 1.6 cm^2).

Figure 31. $R_{thj\text{-}amb}$ vs PCB copper area in open box free air condition



6 Package and packing information

6.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

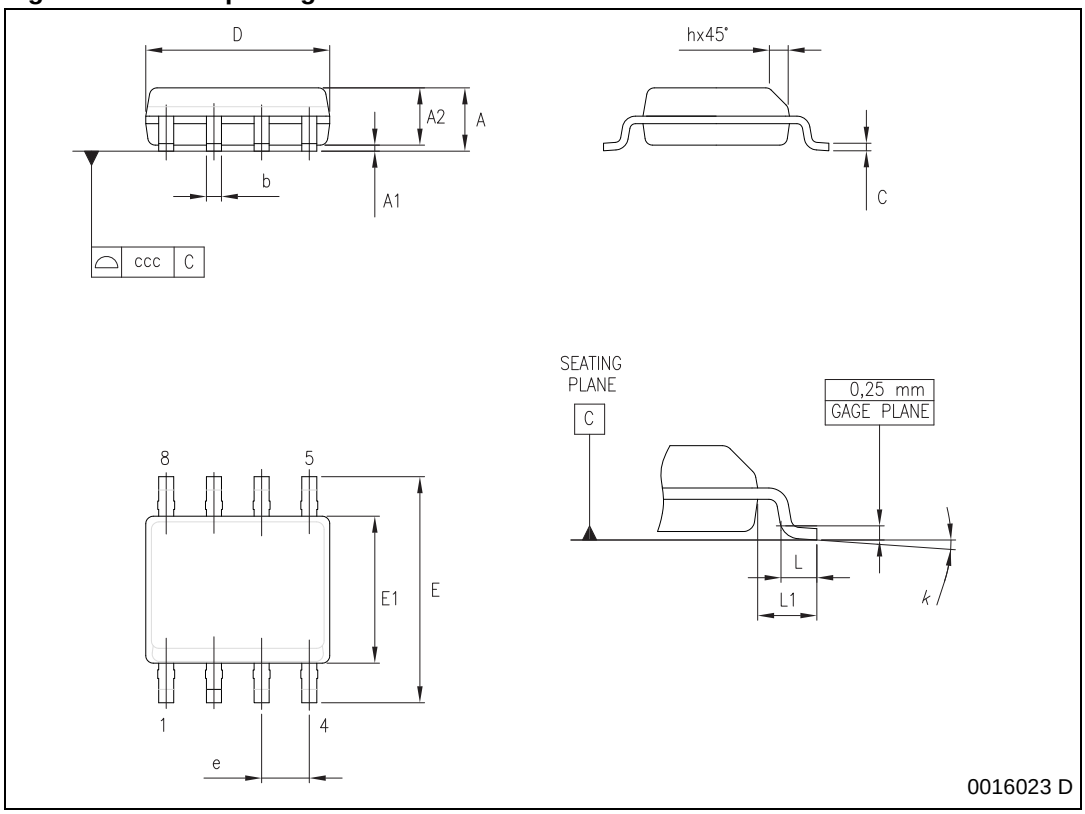
6.2 SO-8 mechanical data

Table 5. SO-8 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.28		0.48
c	0.17		0.23
D(1)	4.80	4.90	5.00
E	5.80	6.00	6.20
E1(2)	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
k	0°		8°
ccc			0.10

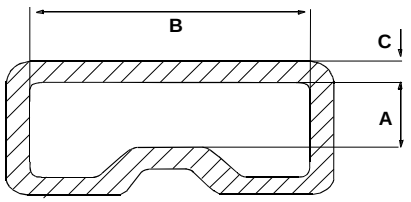
1. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm in total (both side).
2. Dimension “E1” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm per side.

Figure 32. SO-8 package dimension



6.3 SO-8 packing information

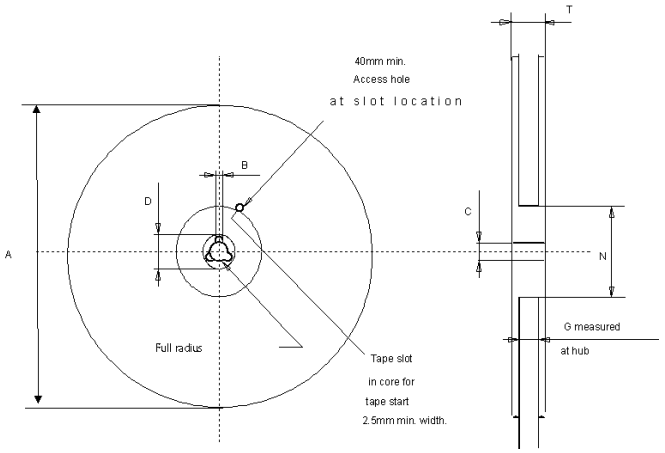
Figure 33. SO-8 Tube Shipment (no suffix)



Base Q.ty	100
Bulk Q.ty	2000
Tube length (± 0.5)	532
A	3.2
B	6
C (± 0.1)	0.6

All dimensions are in mm.

Figure 1. Tape And Reel Shipment (suffix "TR")



REEL DIMENSIONS

Base Q.ty	2500
Bulk Q.ty	2500
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	12.4
N (min)	60
T (max)	18.4

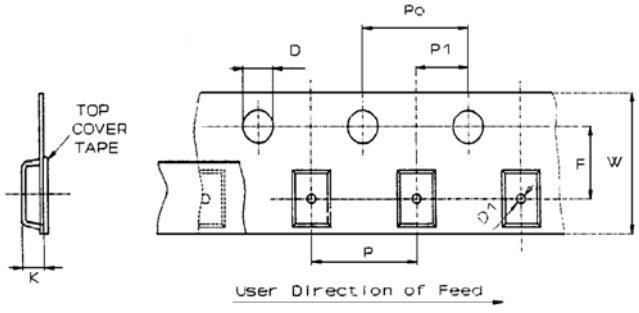
All dimensions are in mm.

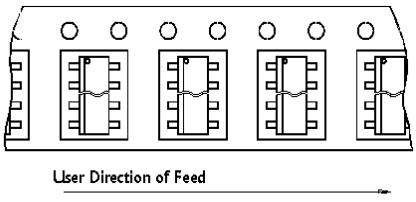
TAPE DIMENSIONS

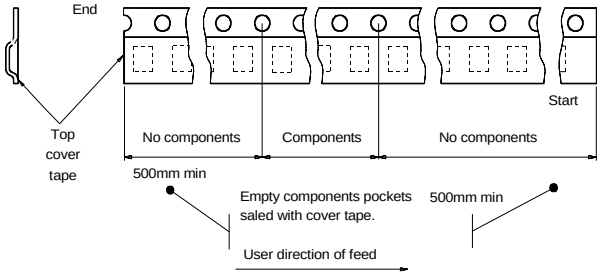
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	**W**	12
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	8
Hole Diameter	**D (± 0.1/-0)**	1.5
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.05)**	5.5
Compartment Depth	**K (max)**	4.5
Hole Spacing	**P1 (± 0.1)**	2

All dimensions are in mm.







7 Revision history

Table 6. Document revision history

Date	Revision	Changes
15-Apr-2009	1	Initial release.
01-Mar-2011	2	Updated *Table 1: Device summary* Inserted *Section 6.3: SO-8 packing information*
18-Sep-2013	3	Updated Disclaimer.

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