

CYPRESS

# ASYNCHRONOUS SRAMs WITH ON-CHIP ERROR-CORRECTING CODE (ECC)



## PRODUCT OVERVIEW

### COMPLETE FREEDOM FROM SOFT-ERRORS

The latest generation Asynchronous SRAMs from Cypress make the best of an advanced process technology by integrating single-bit error correction capability and bit-interleaving techniques to mitigate the effects of soft errors. The result is a family of devices that provide best-in-class features and the highest levels of reliability.

With the performance to serve a wide variety of industrial, communication, data processing, medical, consumer and military applications, Cypress's latest technology Fast and MoBL® SRAM devices are form-fit-function compatible with existing Asynchronous SRAM devices based on older technology nodes. This allows customers to boost system performance and reliability without investing on PCB re-design.

### SOFT-ERROR MITIGATION IN ASYNCHRONOUS SRAM

Cypress's latest generation Asynchronous SRAM devices use (38,32) Hamming Code for single-bit error detection and correction. A hardware ECC block performs all ECC-related functions in line, without user intervention and without affecting the access time performance of the device. The single-bit error detection and correction capability is supplemented by a bit-interleaving scheme to prevent the occurrence of multi-bit errors. Together, these features provide significant improvement in Soft Error Rate (SER) performance, resulting in FIT rates less than 0.1 FIT/Mbit.

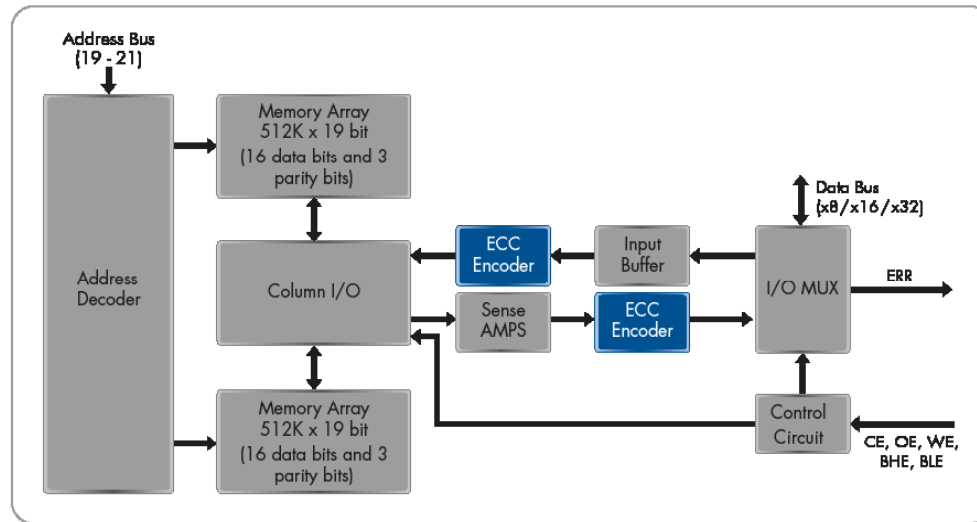
### ENHANCED RELIABILITY WITH ERR PIN

Over a period of time, multiple single event upsets (SEUs) may affect the same word, resulting in an accumulated multi-bit upset (two or more single-bit upsets in the same word). Such an event is highly improbable. But if it does occur, an accumulated multi-bit upset cannot be detected by the ECC logic, and the system may read incorrect data.

To mitigate this problem, Cypress's latest generation Asynchronous SRAM devices include an optional error indication (ERR) pin. During read operation, the ERR pin signals detection and correction of a single-bit error at the accessed memory location. The system can use this information to recognize a single-bit error and write-back corrected data to the memory.

### ADVANTAGES

- Highest level of reliability: Soft-Error Rate < 0.1 FIT/Mbit
- Embedded ECC to detect and correct all single-bit errors
- Bit-interleaving to avoid multi-bit upsets
- Optional ERR pin to indicate the occurrence of single-bit error
- Industry leading access time: 10ns (16-Mbit FAST)
- Ultra-low standby current: 16uA (16-Mbit MoBL)
- Multiple configurations: x8, x16, and x32
- Multiple operating voltages: 1.8V, 3V, 5V
- Available in industrial and automotive temperature grades
- Form-fit-function compatible with current generation ASYNC SRAM devices



Internal Block Diagram of ASYNCHRONOUS SRAM with ECC

## 16-MBIT FAST ASYNCHRONOUS SRAM

| Part Number               | Organization | Voltage      | Speed <sup>(2)</sup>   | Package                         | Temperature Grade      |
|---------------------------|--------------|--------------|------------------------|---------------------------------|------------------------|
| CY7C1069G                 | 2M x 8       | 1.8V, 3V, 5V | 10ns, 12ns, 15ns, 17ns | 54-TSOP II, 48-VFBGA            | Industrial, Automotive |
| CY7C1069GE <sup>(1)</sup> | 2M x 8       | 1.8V, 3V, 5V | 10ns, 12ns, 15ns, 17ns | 54-TSOP II, 48-VFBGA            | Industrial, Automotive |
| CY7C1061G                 | 1M x 16      | 1.8V, 3V, 5V | 10ns, 12ns, 15ns, 17ns | 48-TSOP I, 54-TSOP II, 48-VFBGA | Industrial, Automotive |
| CY7C1061GE <sup>(1)</sup> | 1M x 16      | 1.8V, 3V, 5V | 10ns, 12ns, 15ns, 17ns | 48-TSOP I, 54-TSOP II, 48-VFBGA | Industrial, Automotive |
| CY7C1062G                 | 512K x 32    | 1.8V, 3V     | 10ns, 12ns, 15ns, 17ns | 119-BGA                         | Industrial, Automotive |
| CY7C1062GE <sup>(1)</sup> | 512K x 32    | 1.8V, 3V     | 10ns, 12ns, 15ns, 17ns | 119-BGA                         | Industrial, Automotive |

## 16-MBIT MOBL<sup>®</sup> ASYNCHRONOUS SRAM

| Part Number              | Organization           | Voltage      | Speed <sup>(4)</sup> | Package             | Temperature Grade      |
|--------------------------|------------------------|--------------|----------------------|---------------------|------------------------|
| CY62167G                 | 1M x 16 <sup>(3)</sup> | 1.8V, 3V, 5V | 45ns, 55ns           | 48-TSOP I, 48-VFBGA | Industrial, Automotive |
| CY62167GE <sup>(1)</sup> | 1M x 16 <sup>(3)</sup> | 1.8V, 3V, 5V | 45ns, 55ns           | 48-TSOP I, 48-VFBGA | Industrial, Automotive |
| CY62168G                 | 2M x 8                 | 1.8V, 3V, 5V | 45ns, 55ns           | 48-VFBGA            | Industrial, Automotive |
| CY62168GE <sup>(1)</sup> | 2M x 8                 | 1.8V, 3V, 5V | 45ns, 55ns           | 48-VFBGA            | Industrial, Automotive |
| CY62162G                 | 512K x 32              | 1.8V, 3V     | 45ns, 55ns           | 119-BGA             | Industrial, Automotive |
| CY62162GE <sup>(1)</sup> | 512K x 32              | 1.8V, 3V     | 45ns, 55ns           | 119-BGA             | Industrial, Automotive |

Notes: 1. Part with ERR pin

2. Operating speed is 10ns for Industrial Grade 3 V, 5 V part; 15ns for Industrial Grade 1.8 V part; 12ns for Automotive Grade 3 V, 5 V part; and 17ns for Automotive Grade 1.8 V part

3. 48-pin TSOP I configurable as 1Mx16 or as 2Mx8 SRAM

4. Operating speed is 45ns for Industrial Grade and 55ns for Automotive Grade

## GET STARTED NOW

For more information please visit us at [www.cypress.com/go/AsyncSRAM](http://www.cypress.com/go/AsyncSRAM)

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