MP62340/MP62341

3.3V/5V, Dual-Channel 1A Current-Limited Power Distribution Switches

DESCRIPTION

The MP62340/MP62341 Power Distribution Switch features internal current limiting to prevent damage to host devices due to faulty load conditions. The MP62340/MP62341 analog switch has 80mΩ on-resistance and operates from 2.7V to 5.5V input. It is available with guaranteed current limits, making it ideal for load switching applications. The MP62340/MP62341 has built-in protection for both over current and increased thermal stress. For over current, the device will limit the current by changing to a constant current mode.

As the temperature increases as a result of short circuit, then the device will shut off. The device will recover once the device temperature reduces to approx 120°C.

The MP62340/MP62341 is available in 8-pin MSOP package with exposed pad and SOIC package without exposed pad.

FEATURES

- 1A Continuous Current
- Accurate Current Limit
- 2.7V to 5.5V Supply Range
- 140 μA Quiescent Current
- 80mΩ MOSFET
- Thermal-Shutdown Protection
- Under-Voltage Lockout
- 8ms FLAG Deglitch Time
- No FLAG Glitch During Power Up
- Reverse Current Blocking
- Active High & Active Low Options
- Available is MSOP8E and SOIC8
- UL Approved—E322138

APPLICATIONS

- PDAs
- Portable GPS
- Notebook PC
- Set-top-box
- Telecom and Network Systems
- PC Card Hot Swap
- USB Power Distribution

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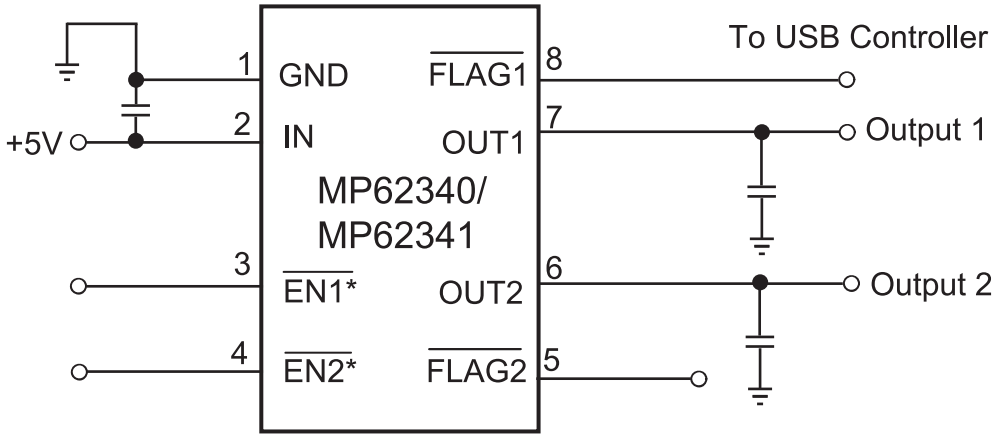
TYPICAL APPLICATION



*** EN is active high for MP62341**

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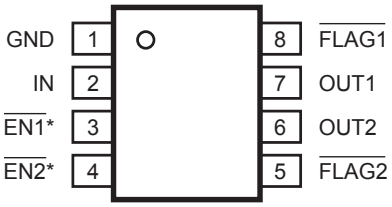
ORDERING INFORMATION

Part Number	Enable	Switch	Maximum Continuous Load Current	Typical Short-Circuit Current @ T_A=25C	Package	Top Marking	Free Air Temperature Range (T_A)
MP62340DS	Active Low	Dual	1A	1.5A	SOIC8	62340DS	–40°C to +85°C
MP62340DH					MSOP8E	62340DH	
MP62341DS	Active High				SOIC8	62341DS	
MP62341DH					MSOP8E	62341DH	

* For Tape & Reel, add suffix –Z (e.g. MP62340DS -LF–Z).
For RoHS compliant packaging, add suffix –LF (e.g. MP62340DS -LF–Z)

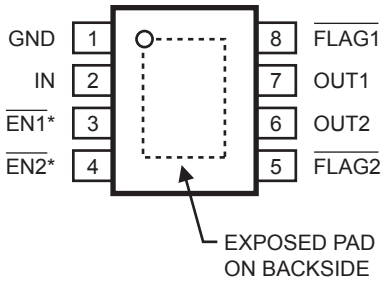
PACKAGE REFERENCE

TOP VIEW



SOIC8

TOP VIEW



MSOP8E

MP62340/MP62341

Dual-Channel

(* EN is active high for MP62341)

ABSOLUTE MAXIMUM RATINGS (1)

IN ..... -0.3V to +6.0V
EN, FLAG, OUT to GND ..... -0.3V to +6.0V
Continuous Power Dissipation (T_A = +25°C) (2)
MSOP8E 2.3W
SOIC8 ..... 1.4W
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Storage Temperature ..... –65°C to +150°C
Operating Junction Temp (T_J) ... –40°C to +125°C

Thermal Resistance (3)	θ_{JA}	θ_{JC}	
SOIC8	90	42	°C/W
MSOP8E	55	12	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of themaximum junction temperature T_J (MAX), the junction-toambient thermal resistance $\theta_{JA,}$ and the ambient temperature $T_{A.}$ The maximum allowable continuous power dissipation at any ambient temperature is calculated by PD (MAX) = (T_J (MAX) - T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Measured on JESD51-7， 4-layer PCB.

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ELECTRICAL CHARACTERISTICS (4)

V_{IN}=5V, T_A=+25°C, unless otherwise noted.

Parameter	Condition	Min	Typ	Max	Units
IN Voltage Range		2.7		5.5	V
Supply Current	One Channel Enabled, I_{OUT}=0, One Switch ON		90	120	µA
Supply Current	Both Channels Enabled, I_{OUT}=0, Both Switches ON		140	160	µA
Shutdown Current	Device Disable, V_{OUT}=float, V_{IN}=5.5V		1		µA
Off Switch Leakage	Device Disable, V_{IN}=5.5V		1		µA
Current Limit		1.1	1.5	2.2	A
Trip Current	Current Ramp (slew rate≤100A/s) on Output	1.6	1.7	2.4	A
Under-voltage Lockout	Rising Edge	1.95		2.65	V
Under-voltage Hysteresis			250		mV
FET On Resistance	I_{OUT}=100mA (-40°C≤T_J≤125°C)		80	130	mΩ
EN Input Logic High Voltage		2			V
EN Input Logic Low Voltage				0.8	V
FLAG Output Logic Low Voltage	I_{SINK}=5mA			0.4	V
FLAG Output High Leakage Current	V_{IN}=V_{FLAG}=5.5V			1	µA
Thermal Shutdown			140		°C
Thermal Shutdown Hysteresis			20		°C
V_{OUT} Rising Time, Tr (5)	V_{IN}=5.5V, C_L =1µF, R_L =5.5Ω		0.9		ms
	V_{IN}=2.7V, C_L =1µF, R_L =5.5Ω		1.7		ms
V_{OUT} Falling Time, Tf (6)	V_{IN}=5.5V, C_L =1µF, R_L =5.5Ω			0.5	ms
	V_{IN}=2.7V, C_L =1µF, R_L =5.5Ω			0.5	ms
Turn On Time, Ton (7)	C_L=100µF, R_L =5.5Ω			3	ms
Turn Off Time, Toff (8)	C_L=100µF, R_L =5.5Ω			10	ms
FLAG Deglitch Time		4	8	15	ms
EN Input Leakage			1		µA
Reverse Leakage Current	V_{OUT}=5.5V, V_{IN}=GND		0.2		µA

Notes:

4) Production test at +25°C. Specifications over the temperature range are guaranteed by design and characterization.
5) Measured from 10% to 90% output signal.
6) Measured from 90% to 10% output signal.
7) Measured from 50% EN signal to 90% output signal.
8) Measured from 50% EN signal to 10% output signal.

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PIN FUNCTIONS

SOIC8 MSOP8E	Name	Description
1	GND, Exposed Pad (MSOP8E	Ground. MSOP8E includes exposed pad. Connect to GND plane for optimal thermal operation.
2	IN	Input Voltage. Accepts 2.7V to 5.5V input.
3	$\overline{EN1}$	Active Low: (MP62340), Active High: (MP62341)
4	$\overline{EN2}$	Active Low: (MP62340), Active High: (MP62341)
5	$\overline{FLAG2}$	IN-to-OUT2 Over-current, active-low output flag. Open-Drain.
6	OUT2	IN-to-OUT2 Power-Distribution Switch Output.
7	OUT1	IN-to-OUT1 Power-Distribution Switch Output
8	$\overline{FLAG1}$	IN-to-OUT1 Over-current, active-low output flag. Open-Drain.

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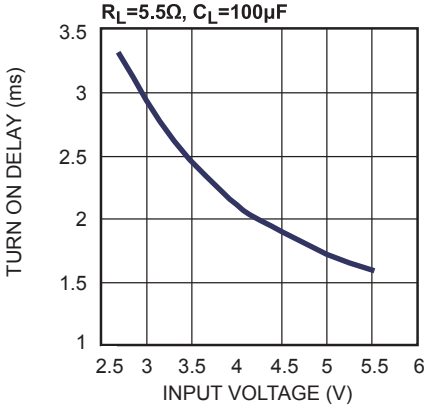
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN}=5V, C_L=1uF, T_A=25℃, for only one channel, unless otherwise noted.

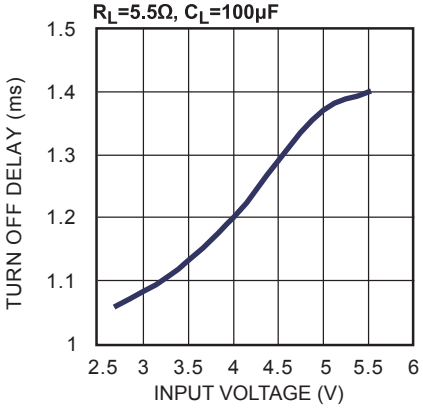
Turn on Delay vs. Input Voltage

R_L=5.5Ω, C_L=100μF



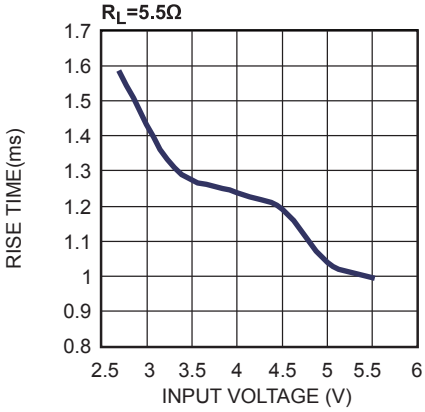
Turn off Delay vs. Input Voltage

R_L=5.5Ω, C_L=100μF



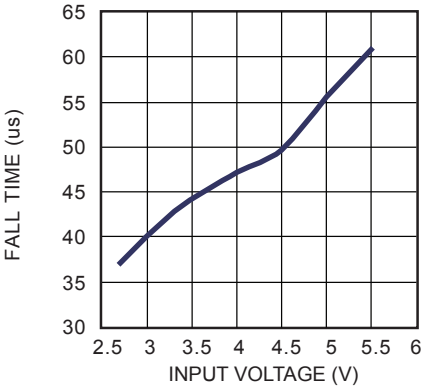
Rise Time vs. Input Voltage

R_L=5.5Ω

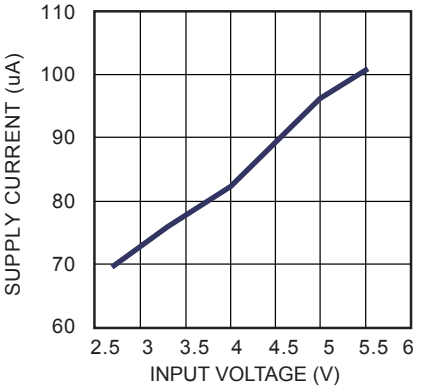


Fall Time vs. Input Voltage

R_L=5.5Ω

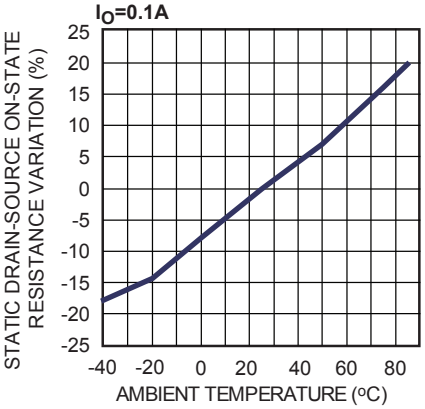


Supply Current, Output Enable vs. Input Voltage



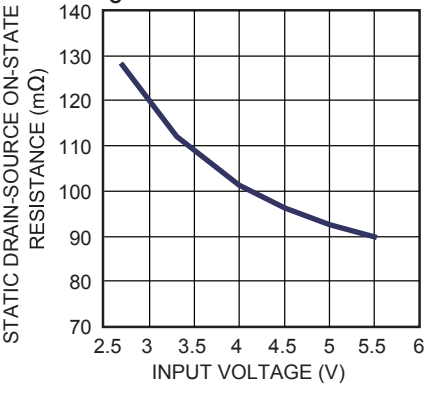
Static Drain-Source On-State Resistance Variation vs. Ambient Temperature

I_O=0.1A

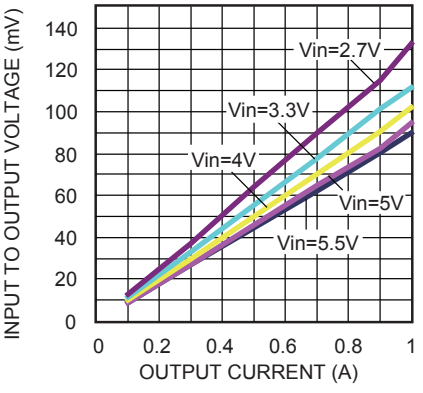


Static Drain-Source On-State Resistance vs. Input Voltage

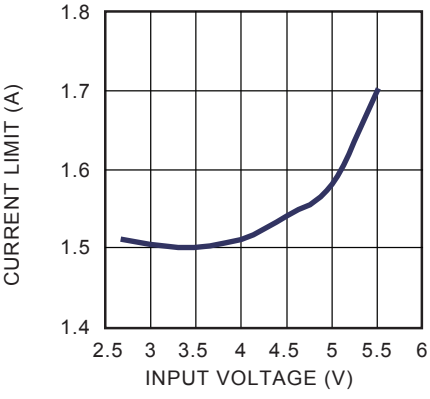
I_O=1A



Input to Output Voltage vs. Load Current



Current Limit vs. Input Voltage



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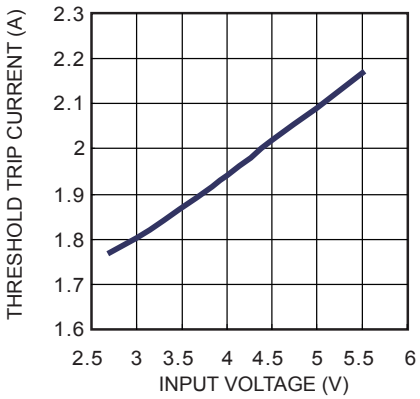
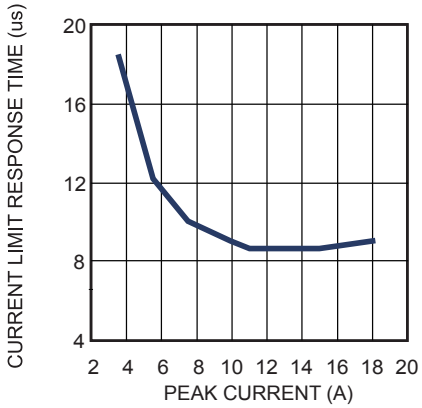
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=5V, C_L=1µF, T_A=25℃, for only one channel, unless otherwise noted.

Threshold Trip Current vs. Input Voltage

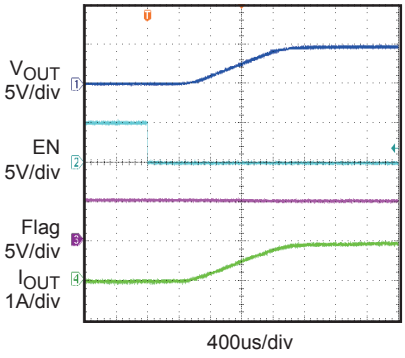


Current Limit Response Time vs. Peak Current



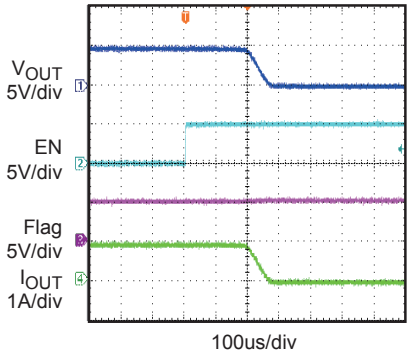
Turn On Delay and Rise Time with 1µF Load

I_{OUT}=1A



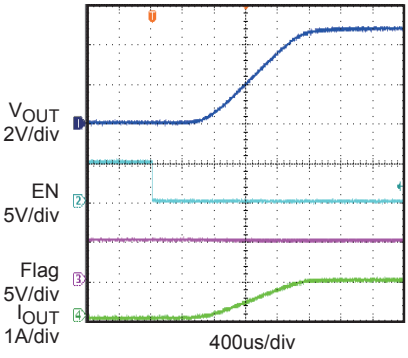
Turn Off Delay and Fall Time with 1µF Load

I_{OUT}=1A



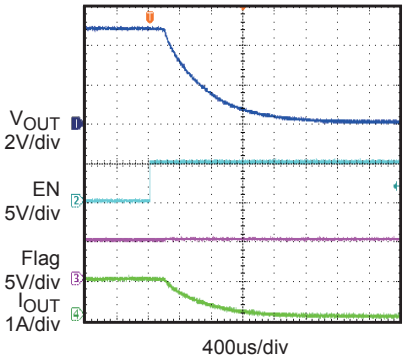
Turn On Delay and Rise Time with 100uF Load

I_{OUT}=1A, C_L=100µF

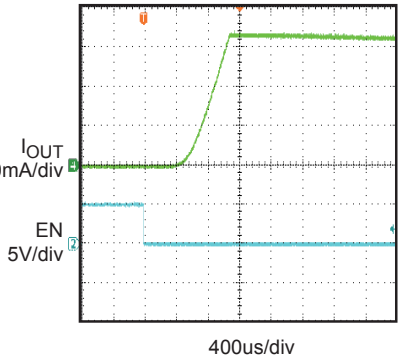


Turn Off Delay and Fall Time with 100µF Load

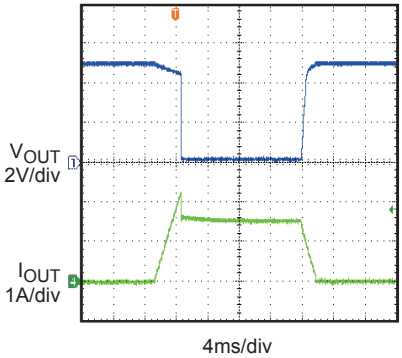
I_{OUT}=1A, C_L=100µF



Short Circuit Current, Device Enabled into Short



Threshold Trip Current with Ramped Load on Enabled Device



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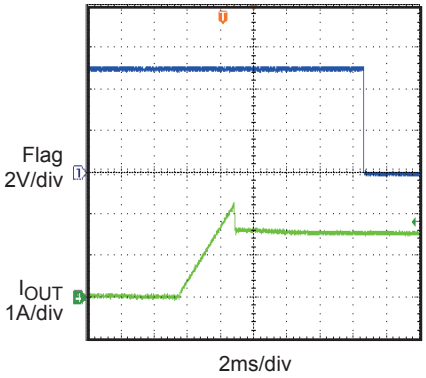
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

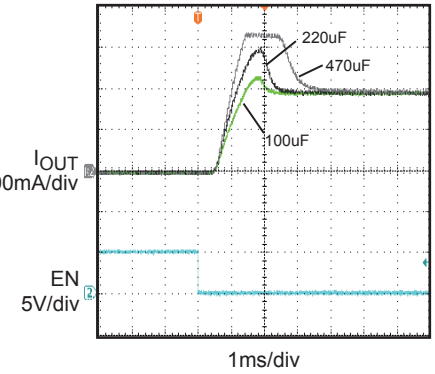
V_{IN}=5V, C_L=1μF, T_A=25℃, for only one channel, unless otherwise noted.

Ramped Load on Enabled Device

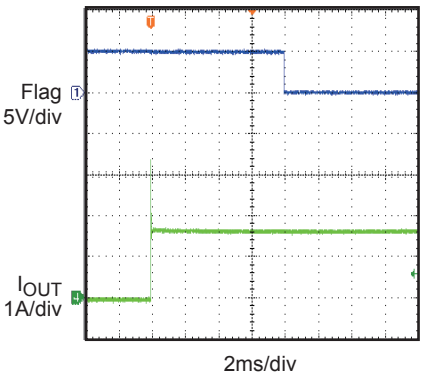


Inrush Current with Different Load Capacitance

I_{OUT}=1A



1Ω Load Connected to Enabled Device



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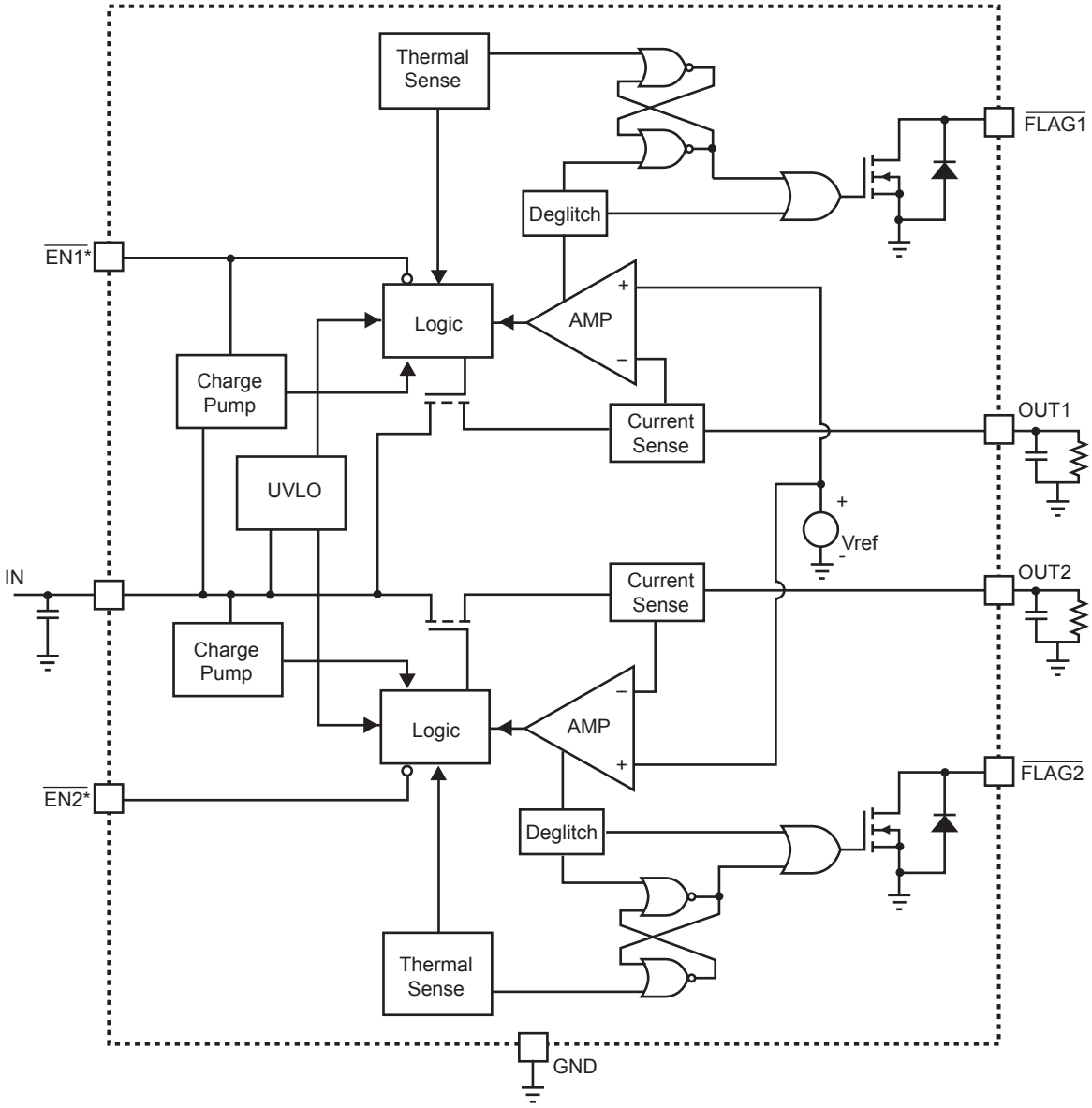
FUNCTION BLOCK DIAGRAM



*** EN is active high for MP62341**

Figure 2—Functional Block Diagram

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DETAILED DESCRIPTION

Over Current

When the load exceeds trip current (minimum threshold current triggering constant-current mode) or a short is present, MP62340/MP62341 switches into to a constant-current mode (current limit value). MP62340/MP62341 will be shutdown only if the over current condition stays long enough to trigger thermal protection.

Trigger over current protection for different overload conditions occurring in applications:

1) The output has been shorted or overloaded before the device is enabled or input applied. MP62340/MP62341 detects the short or overload and immediately switches into a constant-current mode.
2) A short or an overload occurs after the device is enabled. After the current-limit circuit has been tripped (reached the trip current threshold), the device switches into constant-current mode. However, high current may flow for a short period of time before the current-limit circuit can react.
3) Output current has been gradually increased beyond the recommended operating current. The load current rises until the trip current threshold is reached or until the thermal limit of the device is exceeded. MP62340/ MP62341 is capable of delivering current up to the trip current threshold without damaging the device. Once the trip threshold has been reached, the device switches into its constant-current mode.

Flag Response

The FLAG pin is an open drain configuration. This FAULT will report a fail mode after an 8ms deglitch timeout. This is used to ensure that no false fault signals are reported. This internal deglitch circuit eliminates the need for extend components. The FLAG pin is not deglitched during an over temp. or voltage lockout.

Thermal Protection

The purpose of thermal protection is to prevent damage in the IC by allowing exceptive current to flow and heating the junction. The die temp. is internally monitored until the thermal limit is reached. Once this temp. is reached, the switch will turn off and allow the chip to cool. The switch has a built-in hysteresis.

Under-voltage Lockout (UVLO)

This circuit is used to monitor the input voltage to ensure that the MP62340/MP62341 is operating correctly. This UVLO circuit also ensures that there is no operation until the input voltage reaches the minimum spec.

Enable

The logic pin disables the chip to reduce the supply current. The device will operate once the enable signal reaches the appropriate level. The input is compatible with both COMS and TTL.

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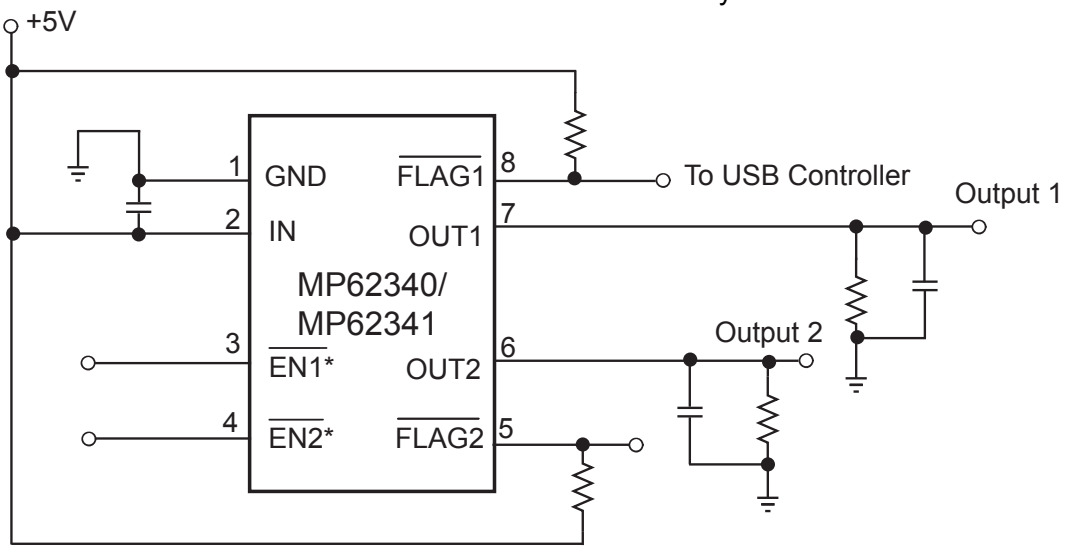
APPLICATION INFORMATION

Power-Supply Considerations

Over 10μF capacitor between IN and GND is recommended. This precaution reduces power-supply transients that may cause ringing on the input and improves the immunity of the device to short-circuit transients.

In order to achieve smaller output load transient, placing a high-value electrolytic capacitor on the output pin(s) is recommended when the output load is heavy.



*** EN is active high for MP62341**

Figure 3—Application Circuit

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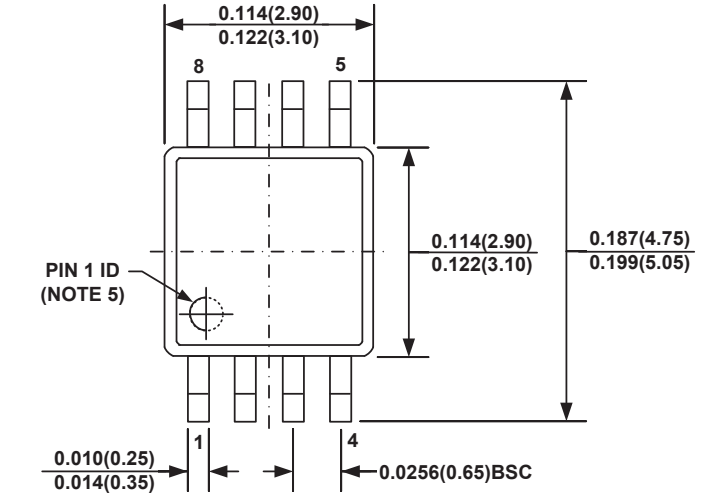
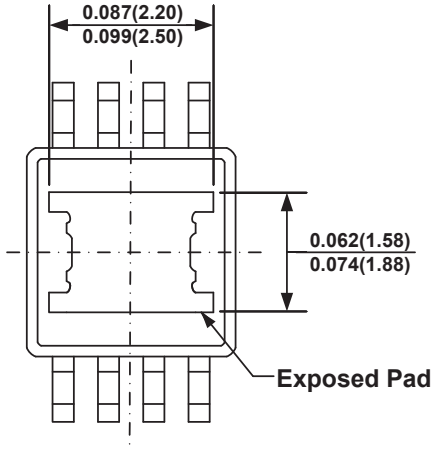
PACKAGE INFORMATION

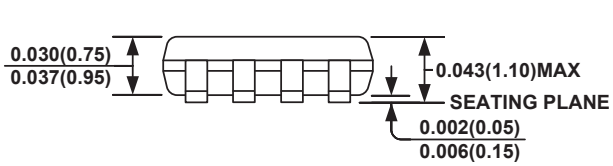
MSOP8E (EXPOSED PAD)



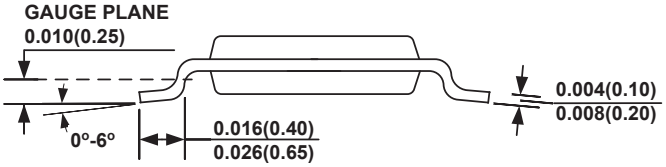
TOP VIEW



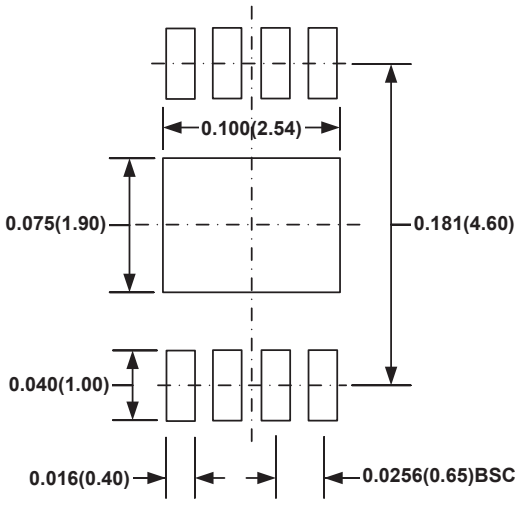
BOTTOM VIEW



FRONT VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) PIN 1 IDENTIFICATION HAS HALF OR FULL CIRCLE OPTION.
6) DRAWING MEETS JEDEC MO-187, VARIATION AA-T.
7) DRAWING IS NOT TO SCALE.

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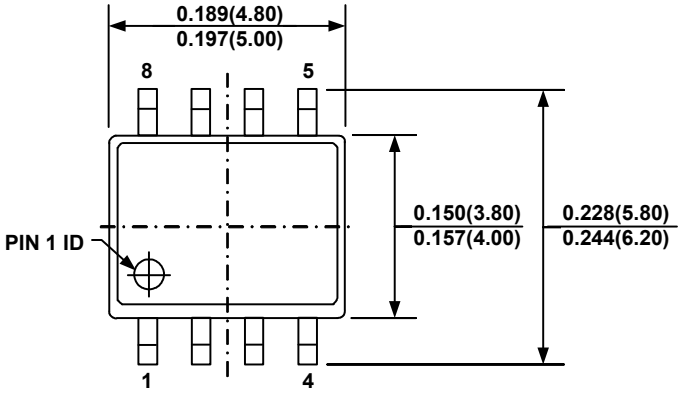
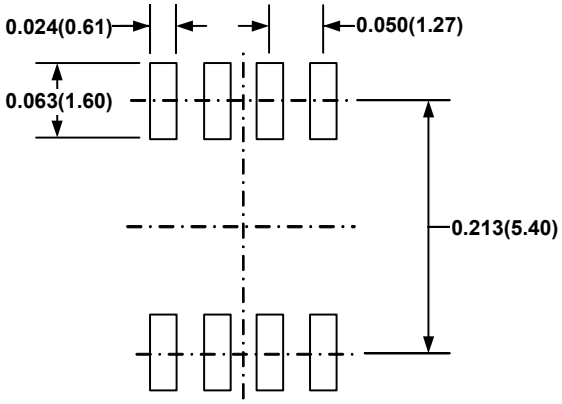
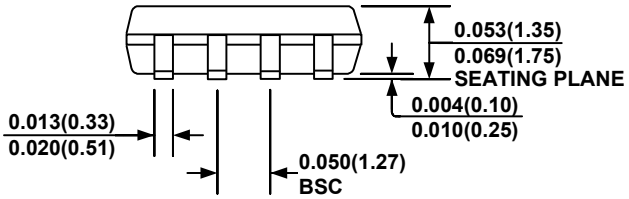
SOIC8



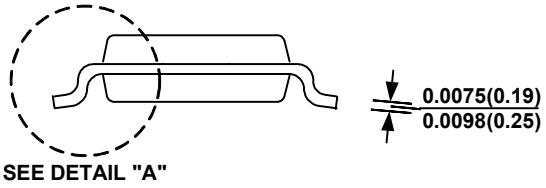
TOP VIEW



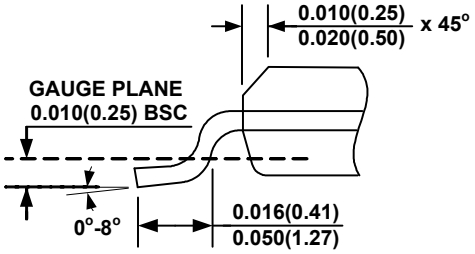
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

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