September 2009

TLE5012
TLE5012-E0318
TLE5012-E0742

GMR-Based Angular Sensor
for Rotor Position Sensing

Target

Data Sheet

V 0.46

Sensors

Never stop thinking

Edition 2009-09

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TLE5012 GMR-Based Angular Sensor

Revision History: 2009-09, V 0.46

Previous Version: V0.41

Page	Subjects (major changes since last revision)
13	PRO-SIL Disclaimer added
17	Table 2, Magnetic Field Induction and Storage Temperature amended
22	Table 8, Angle Delay Time with Prediction added, Figure 12 updated
27	Table 13, Lock updated; more detailed description of CMD word
28	Table 14, STAT updated
31-46	Registertype updated
47	Table 16 notes amended
52	Chapter 3.6 addded
general	Correction of typing errors

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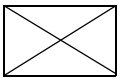
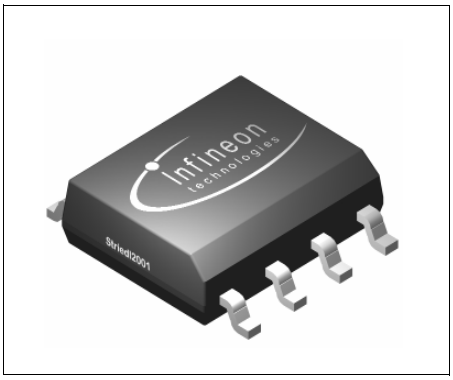


1 Product Description



1.1 Overview

The TLE5012 is a 360° angle sensor that detects the orientation of a magnetic field. This is achieved by measuring sine and cosine angle components with monolithic **i**ntegrated **G**iant **M**agneto **R**esistance (**iGMR**) elements.

High precision angle values are achieved over temperature and lifetime using internal autocalibration algorithm.

Data communications are accomplished with a bi-directional SSC Interface that is SPI compatible.

The absolute angle value and other values are transmitted via SSC or via a Pulse-Width-Modulation (PWM) Protocol. Also the sine and cosine raw values can be read out. These raw signals are digitally processed internally to calculate the angle orientation of the magnetic field (magnet).

The TLE5012 is a precalibrated sensor. The calibration parameters are stored in laser fuses. At start-up the values of the fuses are written into Flip-Flops, where these values can be changed by the application specific parameters. The TLE5012-E0318 and TLE5012-E0742 are especially configured in a Hall-Switch emulation mode for motors with three or seven pole pairs.

Online diagnostic functions are provided to ensure reliable operation.

Product Type	Marking	Ordering Code	Package
TLE5012	5012	SP000477068	PG-DSO-8
TLE5012-E0318	5012E03	SP000611246	PG-DSO-8
TLE5012-E0742	5012E07	SP000611250	PG-DSO-8

1.2 Features

- **G**iant **M**agneto **R**esistance (GMR)-based principle
- Integrated magnetic field sensing for angle measurement
- Full calibrated 0 - 360° angle measurement with revolution counter and angle speed measurement
- Two separate highly accurate single bit SD-ADC
- 15 bit representation of absolute angle value on the output (resolution of 0.01°)
- 16 bit representation of sine / cosine values on the interface
- Max. 1.0° angle error over lifetime and temperature with activated auto-calibration
- Bi-directional SSC Interface up to 8Mbit/s
- Supports SIL3 with diagnostic functions and status information
- Interfaces: SSC, PWM, Incremental Interface (IIF), Hall Switch Mode (HSM)
- 0.25 µm CMOS technology
- Automotive qualified: -40°C to 150°C (Junction Temperature)
- ESD > 2kV (HBM)
- Green package with lead-free (Pb-free) plating

1.3 Application Example

The TLE5012 GMR-Based Angular Sensor is designed for angular position sensing in automotive applications, such as:

- Electrical Commutated Motor (e.g. used in **E**lectric **P**ower **S**teering (**EPS**))
- Rotary Switch
- Steering Angle
- General Angular Sensing

2 Functional Description

2.1 General

The GMR sensor is implemented using vertical integration. This means that the GMR sensitive areas are integrated above the logic portion of the TLE5012 device. These GMR elements change their resistance depending on the direction of the magnetic field.

Four individual GMR elements are connected to one Wheatstone Sensor Bridge. These GMR elements sense one of two components of the applied magnetic field:

- X component, V_x (cosine) or the
- Y component, V_y (sine)

The advantage of a full-bridge structure is that the amplitude of the GMR signal is doubled and temperature effects cancel out each other.

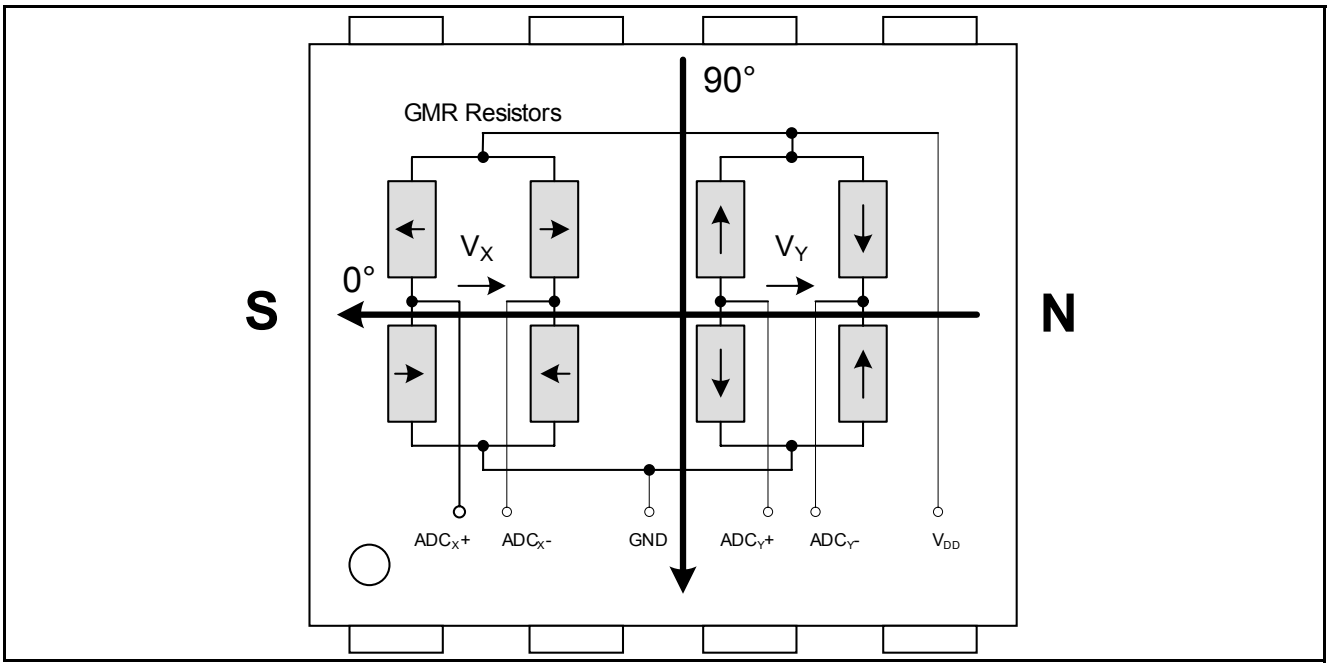


Figure 1 Sensitive Bridges of the GMR Sensor

*Note: In **Figure 1**, the arrows in the resistors symbolize the direction of the Reference Layer, which is used for the further explanation.*

The output signal of each bridge is only unambiguous over 180° between two maxima. Therefore two bridges are orientated orthogonally to each other to measure 360°.

With the trigonometric function ARCTAN, the true 360° angle value can be calulated which is represented by the relation of X and Y signals.

Because only the relative values influence the result, the absolute size of the two signals is of minor importance. Therefore, most influences to the amplitudes are compensated.

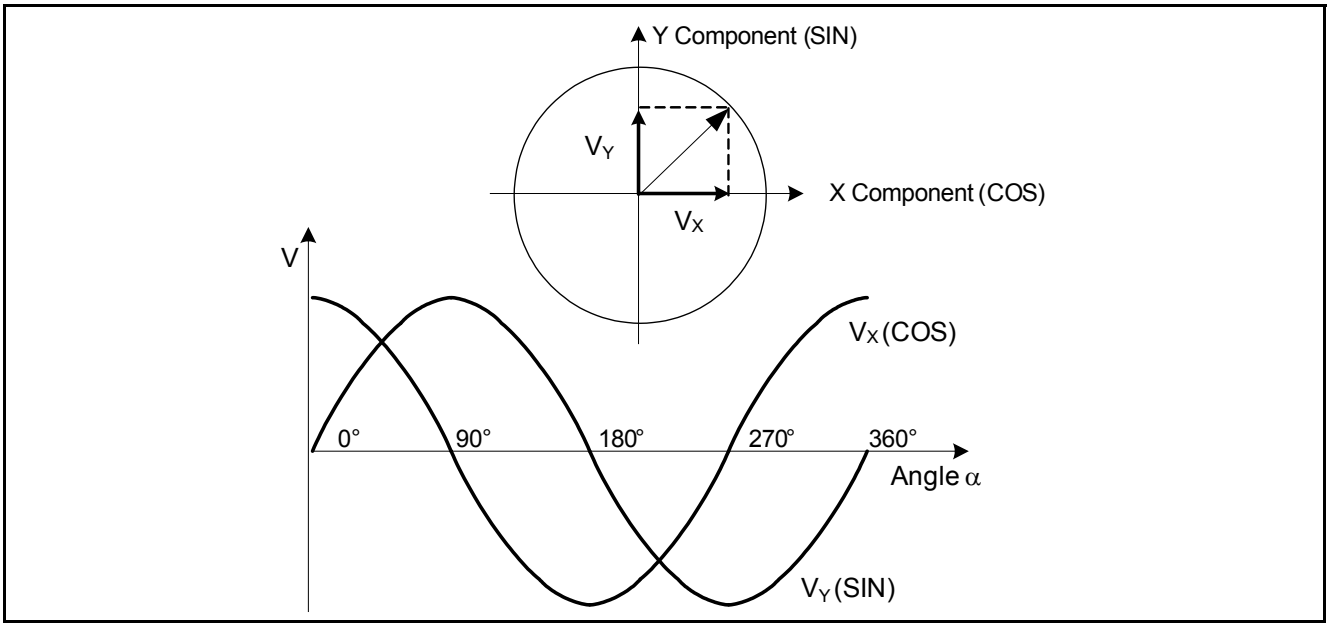


Figure 2 Ideal Output of the GMR Sensor Bridges

2.2 Pin Configuration

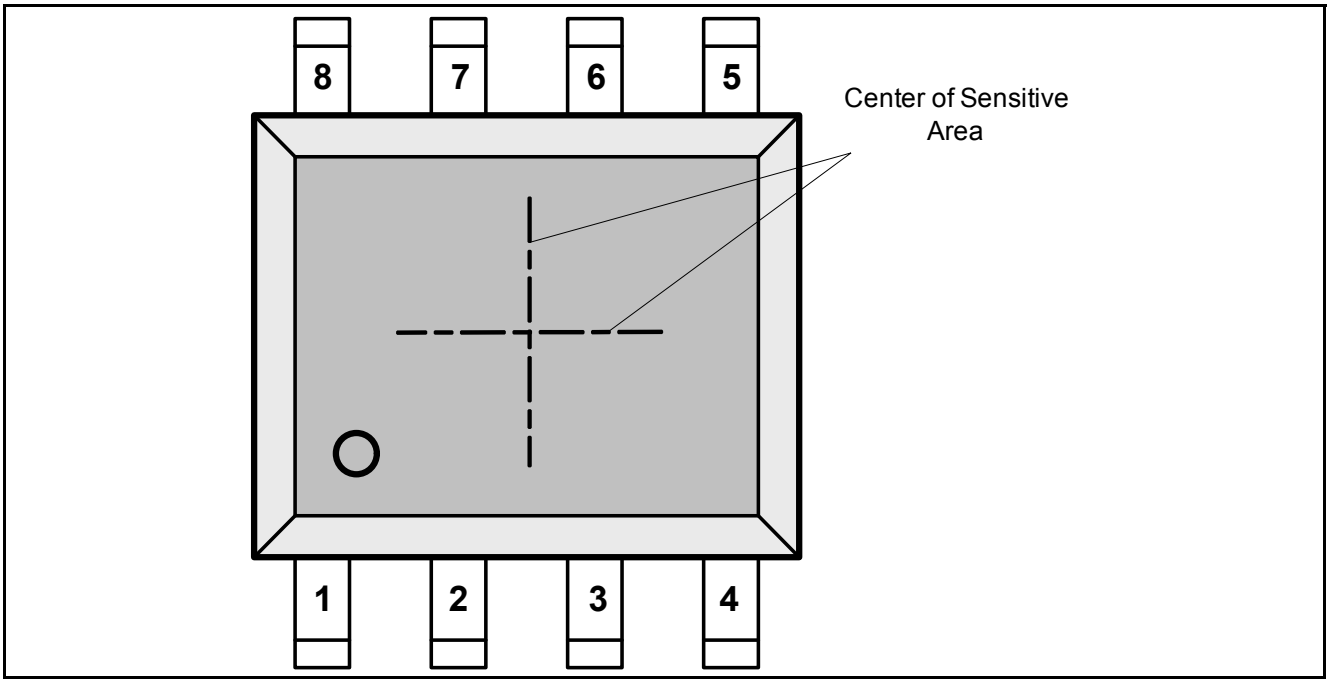


Figure 3 Pin Configuration (Top View)

2.3 Pin Description

Table 1 Pin Description

Pin No.	Symbol	In/Out	Function
1	CLK	I	External Clock (must be connected to GND for PWM output)
2	SCK	I	SSC Clock
3	CSQ	I	SSC Chip Select
4	DATA / HS3	I/O	SSC Data / IIF Index / Hall Switch Signal 3
5	IFA (IIF_A / HS1 / PWM)	O	Interface A: IIF Phase A; Hall Switch Signal 1 or PWM output (depends on external application circuit)
6	V_{DD}	-	Supply Voltage
7	GND	-	Ground
8	IFB (IIF_B / HS2)	O	Interface B: IIF Phase B or Hall Switch Signal 2

2.4 Block Diagram

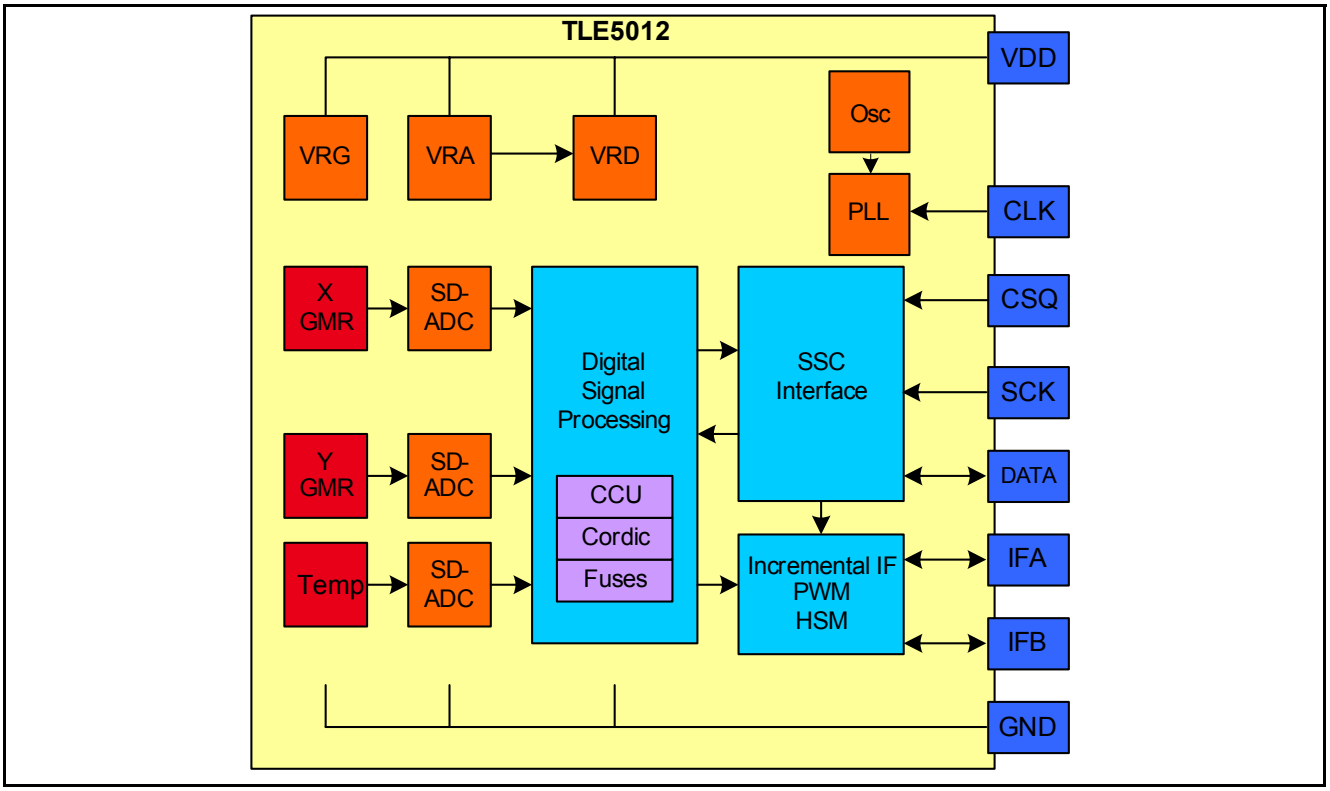


Figure 4 TLE5012 Block Diagram

2.5 Functional Block Description

2.5.1 Internal Power Supply

The internal stages of the TLE5012 are supplied with different voltage regulators.

- GMR Voltage Regulator VRG
- Analog Voltage Regulator VRA
- Digital Voltage Regulator VRD (derived from VRA)

These regulators are directly connected to the supply voltage V_{DD}.

2.5.2 Oscillator and PLL

The internal frequency oscillator feeds the **P**hase **L**ocked **L**oop (**PLL**). Also the external clock (CLK) can be used therefore.

2.5.3 SD-ADC

The SD-ADCs transform the analog GMR-voltages and temperature-voltage into the digital domain.

2.5.4 Digital Signal Processing Unit

The Digital Signal Processing Unit (DSPU) contains the:

- **C**apture **C**ompare **U**nit (**CCU**), which is used to generate the PWM signal
- **CO**ordinate **R**otation **DI**gital **C**omputer (**CORDIC**), which contains the trigonometric function for angle calculation
- Fuses, which contain the calibration parameters

2.5.5 Interfaces

Different Interfaces can be selected:

- SSC Interface
- PWM
- Incremental Interface
- Hall Switch Mode

2.5.6 Safety Features

The TLE5012 offers a multiplicity on safety features to support Safety Integrity Level (SIL). Sensors with this performance are identified by the following logo:

Figure 5 PRO-SIL™ Logo

Safety features are:

- Test vectors switchable to ADC- input
- Inversion or combination of filter input streams
- Data transmission check via 8bit **C**yclic **R**edundancy **C**heck (**CRC**)
- Self test routines
- Two independent active interfaces possible
- Overvoltage and undervoltage detection

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SIL respectively A-SIL certification for such a System has to be reached on system level by the System Responsible at an accredited Certification Authority.

SIL stands for Safety Integrity Level (according to IEC 61508)

A-SIL stands for Automotive-Safety Integrity Level (according to ISO 26262)

3 Specification

3.1 Application Circuit

The application circuit in **Figure 6**, **Figure 7**, **Figure 8** and **Figure 9** show the different communication possibilities of TLE5012.

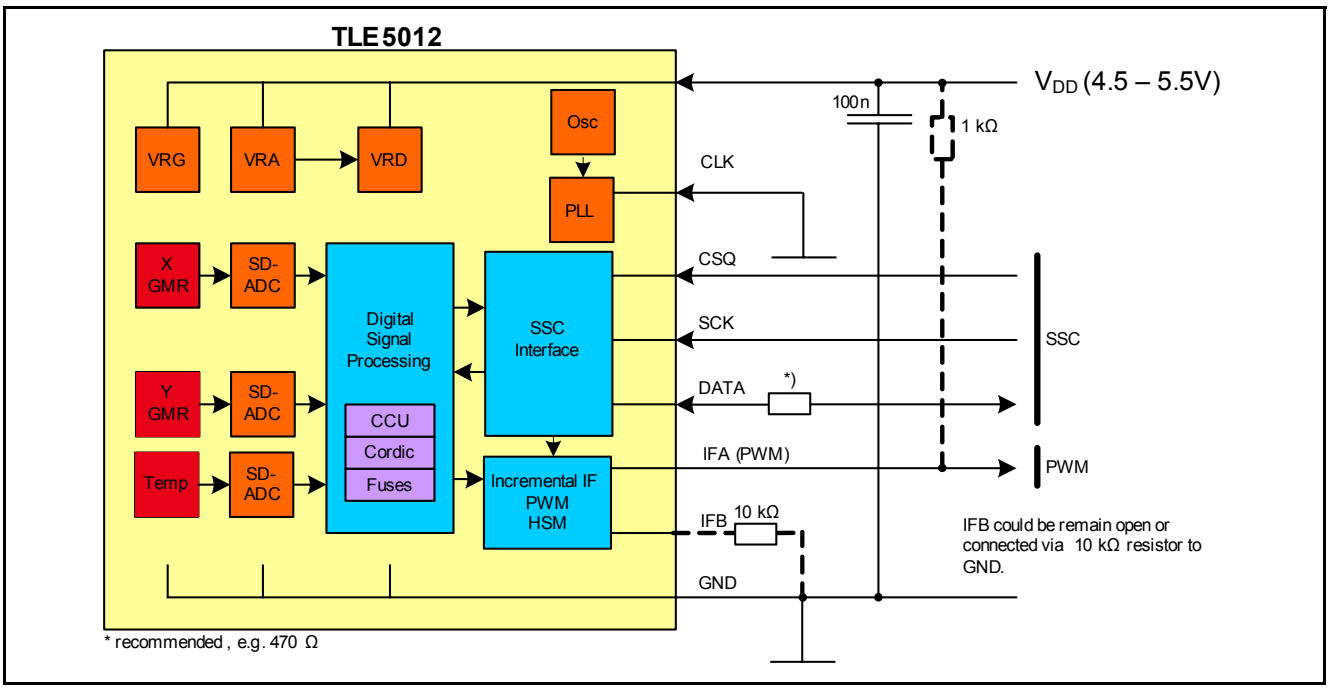


Figure 6 Application Circuit for TLE5012 with SSC and PWM Interface (using internal CLK)

Figure 6 shows a basic block-diagram of the TLE5012 with PWM- Interface. This interface is selectable by connecting CLK to GND. Additionally to the PWM the SSC Interface could be used. Within the SSC- Interface the PWM mode is selectable between Push-Pull and Open Drain.

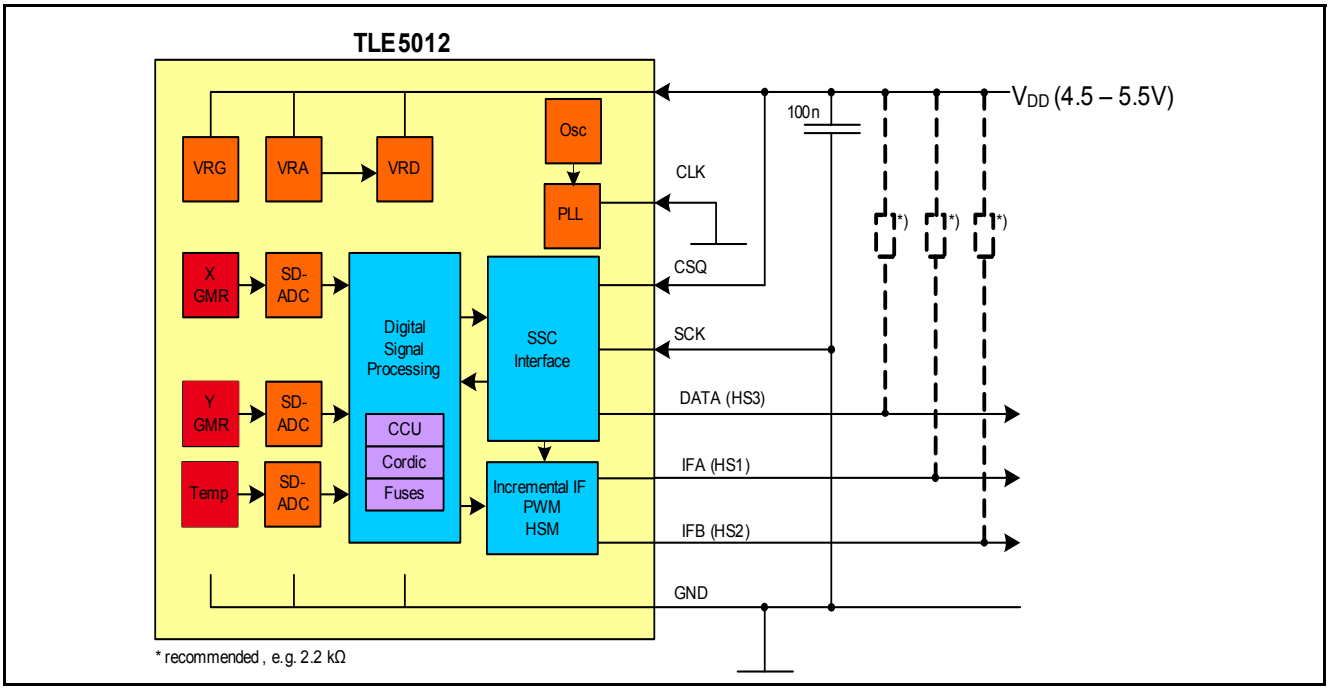


Figure 7 Application Circuit for TLE5012 with HS Mode (using internal CLK)

Figure 7 shows a basic block-diagram of the TLE5012 with HS Mode. This interface is selectable by connecting CLK to GND and CSQ to V_{DD}. Additionally to the HSM the SSC Interface could be used by pulling CSQ to GND. Within the SSC- Interface the HS Mode is selectable between Push-Pull and Open Drain.

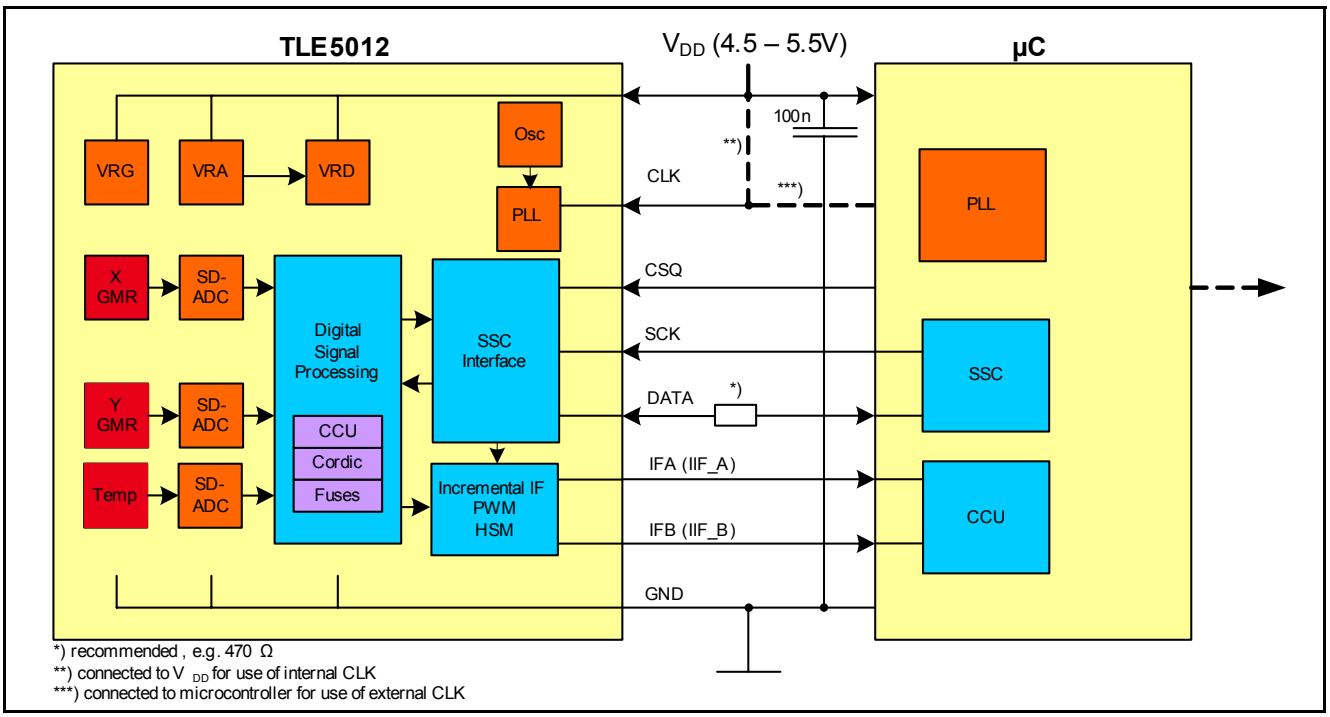


Figure 8 Application Circuit for TLE5012 with SSC and IIF Interface (using external CLK)

Figure 8 shows a basic block-diagram of an angle sensor system using a TLE5012 and a microcontroller for rotor positioning applications. The depicted Interface-Configuration is needed for High-Speed applications like electrical commutated motor drives. It is possible to connect the TLE5012 to a microcontroller via Incremental Interface and for safety reasons also via SSC-Interface.

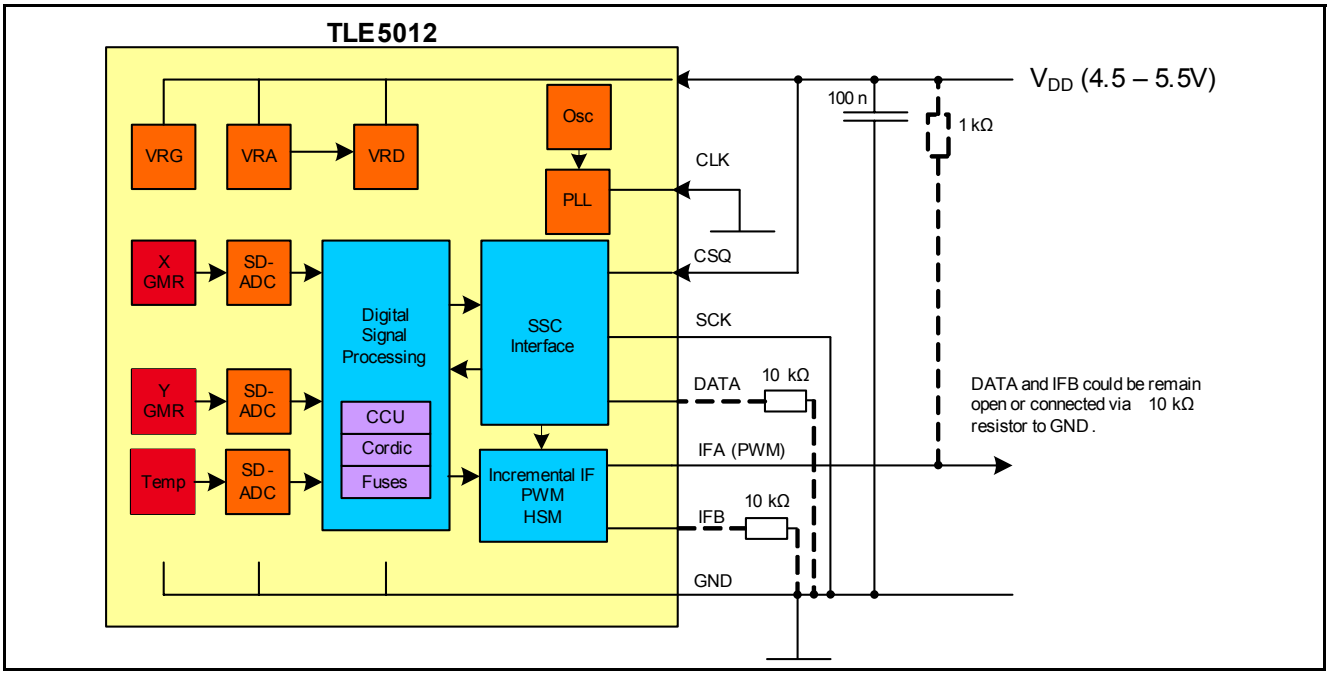


Figure 9 Application Circuit for TLE5012 with only PWM Interface (using internal CLK)

3.2 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Voltage on V_{DD} pin respect to ground (V_{SS})	V_{DD}	-0.5	-	6.5	V	max 40 h/Lifetime
Voltage on any pin respect to ground (V_{SS})	V_{IN}	-0.5	-	6.5	V	additionally V_{DD} + 0.5 V may not be exceeded
Junction Temperature	T_J	-40	-	150	°C	
		-	-	150	°C	for 1000h not additive
Magnetic Field Induction	B	-	-	|125|	mT	max. 5 min @ t_A = 25°C
		-	-	|100|	mT	max. 5 h @ t_A = 25°C
		-	-	|70|	mT	max. 1000h @ t_A = 85°C; not additive
		-	-	|60|	mT	max. 1000h @ t_A = 100°C; not additive
Storage Temperature	T_{ST}	-40	-	150	°C	without magnetic field

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the device.

3.3 Operating Range

The following operating conditions must not be exceeded in order to ensure correct operation of the TLE5012. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed. **Table 3** is valid for -40°C < T_J < 150°C.

Table 3 Operating Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply Voltage	V_{DD}	4.5	5.0	5.5	V	1)
Output Current (DATA-Pad)	I_Q	-	-	-25	mA	PAD_DRV =’0x’, sink current2)
		-	-	-5	mA	PAD_DRV =’10’, sink current2)
		-	-	-0.4	mA	PAD_DRV =’11’, sink current2)
Output Current (IFA / IFB-Pad)	I_Q	-	-	-15	mA	PAD_DRV =’0x’, sink current2)
		-	-	-5	mA	PAD_DRV =’1x’, sink current2)
Input Voltage	V_{IN}	-0.3	-	5.5	V	V_{DD} + 0.3 V may not be exceeded

Table 3 Operating Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Magnetic Induction	B_{XY}	30	-	50	mT	in X/Y direction[3)]
Angle Range	Ang	0	-	360	°	

1) Directly blocked with 100nF ceramic capacitor
2) Max. current to GND over Open Drain Output
3) Values refer to an homogenous magnetic field (B_{XY}) without vertical magnetic induction (B_Z = 0mT).

Note: The thermal resistances listed in ***Table 20 "Package Parameters" on Page 55*** *must be used to calculate the corresponding ambient temperature.*

Calculation of the Junction Temperature

The total power dissipation PTOT of the chip increases its temperature above the ambient temperature.

The power multiplied by the total thermal resistance RthJA (Junction to Ambient) leads to the final junction temperature. RthJA is the sum of the addition of the values of the two components Junction to Case and Case to Ambient.

$$R_{thJA} = R_{thJC} + R_{thCA} \quad (1)$$

$$T_J = T_A + \Delta T$$

$$\Delta T = R_{thJA} \times P_{TOT} = R_{thJA} \times (V_{DD} \times I_{DD} + V_{OUT} \times I_{OUT}) \quad (I_{DD}, I_{OUT} > 0, \text{ if direction is into IC})$$

Example (assuming no load on V_{out}):

$$V_{DD} = 5V \quad (2)$$

$$I_{DD} = 12mA$$

$$\Delta T = 150\left[\frac{K}{W}\right] \times 5[V] \times 0.012[A] + 0[VA] = 9K$$

For moulded sensors, the calculation with RthJC is more adequate.

3.4 Characteristics

3.4.1 Electrical Parameters

The indicated electrical parameters apply to the full operating range, unless otherwise specified. The typical values correspond to a supply voltage V_{DD} = 5.0 V and 25 °C, unless individually specified. All other values correspond to -40 °C < T_J < 150°C.

Table 4 Electrical Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply Current	I_{DD}	-	12	13	mA	
POR Level	V_{POR}	2.0	-	2.9	V	Power On Reset
POR Hysteresis	V_{PORhy}	-	30	-	mV	
Power On Time	t_{Pon}	-	4	5	ms	$V_{DD} > V_{DDmin}$ 1)
Input Signal Low Level	V_L	-	-	0.3 V_{DD}	V	
Input Signal High Level	V_H	0.7 V_{DD}	-	-	V	
Pull-Up Current	I_{PU}	-10	-	-225	µA	CSQ
		-10	-	-150	µA	DATA
Pull-Down Current	I_{PD}	10	-	225	µA	SCK
		10	-	150	µA	CLK, IFA, IFB
Output Signal Low Level	V_{OL}	-	-	1	V	DATA; I_Q = - 25 mA (PAD_DRV='0x'), I_Q = - 5 mA (PAD_DRV='10'), I_Q = - 0.4 mA (PAD_DRV='11')
		-	-	1	V	IFA,IFB; I_Q = - 15 mA (PAD_DRV='0x'), I_Q = - 5 mA (PAD_DRV='1x')

1) Within "Power On Time" write access is not permitted

3.4.2 ESD Protection

Table 5 ESD Protection

Parameter	Symbol	Values		Unit	Notes
		min.	max.		
ESD Voltage	V_{HBM}	-	±2.0	kV	Human Body Model 1)
	V_{SDM}	-	±0.5	kV	Socketed Device Model 2)

1) Human Body Model (HBM) according to: JEDEC EIA/JESD22-A114-B

2) Socketed Device Model (SDM) according to: ESD ASS.STD.DS5.3-93

3.4.3 GMR Parameters

All parameters apply over the full operating range, unless otherwise specified.

Table 6 Basic GMR Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
X, Y output range	RG_{ADC}	-	-	±23230	digits	
X, Y amplitude [1]	A_X, A_Y	6000	9500	15781	digits	at calibration conditions
		3922	-	20620	digits	operating range
X, Y synchronism [2]	k	87.5	100	112.49	%	at calibration conditions
X, Y offset [3]	O_X, O_Y	-2048	0	+2047	digits	at calibration conditions
X, Y orthogonality error	φ	-11.25	0	+11.24	°	at calibration conditions
X, Y without field	X_0, Y_0	-5000	-	+5000	digits	without magnet [4]

1) see **Figure 10**
2) $k = 100*(A_X/A_Y)$
3) $O_Y=(Y_{MAX} + Y_{MIN}) / 2$; $O_X = (X_{MAX} + X_{MIN}) / 2$
4) Not tested

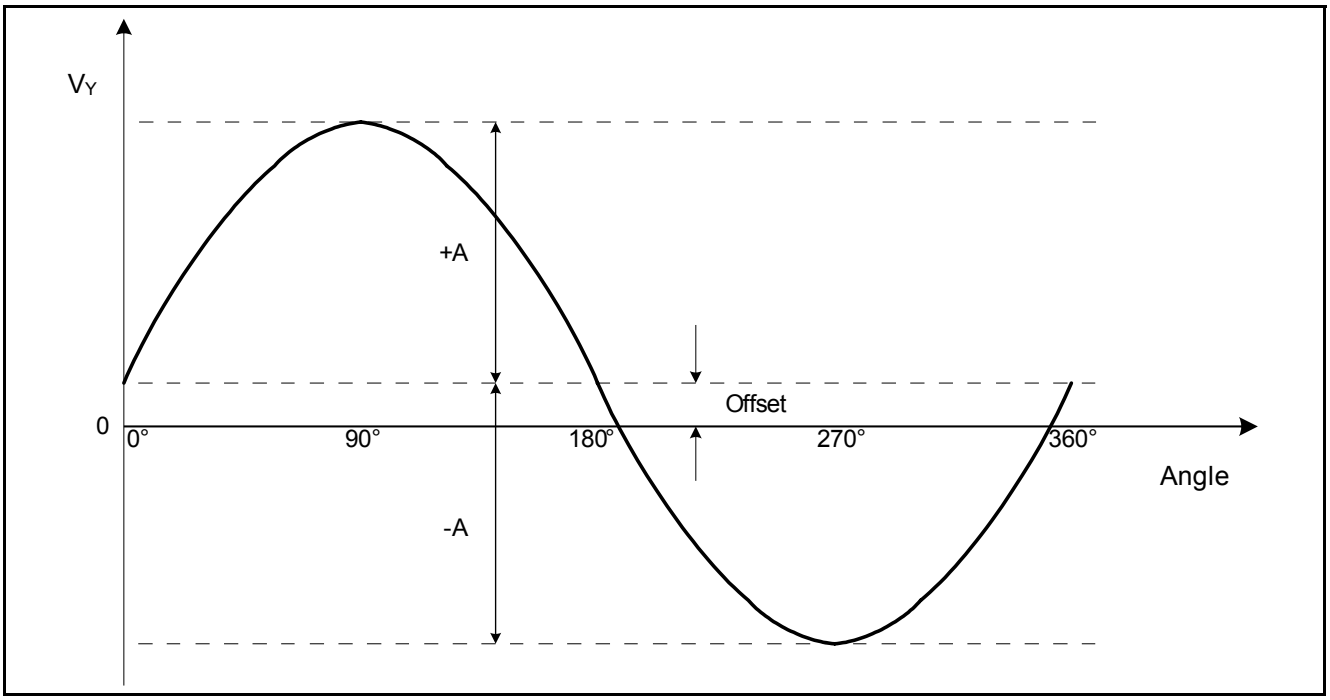


Figure 10 Offset and Amplitude Definition

3.4.4 Angle Performance

After internal calculation the sensor has a remaining error, as shown in **Table 7**. The error value refers to B_Z = 0mT and the operating conditions given in **Table 3 "Operating Range" on Page 17**.

The overall angle error represents the relative angle error. This error describes the deviation to the reference line after zero angle definition.

Table 7 Angle Performance

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Overall Angle Error (with auto-calibration)	α_{Err}	-	0.6[1)]	1.0	°	including lifetime and temperature drift[2)3)]
Overall Angle Error (without auto-calibration)	α_{Err}	-	0.6[1)]	1.6	°	including temperature drift[2)3)]

1) At 25°C, B =30 mT

2) Including hysteresis error, caused by revolution direction change.

3) Only with calibrated GMR-compensation parameters of customer setup; Relative error after zero angle definition.

Autocalibration

The autocalibration enables online parameter calculation and reduces therefore the angle error due to misalignments.

After start-up the parameters out of the fuses get loaded into flip-flops. The TLE5012 updates these parameters after a full revolution. The update can be chosen within the Autocalibration Mode (AUTOCAL) bit. It is possible to do the update after every 22.5°, 11.25° or after t_{upd}.

3.4.5 Signal Processing

The signal path of the TLE5012 is depicted in **Figure 11**. It consists of the GMR-bridge, ADC, filter and angle calculation. Depending on the filter configuration a different total delay time is achieved. Additional to this delay time, the delay time of the interface has to be considered. The delay time leads to an additional angle error at higher speeds. With enabling the prediction, the signal delay time will be reduced (**Figure 12**).

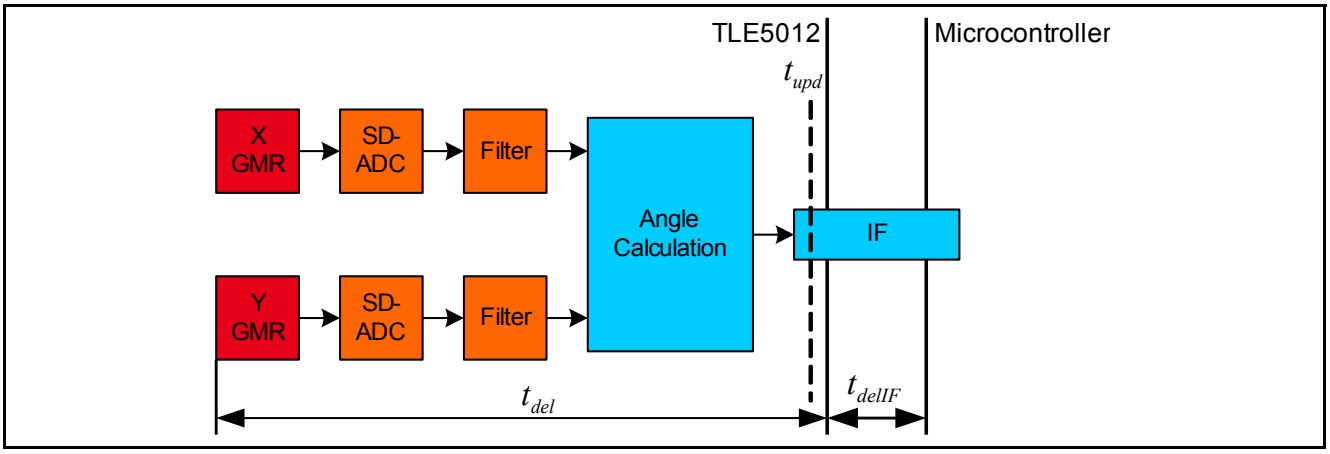


Figure 11 TLE5012 Signal path

At FIR_MD = 0 only raw values can be read out, due to the more time consuming angle calculation.

Table 8 Signal Processing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Update Rate at Interface	t_{upd}	-	21.3	-	µs	FIR_MD = 0 (only raw values)[1)2)]
		-	42.7	-	µs	FIR_MD = 1[1)2)]
		-	85.3	-	µs	FIR_MD = 2 (default)[1)2)]
		-	170.6	-	µs	FIR_MD = 3[1)2)]
Angle Delay Time[3)]	t_{del}	-	60	70	µs	FIR_MD = 1[1)2)]
		-	80	95	µs	FIR_MD = 2[1)2)]
		-	120	140	µs	FIR_MD = 3[1)2)]
Angle Delay Time with Prediction[3)]	t_{del}	-	20	30	µs	FIR_MD = 1; PREDICT = 1 [1)2)]
		-	5	20	µs	FIR_MD = 2; PREDICT = 1 [1)2)]
		-	-40	-20	µs	FIR_MD = 3; PREDICT = 1 [1)2)]
Angle Noise	N_{Angle}	-	0.11	-	°	FIR_MD = 0, (1 Sigma)[2)]
		-	0.08	-	°	FIR_MD = 1, (1 Sigma)[2)]
		-	0.05	-	°	FIR_MD = 2, (1 Sigma)[2)] (default)
		-	0.04	-	°	FIR_MD = 3, (1 Sigma)[2)]

1) depends on internal oscillator frequency variation (**Chapter 3.4.6**)
2) guaranteed by laboratory characterization
3) valid at constant rotation speed

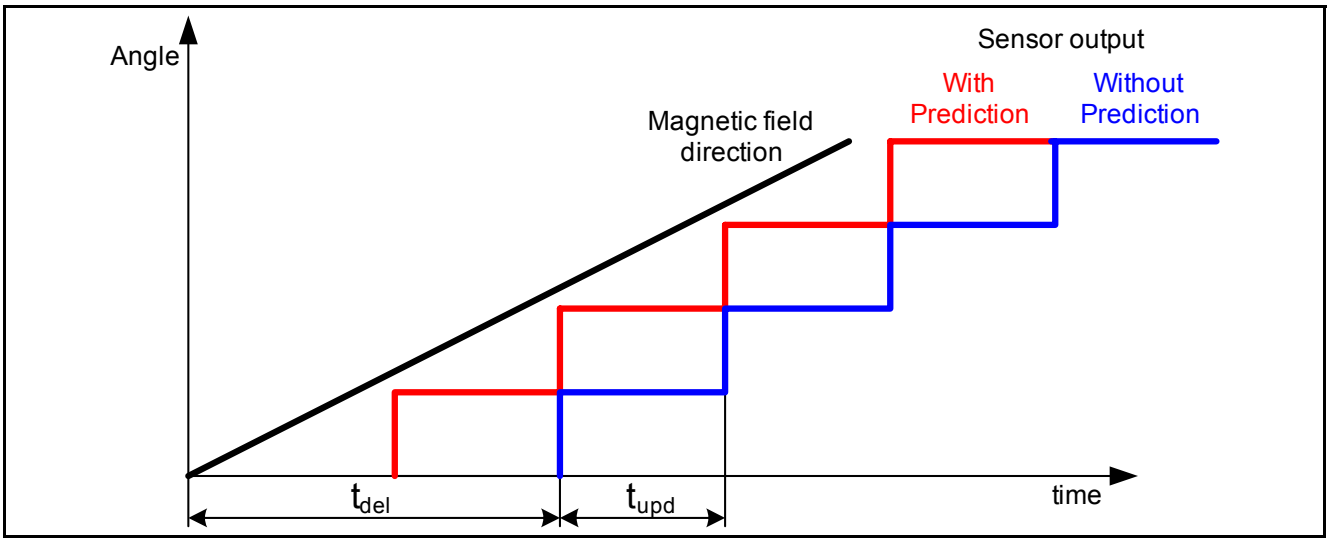


Figure 12 Delay of Sensor Output

3.4.6 Clock Supply (CLK Timing Definition)

If the external clock supply is selected, the clock signal input 'CLK' must fulfill certain requirements which are described in the following:

- The high or low pulse width must not exceed the specified values, because the PLL needs a minimum pulse width and must be spike filtered.
- The duty cycle factor should be 0.5 but can deviate to the values limited by $t_{CLKh(f\_min)}$ and $t_{CLKl(f\_min)}$.
- The PLL is triggered at the positive edge of the clock. If more than 2 edges are missing, a chip reset is generated automatically.

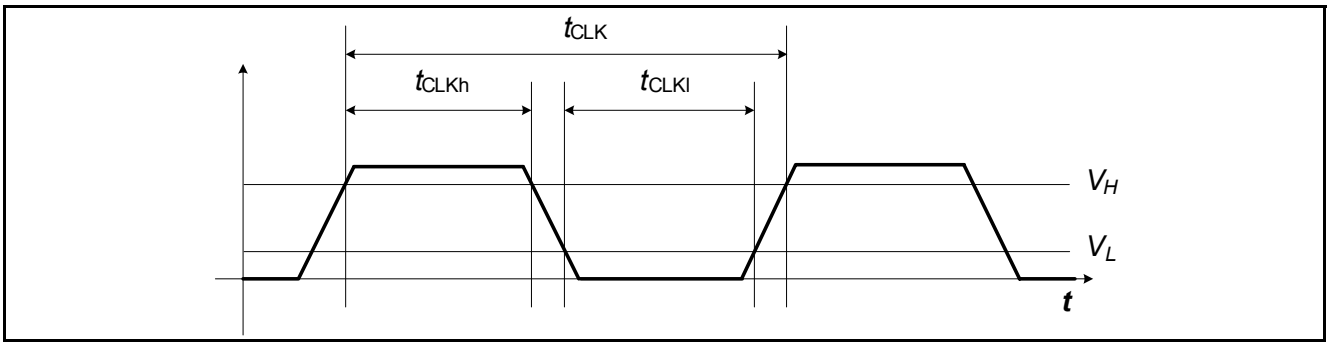


Figure 13 External CLK Timing Definition

Table 9 CLK Timing Specification

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Frequency	f_{CLK}	3.8	4.0	4.2	MHz	
CLK Duty Cycle[1)2)]	CLK_{DUTY}	30	50	70	%	
CLK Rise Time	t_{CLKr}	-	-	30	ns	from V_L to V_H
CLK Fall Time	t_{CLKf}	-	-	30	ns	from V_H to V_L
Digital Clock	f_{DIG}	22.8	24	25.2	MHz	
Internal Oscillator Frequency	f_{CLK}	3.8	4.0	4.2	MHz	

1) Minimum Duty Cycle Factor: $t_{CLKh(f\_min)}$ / $t_{CLK(f\_min)}$ with $t_{CLK(f\_min)}$= 1 / $f_{CLK(f\_min)}$

2) Maximum Duty Cycle Factor: $t_{CLKh(f\_max)}$ / $t_{CLK(f\_min)}$ with $t_{CLKh(f\_max)}$= $t_{CLK(f\_min)}$ - $t_{CLKl(min)}$

3.5 Interfaces

Within the register MOD_3, the driver strength and so the slope can be varied of the sensor output. The driver strength is specified in **Table 3** and the slope fall and rise time in **Table 10**.

Table 10 PAD Characteristic

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output Fall Time	t_{fall}, t_{rise}	-	-	8	ns	DATA, 50pF, PAD_DRV='00'
Output Rise Time		-	-	28	ns	DATA, 50pF, PAD_DRV='01'
		-	-	45	ns	DATA, 50pF, PAD_DRV='10'
		-	-	130	ns	DATA, 20pF, PAD_DRV='11'
		-	-	10	ns	IFA/IFB, 20pF, PAD_DRV='0x'
		-	-	tbd	ns	IFA/IFB, 20pF, PAD_DRV='1x'

3.5.1 Synchronous Serial Communication (SSC) Interface

The 3-pin SSC Interface has a bi-directional push-pull data line, serial clock signal and chip select. The SSC Interface is designed to communicate with a microcontroller peer to peer for fast applications.

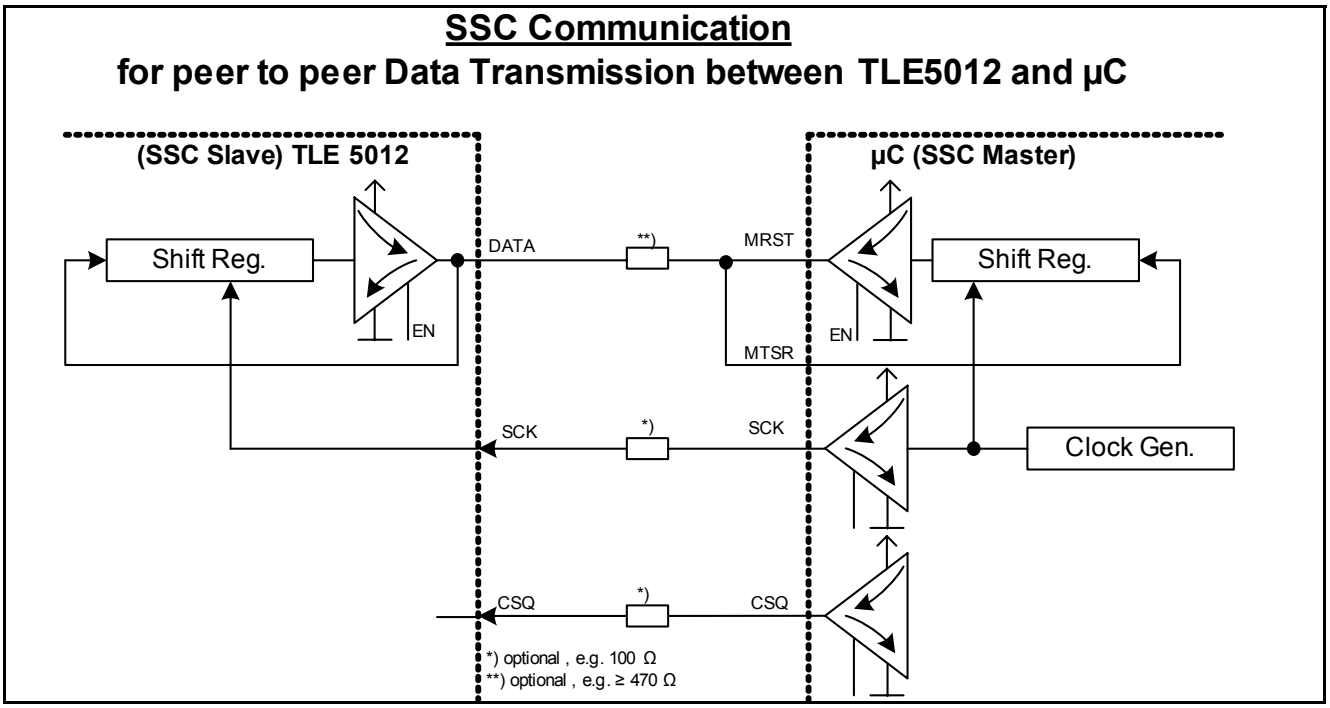


Figure 14 SSC Configuration in Sensor-Slave Mode with Push-Pull Outputs (High Speed Application)

Another possibility is a 3-pin SSC Interface with bidirectional open-drain data line, serial clock signal and chip select. This setup is designed to communicate with a microcontroller in a bus system, together with other SSC slaves (e.g. two TLE5012 for redundancy reasons). This mode can be activated using bit SSC_OD.

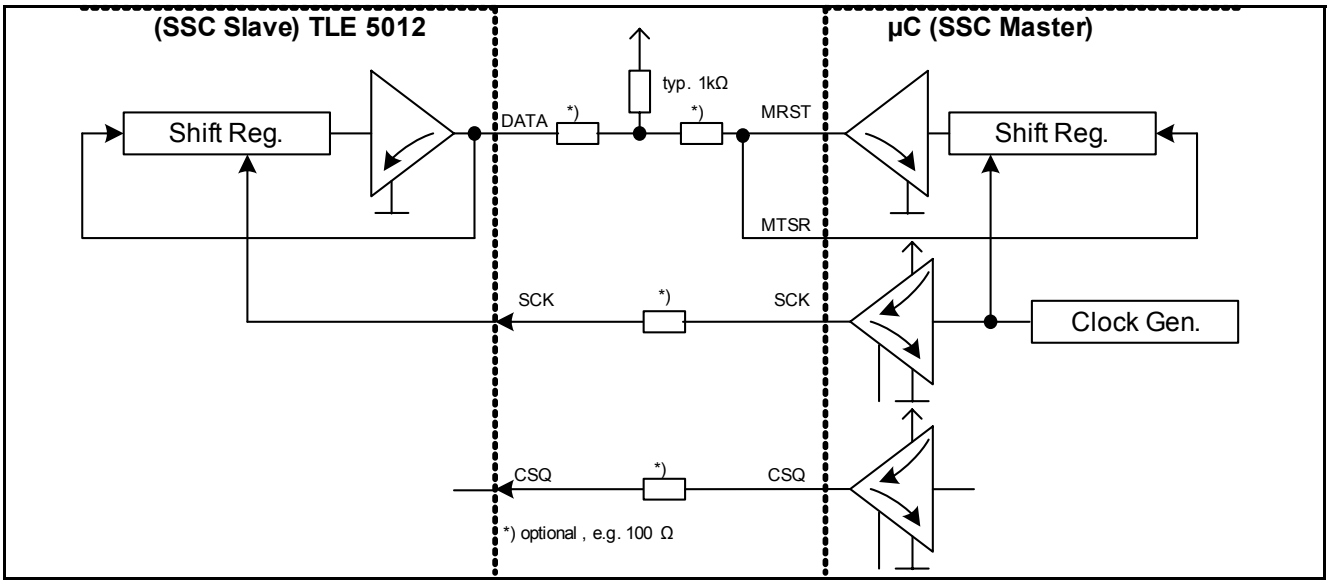


Figure 15 SSC Configuration in Sensor-Slave Mode and Open Drain (Safe Bus Systems)

3.5.1.1 SSC Timing Definition

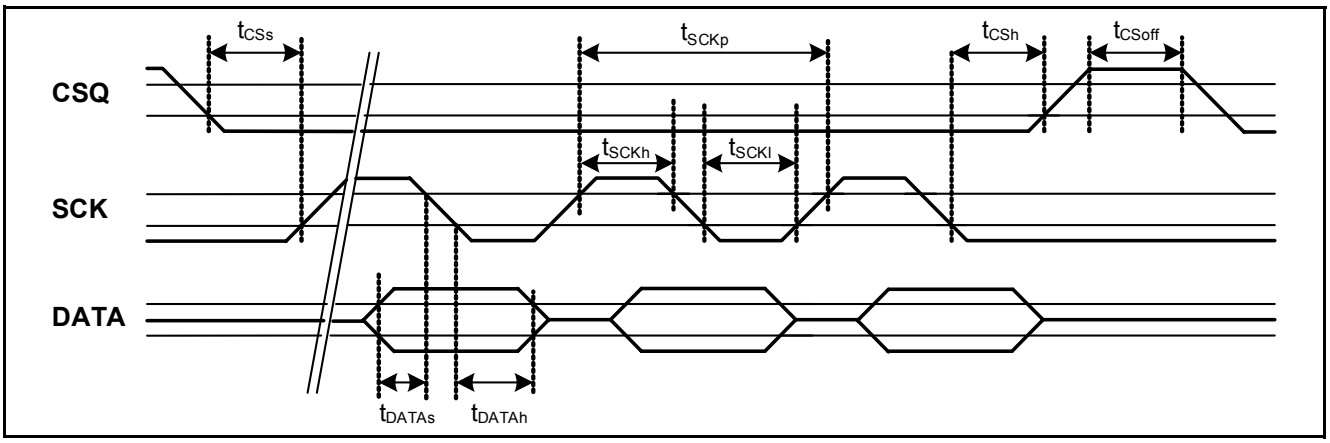


Figure 16 SSC Timing

SSC Inactive Time (CS_{off})

The SSC inactive time defines the delay time after a transfer before the TLE5012 can be selected again.

Table 11 SSC Push-Pull Timing Specification

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SSC Baud Rate	f_{SSC}	-	8.0	-	Mbit/s	
CSQ Setup Time	t_{CSs}	105	-	-	ns	
CSQ Hold Time	t_{CSh}	105	-	-	ns	

Table 11 SSC Push-Pull Timing Specification (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
CSQ off	t_{CSoff}	600	-	-	ns	SSC inactive time
SCK Period	t_{SCKp}	120	125	-	ns	
SCK High	t_{SCKh}	40	-	-	ns	
SCK Low	t_{SCKl}	30	-	-	ns	
DATA Setup Time	t_{DATAs}	25	-	-	ns	
DATA Hold Time	t_{DATAh}	40	-	-	ns	
Write Read Delay	t_{wr_delay}	130	-	-	ns	

Table 12 SSC Open Drain Timing Specification

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SSC Baud Rate	f_{SSC}	-	2.0	-	Mbit/s	Pull-up Resistor = 1kΩ
CSQ Setup Time	t_{CSs}	300	-	-	ns	
CSQ Hold Time	t_{CSh}	400	-	-	ns	
CSQ off	t_{CSoff}	600	-	-	ns	SSC inactive time
SCK Period	t_{SCKp}	500	-	-	ns	
SCK High	t_{SCKh}	-	190	-	ns	
SCK Low	t_{SCKl}	-	190	-	ns	
DATA Setup Time	t_{DATAs}	25	-	-	ns	
DATA Hold Time	t_{DATAh}	40	-	-	ns	
Write Read Delay	t_{wr_delay}	130	-	-	ns	

3.5.1.2 SSC Data Transfer

The SSC data transfer is word aligned. The following transfer words are possible:

- Command word (to access and change operating modes of the TLE5012)
- Data words (any data transferred in any direction)
- Safety word (confirms the data transfer and provide status information)

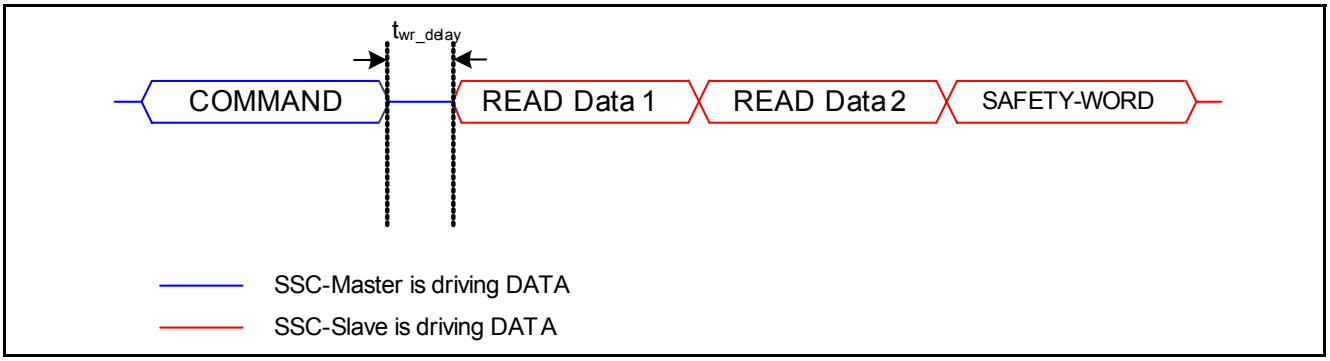


Figure 17 SSC Data Transfer (Data Read Example)

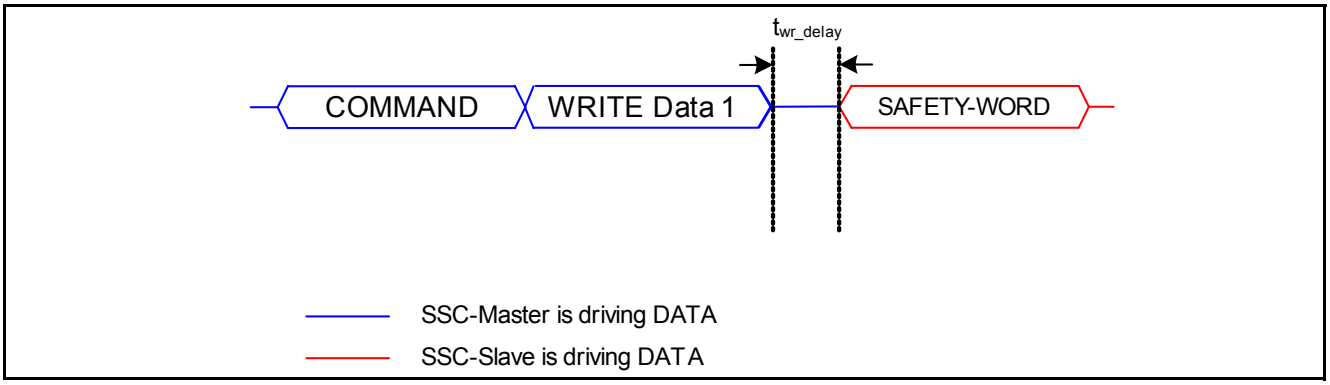


Figure 18 SSC Data Transfer (Data Write Example)

Command Word

The TLE5012 is controlled by a command word. It is sent first at every data transmission.The structure of the command word is shown in **Table 13**, where the UPD-bit allows the access to current values or updated values. If an update command is issued and the update bit (UPD) is set, the immediate values are stored in the update buffer simultaneously. This enables a snapshot of all necessary system parameters at the same time. Bits with an update buffer are marked by an “u” in type of register description. The initialization of such an update is descripted on page **29**.

Table 13 Structure of the Command Word

Name	Bits	Description
RW	[15]	Read - Write 0:Write 1:Read
Lock	[14..11]	4 bit Lock Value 0000_B: Default Operating Access for addresses 0x00:0x04 1010_B: Config- Access for addresses 0x05:0x11

Table 13 Structure of the Command Word

Name	Bits	Description
UPD	[10]	Update-Register Access 0: Access to current values 1: Access to updated values
ADDR	[9..4]	6 bit Address
ND	[3..0]	4 bit Number of Data-Words

Safety Word

The safety word contains following bits:

Table 14 Structure of the Safety Word

Name	Bits	Description
STAT	Chip and Interface Status	
	[15]	Indication of Chip-Reset (resets after readout) via SSC 0: Reset occurred 1: No reset Reset: 1_B
	[14]	System Error (e.g. Overvoltage; Undervoltage; V_{DD}-, GND- off; ROM;...) 0: Error occurred (S_VR; S_DSPU; S_OV; S_XYOL: S_MAGOL; S_ADCM) 1: No error
	[13]	Interface Access Error (access to wrong address; wrong lock) 0: Error occurred 1: No error
	[12]	Valid Angle Value (no system error; no interface error; NO_GMR_A = ’0’; NO_GMR_XY=’0’) 0: Angle value invalid 1: Angle value valid
RESP	[11..8]	Sensor Number Response Indicator The sensor no. bit is pulled low and the other bits are high.
CRC	[7..0]	Cyclic Redundancy Check (CRC)

Data Communication via SSC

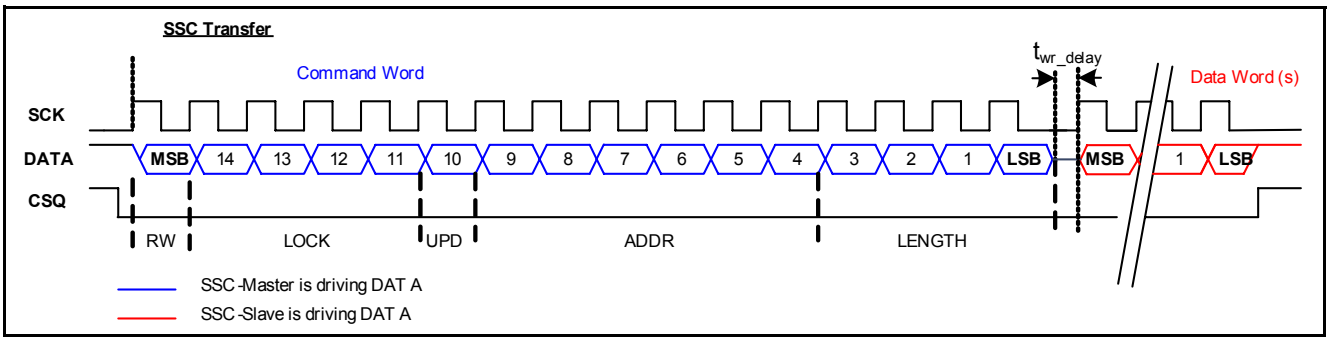


Figure 19 SSC Bit Ordering (Read Example)

The data communication via SSC interface has the following characteristic:

- The data transmission order is “Most Significant Bit (MSB) first”.
- Data is put on the data line with the rising edge on SCK and read with the falling edge on SCK.
- The SSC Interface is word-aligned. All functions are activated after each transmitted word.
- A “high” condition on the negated Chip Select pin (CSQ) of the selected TLE5012 interrupts the transfer immediately. The CRC calculator is automatically reset.
- After changing the data direction, a delay (t_{wr_delay}) has to be considered before continuing the data transfer. This is necessary for internal register access.
- Every access to the TLE5012 with the number of data (ND) ≥ 1 is performed with address auto-increment.
- At an overflow at address $3F_H$ the transfer continuous at address 00_H.
- With ND = 0 no auto-increment is done and a continuously readout of the same address can be realized. Afterwards no Safety Word is send and the transfer ends with high condition on CSQ.
- After every data transfer with ND ≥ 1 the 16 bit Safety Word will be appended by the selected TLE5012.
- At a rising edge of CSQ without data transfer before (no SCK-pulse), the update-registers are updated with according values.
- After sending the Safety Word the transfer ends. To start another data transfer, the CSQ has to be deselected once for t_{CSoff}.
- The SSC is default Push-Pull. The Push-Pull driver is only active, if the TLE5012 has to send data, otherwise the Push-Pull is disabled for receiving data from the microcontroller.

Cyclic Redundancy Check (CRC)

- This CRC is according to the J1850 Bus-Specification.
- Every new transfer resets the CRC generation.
- Every Byte of a transfer will be taken into account to generate the CRC (also the sent command(s)).
- Generator-Polynomial: X8+X4+X3+X2+1, but for the CRC generation the fast-CRC generation circuit is used (see **Figure 20**)
- The remainder of the fast CRC circuit is initial set to ’11111111_B’.
- Remainder is inverted before transmission.

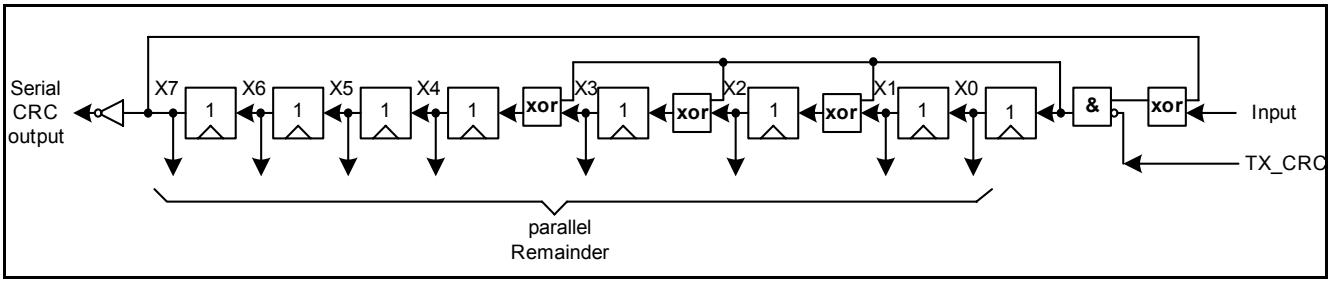


Figure 20 Fast CRC Polynomial Division Circuit

3.5.1.3 Registers Chapter

This chapter defines the registers of the TLE5012. It also defines the read/write access rights of the specific registers. **Table 15** identifies the values with symbols. Access to the registers is accomplished via the SSC Interface.

Table 15 Registers Overview

Register Short Name	Register Long Name	Offset Address	Page Number
Registers Chapter, TLE5012 Register			
STAT	Status Register	00_H	**31**
ACSTAT	Activation Status Register	01_H	**33**
AVAL	Angle Value Register	02_H	**34**
ASPD	Angle Speed Register	03_H	**35**
AREV	Angle Revolution Register	04_H	**35**
FSYNC	Frame Synchronization Register	05_H	**36**
MOD_1	Interface Mode1 Register	06_H	**37**
SIL	SIL Register	07_H	**38**
MOD_2	Interface Mode2 Register	08_H	**39**
MOD_3	Interface Mode3 Register	09_H	**40**
OFFX	Offset X	$0A_H$	**41**
OFFY	Offset Y	$0B_H$	**42**
SYNCH	Synchronicity	$0C_H$	**42**
IFAB	IFAB Register	$0D_H$	**43**
MOD_4	Interface Mode4 Register	$0E_H$	**44**
TCO_Y	Temperature Coeffizient Register	$0F_H$	**45**
ADC_X	X-raw value	10_H	**45**
ADC_Y	Y-raw value	11_H	**46**

The register is addressed wordwise.

3.5.1.3.1 TLE5012 Register

Status Register

STAT	Offset	Reset Value
Status Register	**00_H**	**8001_H**

15	14	13	12	11	10	9	8
RD_ST	**S_NR**		**NO_GMR_A**	**NO_GMR_XY**	**S_ROM**	**S_ADCT**	Res
r	rw		ru	ru	r	ru	
7	6	5	4	3	2	1	0
S_MAGOL	**S_XYOL**	**S_OV**	**S_DSPU**	**S_FUSE**	**S_VR**	**S_WD**	**S_RST**
ru	ru	ru	ru	ru	ru	ru	ru

Field	Bits	Type	Description
RD_ST	15	r	**Read Status** 0_B after readout 1_B status values changed Reset: 1_B
S_NR	14:13	rw	**Slave Number** is given at startup by the external circuit of IFA and IFB. Reset: 00_B
NO_GMR_A	12	ru	**No GMR Angle Value** 0_B valid GMR angle value on the interface 1_B no valid GMR angle value on the interface Reset: 0_B
NO_GMR_XY	11	ru	**No GMR XY Values** 0_B valid GMR_XY values on the interface 1_B no valid GMR_XY values on the interface Reset: 0_B
S_ROM	10	r	**Status ROM** 0_B after readout, CRC ok 1_B CRC fail or running Reset: 0_B
S_ADCT	9	ru	**Status ADC-Test** 0_B after readout 1_B Test vectors out of limit Reset: 0_B

Field	Bits	Type	Description
S_MAGOL	7	ru	**Status Magnitude Out of Limit** 0_B after readout 1_B GMR-magnitude out of limit (>23230 digits) Reset: 0_B
S_XYOL	6	ru	**Status X,Y Data Out of Limit** 0_B after readout 1_B X,Y data out of limit (>23230 digits) Reset: 0_B
S_OV	5	ru	**Status Overflow** 0_B after readout 1_B DSPU overflow occurred Reset: 0_B
S_DSPU	4	ru	**Status Digital Signal Processing Unit** 0_B after readout 1_B DSPU self test not ok, or selftest is running Reset: 0_B
S_FUSE	3	ru	**Status Fuse CRC** 0_B after readout, Fuse CRC ok 1_B Fuse CRC fail Reset: 0_B
S_VR	2	ru	**Status Voltage Regulator** 0_B after readout 1_B V_{DD} overvoltage; V_{DD} undervoltage; V_{DD}-off; GND-off; or V_{OVG}; V_{OVA}; V_{OVD} too high Reset: 0_B
S_WD	1	ru	**Status Watchdog** 0_B after chip reset 1_B watchdog counter expired Reset: 0_B
S_RST	0	ru	**Status Reset** 0_B after readout 1_B indication of power-up, short power-break or active reset Reset: 1_B

Activation Status Register

ACSTAT — **Activation Status Register**

Offset 01_H

Reset Value $5EFE_H$

15	14	13	12	11	10	9	8
Res						AS_ADCT	Res
rw						rw	

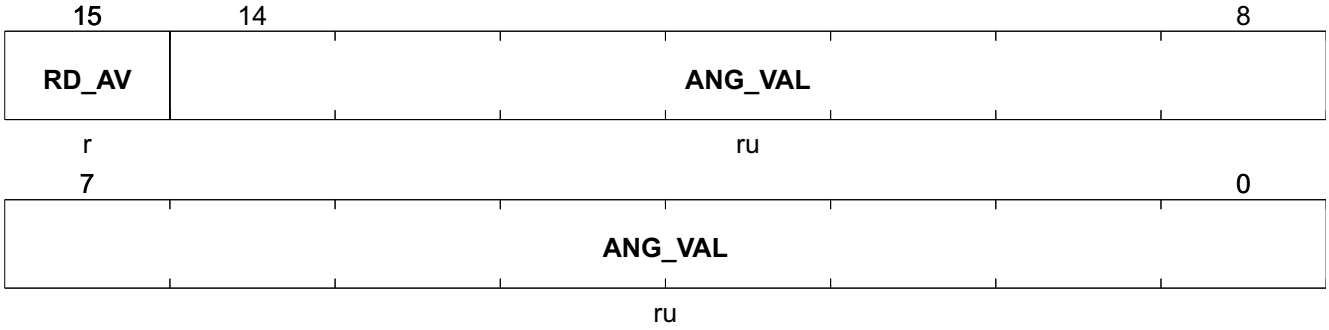
7	6	5	4	3	2	1	0
AS_VEC_MAG	AS_VEC_XY	AS_OV	AS_DSPU	AS_FUSE	AS_VR	AS_WD	AS_RST
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
Res	15:10	rw	**Reserved** Reset: 010111_B
AS_ADCT	9	rw	**Enable GMR Vector check** Reset: 1_B
AS_VEC_MAG	7	rw	**Activation of ADC-Redundancy-BIST** 0_B after execution 1_B activation of redundancy BIST Reset: 1_B
AS_VEC_XY	6	rw	**Activation of ADC-BIST** 0_B after execution 1_B activation of BIST Reset: 1_B
AS_OV	5	rw	**Enable of DSPU Overflow Check** Reset: 1_B
AS_DSPU	4	rw	**Activation DSPU BIST** 0_B after execution 1_B activation of DSPU BIST Reset: 1_B
AS_FUSE	3	rw	**Activation Fuse CRC** 0_B after execution 1_B activation of Fuse CRC Reset: 1_B
AS_VR	2	rw	**Enable Voltage Regulator Check** Reset: 1_B
AS_WD	1	rw	**Enable DSPU Watchdog-HW-Reset** Reset: 1_B

Field	Bits	Type	Description
AS_RST	0	rw	**Activation of Hardware Reset** Activation occurs after CSQ switches from ’0’ to ’1’ after SSC transfer. 0_B after execution 1_B activation of HW Reset Reset: 0_B

Angle Value Register

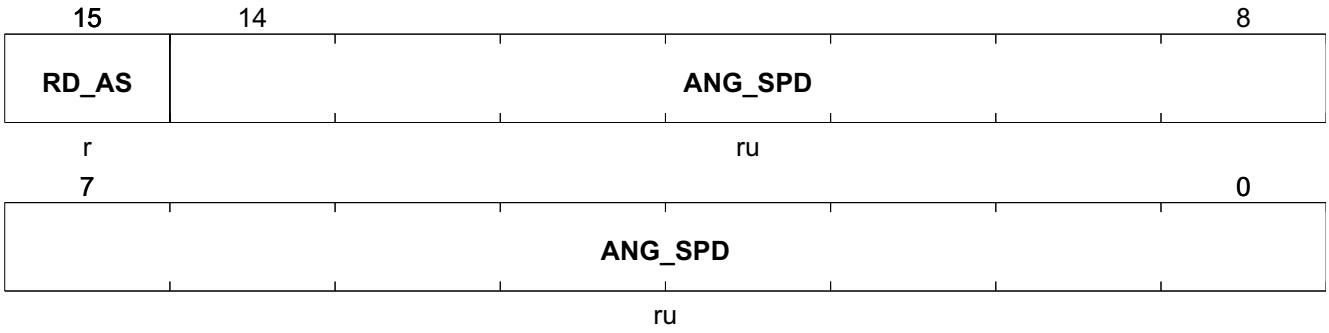
AVAL	Offset	Reset Value
Angle Value Register	**02_H**	**8000_H**



Field	Bits	Type	Description
RD_AV	15	r	**Read Status, Angle Value** 0_B after readout 1_B new angle value (ANG_VAL) present Reset: 1_B
ANG_VAL	14:0	ru	**Calculated Angle Value** (ANG_RANGE = 0x080) 4000_H -180° 0000_H 0° $3FFF_H$ +179.99° Reset: 0_H

Angle Speed Register

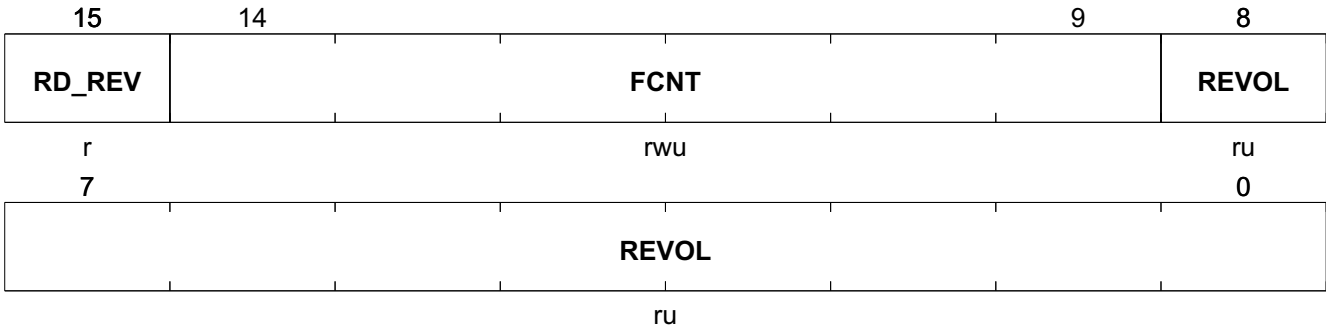
ASPD	Offset	Reset Value
Angle Speed Register	**03_H**	**8000_H**



Field	Bits	Type	Description
RD_AS	15	r	**Read Status, Angle Speed** 0_B after readout 1_B new angle speed value (ANG_SPD) present Reset: 1_B
ANG_SPD	14:0	ru	**Calculated Angle Speed** Without prediction difference between two consecutive angle values. With prediction, difference between three consecutive angle values. Reset: 0_H

Angle Revolution Register

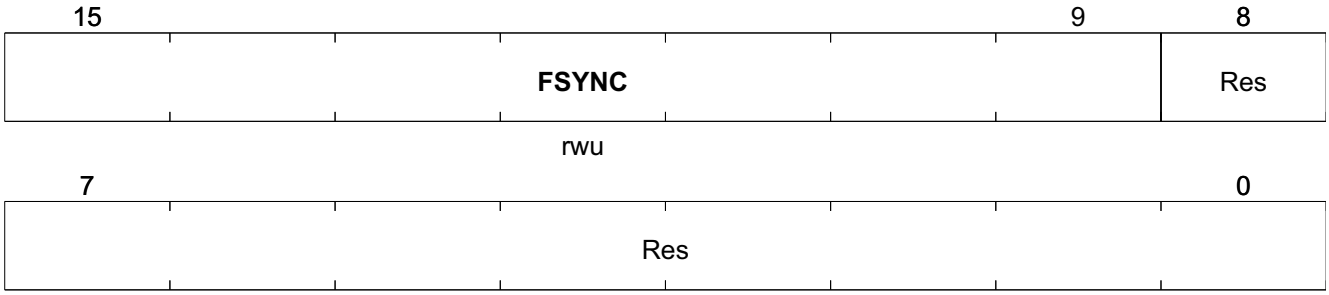
AREV	Offset	Reset Value
Angle Revolution Register	**04_H**	**8000_H**



Field	Bits	Type	Description
RD_REV	15	r	**Read Status, Revolution** 0_B after readout 1_B new value (REVOL) present Reset: 1_B
FCNT	14:9	rwu	**Frame Counter (unsigned 6 bit value)** Counts every new angle value Reset: 0_H
REVOL	8:0	ru	**Number of Revolutions (signed 9 bit value)** If prediction is enabled, revolution counter is one schedule delayed related to ANG_VAL. Reset: 0_H

Frame Synchronization Register

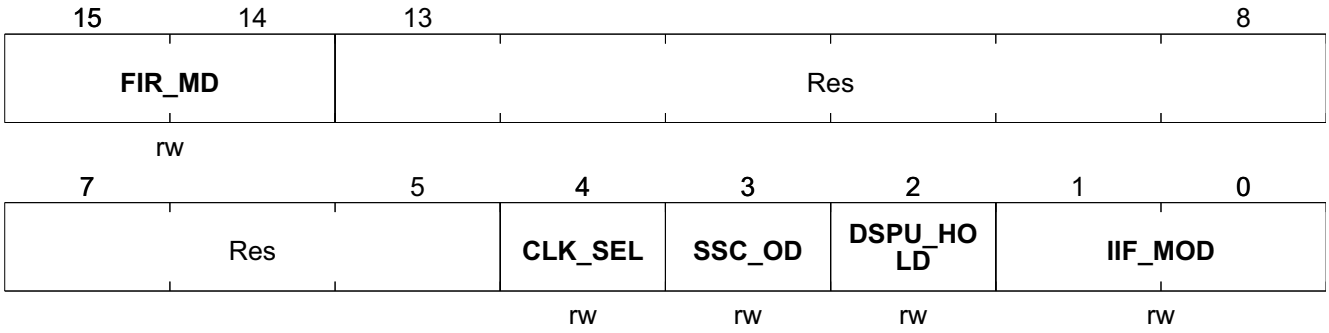
FSYNC	Offset	Reset Value
Frame Synchronization Register	**05_H**	**0000_H**



Field	Bits	Type	Description
FSYNC	15:9	rwu	**Frame Synchronization Counter Value** Sub counter within one frame. Reset: 0_H

Interface Mode1 Register

MOD_1	Offset	Reset Value
Interface Mode1 Register	06_H	8001_H



Field	Bits	Type	Description
FIR_MD	15:14	rw	**Filter Decimation Setting** 00_B 21.3µs 01_B 42.7µs 10_B 85.3µs 11_B 170.6µs Reset: 10_B
CLK_SEL	4	rw	**Clock Source Select** 0_B internal oscillator 1_B external 4MHz clock Reset: 0_B
SSC_OD	3	rw	**SSC-Interface** 0_B Push-Pull 1_B Open Drain (default within TLE5012-E0318 and TLE5012-E0742) Reset: 0_B
DSPU_HOLD	2	rw	**Hold DSPU Operation** 0_B DSPU in normal schedule operation 1_B DSPU is on hold Reset: 0_B
IIF_MOD	1:0	rw	**Incremental Interface Mode** 00_B IIF disabled 01_B A/B operation with Index on DATA 10_B not allowed 11_B not allowed Reset: 01_B

SIL Register

SIL	Offset	Reset Value
SIL Register	07_H	0000_H

15	14	13	11	10	9	8
FILT_PAR	**FILT_INV**	Res		**FUSE_REL**	Res	
rw	rw			rw		

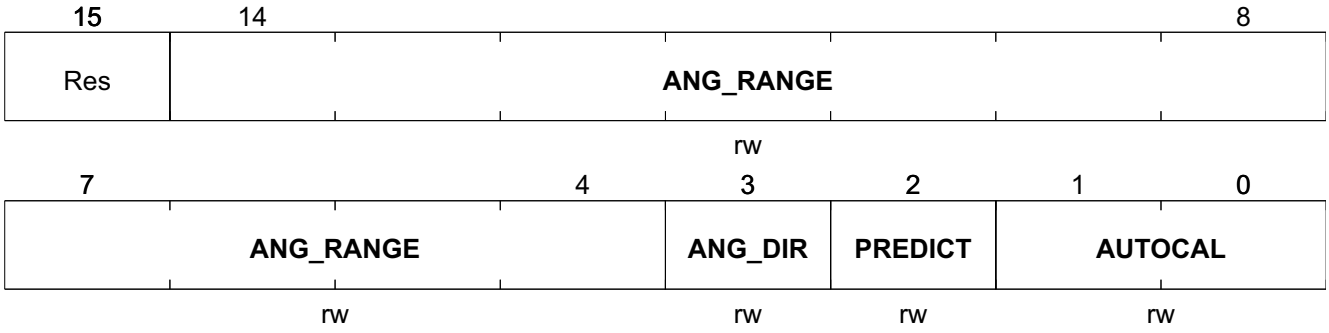
7	6	5	3	2	0
Res	**ADCTV_EN**	**ADCTV_Y**		**ADCTV_X**	
	rw	rw		rw	

Field	Bits	Type	Description
FILT_PAR	15	rw	**Filter Parallel** 0_B filter parallel disabled 1_B filter parallel enabled (source: X-value) Reset: 0_B
FILT_INV	14	rw	**Filter Inverted** 0_B filter inverted disabled 1_B filter inverted enabled Reset: 0_B
FUSE_REL	10	rw	**Fuse Reload** 0_B fuse reload disabled 1_B fuse parameters reloaded to DSPU at next cycle start Reset: 0_B
ADCTV_EN	6	rw	**ADC-Test vectors** 0_B ADC-Test vectors disabled 1_B ADC-Test vectors enabled Reset: 0_B
ADCTV_Y	5:3	rw	**Test vector Y** 000_B 0V 001_B +70% 010_B +100% 011_B +Overflow 101_B -70% 110_B -100% 111_B -Overflow Reset: 0_H

Field	Bits	Type	Description
ADCTV_X	2:0	rw	**Test vector X** 000_B 0V 001_B +70% 010_B +100% 011_B +OV 101_B -70% 110_B -100% 111_B -OV Reset: 0_H

Interface Mode2 Register

MOD_2	Offset	Reset Value
Interface Mode2 Register	**08_H**	**0800_H**

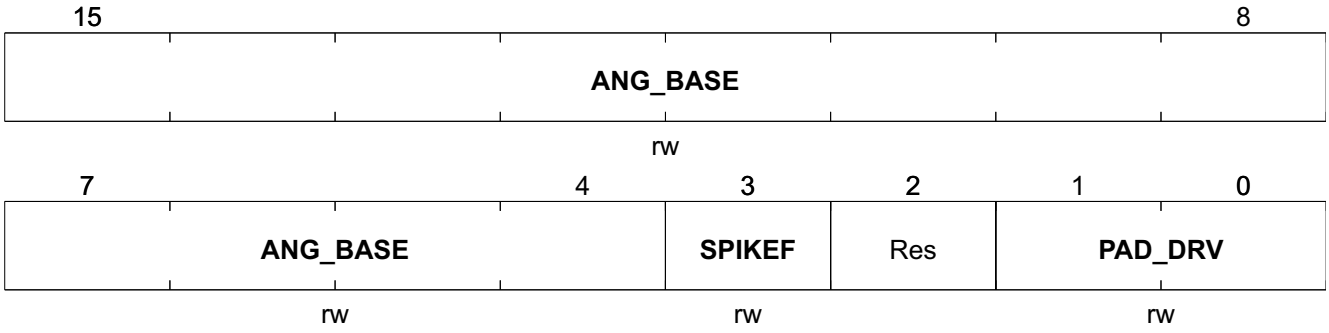


Field	Bits	Type	Description
ANG_RANGE	14:4	rw	**Angle Range** Angle Range [°] = 360° * (2^7 / ANG_RANGE) 200_H represents 90° 080_H represents 360° Reset: 080_H
ANG_DIR	3	rw	**Angle Direction** 0_B counterclockwise rotation of magnet 1_B clockwise rotation of magnet Reset: 0_B
PREDICT	2	rw	**Prediction** 0_B prediction disabled 1_B prediction enabled (default within TLE5012-E0318 and TLE5012-E0742) Reset: 0_B

Field	Bits	Type	Description
AUTOCAL	1:0	rw	**Autocalibration Mode** 00_B no autocalibration 01_B autocalibration time mode (1LSB parameter change every t_{upd}) (default within TLE5012-E0318 and TLE5012-E0742) 10_B autocalibration angle mode1 (1LSB parameter change every 22.5°) 11_B autocalibration angle mode2 (1LSB parameter change every 11.25°) Reset: 00_B

Interface Mode3 Register

MOD_3	Offset	Reset Value
Interface Mode3 Register	**09_H**	**0000_H**

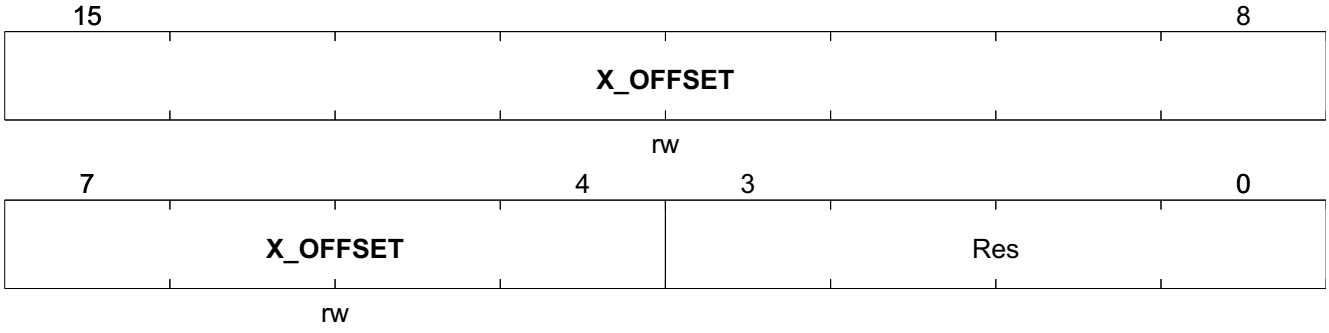


Field	Bits	Type	Description
ANG_BASE	15:4	rw	**Angle Base** 800_H -180° 000_H 0° 001_H 0.0879° $7FF_H$ +179.912° Reset: 000_H
SPIKEF	3	rw	**Analog Spike Filters of Input Pads** 0_B spike filter disabled 1_B spike filter enabled Reset: 0_B

Field	Bits	Type	Description
PAD_DRV	1:0	rw	**Configuration of Pad-Driver** 00_B IFA/IFB: strong driver, DATA: strong driver, fast edge 01_B IFA/IFB: strong driver, DATA: strong driver, slow edge 10_B IFA/IFB: weak driver, DATA: medium driver, fast edge (default within TLE5012-E0318 and TLE5012-E0742) 11_B IFA/IFB: weak driver, DATA: weak driver, slow edge Reset: 00_B

Offset X Register

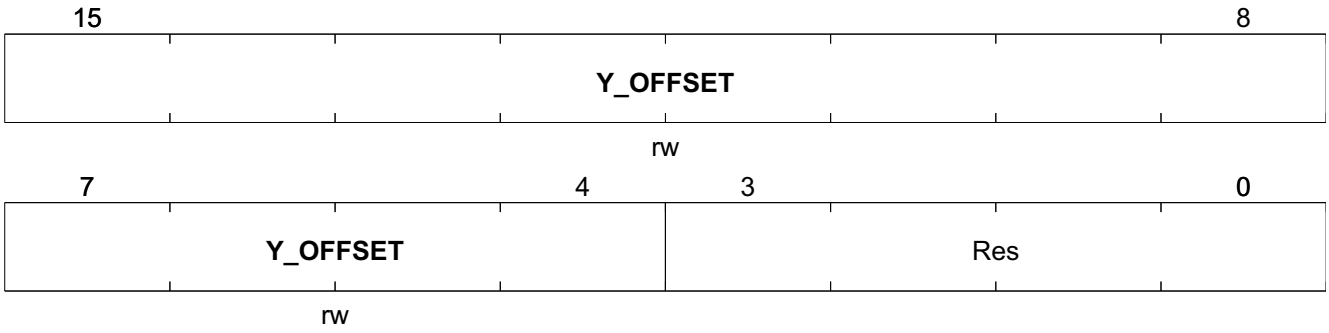
OFFX	Offset	Reset Value
Offset X	**$0A_H$**	**0000_H**



Field	Bits	Type	Description
X_OFFSET	15:4	rw	**Offset Correction of X-value** Reset: 0_H

Offset Y Register

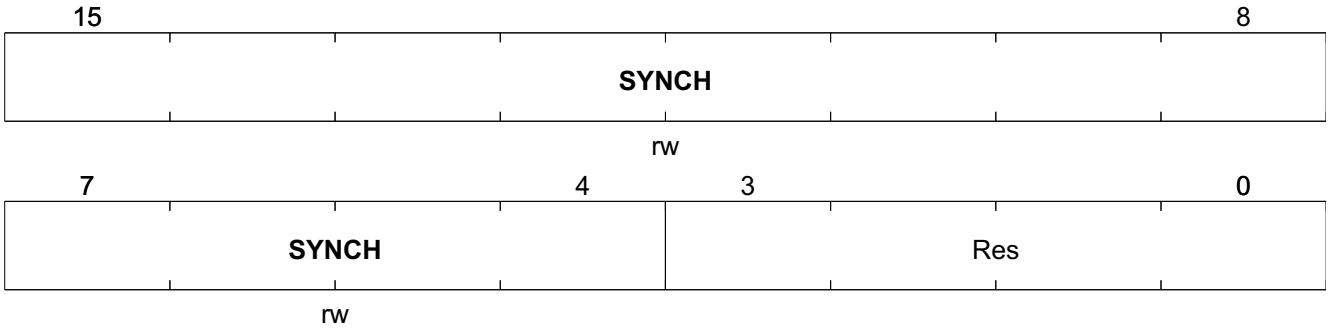
OFFY	Offset	Reset Value
Offset Y	$0B_H$	0000_H



Field	Bits	Type	Description
Y_OFFSET	15:4	rw	**Offset Correction of Y-value** Reset: 0_H

Synchronicity Register

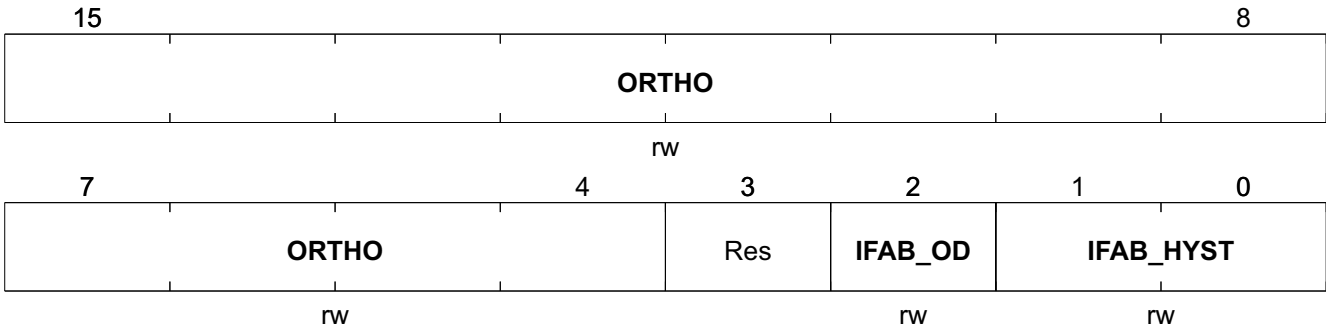
SYNCH	Offset	Reset Value
Synchronicity	$0C_H$	0000_H



Field	Bits	Type	Description
SYNCH	15:4	rw	**Amplitude Synchronicity** $+2047_D$ 112.494% 0_D 100% -2048_D 87.500% Reset: 0_H

IFAB Register

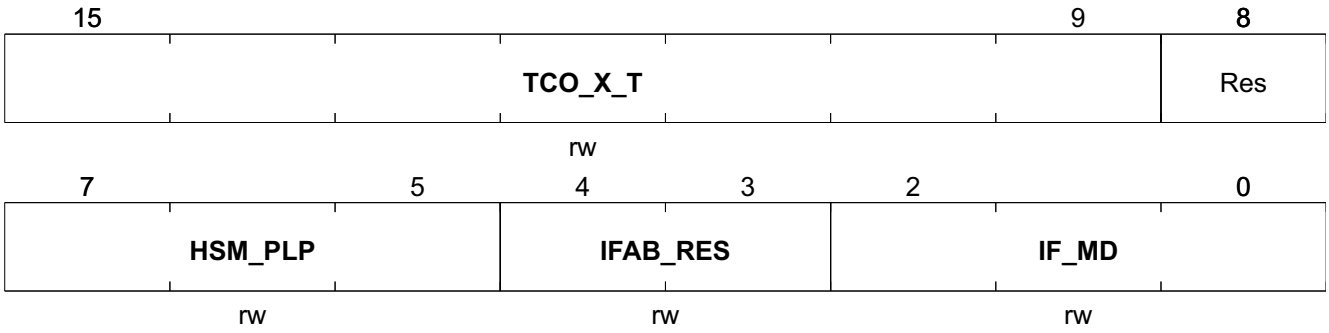
IFAB	Offset	Reset Value
IFAB Register	$0D_H$	0003_H



Field	Bits	Type	Description
ORTHO	15:4	rw	**Orthogonality Correction of X and Y Components** $+2047_D$ 11.2445° 0_D 0° -2048_D -11.2500° Reset: 0_H
IFAB_OD	2	rw	**IFA & IFB Open Drain** 0_B Push-Pull 1_B Open Drain (default within TLE5012-E0318 and TLE5012-E0742) Reset: 0_B
IFAB_HYST	1:0	rw	**HSM Hysteresis** 00_B 0° 01_B 0.09° 10_B 0.27° 11_B 0.625° Reset: 11_B

Interface Mode4 Register

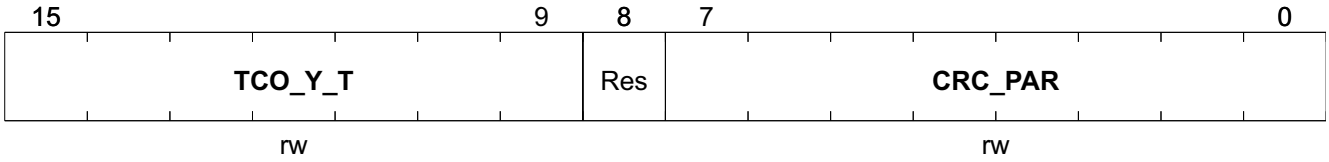
MOD_4	Offset	Reset Value
Interface Mode4 Register	$0E_H$	0000_H



Field	Bits	Type	Description
TCO_X_T	15:9	rw	**Offset Temperature Coefficient for X-Component** Reset: 0_H
HSM_PLP	7:5	rw	**Hall Switch Mode; Polepair Configuration** 000_B 2 pole pairs 001_B 3 pole pairs (default within TLE5012-E0318) 010_B 4 pole pairs 011_B 6 pole pairs 100_B 7 pole pairs (default within TLE5012-E0742) 101_B 8 pole pairs 110_B 12 pole pairs 111_B 16 pole pairs Reset: 000_B
IFAB_RES	4:3	rw	**IFAB Resolution** 00_B 12bit = 0.088° (244Hz) 01_B 11bit = 0.176° (488Hz) 10_B 10bit = 0.352° (977Hz) 11_B 9bit = 0.703° (1953Hz) Reset: 00_B
IF_MD	2:0	rw	**Interface Mode** PWM, HSM if CLK is connected to GND at startup. *Note: Not mentioned combinations are not allowed* 000_B SSC mode; IIF 001_B SSC mode; PWM 010_B SSC mode; HSM (default within TLE5012-E0318 and TLE5012-E0742) Reset: 000_B

Temperature Coeffizient Register

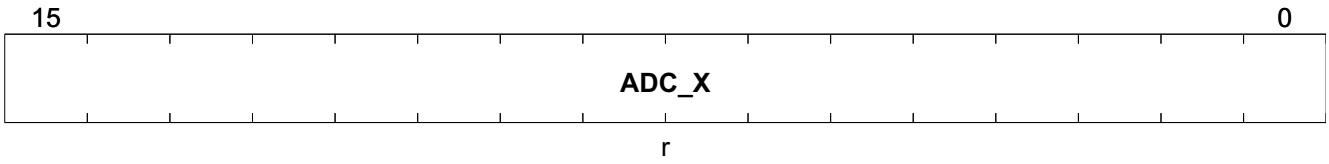
TCO_Y	Offset	Reset Value
Temperature Coeffizient Register	$0F_H$	0000_H



Field	Bits	Type	Description
TCO_Y_T	15:9	rw	**Offset Temperature Coefficient for Y-Component** Reset: 0_H
CRC_PAR	7:0	rw	**CRC of Parameters** CRC of parameters from address 08_H to $0F_H$ Reset: 0_H

X-raw Value Register

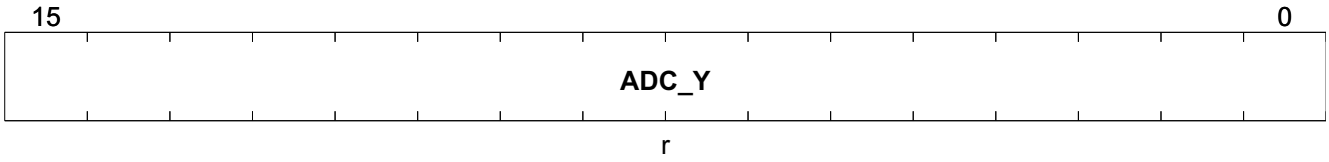
ADC_X	Offset	Reset Value
X-raw value	10_H	0000_H



Field	Bits	Type	Description
ADC_X	15:0	r	**ADC value of X-GMR** Read out of this register will update ADC_Y Reset: 0_H

Y-raw Value Register

ADC_Y	Offset	Reset Value
Y-raw value	11_H	0000_H



Field	Bits	Type	Description
ADC_Y	15:0	r	**ADC value of Y-GMR** Updated when ADC_X or ADC_Y is read. Reset: 0_H

3.5.2 Pulse Width Modulation Interface

The **P**ulse **W**idth **M**odulation (**PWM**) Interface can be selected by connecting CLK to V_{DD}.

The PWM update rate can be programmed within the register $0E_H$ (IFAB_RES) in following steps:

- 0.25 kHz with 12 bit resolution
- 0.5 kHz with 11 bit resolution
- 1.0 kHz with 10 bit resolution (default)
- 2.0 kHz with 9 bit resolution

PWM uses a square wave with constant frequency whose duty cycle is modulated resulting in an average value of the waveform.

Figure 21 shows the principle behavior of a PWM with different duty cycles and the definition of timing values. The duty cycle of a PWM is defined by following general formulas:

$$Duty\ Cycle = \frac{t_{on}}{t_{PWM}}$$

$$t_{PWM} = t_{on} + t_{off}$$

$$f_{PWM} = \frac{1}{t_{PWM}} \quad (3)$$

The range between 0 - 6.25% and 93.75 - 100% is used only for diagnostic purposes. More details are given in **Table 16**.

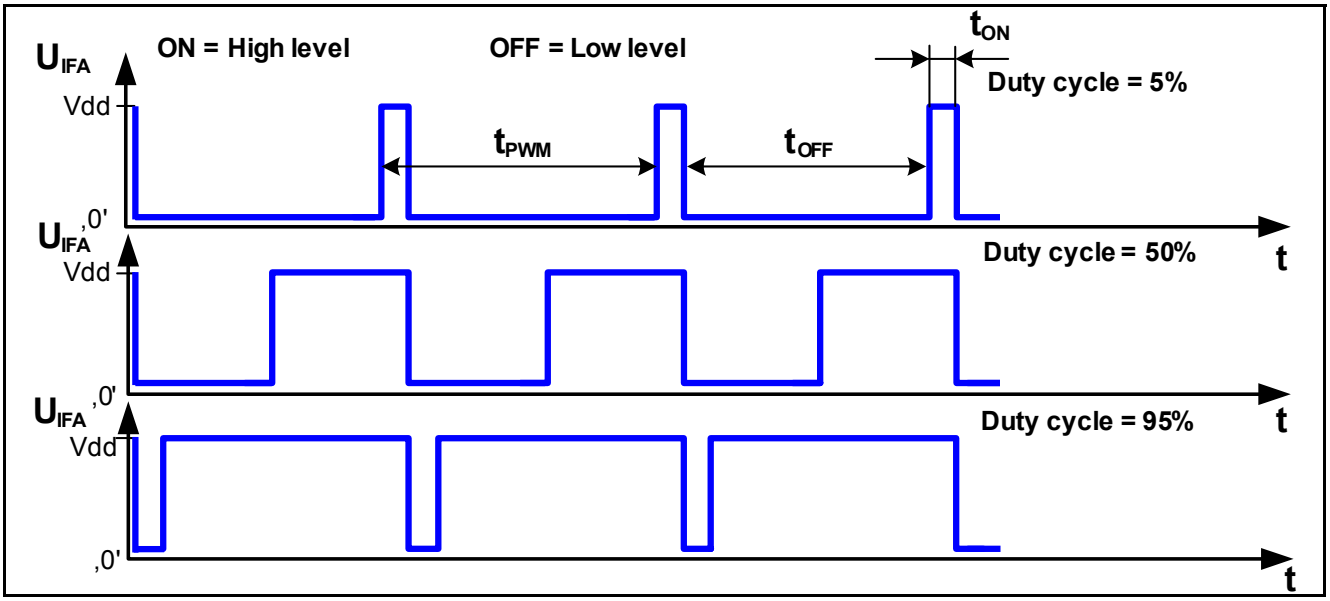


Figure 21 Typical Example for a PWM Signal

Table 16 PWM Interface

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
PWM Output Frequency	f_{PWM}	244	-	1953	Hz	selectable by IFAB_RES[1)]
Output Duty Cycle Range	DY_{PWM}	6.25	-	93.75	%	Absolute Angle
		-	2	-	%	Electrical Error (S_RST; S_VR)
		-	98	-	%	System Error (S_FUSE; S_OV; S_XYOL; S_MAGOL; S_ADCT)
		0	-	1	%	Short to GND
		99	-	100	%	Short to V_{DD}, Power-Loss
PWM Period Variation	t_{PWMvar}	-5	-	5	%	2)

1) $f_{PWM} = (f_{DIG} * 2^{IFAB\_RES}) / (24 * 4096)$

2) depends on internal oscillator frequency variation (**Chapter 3.4.6**)

3.5.3 Hall Switch Mode

The **H**all **S**witch **M**ode (**HSM**) within the TLE5012 allows to emulate the output of three Hall switches. Hall switches are often used in electrical commutated motors to get information of the rotor position. With these three output signals the motor will be commutated in the right way. Depending on the used pole pairs of the rotor, different amount of electrical periods have to be realized. This is selectable within $0E_H$ (HSM_PLP). Within the TLE5012-E0318 three polepairs and within the TLE5012-E0742 seven polepairs are fused. **Figure 22** depicts the three output signals with the relationship between electrical angle and mechanical angle. The mechanical 0° point is always used as reference.

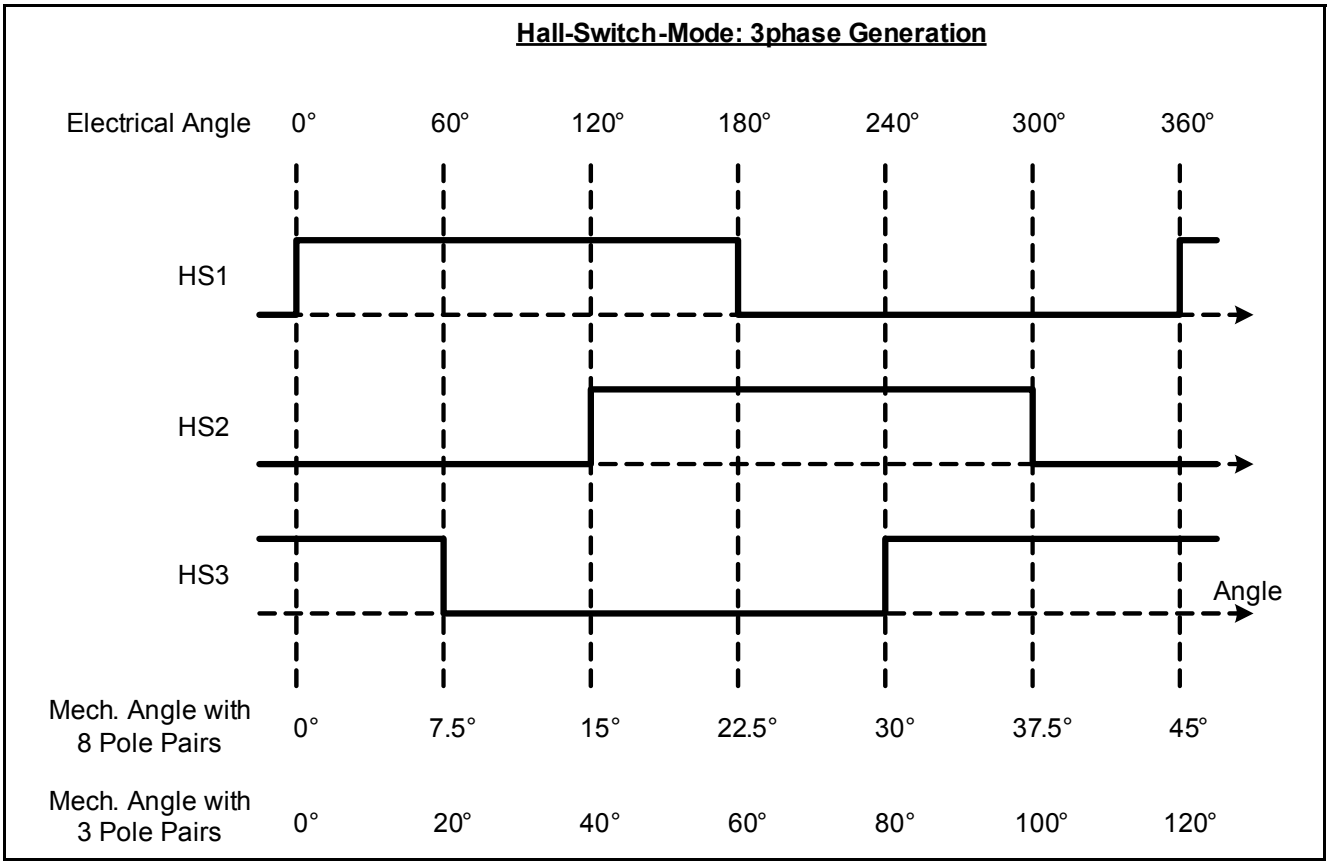


Figure 22 Hall Switch Mode

The HSM Interface can be selected by connecting CLK to GND and CSQ has to be logic “1”.

Table 17 Hall Switch Mode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rotation Speed	n	-	-	10000	rpm	

Table 17 Hall Switch Mode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Electrical Angle Accuracy	α_{elect}	-	1.2	2	°	2 polepairs with autocalibration[1)2)]
		-	1.8	3		3 polepairs with autocal.[1)2)]
		-	2.4	4		4 polepairs with autocal.[1)2)]
		-	3.6	6		6 polepairs with autocal.[1)2)]
		-	4.2	7		7 polepairs with autocal.[1)2)]
		-	4.8	8		8 polepairs with autocal.[1)2)]
		-	7.2	12		12 polepairs with autocal.[1)2)]
		-	9.6	16		16 polepairs with autocal.[1)2)]
Mechanical Angle Switching Hysteresis	$\alpha_{HShystm}$	0	-	0.625	°	selectable by IFAB_HYST[3)]
Electrical Angle Switching Hysteresis[4)]	$\alpha_{HShystel}$	-	1.25	-	°	2 polepairs; IFAB_HYST=11[1)2)]
		-	1.88	-		3 polepairs; IFAB_HYST=11[1)2)]
		-	2.50	-		4 polepairs; IFAB_HYST=11[1)2)]
		-	3.75	-		6 polepairs; IFAB_HYST=11[1)2)]
		-	4.38	-		7 polepairs; IFAB_HYST=11[1)2)]
		-	5.00	-		8 polepairs; IFAB_HYST=11[1)2)]
		-	7.50	-		12 polepairs; IFAB_HYST=11[1)2)]
		-	10	-		16 polepairs; IFAB_HYST=11[1)2)]
Fall Time	t_{HSfall}	-	0.02	1	µs	R_L = 2.2kΩ; C_L < 50pF
Rise Time	t_{HSrise}	-	0.4	1	µs	R_L = 2.2kΩ; C_L < 50pF

1) depends on internal oscillator frequency variation (**Chapter 3.4.6**)
2) guaranteed by design
3) including GMR hysteresis
4) The hysteresis has to be considered only at change of rotation direction.

To avoid switching on mechanical vibrations of the rotor, a hysteresis is recommended (**Figure 23**).

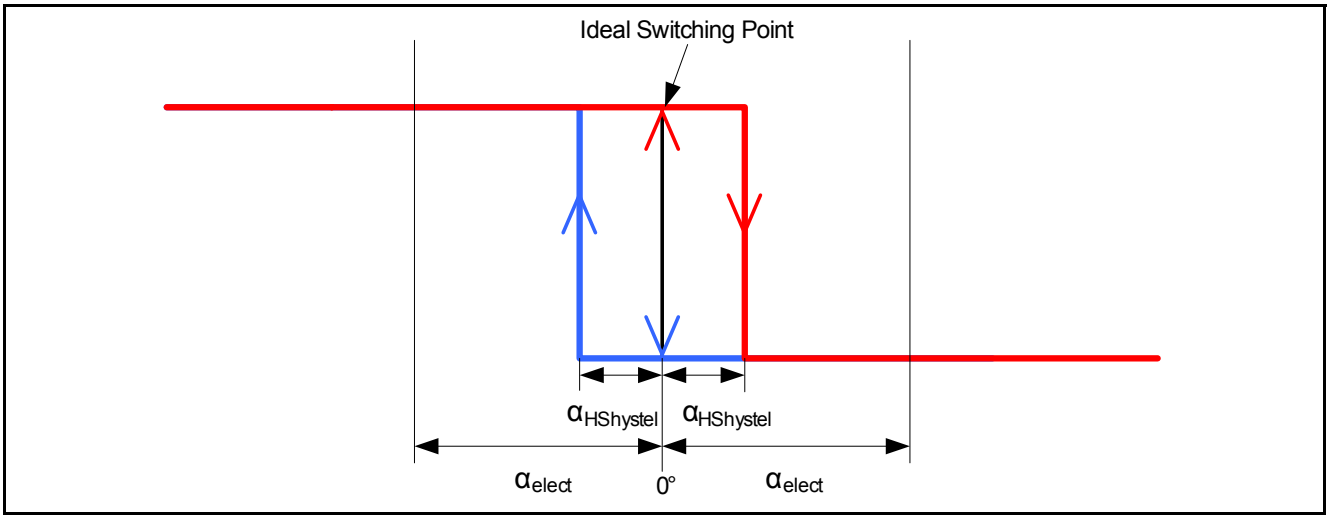


Figure 23 HS Hysteresis

3.5.4 Incremental Interface

The **I**ncremental **I**nter**f**ace (**IIF**) uses an up/down counter of a microcontroller for the angle transmission. The synchronization is done by the parallel active SSC-Interface. The angle value read out by the SSC-Interface can be compared with the stored counter value. In case of a non-synchronization, the microcontroller add the difference to the actual counter value to synchronize the TLE5012 with the microcontroller. The resolution of the IIF can be selected within the interface mode4 register (MOD_4) under IFAB_RES.

A/B Mode

The phase shift between phase A and B indicates a clockwise (B follows A) or a counterclockwise (A follows B) rotation of the magnet.

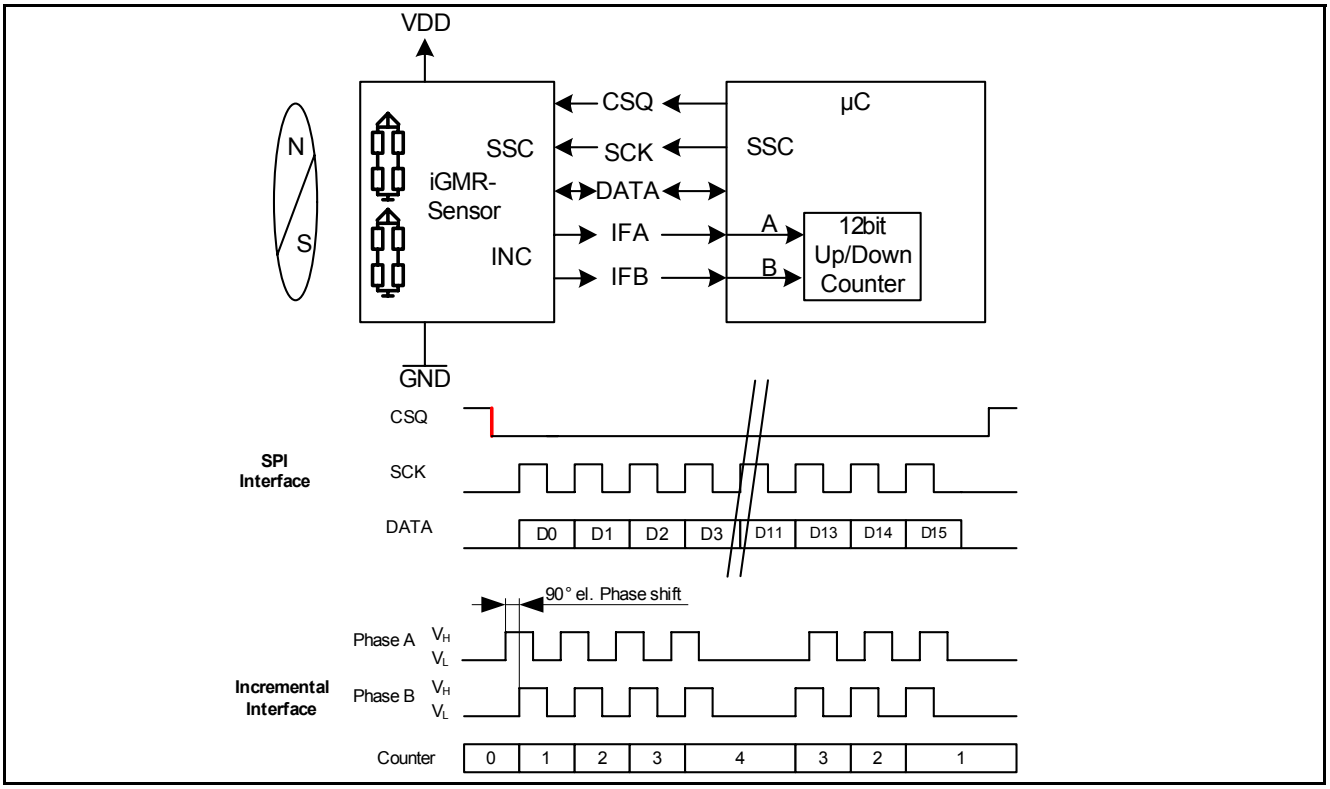


Figure 24 Incremental Interface Protocol with symbolically illustration of SPI-Interface

Index Signal

The Index-Signal is generated via Data pin, while CSQ is high (no SSC-communication). The Index-Signal is coded in quadrants via a PWM-sequence, **Figure 25**.

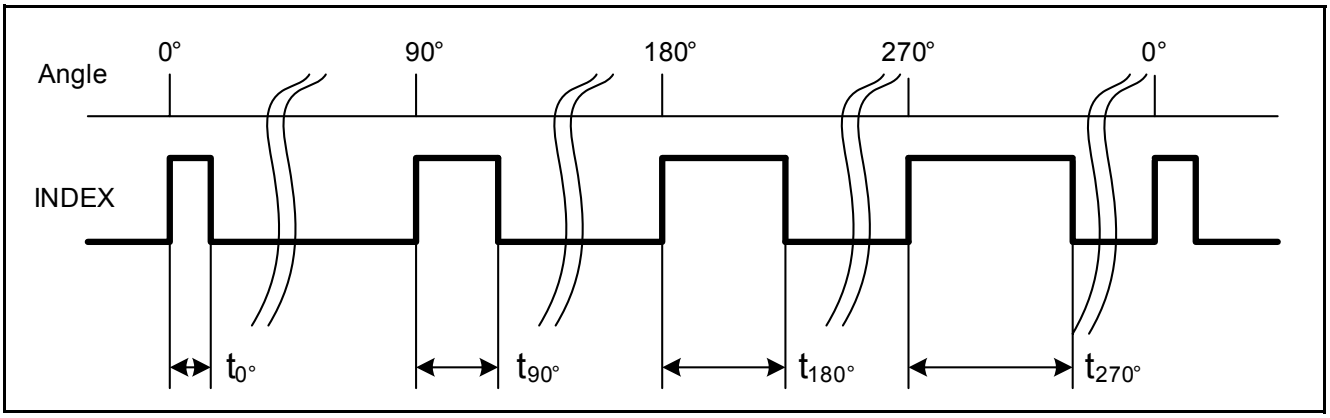


Figure 25 IIF Index Coding

Table 18 Incremental Interface

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Incremental output Frequency	f_{Inc}	-	-	1.0	MHz	Frequency of Phase A and Phase B

Table 18 Incremental Interface (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Index	$t_{0°}$	-	5	-	µs	0°
	$t_{90°}$	-	10	-	µs	90°
	$t_{180°}$	-	15	-	µs	180°
	$t_{270°}$	-	20	-	µs	270°

3.6 Test Structure

3.6.1 ADC Test Vectors

It is possible to feed the ADCs with appropriate values to simulate a certain magnet position and other GMR effects. This test can be activated within SIL register (ADCTV_EN). With ADCTV_Y and ADCTV_X the vector length can be adjusted like **Figure 26**.

The values are generated with resistors on the chip.

The following X/Y ADC values can be programmed:

- 4 points, circle amplitude = 70% (0°,90°, 180°, 270°)
- 8 points, circle amplitude = 100% (0°, 45°, 90°, 135°, 180°, 225°, 270°, 315°)
- 8 points, circle amplitude = 122.1% (35.3°, 54.7°, 125.3°, 144.7°, 215.3°, 234.7°, 305.3°, 324.7°)
- 4 points, circle amplitude = 141.4% (45°, 135°, 225°, 315°)

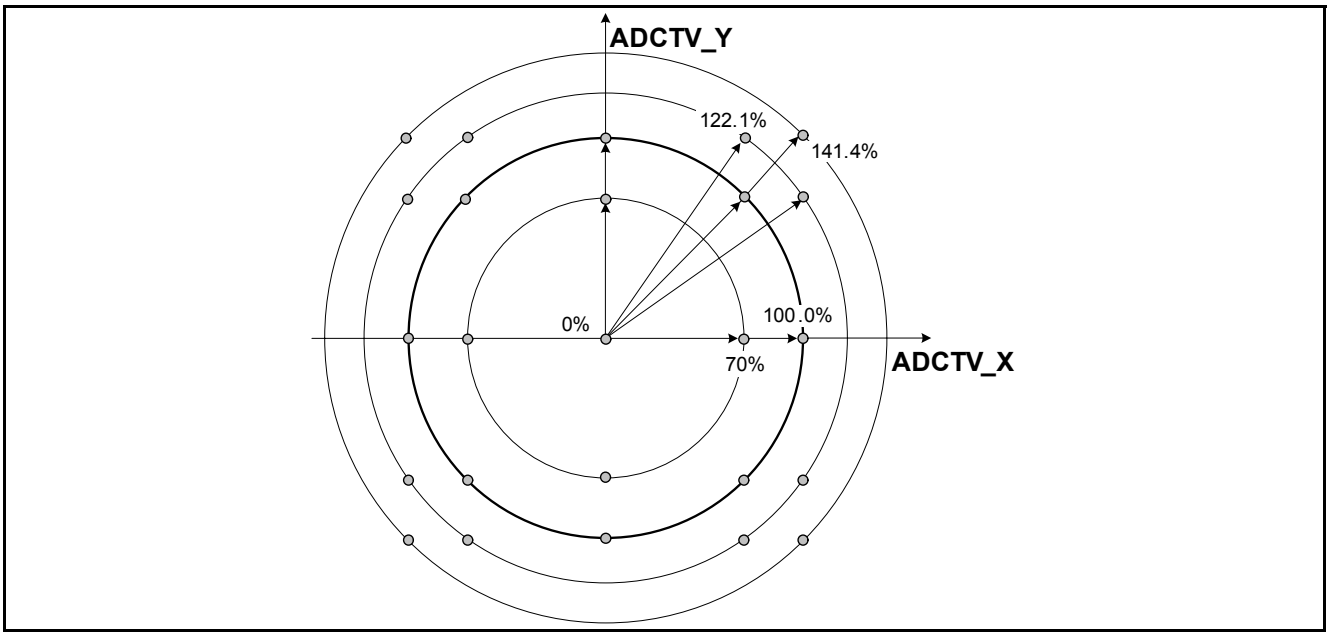


Figure 26 ADC Test Vectors

3.7 Overvoltage Comparators

Various comparators monitor the voltage in order to ensure error free operation. The overvoltages must be active at least 256 periods of t_{DIG} to set the test comparator bits in the SSC Interface registers. This works as digital spike suppression.

Table 19 Test Comparators

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Overvoltage Detection	V_{OVG}	-	2.80	-	V	
	V_{OVA}	-	2.80	-	V	
	V_{OVD}	-	2.80	-	V	
V_{DD} Overvoltage	V_{DDOV}	-	6.05	-	V	
V_{DD} Undervoltage	V_{DDUV}	-	2.70	-	V	
GND - Off Voltage	V_{GNDoff}	-	-0.55	-	V	
V_{DD} - Off Voltage	V_{VDDoff}	-	0.55	-	V	
Spike Filter Delay	t_{DEL}	-	10	-	µs	

3.7.1 Internal Supply Voltage Comparators

Every voltage regulator has an overvoltage comparator to detect a malfunction. If the nominal output voltage of 2.5 V is larger than V_{OVG}, V_{OVA} and V_{OVD}, then this overvoltage comparator is activated.

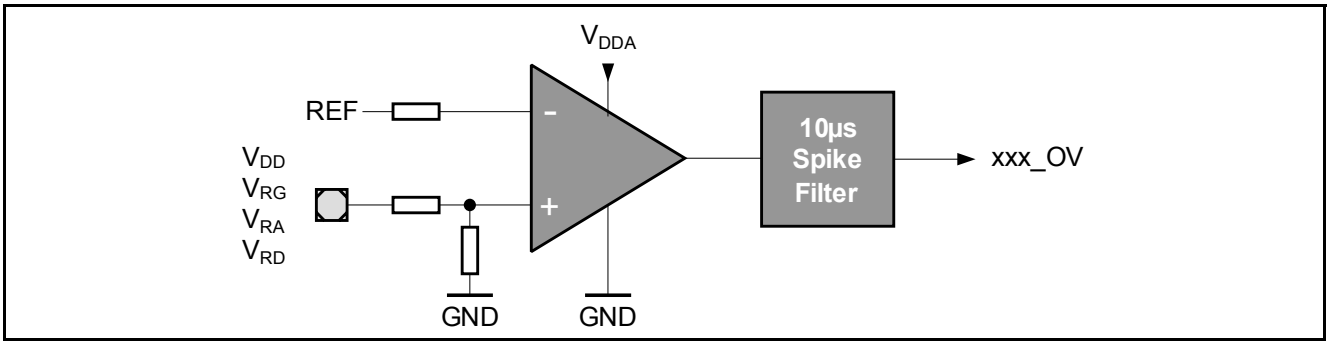


Figure 27 OV Comparator

3.7.2 V_{DD} Overvoltage Detection

The Overvoltage Detection Comparator monitors the external supply voltage at the V_{DD} pin. It activates the S_VR bit.(**Figure 27**)

3.7.3 GND - Off Comparator

The GND - Off Comparator is used to detect a voltage difference between the GND pin and SCK. It activates the S_VR bit of the SSC - Interface. This circuit can detect a disconnection of the Supply GND Pin.

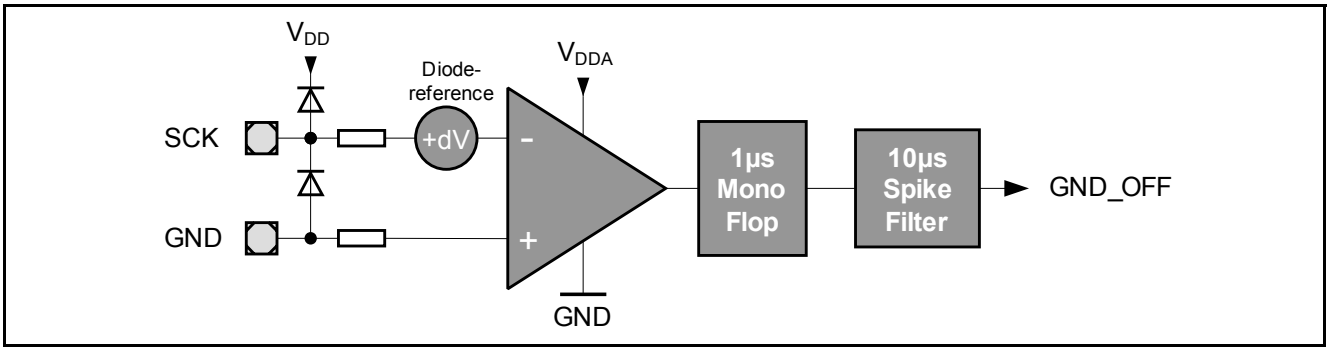


Figure 28 GND - Off Comparator

3.7.4 V_{DD} - Off Comparator

The V_{DD} - Off Comparator detects a disconnection of the VDD pin supply voltage. In this case, the TLE5012 is supplied by the SCK and CSQ input pins via the ESD structures. It activates the S_VR bit.

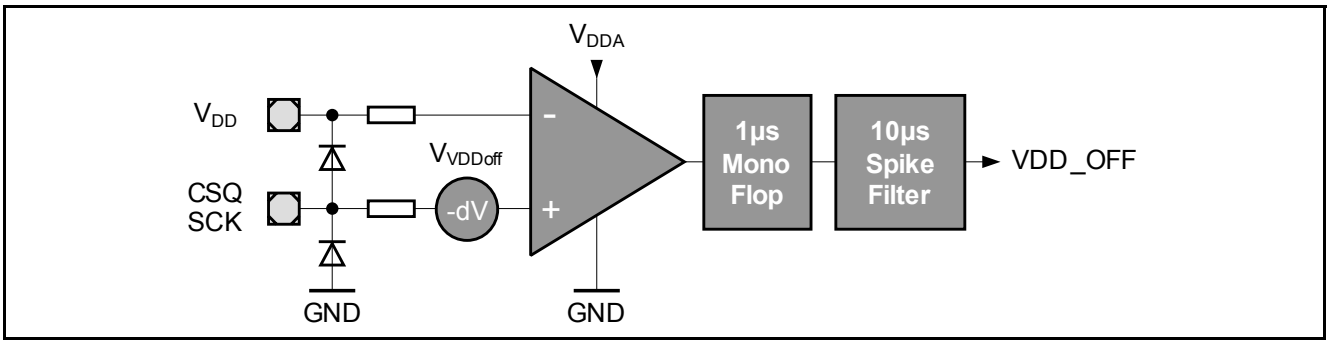


Figure 29 V_{DD} - Off Comparator

4 Package Information

4.1 Package Parameters

Table 20 Package Parameters

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Thermal Resistance	R_{thJA}	-	150	200	K/W	Junction to Air[1)]
	R_{thJC}	-	-	75	K/W	Junction to Case
	R_{thJL}	-	-	85	K/W	Junction to Lead
Soldering Moisture Level	MSL 3					260°C
Lead Frame	Cu					
Plating	Sn 100%					> 7 µm

1) according to Jedec JESD51-7

4.2 Package Outline

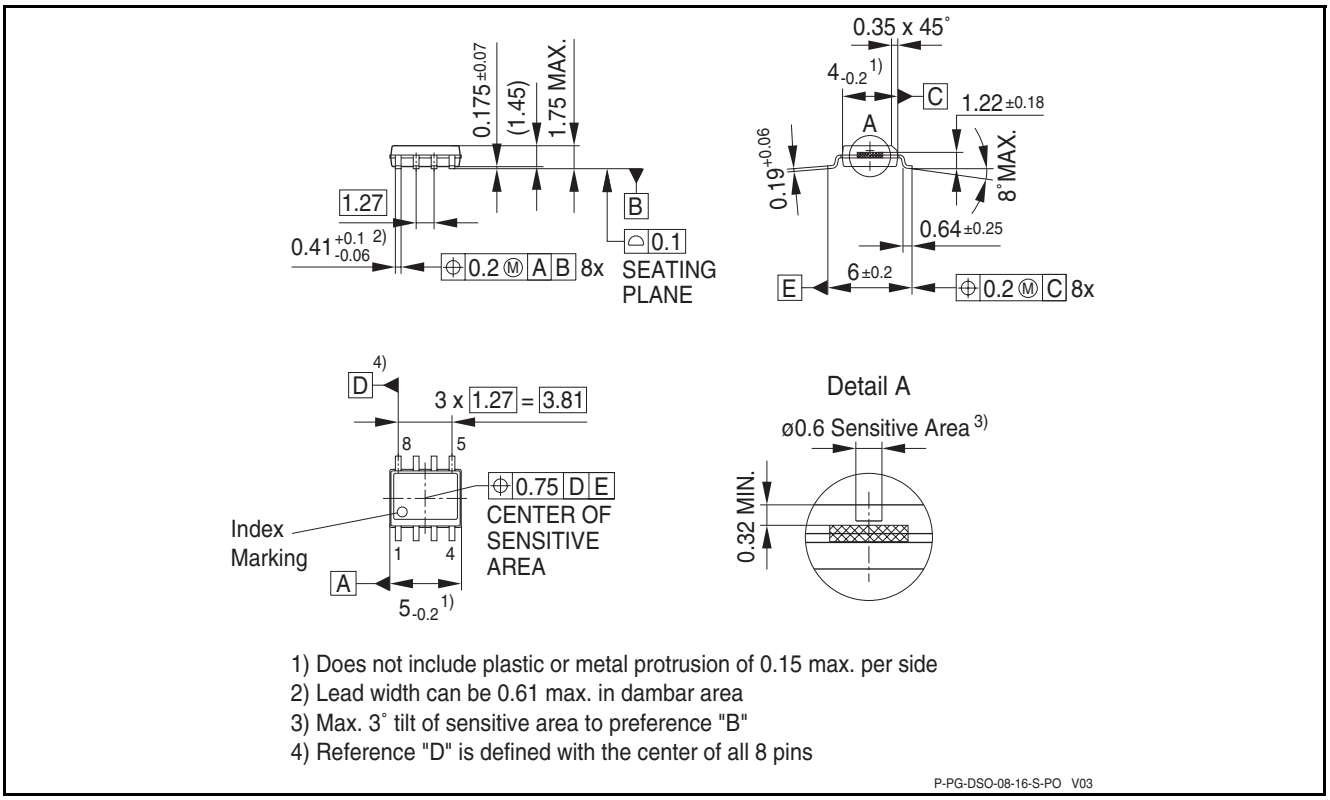


Figure 30 PG-DSO-8 Package Dimension

4.3 Footprint

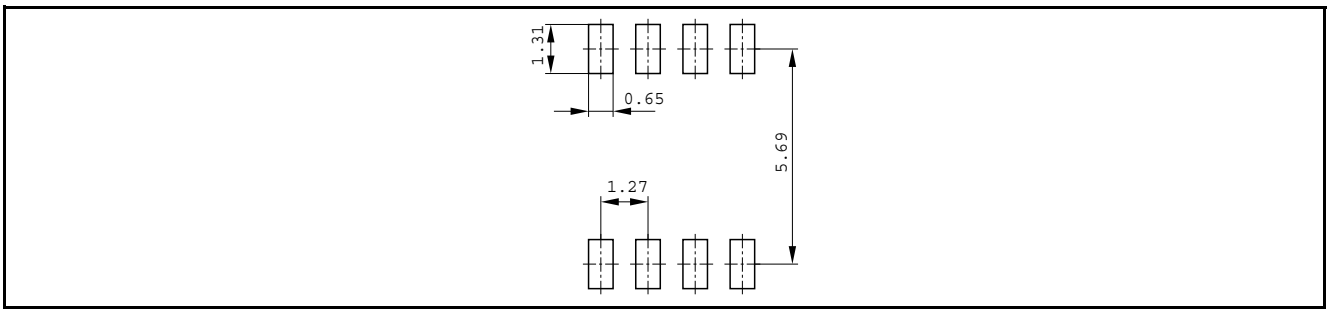


Figure 31 Footprint PG-DSO-8

4.4 Packing

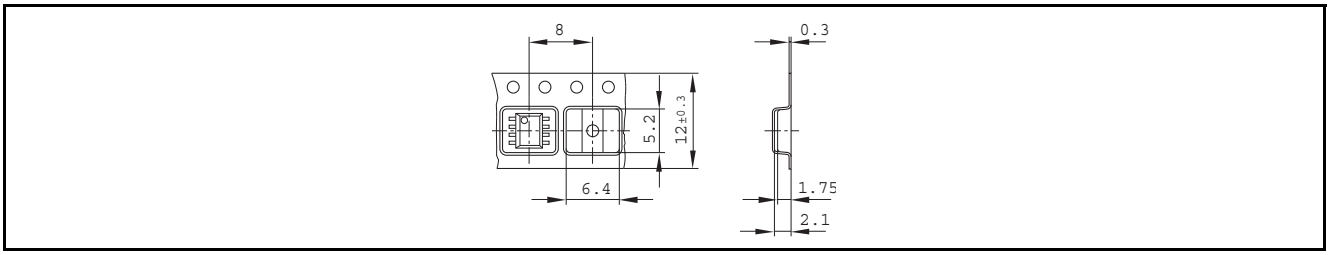


Figure 32 Tape and Reel

4.5 Marking

Position	Marking	Description
1st Line	5012xx	See ordering table on page 7
2nd Line	xxx	Lot code
3rd Line	Gxxxx	G..green, 4-digit..date code

Processing

Note: For processing recommendations, please refer to Infineon's Notes on processing

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