HIP4082

80V, 1.25A Peak Current H-Bridge FET Driver

FN3676
Rev.6.00
Feb 12, 2020

The HIP4082 is a medium frequency, medium voltage H-Bridge N-Channel MOSFET driver IC, available in 16 lead plastic SOIC (N) and DIP packages.

Specifically targeted for PWM motor control and UPS applications, bridge based designs are made simple and flexible with the HIP4082 H-bridge driver. With operation up to 80V, the device is best suited to applications of moderate power levels.

Similar to the HIP4081, it has a flexible input protocol for driving every possible switch combination except those which would cause a shoot-through condition. The HIP4082's reduced drive current allows smaller packaging and it has a much wider range of programmable dead times (0.1 to 4.5µs) making it ideal for switching frequencies up to 200kHz. The HIP4082 does not contain an internal charge pump, but does incorporate non-latching level-shift translation control of the upper drive circuits.

This set of features and specifications is optimized for applications where size and cost are important. For applications needing higher drive capability the HIP4080A and HIP4081A are recommended.

Features

- Independently Drives 4 N-Channel FET in Half Bridge or Full Bridge Configurations
- Bootstrap Supply Max Voltage to 95VDC
- Drives 1000pF Load in Free Air at 50°C with Rise and Fall Times of Typically 15ns
- User-Programmable Dead Time (0.1 to 4.5µs)
- DIS (Disable) Overrides Input Control and Refreshes Bootstrap Capacitor when Pulled Low
- Input Logic Thresholds Compatible with 5V to 15V Logic Levels
- Shoot-Through Protection
- Undervoltage Protection
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- UPS Systems
- DC Motor Controls
- Full Bridge Power Supplies
- Switching Power Amplifiers
- Noise Cancellation Systems
- Battery Powered Vehicles
- Peripherals
- Medium/Large Voice Coil Motors
- Related Literature
  - TB363, Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HIP4082IBZ* (Note)	4082IBZ	-55 to +125	16 Ld SOIC (N) (Pb-free)	M16.15
HIP4082IPZ (Note)	HIP4082IPZ	-55 to +125	16 Ld PDIP** (Pb-free)	E16.3

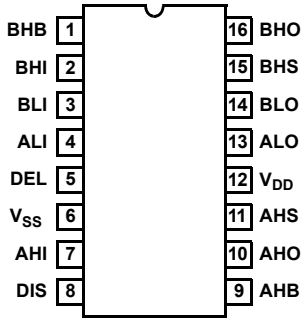
*Add “T” suffix for tape and reel.

NOTE: Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

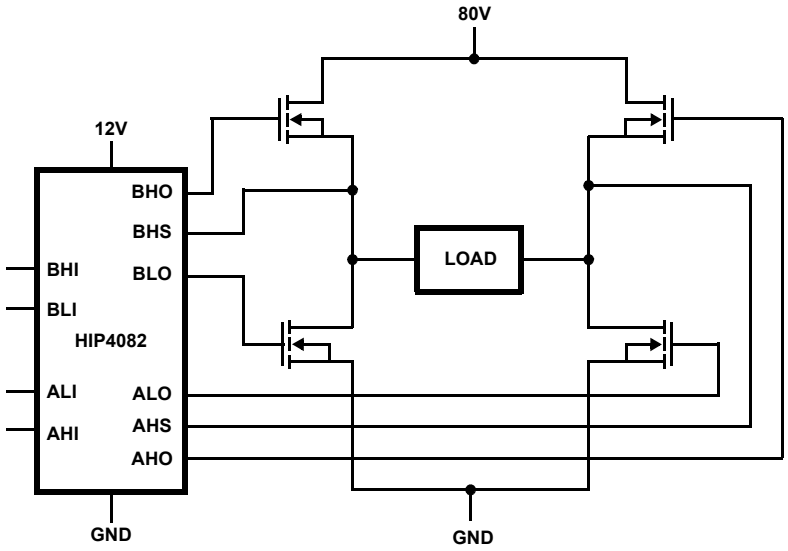
**Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

Pinout

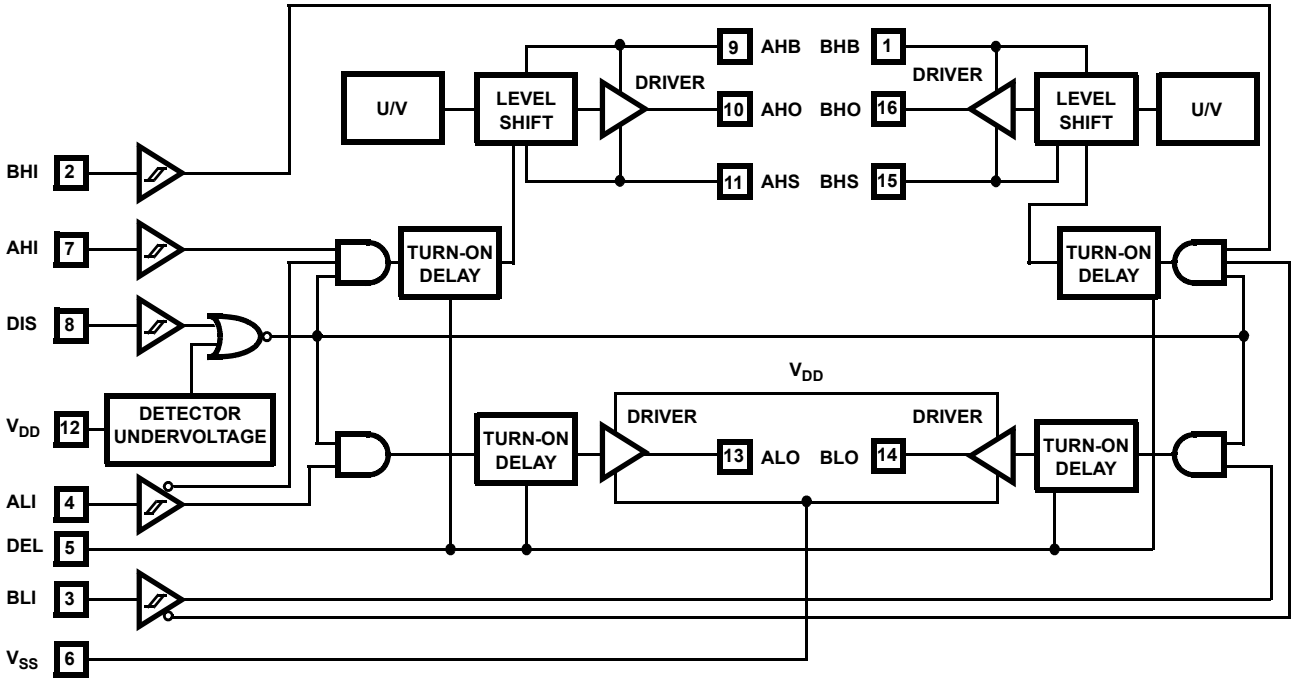
HIP4082
(PDIP, SOIC)
TOP VIEW



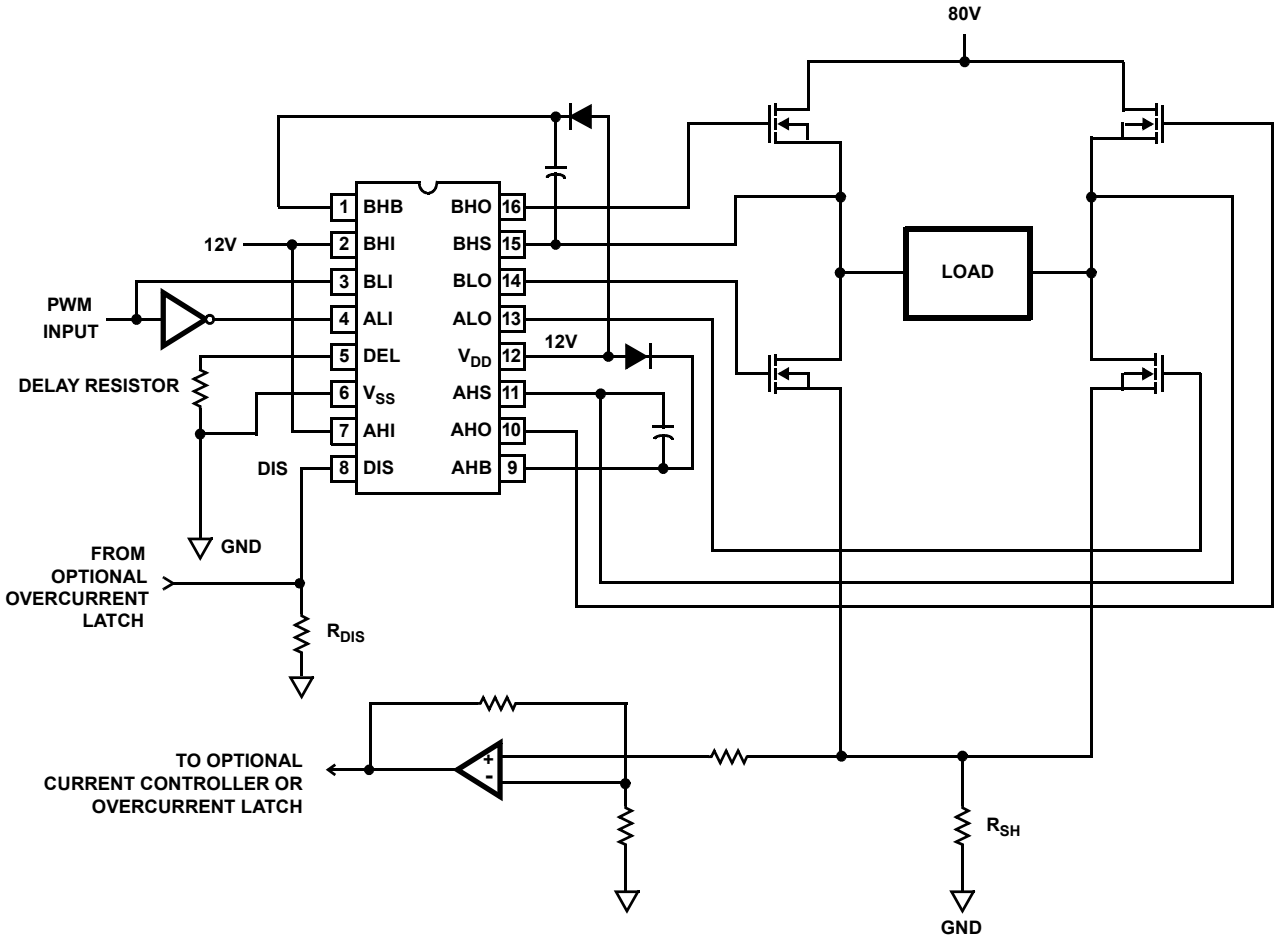
Application Block Diagram



Functional Block Diagram



Typical Application (PWM Mode Switching)



Absolute Maximum Ratings

Supply Voltage, V_{DD} . . . . . -0.3V to 16V
Logic I/O Voltages . . . . . -0.3V to V_{DD} +0.3V
Voltage on AHS, BHS . . . . . -6V (Transient) to 80V (25°C to 150°C)
Voltage on AHS, BHS . . . . . -6V (Transient) to 70V (-55°C to150°C)
Voltage on AHB, BHB . . . . . $V_{AHS, BHS}$ -0.3V to $V_{AHS, BHS}$ +V_{DD}
Voltage on ALO, BLO. . . . . V_{SS} -0.3V to V_{DD} +0.3V
Voltage on AHO, BHO . . . $V_{AHS, BHS}$ -0.3V to $V_{AHB, BHB}$ +0.3V Input Current, DEL . . . . . -5mA to 0mA
Phase Slew Rate 20V/ns
NOTE: All voltages are relative V_{SS} unless otherwise specified.

Operating Conditions

Supply Voltage, V_{DD} . . . . . +8.5V to +15V
Voltage on V_{SS}. . . . . -1.0V to +1.0V
Voltage on AHB, BHB . . . . . $V_{AHS, BHS}$ +7.5V to $V_{AHS, BHS}$ +V_{DD}
Input Current, DEL . . . . . -4mA to -100µA

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)
SOIC Package	115
DIP Package	90

Maximum Power Dissipation. . . . . See Curve
Storage Temperature Range . . . . . -65°C to +150°C
Operating Max. Junction Temperature. . . . . +150°C
Lead Temperature (Soldering 10s) . . . . . +300°C
(For SOIC - Lead Tips Only))

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

$V_{DD} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{AHS} = V_{BHS} = 0V$, $R_{DEL} = 100K$

PARAMETER	SYMBOL	TEST CONDITIONS	T_J = +25°C			T_J = -55°C TO +150°C		UNITS
			MIN	TYP	MAX	MIN	MAX	
SUPPLY CURRENTS & UNDER VOLTAGE PROTECTION								
V_{DD} Quiescent Current	I_{DD}	All inputs = 0V, R_{DEL} = 100K	1.2	2.3	3.5	0.85	4	mA
		All inputs = 0V, R_{DEL} = 10K	2.2	4.0	5.5	1.9	6.0	mA
V_{DD} Operating Current	I_{DDO}	f = 50kHz, no load	1.5	2.6	4.0	1.1	4.2	mA
		50kHz, no load, R_{DEL} = 10kΩ	2.5	4.0	6.4	2.1	6.6	mA
AHB, BHB Off Quiescent Current	I_{AHBL}, I_{BHBL}	AHI = BHI = 0V	0.5	1.0	1.5	0.4	1.6	mA
AHB, BHB On Quiescent Current	I_{AHBH}, I_{BHBH}	AHI = BHI = V_{DD}	65	145	240	40	250	µA
AHB, BHB Operating Current	I_{AHBO}, I_{BHBO}	f = 50kHz, CL = 1000pF	.65	1.1	1.8	.45	2.0	mA
AHS, BHS Leakage Current	I_{HLK}	V_{AHS} = V_{BHS} = 80V V_{AHB} = V_{BHB} = 96 V_{DD} = Not Connected	-	-	1.0	-	-	µA
V_{DD} Rising Undervoltage Threshold	V_{DDUV+}		6.8	7.6	8.25	6.5	8.5	V
V_{DD} Falling Undervoltage Threshold	V_{DDUV-}		6.5	7.1	7.8	6.25	8.1	V
Undervoltage Hysteresis	UVHYS		0.17	0.4	0.75	0.15	0.90	V
AHB, BHB Undervoltage Threshold	VHBUV	Referenced to AHS & BHS	5	6.0	7	4.5	7.5	V
INPUT PINS: ALI, BLI, AHI, BHI, & DIS								
Low Level Input Voltage	V_{IL}	Full Operating Conditions	-	-	1.0	-	0.8	V
High Level Input Voltage	V_{IH}	Full Operating Conditions	2.5	-	-	2.7		V
Input Voltage Hysteresis			-	35	-	-	-	mV
Low Level Input Current	I_{IL}	V_{IN} = 0V, Full Operating Conditions	-145	-100	-60	-150	-50	µA
High Level Input Current	I_{IH}	V_{IN} = 5V, Full Operating Conditions	-1	-	+1	-10	+10	µA
TURN-ON DELAY PIN DEL								
Dead Time	T_{DEAD}	R_{DEL} = 100K	2.5	4.5	8.0	2.0	8.5	µs
		R_{DEL} = 10K	0.27	0.5	0.75	0.2	0.85	µs

Electrical Specifications $V_{DD} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{AHS} = V_{BHS} = 0V$, $R_{DEL} = 100K$ **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	T_J = +25°C			T_J = -55°C TO +150°C		UNITS
			MIN	TYP	MAX	MIN	MAX	
GATE DRIVER OUTPUT PINS: ALO, BLO, AHO, & BHO								
Low Level Output Voltage	V_{OL}	I_{OUT} = 50mA	0.65		1.1	0.5	1.2	V
High Level Output Voltage	V_{DD}-V_{OH}	I_{OUT} = -50mA	0.7		1.2	0.5	1.3	V
Peak Pullup Current	I_O+	V_{OUT} = 0V	1.1	1.4	2.5	0.85	2.75	A
Peak Pulldown Current	I_O-	V_{OUT} = 12V	1.0	1.3	2.3	0.75	2.5	A

Switching Specifications $V_{DD} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{AHS} = V_{BHS} = 0V$, R_{DEL}= 100K, C_L = 1000pF.

PARAMETER	SYMBOL	TEST CONDITIONS	T_J = +25°C			T_J = -55°C TO +150°C		UNITS
			MIN	TYP	MAX	MIN	MAX	
Lower Turn-off Propagation Delay (ALI-ALO, BLI-BLO)	T_{LPHL}		-	25	50	-	70	ns
Upper Turn-off Propagation Delay (AHI-AHO, BHI-BHO)	T_{HPHL}		-	55	80	-	100	ns
Lower Turn-on Propagation Delay (ALI-ALO, BLI-BLO)	T_{LPLH}		-	40	85	-	100	ns
Upper Turn-on Propagation Delay (AHI-AHO, BHI-BHO)	T_{HPLH}		-	75	110	-	150	ns
Rise Time	T_R		-	9	20	-	25	ns
Fall Time	T_F		-	9	20	-	25	ns
Minimum Input Pulse Width	$T_{PWIN-ON/OFF}$		50	-	-	50	-	ns
Output Pulse Response to 50 ns Input Pulse	T_{PWOUT}			63			80	ns
Disable Turn-off Propagation Delay (DIS - Lower Outputs)	T_{DISLOW}		-	50	80	-	90	ns
Disable Turn-off Propagation Delay (DIS - Upper Outputs)	$T_{DISHIGH}$		-	75	100	-	125	ns
Disable Turn-on Propagation Delay (DIS - ALO & BLO)	T_{DLPLH}		-	40	70	-	100	ns
Disable Turn-on Propagation Delay (DIS- AHO & BHO)	T_{DHPLH}	R_{DEL} = 10K	-	1.2	2	-	3	µs
Refresh Pulse Width (ALO & BLO)	T_{REF-PW}		375	580	900	350	950	ns

TRUTH TABLE

INPUT					OUTPUT	
ALI, BLI	AHI, BHI	VDDUV	VHBUV	DIS	ALO, BLO	AHO, BHO
X	X	X	X	1	0	0
X	X	1	X	X	0	0
0	X	0	1	0	0	0
1	X	0	X	0	1	0
0	1	0	0	0	0	1
0	0	0	0	0	0	0

NOTE: X signifies that input can be either a “1” or “0”.

Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1	BHB	B High-side Bootstrap supply. External bootstrap diode and capacitor are required. Connect cathode of bootstrap diode and positive side of bootstrap capacitor to this pin.
2	BHI	B High-side Input. Logic level input that controls BHO driver (Pin 16). BLI (Pin 3) high level input overrides BHI high level input to prevent half-bridge shoot-through, see Truth Table. DIS (Pin 8) high level input overrides BHI high level input. The pin can be driven by signal levels of 0V to 15V (no greater than V_{DD}).
3	BLI	B Low-side Input. Logic level input that controls BLO driver (Pin 14). If BHI (Pin 2) is driven high or not connected externally then BLI controls both BLO and BHO drivers, with dead time set by delay currents at DEL (Pin 5). DIS (Pin 8) high level input overrides BLI high level input. The pin can be driven by signal levels of 0V to 15V (no greater than V_{DD}).
4	ALI	A Low-side Input. Logic level input that controls ALO driver (Pin 13). If AHI (Pin 7) is driven high or not connected externally then ALI controls both ALO and AHO drivers, with dead time set by delay currents at DEL (Pin 5). DIS (Pin 8) high level input overrides ALI high level input. The pin can be driven by signal levels of 0V to 15V (no greater than V_{DD}).
5	DEL	Turn-on DELay. Connect resistor from this pin to V_{SS} to set timing current that defines the dead time between drivers. All drivers turn-off with no adjustable delay, so the DEL resistor guarantees no shoot-through by delaying the turn-on of all drivers. The voltage across the DEL resistor is approximately Vdd -2V.
6	V_{SS}	Chip negative supply, generally will be ground.
7	AHI	A High-side Input. Logic level input that controls AHO driver (Pin 10). ALI (Pin 4) high level input overrides AHI high level input to prevent half-bridge shoot-through, see Truth Table. DIS (Pin 8) high level input overrides AHI high level input. The pin can be driven by signal levels of 0V to 15V (no greater than V_{DD}).
8	DIS	DISable input. Logic level input that when taken high sets all four outputs low. DIS high overrides all other inputs. When DIS is taken low the outputs are controlled by the other inputs. The pin can be driven by signal levels of 0V to 15V (no greater than V_{DD}).
9	AHB	A High-side Bootstrap supply. External bootstrap diode and capacitor are required. Connect cathode of bootstrap diode and positive side of bootstrap capacitor to this pin.
10	AHO	A High-side Output. Connect to gate of A High-side power MOSFET.
11	AHS	A High-side Source connection. Connect to source of A High-side power MOSFET. Connect negative side of bootstrap capacitor to this pin.
12	V_{DD}	Positive supply to control logic and lower gate drivers. De-couple this pin to V_{SS} (Pin 6).
13	ALO	A Low-side Output. Connect to gate of A Low-side power MOSFET.
14	BLO	B Low-side Output. Connect to gate of B Low-side power MOSFET.
15	BHS	B High-side Source connection. Connect to source of B High-side power MOSFET. Connect negative side of bootstrap capacitor to this pin.
16	BHO	B High-side Output. Connect to gate of B High-side power MOSFET.

Timing Diagrams

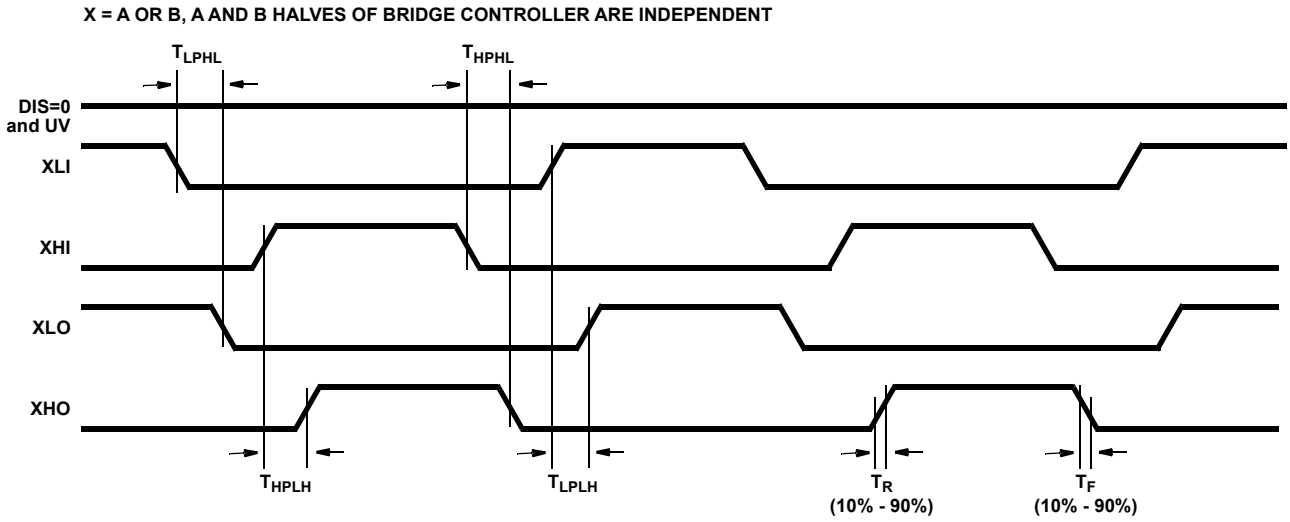


FIGURE 1. INDEPENDENT MODE

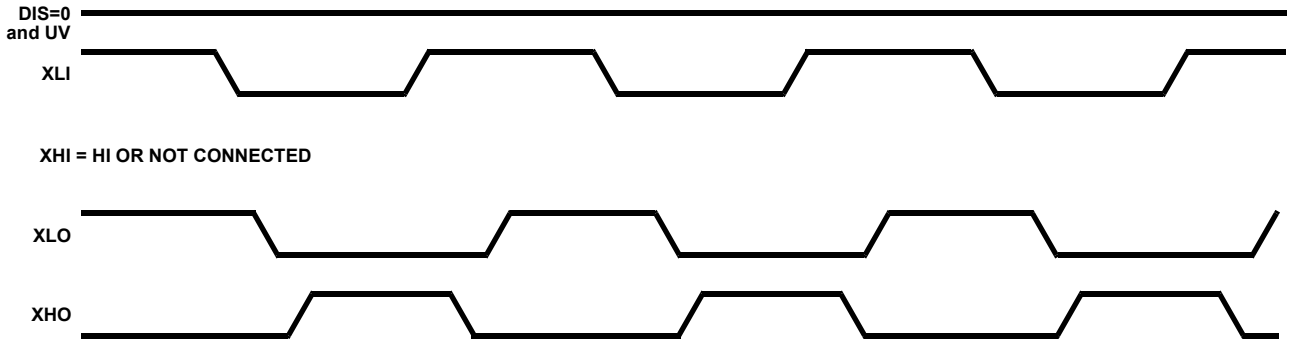


FIGURE 2. BISTATE MODE

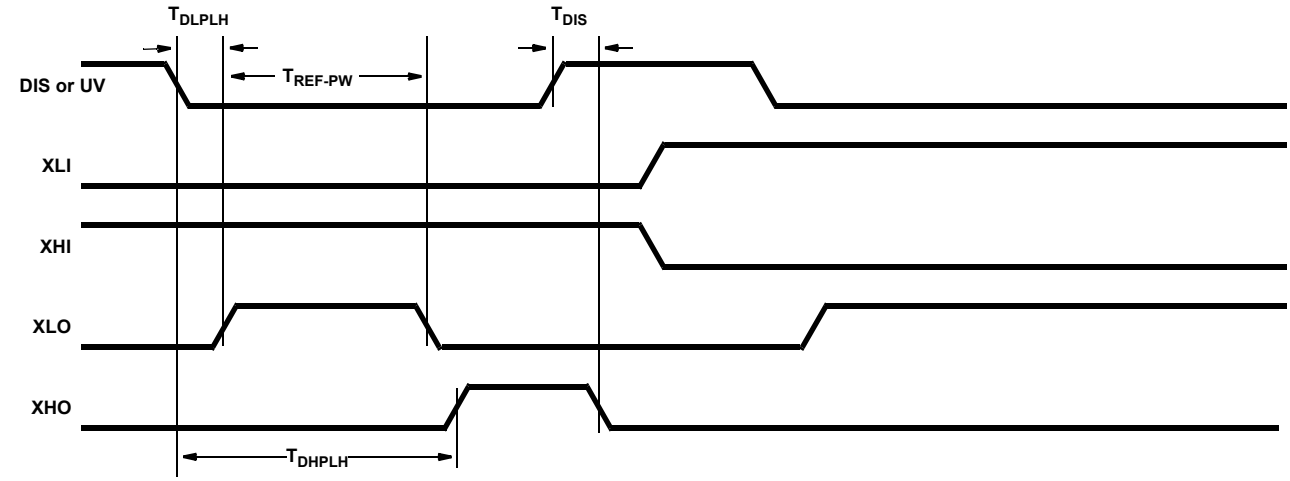


FIGURE 3. DISABLE FUNCTION

Performance Curves

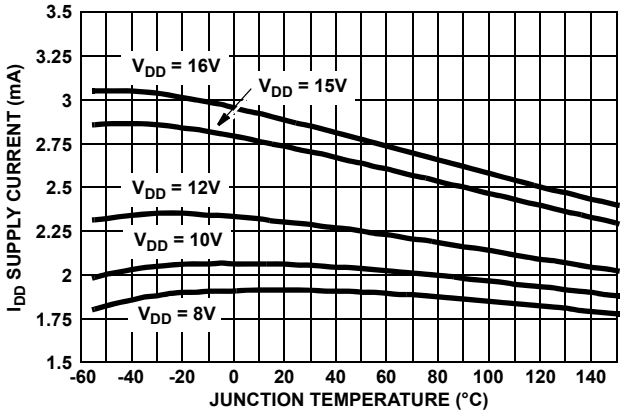


FIGURE 4. I_{DD} SUPPLY CURRENT vs TEMPERATURE AND V_{DD} SUPPLY VOLTAGE

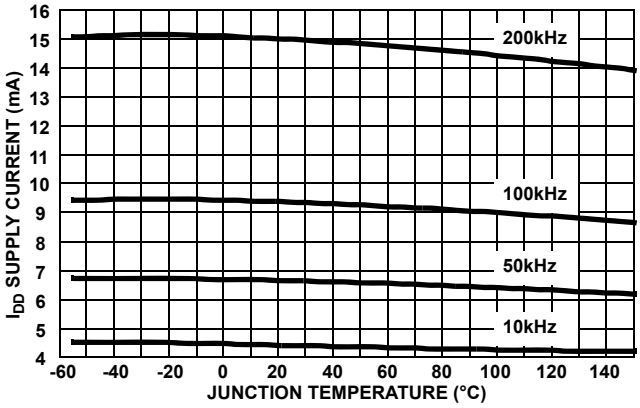


FIGURE 5. V_{DD} SUPPLY CURRENT vs TEMPERATURE AND SWITCHING FREQUENCY (1000pF LOAD)

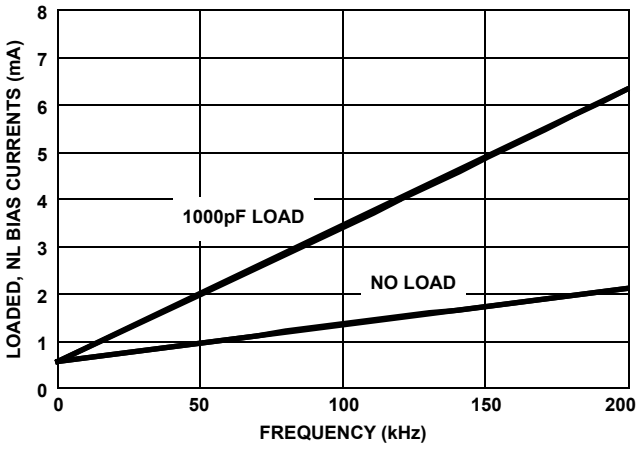


FIGURE 6. FLOATING (IXHB) BIAS CURRENT vs FREQUENCY AND LOAD

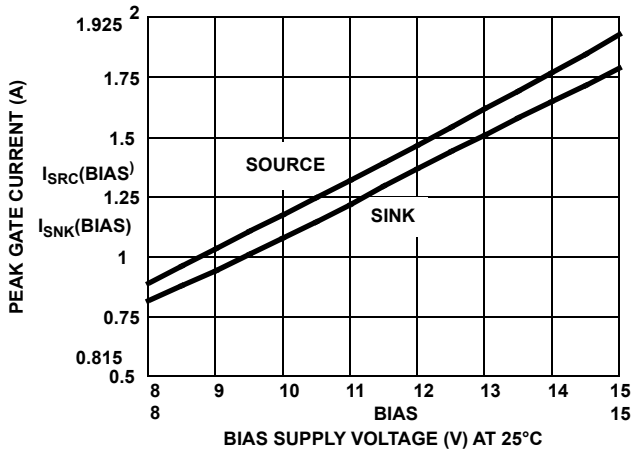


FIGURE 7. GATE SOURCE/SINK PEAK CURRENT vs BIAS SUPPLY VOLTAGE AT 25°C

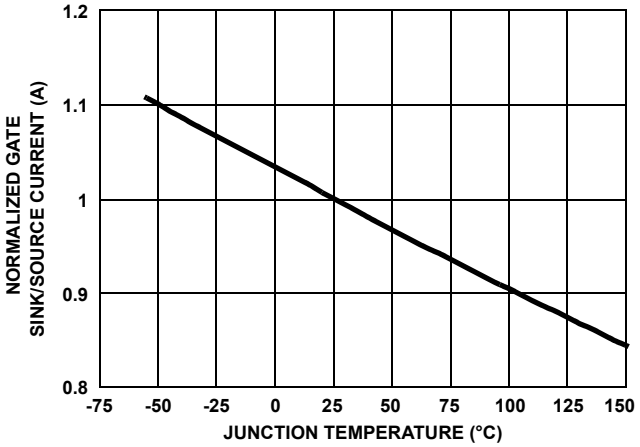


FIGURE 8. GATE CURRENT vs TEMPERATURE, NORMALIZED TO 25°C

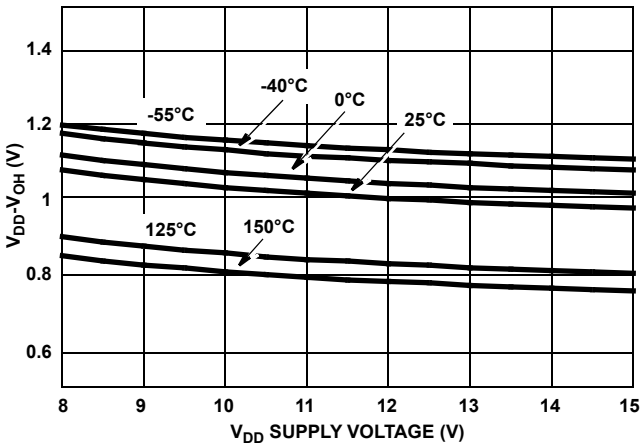


FIGURE 9. V_{DD}-V_{OH} vs BIAS VOLTAGE TEMPERATURE

Performance Curves (Continued)

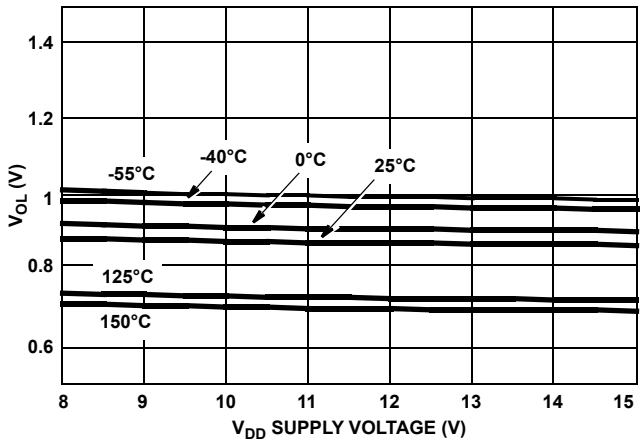


FIGURE 10. V_{OL} vs BIAS VOLTAGE AND TEMPERATURE

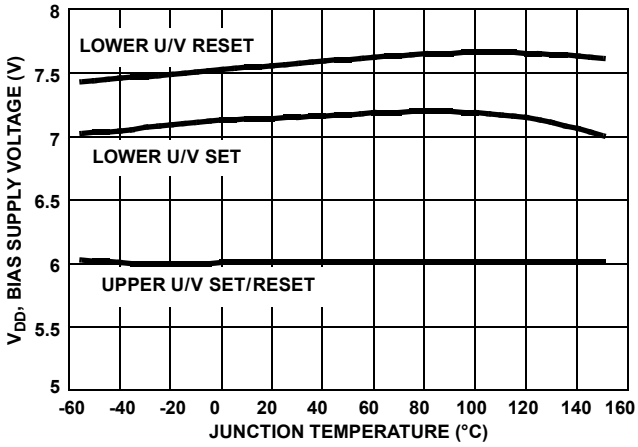


FIGURE 11. UNDERVOLTAGE TRIP VOLTAGES vs TEMPERATURE

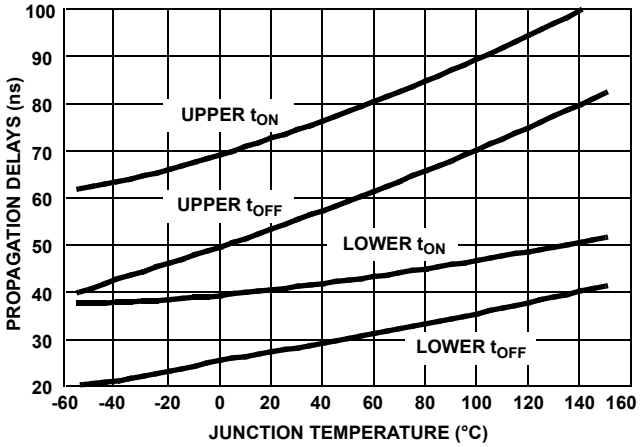


FIGURE 12. UPPER LOWER TURN-ON/TURN-OFF PROPAGATION DELAY vs TEMPERATURE

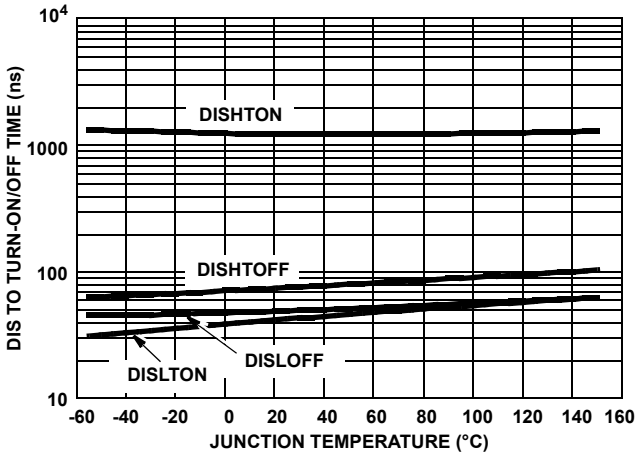


FIGURE 13. UPPER/LOWER DIS(ABLE) TO TURN-ON/OFF vs TEMPERATURE (°C)

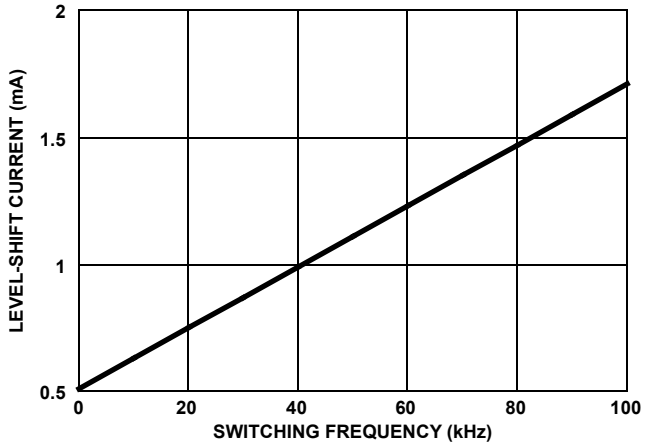


FIGURE 14. FULL BRIDGE LEVEL-SHIFT CURRENT vs FREQUENCY (kHz)

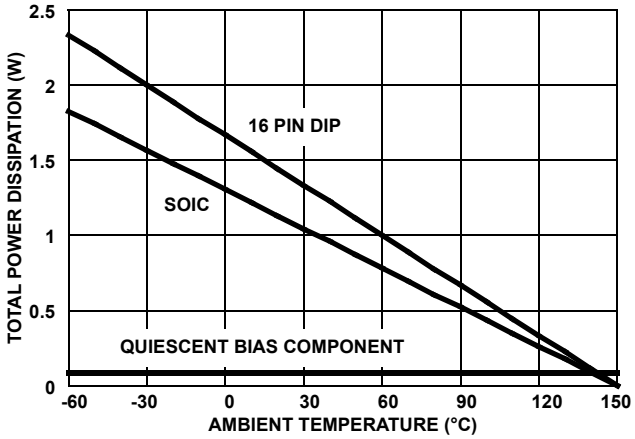


FIGURE 15. MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE

Performance Curves (Continued)

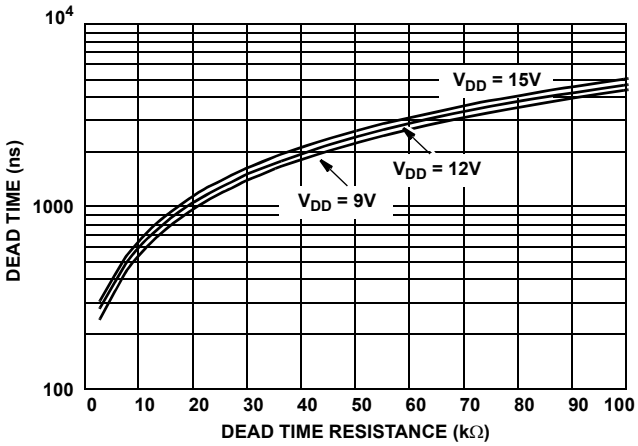


FIGURE 16. DEAD-TIME vs DEL RESISTANCE AND BIAS SUPPLY (V_{DD}) VOLTAGE

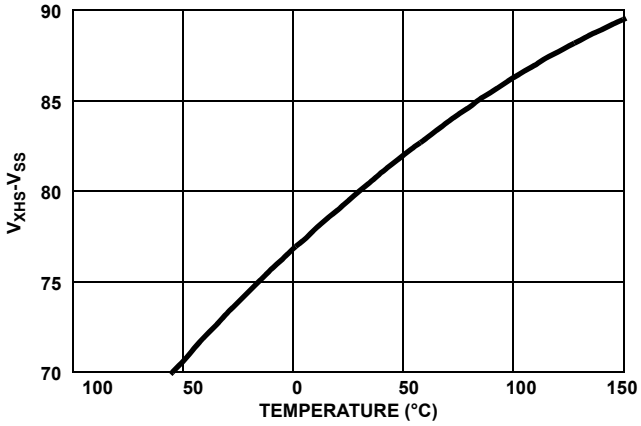


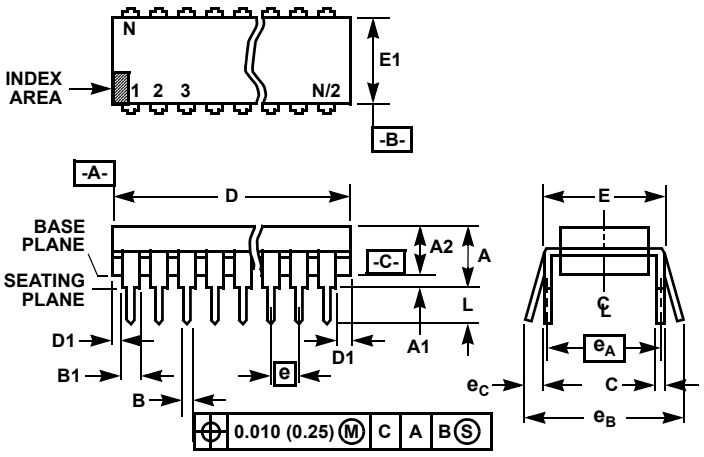
FIGURE 17. MAXIMUM OPERATING PEAK AHS/BHS VOLTAGE vs TEMPERATURE

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
Feb 12, 2020	FN3676.6	Updated Ordering information table on page 2. Removed About Intersil section. Updated POD M16.15 to the latest revision, changes are as follows: -Updated graphics to new standard layout, removing the dimension table. Updated disclaimer.
Sep 30, 2015	FN3676.5	Updated the Ordering Information Table on page 2. Added Revision History and About Intersil sections.

Package Outline Drawings



NOTES:

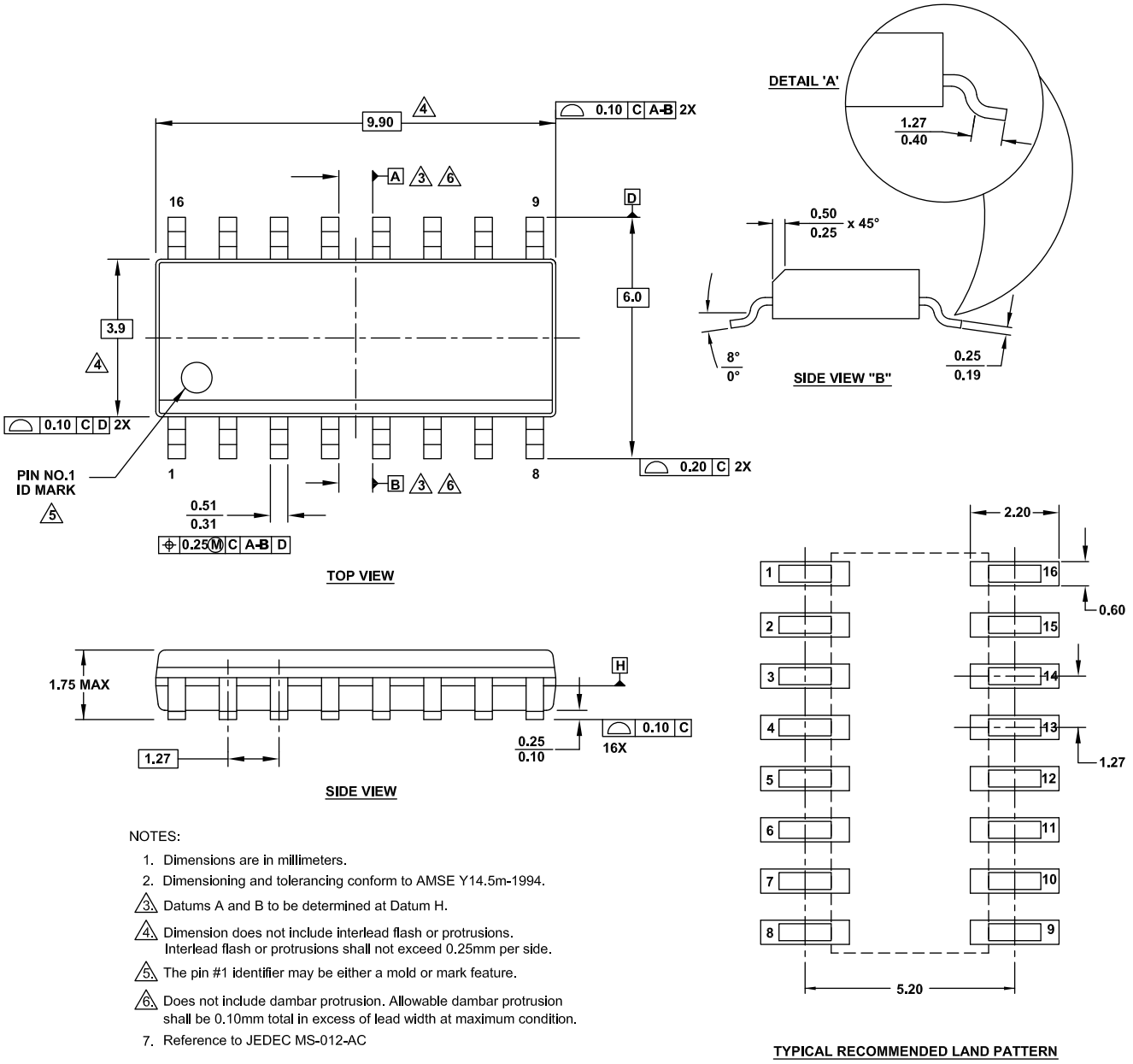
1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E16.3 (JEDEC MS-001-BB ISSUE D)
16 LEAD DUAL-IN-LINE PLASTIC PACKAGE (PDIP)

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	16		16		9

Rev. 0 12/93

M16.15 (JEDEC MS-012-AC ISSUE C)
16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE
Rev 2, 11/17



NOTES:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Datums A and B to be determined at Datum H.
4. Dimension does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm total in excess of lead width at maximum condition.
7. Reference to JEDEC MS-012-AC

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