

74LVC1G86

2-input EXCLUSIVE-OR gate

Rev. 12 — 9 March 2017

Product data sheet

1 General description

The 74LVC1G86 provides the 2-input EXCLUSIVE-OR function.

Inputs can be driven from either 3.3 V or 5 V devices. These features allow the use of these devices in a mixed 3.3 V and 5 V environment.

This device is fully specified for partial Power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

2 Features and benefits

- Wide supply voltage range from 1.65 V to 5.5 V
- High noise immunity
- Complies with JEDEC standard:
 - JESD8-7 (1.65 V to 1.95 V)
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - HBM JESD22-A114F exceeds 2 000 V
 - MM JESD22-A115-A exceeds 200 V
- ± 24 mA output drive ($V_{CC} = 3.0$ V)
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- Multiple package options
- Specified from -40 °C to $+85$ °C and -40 °C to $+125$ °C

3 Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC1G86GW	-40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	SOT353-1
74LVC1G86GV	-40 °C to +125 °C	SC-74A	plastic surface-mounted package; 5 leads	SOT753
74LVC1G86GM	-40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm	SOT886
74LVC1G86GF	-40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1 x 0.5 mm	SOT891
74LVC1G86GN	-40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 0.9 x 1.0 x 0.35 mm	SOT1115
74LVC1G86GS	-40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 1.0 x 1.0 x 0.35 mm	SOT1202
74LVC1G86GX	-40 °C to +125 °C	X2SON5	X2SON5: plastic thermal enhanced extremely thin small outline package; no leads; 5 terminals; body 0.8 x 0.8 x 0.35 mm	SOT1226

4 Marking

Table 2. Marking codes

Type number	Marking ^[1]
74LVC1G86GW	VH
74LVC1G86GV	V86
74LVC1G86GM	VH
74LVC1G86GF	VH
74LVC1G86GN	VH
74LVC1G86GS	VH
74LVC1G86GX	VH

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5 Functional diagram

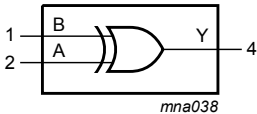


Figure 1. Logic symbol

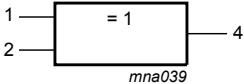


Figure 2. IEC logic symbol

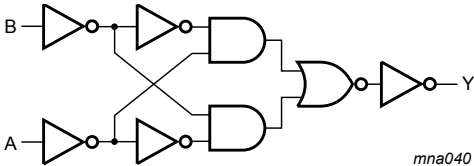


Figure 3. Logic diagram

6 Pinning information

6.1 Pinning

74LVC1G86

B 1 5 V_{CC}

A 2

GND 3 4 Y

001aaf186

Figure 4. Pin configuration SOT353-1 and SOT753

74LVC1G86

B 1 6 V_{CC}

A 2 5 n.c.

GND 3 4 Y

001aaf187

Transparent top view

Figure 5. Pin configuration SOT886

74LVC1G86

B 1 6 V_{CC}

A 2 5 n.c.

GND 3 4 Y

001aaf259

Transparent top view

Figure 6. Pin configuration SOT891, SOT1115 and SOT1202

74LVC1G86

B 1 5 V_{CC}

A 2 4 Y

3 GND

aaa-003031

Transparent top view

Figure 7. Pin configuration SOT1226 (X2SON5)

6.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	TSSOP5 and X2SON5	XSON6	
B	1	1	data input
A	2	2	data input
GND	3	3	ground (0 V)
Y	4	4	data output
n.c.	-	5	not connected
V _{CC}	5	6	supply voltage

7 Functional description

Table 4. Function table ^[1]

Input		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

[1] H = HIGH voltage level;
L = LOW voltage level

8 Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V	-50	-	mA
V_I	input voltage	^[1]	-0.5	+6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	±50	mA
V_O	output voltage	Active mode ^{[1] [2]}	-0.5	$V_{CC} + 0.5$	V
		Power-down mode ^{[1] [2]}	-0.5	+6.5	V
I_O	output current	$V_O = 0$ V to V_{CC}	-	±50	mA
I_{CC}	supply current		-	+100	mA
I_{GND}	ground current		-100	-	mA
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C ^[3]	-	250	mW
T_{stg}	storage temperature		-65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] When $V_{CC} = 0$ V (Power-down mode), the output voltage can be 5.5 V in normal operation.

[3] For TSSOP5 and SC-74A packages: above 87.5 °C the value of P_{tot} derates linearly with 4.0 mW/K.
For XSON6 and X2SON5 packages: above 118 °C the value of P_{tot} derates linearly with 7.8 mW/K.

9 Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	Active mode	0	-	V_{CC}	V
		$V_{CC} = 0$ V; Power-down mode	0	-	5.5	V
T_{amb}	ambient temperature		-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65$ V to 2.7 V	-	-	20	ns/V
		$V_{CC} = 2.7$ V to 5.5 V	-	-	10	ns/V

10 Static characteristics

Table 7. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.65V_{CC}$	-	-	$0.65V_{CC}$	-	V
		$V_{CC} = 2.3$ V to 2.7 V	1.7	-	-	1.7	-	V
		$V_{CC} = 2.7$ V to 3.6 V	2.0	-	-	2.0	-	V
		$V_{CC} = 4.5$ V to 5.5 V	$0.7V_{CC}$	-	-	$0.7V_{CC}$	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	-	-	$0.35V_{CC}$	-	$0.35V_{CC}$	V
		$V_{CC} = 2.3$ V to 2.7 V	-	-	0.7	-	0.7	V
		$V_{CC} = 2.7$ V to 3.6 V	-	-	0.8	-	0.8	V
		$V_{CC} = 4.5$ V to 5.5 V	-	-	$0.3V_{CC}$	-	$0.3V_{CC}$	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}						
		$I_O = -100$ μ A; $V_{CC} = 1.65$ V to 5.5 V	$V_{CC} - 0.1$	-	-	$V_{CC} - 0.1$	-	V
		$I_O = -4$ mA; $V_{CC} = 1.65$ V	1.2	-	-	0.95	-	V
		$I_O = -8$ mA; $V_{CC} = 2.3$ V	1.9	-	-	1.7	-	V
		$I_O = -12$ mA; $V_{CC} = 2.7$ V	2.2	-	-	1.9	-	V
		$I_O = -24$ mA; $V_{CC} = 3.0$ V	2.3	-	-	2.0	-	V
		$I_O = -32$ mA; $V_{CC} = 4.5$ V	3.8	-	-	3.4	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}						
		$I_O = 100$ μ A; $V_{CC} = 1.65$ V to 5.5 V	-	-	0.10	-	0.10	V
		$I_O = 4$ mA; $V_{CC} = 1.65$ V	-	-	0.45	-	0.70	V
		$I_O = 8$ mA; $V_{CC} = 2.3$ V	-	-	0.30	-	0.45	V
		$I_O = 12$ mA; $V_{CC} = 2.7$ V	-	-	0.40	-	0.60	V

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
		$I_O = 24 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.55	-	0.80	V
		$I_O = 32 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	-	0.55	-	0.80	V
I_I	input leakage current	$V_I = 5.5 \text{ V or GND}; V_{CC} = 0 \text{ V to } 5.5 \text{ V}$	-	± 0.1	± 1	-	± 1	μA
I_{OFF}	power-off leakage current	$V_{CC} = 0 \text{ V}; V_I \text{ or } V_O = 5.5 \text{ V}$	-	± 0.1	± 2	-	± 2	μA
I_{CC}	supply current	$V_I = 5.5 \text{ V or GND}; I_O = 0 \text{ A}; V_{CC} = 1.65 \text{ V to } 5.5 \text{ V}$	-	0.1	4	-	4	μA
ΔI_{CC}	additional supply current	per pin; $V_{CC} = 2.3 \text{ V to } 5.5 \text{ V}; V_I = V_{CC} - 0.6 \text{ V}; I_O = 0 \text{ A}$	-	5	500	-	500	μA
C_I	input capacitance	$V_{CC} = 3.3 \text{ V}; V_I = \text{GND to } V_{CC}$	-	5	-	-	-	pF

[1] All typical values are measured at $V_{CC} = 3.3 \text{ V}$ and $T_{amb} = 25 \text{ °C}$.

11 Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 9](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t_{pd}	propagation delay	A, B to Y; see Figure 8 ^[2]						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	1.0	3.7	9.9	1.0	13.0	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	0.5	2.5	5.5	0.5	7.0	ns
		$V_{CC} = 2.7 \text{ V}$	0.5	2.8	5.8	0.5	7.5	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	0.5	2.3	5.0	0.5	6.5	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	0.5	1.9	4.0	0.5	5.5	ns
C_{PD}	power dissipation capacitance	$V_I = \text{GND to } V_{CC}$ ^[3]						
		$V_{CC} = 3.3 \text{ V}$	-	25	-	-	-	pF

[1] All typical values are measured at nominal V_{CC} .

[2] t_{pd} is the same as t_{PLH} and t_{PHL} .

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

11.1 Waveforms and test circuit

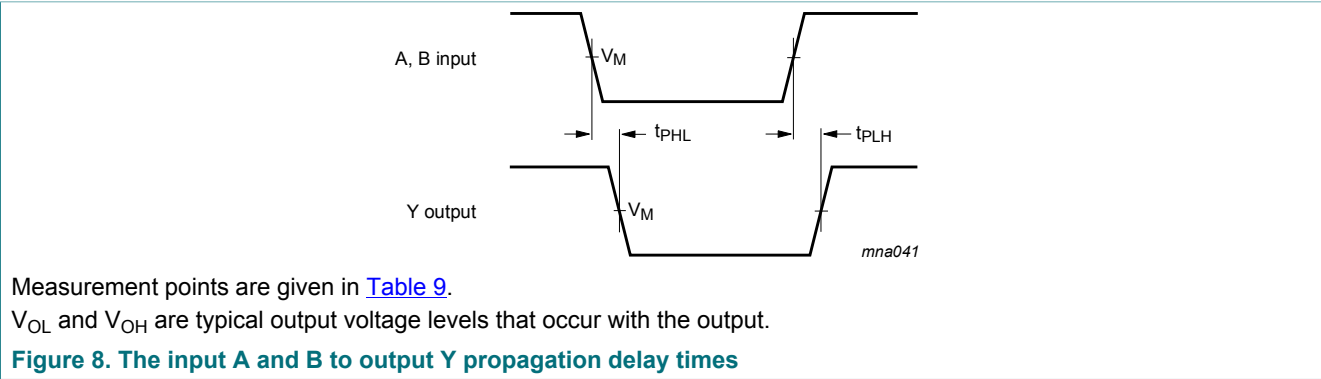
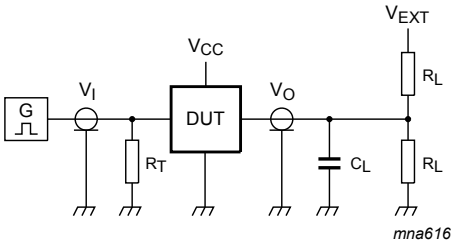


Table 9. Measurement points

Supply voltage	Input	Output
V_{CC}	V_M	V_M
1.65 V to 1.95 V	$0.5V_{CC}$	$0.5V_{CC}$
2.3 V to 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$
2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	1.5 V	1.5 V
4.5 V to 5.5 V	$0.5V_{CC}$	$0.5V_{CC}$



Test data is given in [Table 10](#).

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

V_{EXT} = External voltage for measuring switching times.

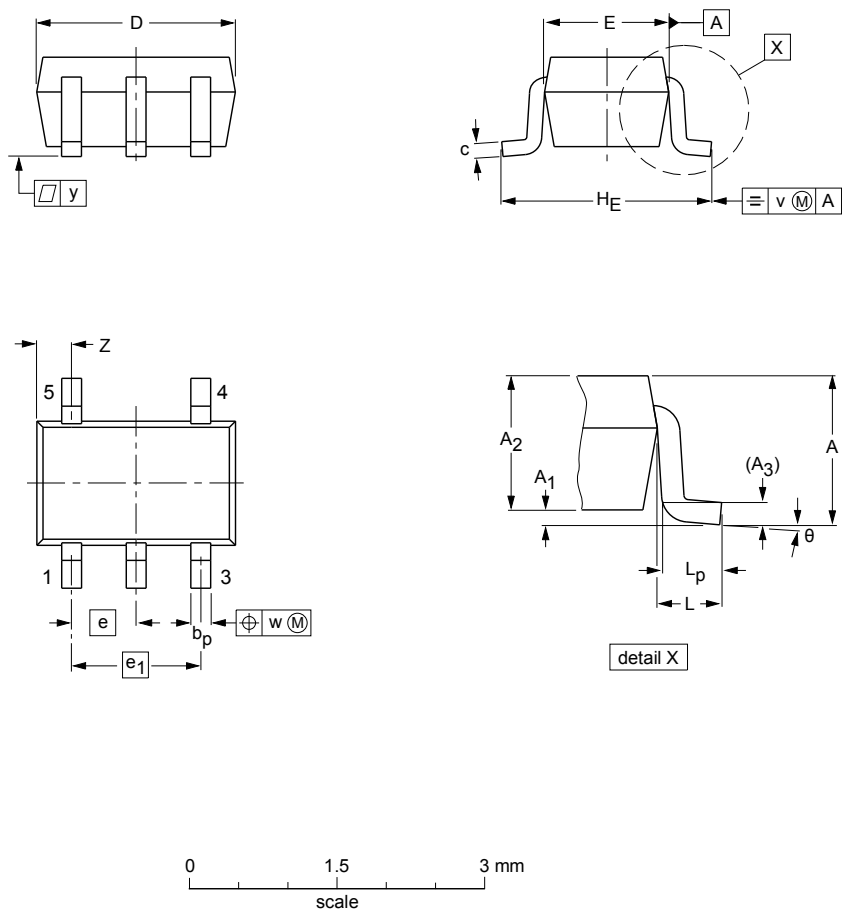
Figure 9. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input	Load			V_{EXT}
V_{CC}	V_I	$t_r = t_f$	C_L	R_L	t_{PLH}, t_{PHL}
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	30 pF	1 k Ω	open
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
4.5 V to 5.5 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω	open

12 Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm SOT353-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	H _E	L	L _p	v	w	y	Z ⁽¹⁾	θ
mm	1.1	0.1 0	1.0 0.8	0.15	0.30 0.15	0.25 0.08	2.25 1.85	1.35 1.15	0.65	1.3	2.25 2.0	0.425	0.46 0.21	0.3	0.1	0.1	0.60 0.15	7° 0°

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.


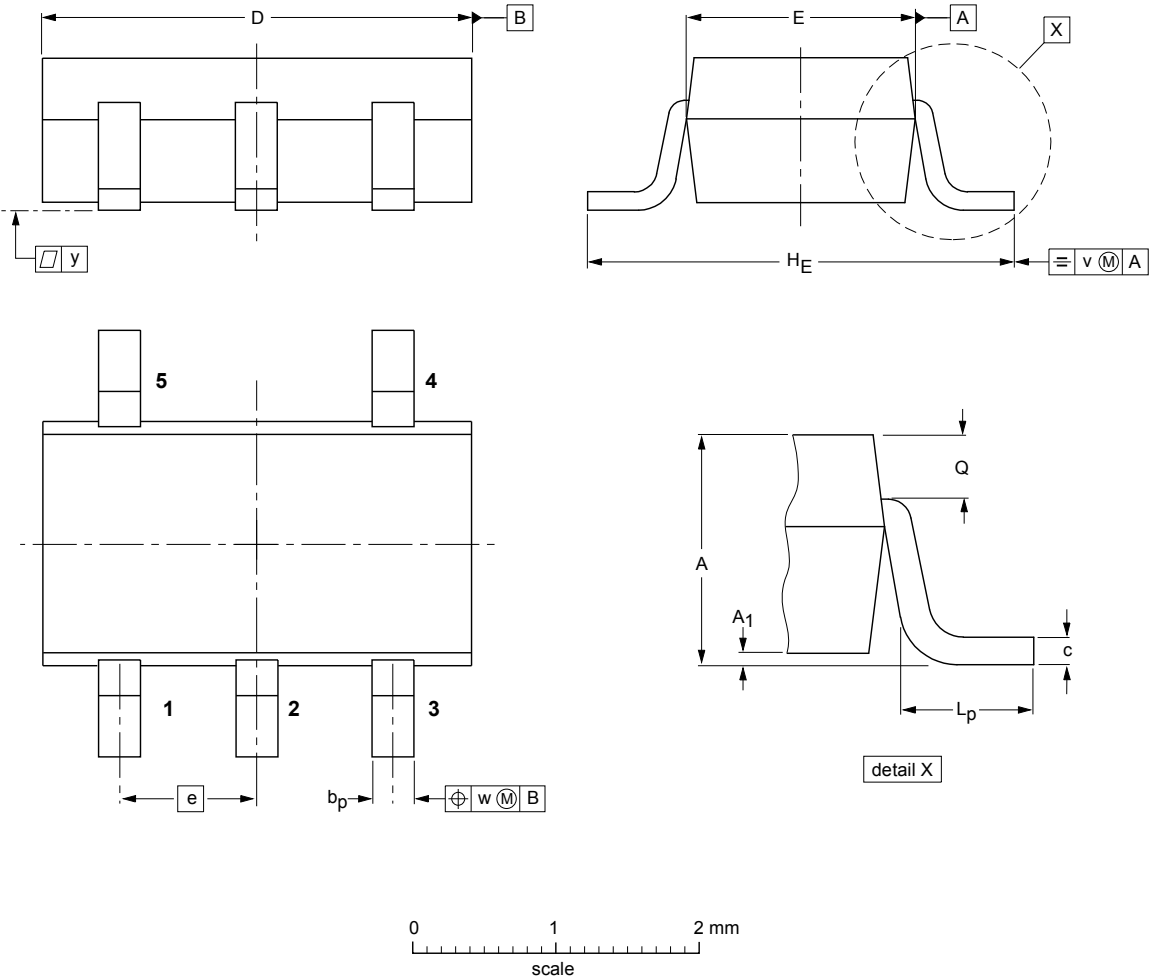
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT353-1		MO-203	SC-88A			00-09-01 03-02-19

Figure 10. Package outline SOT353-1 (TSSOP5)

Plastic surface-mounted package; 5 leads

SOT753



DIMENSIONS (mm are the original dimensions)

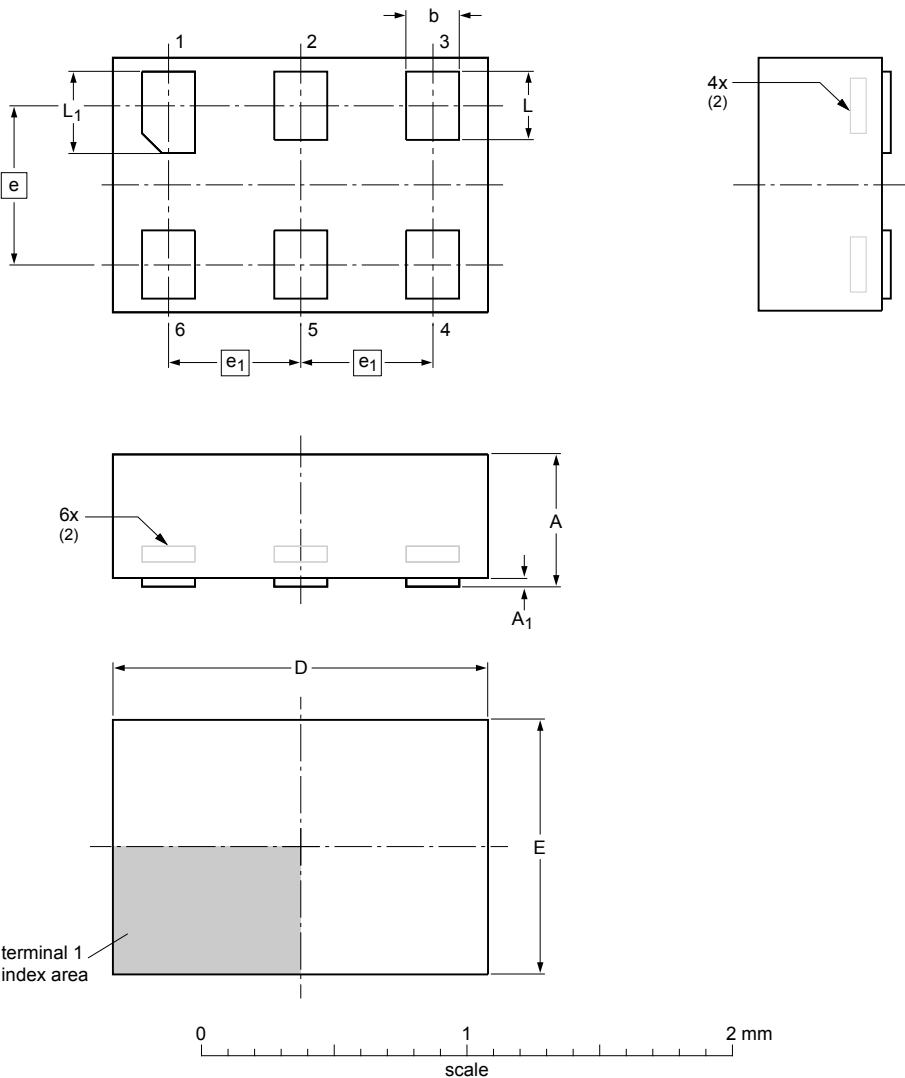
UNIT	A	A ₁	b _p	c	D	E	e	H _E	L _p	Q	v	w	y
mm	1.1 0.9	0.100 0.013	0.40 0.25	0.26 0.10	3.1 2.7	1.7 1.3	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT753			SC-74A			02-04-16 06-03-16

Figure 11. Package outline SOT753 (SC-74A)

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm

SOT886



Dimensions (mm are the original dimensions)

Unit	A ⁽¹⁾	A ₁	b	D	E	e	e ₁	L	L ₁
mm	max	0.5	0.04	0.25	1.50	1.05		0.35	0.40
	nom			0.20	1.45	1.00	0.6	0.30	0.35
	min			0.17	1.40	0.95		0.27	0.32

- Notes
- 1. Including plating thickness.
 - 2. Can be visible in some manufacturing processes.

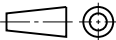
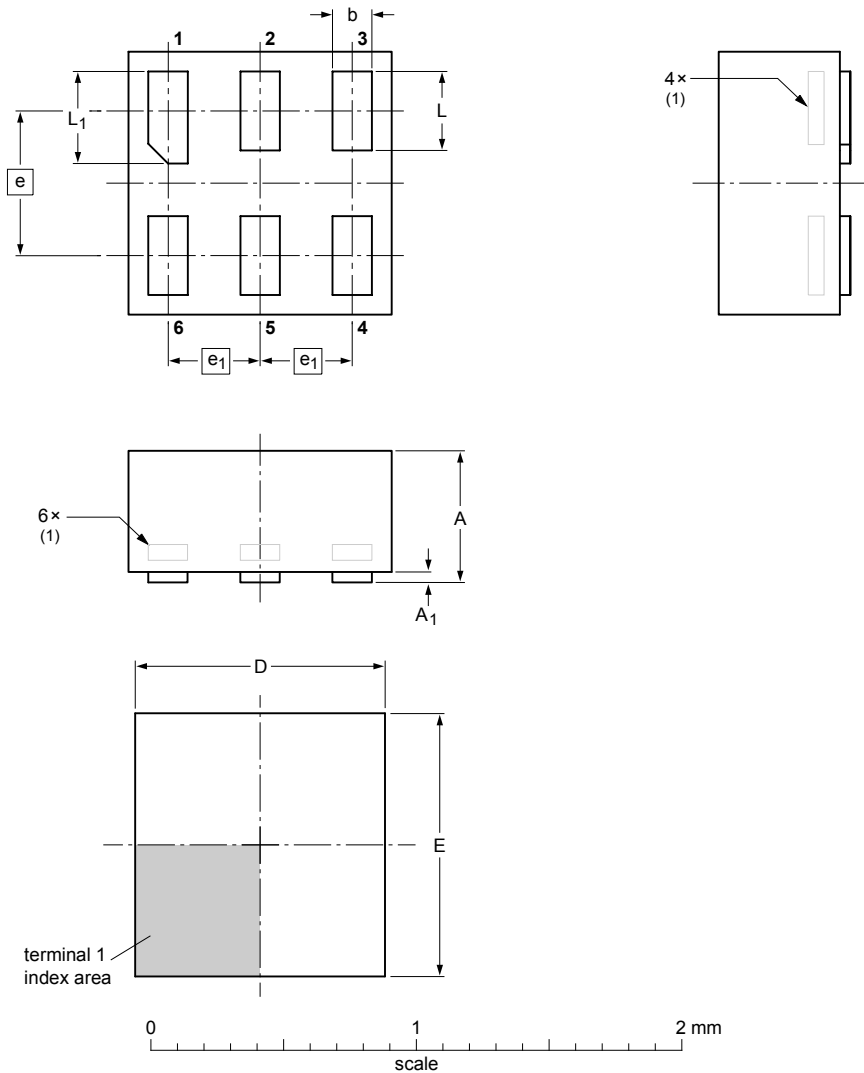
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT886	MO-252					04-07-22 12-01-05

Figure 12. Package outline SOT886 (XSON6)

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1 x 0.5 mm

SOT891



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A ₁ max	b	D	E	e	e ₁	L	L ₁
mm	0.5	0.04	0.20 0.12	1.05 0.95	1.05 0.95	0.55	0.35	0.35 0.27	0.40 0.32

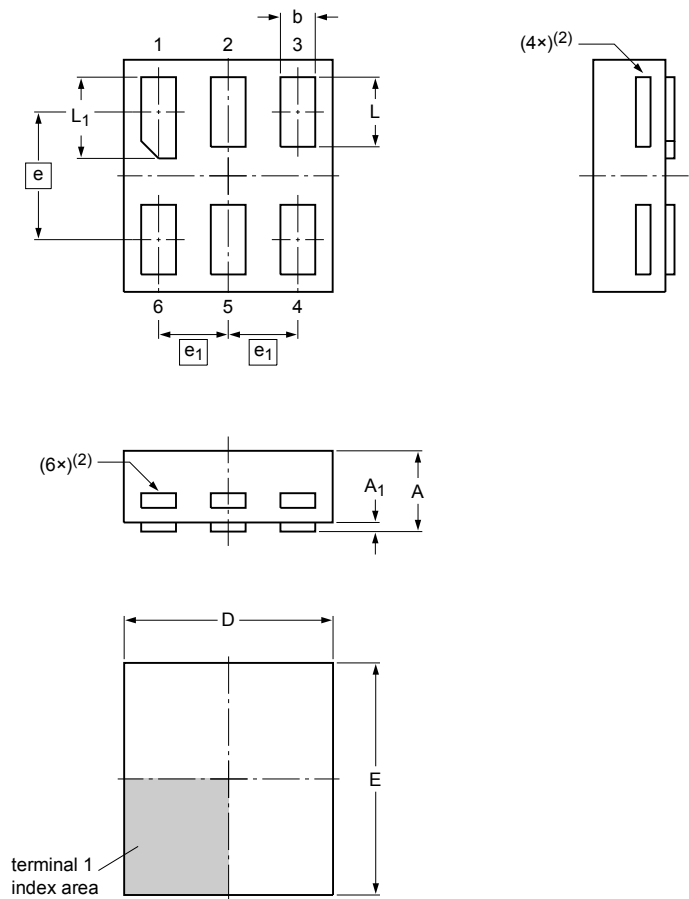
Note
1. Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT891						05-04-06 07-05-15

Figure 13. Package outline SOT891 (XSON6)

XSON6: extremely thin small outline package; no leads;
6 terminals; body 0.9 x 1.0 x 0.35 mm

SOT1115



Dimensions

Unit	A ⁽¹⁾	A ₁	b	D	E	e	e ₁	L	L ₁
mm	max	0.35	0.04	0.20	0.95	1.05		0.35	0.40
	nom			0.15	0.90	1.00	0.55	0.30	0.35
	min			0.12	0.85	0.95		0.27	0.32

Note

- 1. Including plating thickness.
- 2. Visible depending upon used manufacturing technology.

sot1115_po

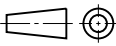
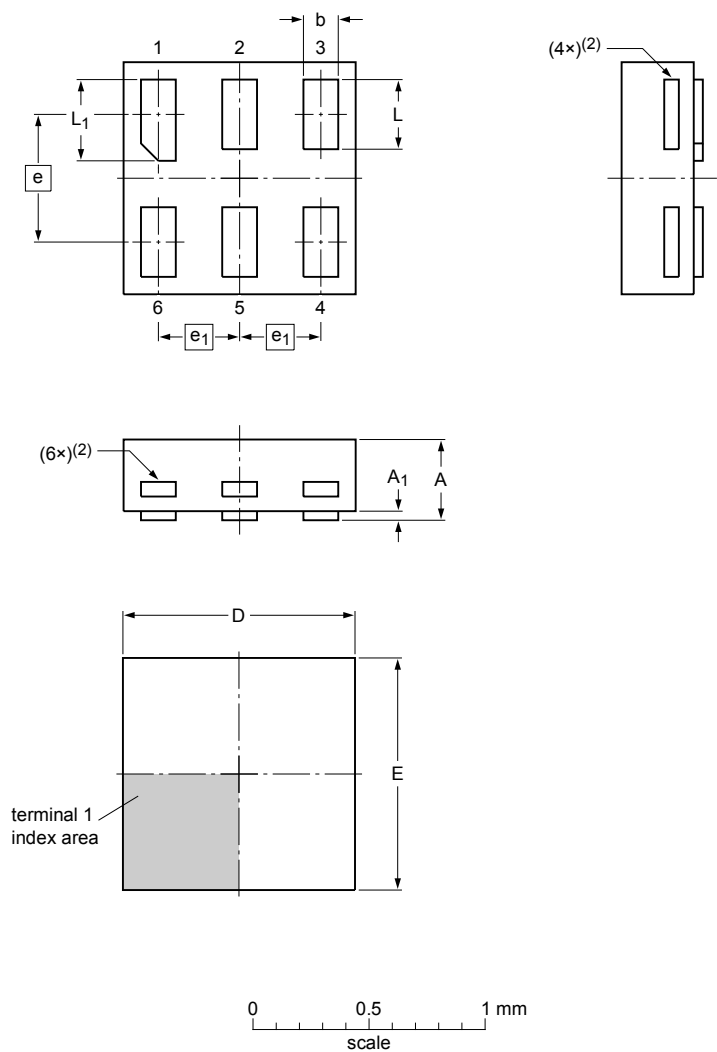
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1115						10-04-02 10-04-07

Figure 14. Package outline SOT1115 (XSON6)

XSON6: extremely thin small outline package; no leads;
6 terminals; body 1.0 x 1.0 x 0.35 mm

SOT1202



Dimensions

Unit	A ⁽¹⁾	A ₁	b	D	E	e	e ₁	L	L ₁
mm	max	0.35	0.04	0.20	1.05	1.05		0.35	0.40
	nom			0.15	1.00	1.00	0.55	0.30	0.35
	min			0.12	0.95	0.95		0.27	0.32

Note

1. Including plating thickness.
2. Visible depending upon used manufacturing technology.

sot1202_po


Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1202						10-04-02 10-04-06

Figure 15. Package outline SOT1202 (XSON6)

X2SON5: plastic thermal enhanced extremely thin small outline package; no leads;
5 terminals; body 0.8 x 0.8 x 0.35 mm

SOT1226

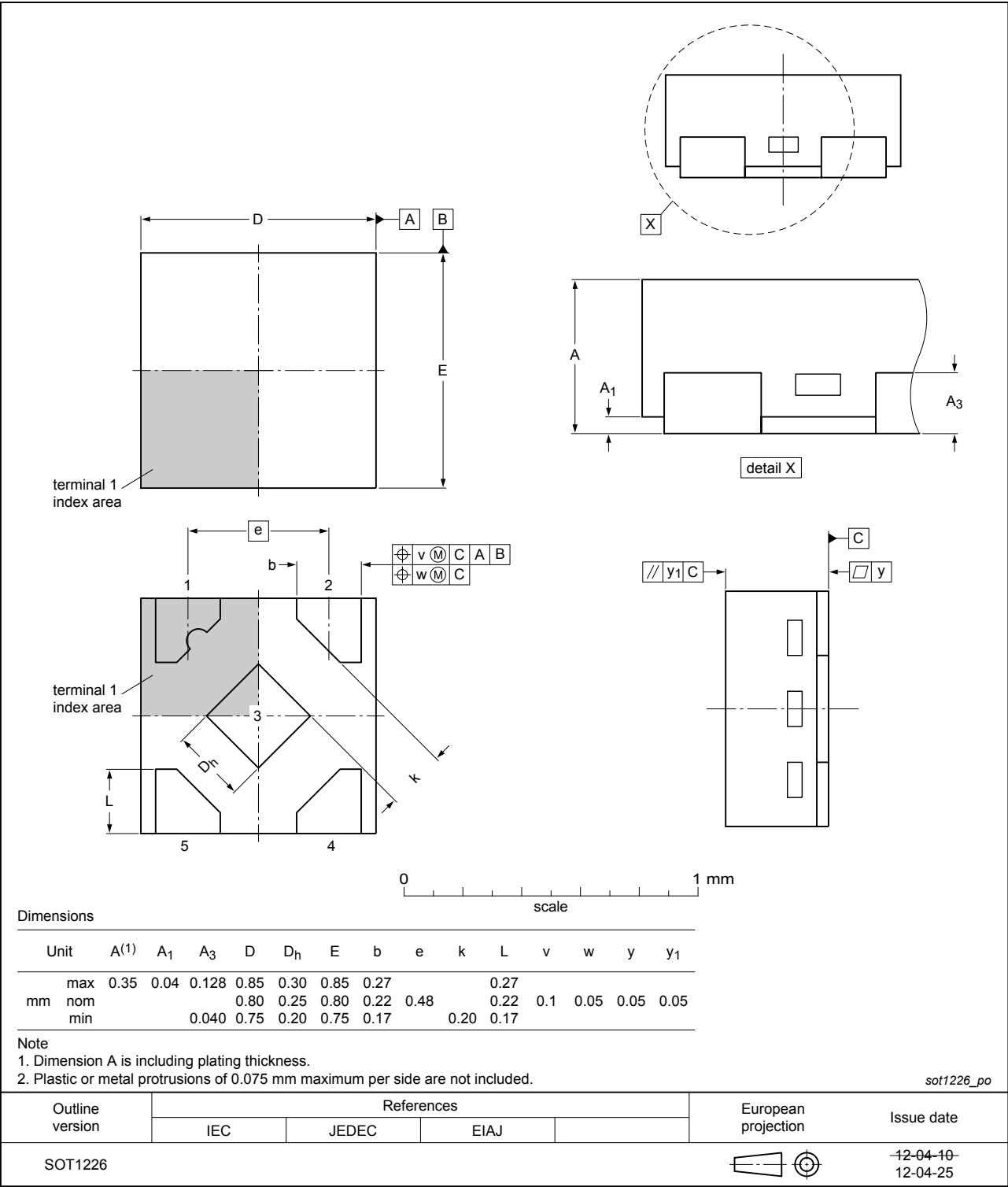


Figure 16. Package outline SOT1226 (X2SON5)

13 Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14 Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC1G86 v.12	20170309	Product data sheet	-	74LVC1G86 v.11
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. 			
74LVC1G86 v.11	20161212	Product data sheet	-	74LVC1G86 v.10
Modifications:	<ul style="list-style-type: none"> Table 7: The maximum limits for leakage current and supply current have changed. 			
74LVC1G86 v.10	20120702	Product data sheet	-	74LVC1G86 v.9
Modifications:	<ul style="list-style-type: none"> Added type number 74LVC1G86GX (SOT1226) 			
74LVC1G86 v.9	20120305	Product data sheet	-	74LVC1G86 v.8
Modifications:	<ul style="list-style-type: none"> Package outline drawing of SOT886 (Figure 12) modified. 			
74LVC1G86 v.8	20111201	Product data sheet	-	74LVC1G86 v.7
Modifications:	<ul style="list-style-type: none"> Legal pages updated. 			
74LVC1G86 v.7	20100914	Product data sheet	-	74LVC1G86 v.6
74LVC1G86 v.6	20070718	Product data sheet	-	74LVC1G86 v.5
74LVC1G86 v.5	20060913	Product data sheet	-	74LVC1G86 v.4
74LVC1G86 v.4	20040908	Product specification	-	74LVC1G86 v.3
74LVC1G86 v.3	20021115	Product specification	-	74LVC1G86 v.2
74LVC1G86 v.2	20010406	Preliminary specification	-	74LVC1G86 v.1
74LVC1G86 v.1	20001222	Preliminary specification	-	-

15 Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

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For sales office addresses, please send an email to: salesaddresses@nexperia.com

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