IS43/46DR81280C
IS43/46DR16640C

128Mx8, 64Mx16 DDR2 DRAM

JANUARY 2016

FEATURES

- V_{DD} = 1.8V ±0.1V, V_{DDQ} = 1.8V ±0.1V
- JEDEC standard 1.8V I/O (SSTL_18-compatible)
- Double data rate interface: two data transfers per clock cycle
- Differential data strobe (DQS, $\overline{DQS}$)
- 4-bit prefetch architecture
- On chip DLL to align DQ and DQS transitions with CK
- 8 internal banks for concurrent operation
- Programmable CAS latency (CL) 3, 4, 5, 6 and 7 supported
- Posted CAS and programmable additive latency (AL) 0, 1, 2, 3, 4, 5 and 6 supported
- WRITE latency = READ latency - 1 tCK
- Programmable burst lengths: 4 or 8
- Adjustable data-output drive strength, full and reduced strength options
- On-die termination (ODT)

OPTIONS

- Configuration(s):
  128Mx8 (16Mx8x8 banks): IS43/46DR81280C
  64Mx16 (8Mx16x8 banks): IS43/46DR16640C
- Package:
  x8: 60-ball BGA (8mm x 10.5mm)
  x16: 84-ball WBGA (8mm x 12.5mm)
- Timing – Cycle time
  2.5ns @CL=5 DDR2-800D
  2.5ns @CL=6 DDR2-800E
  3.0ns @CL=5 DDR2-667D
  3.75ns @CL=4 DDR2-533C
  5ns @CL=3 DDR2-400B
- Temperature Range:
  Commercial (0°C ≤ Tc ≤ 85°C)
  Industrial (-40°C ≤ Tc ≤ 95°C; -40°C ≤ T_A ≤ 85°C)
  Automotive, A1 (-40°C ≤ Tc ≤ 95°C; -40°C ≤ T_A ≤ 85°C)
  Automotive, A2 (-40°C ≤ Tc; T_A ≤ 105°C)
  Tc = Case Temp, T_A = Ambient Temp

DESCRIPTION

ISSI's 1Gb DDR2 SDRAM uses a double-data-rate architecture to achieve high-speed operation. The double-data rate architecture is essentially a 4n-prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O balls.

ADDRESS TABLE

Parameter	128M x 8	64M x 16
Configuration	16M x 8 x 8 banks	8M x 16 x 8 banks
Refresh Count	8K/64ms	8K/64ms
Row Addressing	16K (A0-A13)	8K (A0-A12)
Column Addressing	1K (A0-A9)	1K (A0-A9)
Bank Addressing	BA0 - BA2	BA0 - BA2
Precharge Addressing	A10	A10

KEY TIMING PARAMETERS

Speed Grade	-25D	-3D
tRCD	12.5	15
tRP	12.5	15
tRC	55	55
tRAS	40	40
tCK @CL=3	5	5
tCK @CL=4	3.75	3.75
tCK @CL=5	2.5	3
tCK @CL=6	2.5	—

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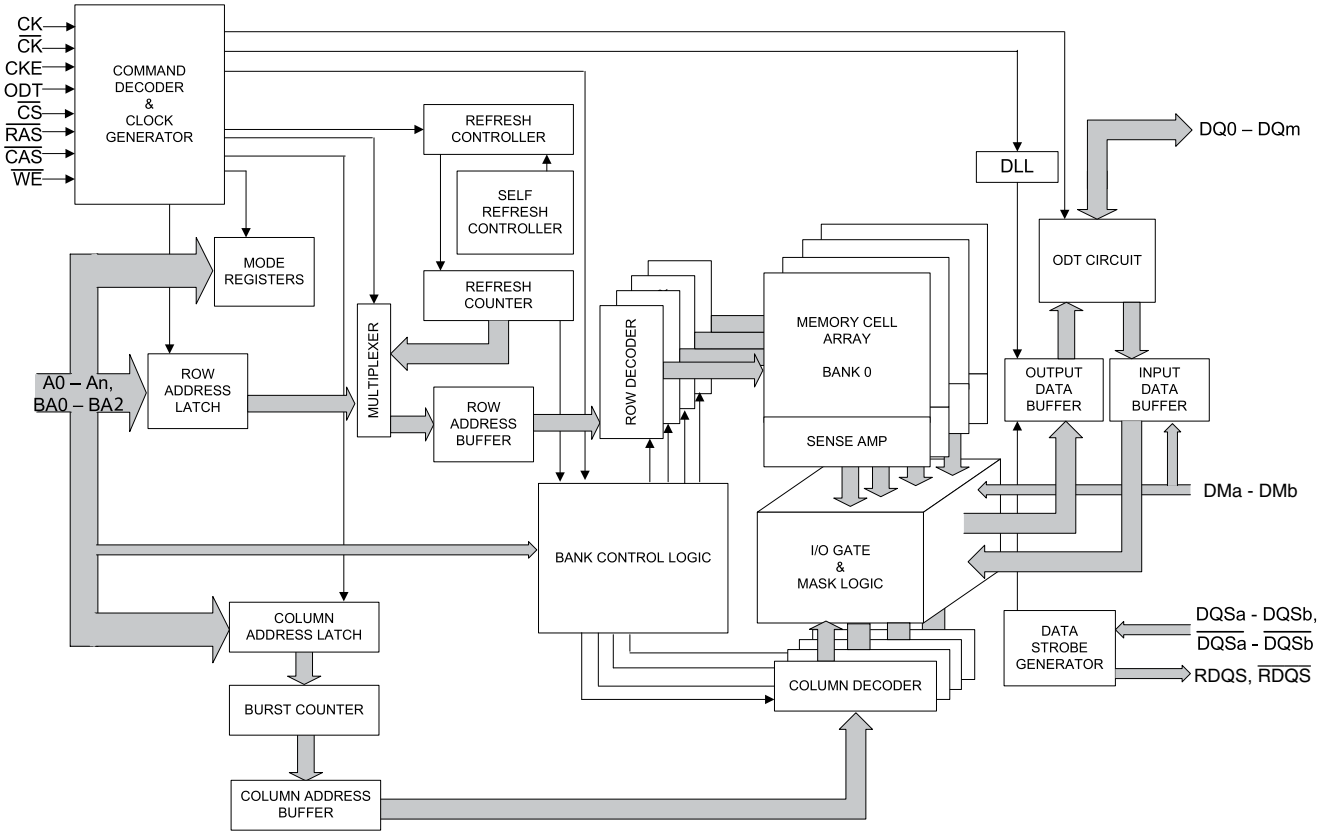
a.) the risk of injury or damage has been minimized;
b.) the user assume all such risks; and
c.) potential liability of Integrated Silicon Solution, Inc is adequately protected under the circumstances

GENERAL DESCRIPTION

Read and write accesses to the DDR2 SDRAM are burst oriented; accesses start at a selected location and continue for a burst length of four or eight in a programmed sequence. Accesses begin with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the active command are used to select the bank and row to be accessed (BA0-BA2 select the bank; A0-A12(x16) or A0-A13(x8) select the row). The address bits registered coincident with the Read or Write command are used to select the starting column location A0-A9 for the burst access and to determine if the auto precharge A10 command is to be issued. Prior to normal operation, the DDR2 SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

FUNCTIONAL BLOCK DIAGRAM



Notes:
1. An:n = no. of address pins - 1
2. DQm: m = no. of data pins - 1
3. For x8 devices:
DMa - DMb = DM; DQSa - DQSb = DQS; DQSa - DQSb = DQS; RDQS, RDQS available only for x8
4. For x16 devices:
DMa - DMb = UDM, LDM; DQSa - DQSb = UDQS, LDQS; DQSa - DQSb = UDQS, LDQS

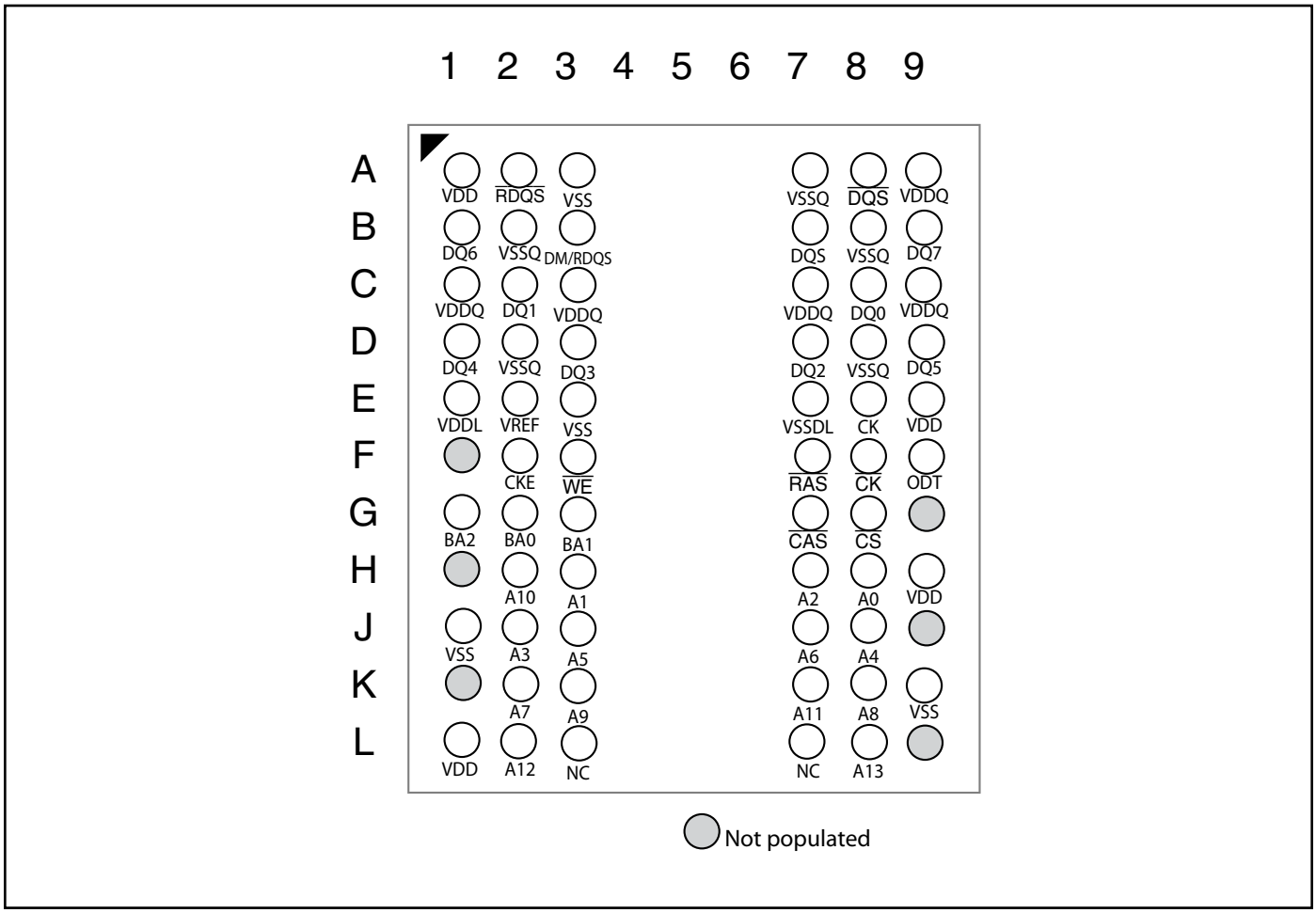
PIN DESCRIPTION TABLE

Symbol	Type	Function
CK, $\overline{CK}$	Input	Clock: CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to the crossings of CK and $\overline{CK}$ (both directions of crossing).
CKE	Input	Clock Enable: CKE HIGH activates, and CKE LOW deactivates, internal clock signals and device input buffers and output drivers. Taking CKE LOW provides Precharge Power-Down and Self Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit, and for self refresh entry. CKE is asynchronous for self refresh exit. After VREF has become stable during the power on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper self-refresh entry and exit, VREF must be maintained to this input. CKE must be maintained HIGH throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during self refresh.
$\overline{CS}$	Input	Chip Select: All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external Rank selection on systems with multiple Ranks. $\overline{CS}$ is considered part of the command code.
ODT	Input	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is applied to each DQ, DQS, $\overline{DQS}$, DM signals. The ODT pin will be ignored if the EMR(1) is programmed to disable ODT.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	Command Inputs: $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DM (x8) or UDM, LDM (x16)	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. For x8, the function of DM is enabled by EMRS command to EMR(1) [A11].
BA0 - BA2	Input	Bank Address Inputs: BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines if the mode register or one of the extended mode registers is to be accessed during a MRS or EMRS command cycle.
A0 - A13	Input	Address Inputs: Provide the row address for Active commands and the column address and Auto Precharge bit for Read/Write commands to select one location out of the memory array in the respective bank. A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0 - BA2. The address inputs also provide the op-code during MRS or EMRS commands.

Symbol	Type	Function
DQ0-7 x8 DQ0-15 x16	Input/ Output	Data Input/Output: Bi-directional data bus.
DQS, ($\overline{\text{DQS}}$) RDQS, ($\overline{\text{RDQS}}$) x8 UDQS, ($\overline{\text{UDQS}}$), LDQS, ($\overline{\text{LDQS}}$) x16	Input/ Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobes DQS(n) may be used in single ended mode or paired with optional complementary signals $\overline{\text{DQS}}$(n) to provide differential pair signaling to the system during both reads and writes. A control bit at EMR(1)[A10] enables or disables all complementary data strobe signals. x8 DQS corresponds to the data on DQ0-DQ7 RDQS corresponds to the Read data on DQ0-DQ7, and is enabled by EMRS command to EMR(1) [A11]. x16 LDQS corresponds to the data on DQ0-DQ7 UDQS corresponds to the data on DQ8-DQ15
NC		No Connect: No internal electrical connection is present.
VDDQ	Supply	DQ Power Supply: 1.8 V +/- 0.1 V
VSSQ	Supply	DQ Ground
VDDL	Supply	DLL Power Supply: 1.8 V +/- 0.1 V
VSSDL	Supply	DLL Ground
VDD	Supply	Power Supply: 1.8 V +/- 0.1 V
VSS	Supply	Ground
VREF	Supply	Reference voltage

PIN CONFIGURATION

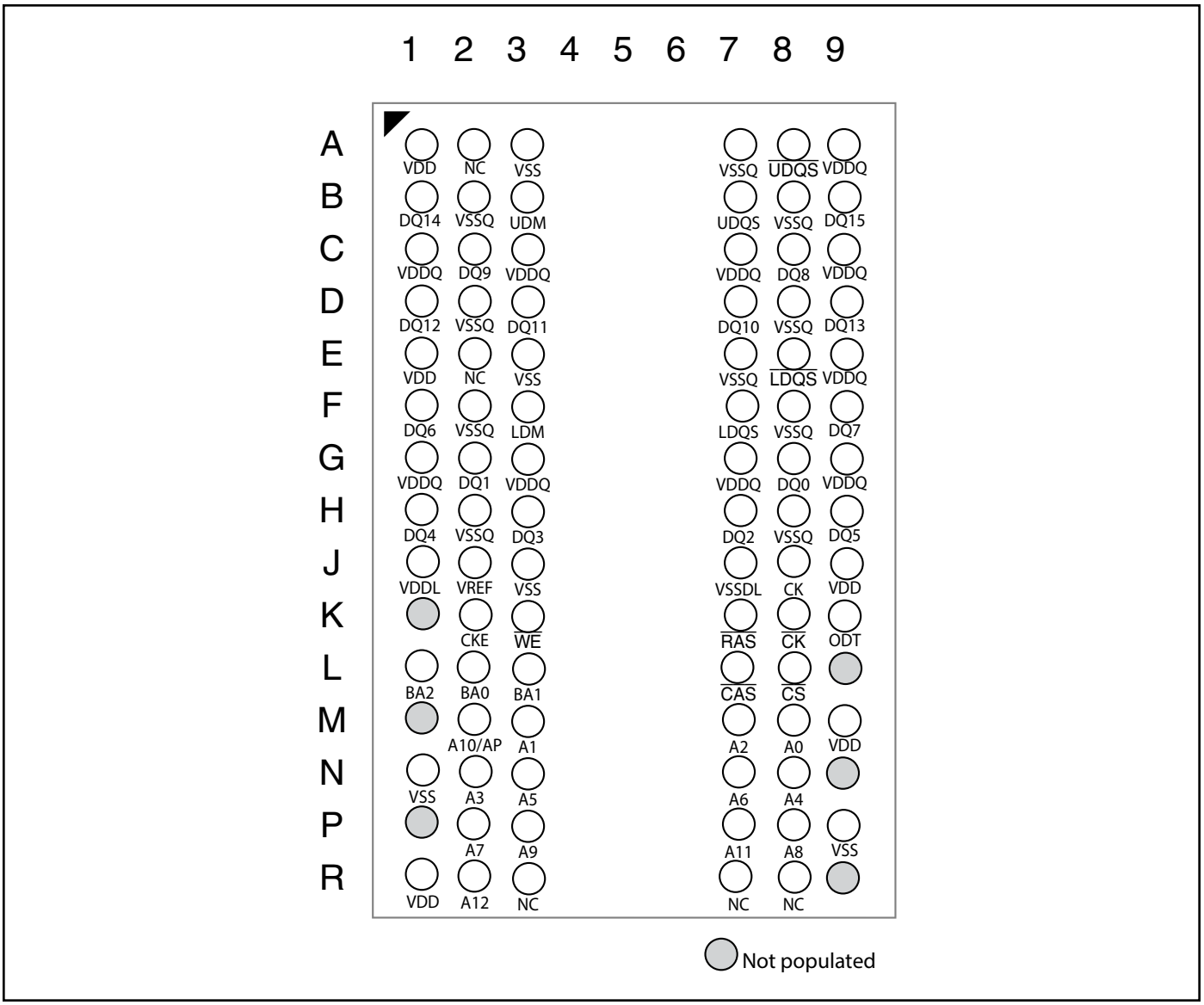
PACKAGE CODE: B 60 BALL FBGA (Top View) (8.00 mm x 10.5 mm Body, 0.8 mm Ball Pitch)



Pin name	Function	Pin name	Function
A0 to A13	Address inputs	ODT	ODT control
BA0 to BA2	Bank select	VDD	Supply voltage for internal circuit
DQ0 to DQ7	Data input/output	VSS	Ground for internal circuit
DQS, /DQS	Differential data strobe	VDDQ	Supply voltage for DQ circuit
/CS	Chip select	VSSQ	Ground for DQ circuit
/RAS, /CAS, /WE	Command input	VREF	Input reference voltage
CKE	Clock enable	VDDL	Supply voltage for DLL circuit
CK, /CK	Differential clock input	VSSDL	Ground for DLL circuit
DM	Write data mask	NC	No connection
RDQS, /RDQS	Differential Redundant Data Strobe		

PIN CONFIGURATION

PACKAGE CODE: B 84 BALL FBGA (Top View) (8.00 mm x 12.50 mm Body, 0.8 mm Ball Pitch)



Pin name	Function	Pin name	Function
A0 to A12	Address inputs	ODT	ODT control
BA0 to BA2	Bank select	VDD	Supply voltage for internal circuit
DQ0 to DQ15	Data input/output	VSS	Ground for internal circuit
LDQS, UDQS /LDQS, /UDQS	Differential data strobe	VDDQ	Supply voltage for DQ circuit
/CS	Chip select	VSSQ	Ground for DQ circuit
/RAS, /CAS, /WE	Command input	VREF	Input reference voltage
CKE	Clock enable	VDDL	Supply voltage for DLL circuit
CK, /CK	Differential clock input	VSSDL	Ground for DLL circuit
LDM to UDM	Write data mask	NC	No connection

ELECTRICAL SPECIFICATIONS

Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Notes
V_{DD}	Voltage on VDD pin relative to Vss	- 1.0~ 2.3	V	1,3
V_{DDQ}	Voltage on VDDQ pin relative to Vss	- 0.5~ 2.3	V	1,3
V_{DDL}	Voltage on VDDL pin relative to Vss	- 0.5~ 2.3	V	1,3
V_{IN}, V_{OUT}	Voltage on any pin relative to Vss	- 0.5~ 2.3	V	1,4
T_{STG}	Storage Temperature	-55 to +150	°C	1, 2
I_I	Input Leakage Current	- 5~ 5	uA	4
I_{OZ}	Output Leakage Current	- 5~ 5	uA	4
I_{VREF}	V_{REF} Leakage Current	- 2~ 2	uA	3

Notes:
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300mV of each other at all times; and VREF must be not greater than 0.6 x VDDQ. When VDD and VDDQ and VDDL are less than 500 mV, Vref may be equal to or less than 300 mV.
4. Voltage on any input or I/O may not exceed voltage on VDDQ.

AC & DC Recommended Operating Conditions

Recommended DC Operating Conditions (SSTL-1.8)

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.7	1.8	1.9	V	1
VDDL	Supply Voltage for DLL	1.7	1.8	1.9	V	5
VDDQ	Supply Voltage for Output	1.7	1.8	1.9	V	1, 5
VREF	Input Reference Voltage	0.49 x VDDQ	0.50 x VDDQ	0.51 x VDDQ	V	2. 3
VTT	Termination Voltage	VREF - 0.04	VREF	VREF + 0.04	V	4

Notes:
1. There is no specific device VDD supply voltage requirement for SSTL_18 compliance. However under all conditions VDDQ must be less than or equal to VDD.
2. The value of VREF may be selected by the user to provide optimum noise margin in the system. Typically the value of VREF is expected to be about 0.5 x VDDQ of the transmitting device and VREF is expected to track variations in VDDQ.
3. Peak to peak ac noise on VREF may not exceed +/-2 % VREF(dc).
4. VTT of transmitting device must track VREF of receiving device.
5. VDDQ tracks with VDD, VDDL tracks with VDD. AC parameters are measured with VDD, VDDQ and VDDL tied together

Operating Temperature Condition

Symbol	Parameter	Rating[1,2,3]	Units
TOPER	Commercial Temperature	T_C = 0 to +85	°C
	Industrial Temperature,	T_C = -40 to +95	°C
	Automotive Temperature (A1)	T_A = -40 to +85	°C
	Automotive Temperature (A2)	T_C = -40 to +105	°C
		T_A = -40 to +105	°C

Notes:
1. T_C = Operating case temperature at center of package
2. T_A = Operating ambient temperature immediately above package center.
3. Both temperature specifications must be met.

Thermal Resistance:

Package	Substrate	Theta-ja (Airflow = 0m/s)	Theta-ja (Airflow = 1m/s)	Theta-ja (Airflow = 2m/s)	Theta-jc	Units
60-ball BGA	4-layer	55.1	34.7	32.2	8.0	C/W
84-ball BGA	4-layer	53.4	33.6	31.3	7.9	C/W

ODT DC Electrical Characteristics

PARAMETER/CONDITION	SYMBOL	MIN	NOM	MAX	UNITS	NOTES
R_{TT} effective impedance value for EMR(1)[A6,A2]=0,1; 75 Ω	R_{TT}1(eff)	60	75	90	Ω	1
R_{TT} effective impedance value for EMR(1)[A6,A2]=1,0; 150 Ω	R_{TT}2(eff)	120	150	180	Ω	1
R_{TT} effective impedance value for EMR(1)[A6,A2]=1,1; 50 Ω	R_{TT}3(eff)	40	50	60	Ω	1
Deviation of VM with respect to VDDQ/2	ΔVM	- 6		+ 6	%	1

Notes:
1. Test condition for R_{TT} measurements

Measurement Definition for R_{TT}(eff): Apply VIH (ac) and VIL (ac) to test pin separately, then measure current I(VIH (ac)) and I(VIL (ac)) respectively. VIH (ac), VIL (ac), and VDDQ values defined in SSTL_18

$$R_{TT}\ (eff) \quad \frac{V_{IH}\ (ac) - V_{IL}\ (ac)}{I(V_{IH}\ (ac)) - I(V_{IL}\ (ac))}$$

Measurement Definition for VM: Measure voltage (VM) at test pin (midpoint) with no load.

$\Delta VM = [(2 \times VM / VDDQ) - 1] \times 100\%$

Input DC logic level

Symbol	Parameter	Min.	Max.	Units	Notes
VIH(dc)	dc input logic HIGH	VREF + 0.125	VDDQ + 0.3	V	
VIL(dc)	dc input logic LOW	- 0.3	VREF - 0.125	V	

Input AC logic level

Symbol	Parameter	DDR2-400, DDR2-533		DDR2-667, DDR2-800		Units	Notes
		Min.	Max.	Min.	Max		
VIH (ac)	ac input logic HIGH	VREF + 0.250	VDDQ + Vpeak	VREF + 0.200	VDDQ + Vpeak	V	1
VIL (ac)	ac input logic LOW	VSSQ - Vpeak	VREF - 0.250	VSSQ - Vpeak	VREF - 0.200	V	1

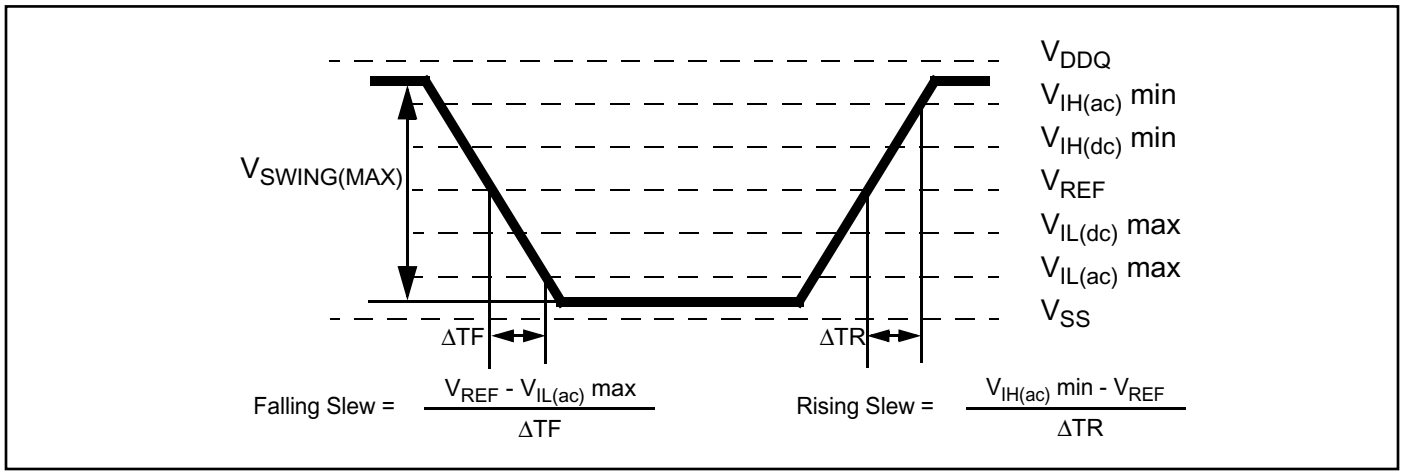
Notes:
1. Refer to Overshoot/undershoot specifications for Vpeak value: maximum peak amplitude allowed for overshoot and undershoot.

AC Input Test Conditions

Symbol	Condition	Value	Units	Notes
VREF	Input reference voltage	0.5 x VDDQ	V	1
VSWING(MAX)	Input signal maximum peak to peak swing	1.0	V	1
SLEW	Input signal minimum slew rate	1.0	V/ns	2, 3

Notes:
1. Input waveform timing is referenced to the input signal crossing through the VIH/IL(AC) level applied to the device under test.
2. The input signal minimum slew rate is to be maintained over the range from VREF to VIH(ac) min for rising edges and the range from VREF to VIL(ac) max for falling edges as shown in the below figure.
3. AC timings are referenced with input waveforms switching from VIL(ac) to VIH(ac) on the positive transitions and VIH(ac) to VIL(ac) on the negative transitions.

AC input test signal waveform

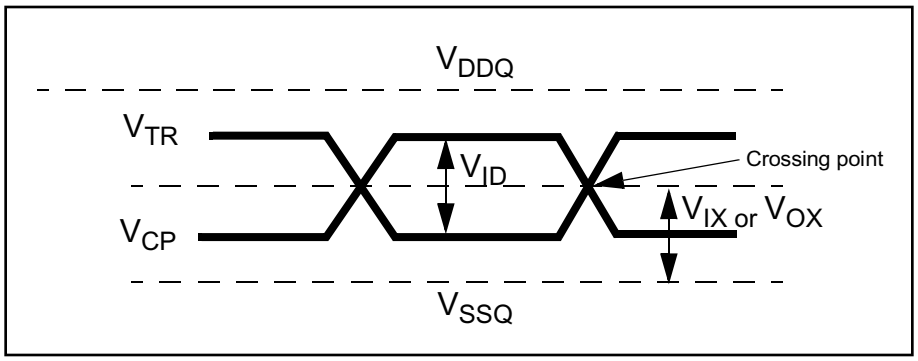


Differential input AC Logic Level

Symbol	Parameter	Min.	Max.	Units	Notes
VID (ac)	ac differential input voltage	0.5	VDDQ	V	1,3
VIX (ac)	ac differential crosspoint voltage	0.5 x VDDQ - 0.175	0.5 x VDDQ + 0.175	V	2

Notes:
1. VID(AC) specifies the input differential voltage |VTR -VCP | required for switching, where VTR is the true input signal (such as CK, DQS and VCP is the complementary input signal (such as $\overline{CK}$ or $\overline{DQS}$). The minimum value is equal to VIH(AC) - VIL(AC).
2. The typical value of VIX(AC) is expected to be about 0.5 x VDDQ of the transmitting device and VIX(AC) is expected to track variations in VDDQ. VIX(AC) indicates the voltage at which differential input signals must cross.
3. Refer to Overshoot/undershoot specifications for Vpeak value: maximum peak amplitude allowed for overshoot and undershoot.

Differential signal levels



Differential AC Output Parameters

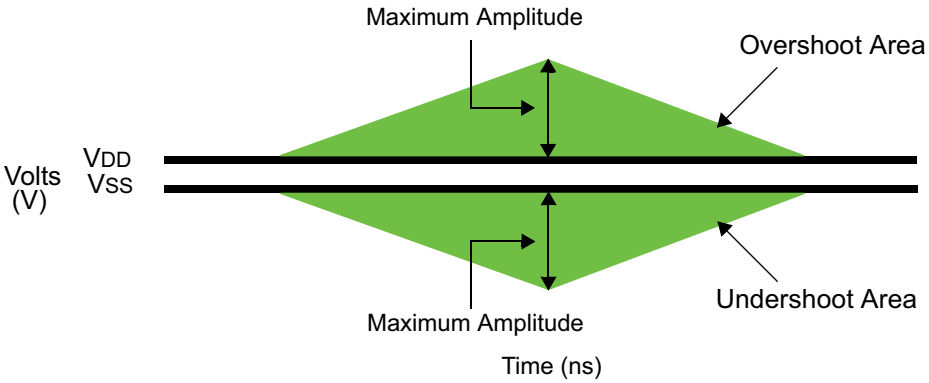
Symbol	Parameter	Min.	Max.	Units	Notes
VOX (ac)	ac differential crosspoint voltage	0.5 x VDDQ - 0.125	0.5 x VDDQ + 0.125	V	1

Note:
1. The typical value of VOX(AC) is expected to be about 0.5 x VDDQ of the transmitting device and VOX(AC) is expected to track variations in VDDQ. VOX(AC) indicates the voltage at which differential output signals must cross.

OVERSHOOT/UNDERSHOOT SPECIFICATION

AC overshoot/undershoot specification for Address and Control pins

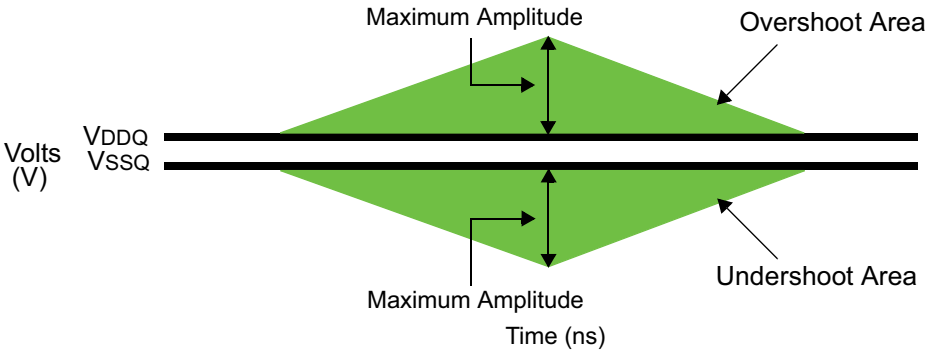
Parameter	Specification			
	DDR2-400	DDR2-533	DDR2-667	DDR2-800
Maximum peak amplitude allowed for overshoot area	0.5V	0.5V	0.5V	0.5V
Maximum peak amplitude allowed for undershoot area	0.5V	0.5V	0.5V	0.5V
Maximum overshoot area above VDD (see figure below)	1.33 V-ns	1.0 V-ns	0.8 V-ns	0.66 V-ns
Maximum undershoot area below VSS (see figure below)	1.33 V-ns	1.0 V-ns	0.8 V-ns	0.66 V-ns



AC overshoot and undershoot definition for address and control pins

AC overshoot/undershoot specification for Clock, Data, Strobe, and Mask pins: DQ, (U/L/R) DQS, (U/L/R) DQS, DM, CK, CK

Parameter	Specification			
	DDR2-400	DDR2-533	DDR2-667	DDR2-800
Maximum peak amplitude allowed for overshoot area	0.5V	0.5V	0.5V	0.5V
Maximum peak amplitude allowed for undershoot area	0.5V	0.5V	0.5V	0.5V
Maximum overshoot area above VDDQ (See Figure below)	0.38 V-ns	0.28 V-ns	0.23 V-ns	0.23 V-ns
Maximum undershoot area below VSSQ (See Figure below)	0.38 V-ns	0.28 V-ns	0.23 V-ns	0.23 V-ns



AC overshoot and undershoot definition for clock, data, strobe, and mask pins

Output Buffer Characteristics

Output AC Test Conditions

Symbol	Parameter	SSTL_18	Units	Notes
VOTR	Output Timing Measurement Reference Level	0.5 x VDDQ	V	1

Output DC Current Drive

Symbol	Parameter	SSTL_18	Units	Notes
IOH(dc)	Output Minimum Source DC Current	- 13.4	mA	1, 3, 4
IOL(dc)	Output Minimum Sink DC Current	13.4	mA	2, 3, 4

Notes:
1. VDDQ = 1.7 V; VOUT = 1420 mV. (VOUT - VDDQ)/IOH must be less than 21 Ω for values of VOUT between VDDQ and VDDQ - 280 mV.
2. VDDQ = 1.7 V; VOUT = 280 mV. VOUT/IOL must be less than 21 Ω for values of VOUT between 0 V and 280 mV.
3. The dc value of VREF applied to the receiving device is set to VTT
4. The values of IOH(dc) and IOL(dc) are based on the conditions given in Notes 1 and 2. They are used to test device drive current capability to ensure VIH min plus a noise margin and VIL max minus a noise margin are delivered to an SSTL_18 receiver. The actual current values are derived by shifting the desired driver operating point (see Section 3.3 of JESD8-15A) along a 21 Ω load line to define a convenient driver current for measurement.

OCD Default Characteristics

Description	Parameter	Min	Nom	Max	Unit	Notes
Output impedance		See full strength default driver characteristics			Ω	1
Output impedance step size for OCD calibration		0		1.5	Ω	6
Pull-up and pull-down mismatch		0		4	Ω	1,2,3
Output slew rate	Sout	1.5		5	V/ns	1,4,5,7,8,9

Notes:
1. Absolute Specifications (TOPER; VDD = +1.8V ±0.1V, VDDQ = +1.8V ±0.1V). DRAM I/O specifications for timing, voltage, and slew rate are no longer applicable if OCD is changed from default settings.
2. Impedance measurement condition for output source dc current: VDDQ = 1.7 V; VOUT = 1420 mV; (VOUTVDDQ)/IOH must be less than 23.4 Ω for values of VOUT between VDDQ and VDDQ - 280 mV. Impedance measurement condition for output sink dc current: VDDQ = 1.7 V; VOUT = 280 mV; VOUT/IOL must be less than 23.4 Ω for values of VOUT between 0 V and 280 mV.
3. Mismatch is absolute value between pull-up and pull-down, both are measured at same temperature and voltage.
4. Slew rate measured from VIL(ac) to VIH(ac).
5. The absolute value of the slew rate as measured from DC to DC is equal to or greater than the slew rate as measured from AC to AC. This is guaranteed by design and characterization.
6. This represents the step size when the OCD is near 18 Ω at nominal conditions across all process corners/variations and represents only the DRAM uncertainty. A 0 Ω value (no calibration) can only be achieved if the OCD impedance is 18 Ω +/-0.75 Ω under nominal conditions.
7. DRAM output slew rate specification applies to 400 MT/s, 533 MT/s & 667 MT/s speed bins.
8. Timing skew due to DRAM output slew rate mis-match between DQS / DQS and associated DQ's is included in tDQSQ and tQHS specification.
9. DDR2 SDRAM output slew rate test load is defined in General Note 3 of the AC Timing specification Table.

IDD Specifications & Test Conditions

Symbol	Conditions		-25D/-25E	-3D	-37C	-5B	Units
			DDR2-800D/800E	DDR2-667D	DDR2-533C	DDR2-400B	
IDD0	Operating one bank active-precharge current; tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD); CKE is HIGH, CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		100	90	85	80	mA
IDD1	Operating one bank active-read-precharge current; IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRC = tRC (IDD), tRAS = tRASmin(IDD), tRCD = tRCD(IDD); CKE is HIGH, CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W		115	105	95	85	mA
IDD2P	Precharge power-down current; All banks idle; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		25	23	20	20	mA
IDD2Q	Precharge quiet standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, CS is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		35	30	25	23	mA
IDD2N	Precharge standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, CS is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		35	30	28	25	mA
IDD3P	Active power-down current; All banks open; tCK = tCK(IDD); CKE is LOW;	Power Down Fast Exit	40	35	35	35	mA
	Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Power Down Slow Exit	30	28	28	28	
IDD3N	Active standby current; All banks open; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		80	70	65	60	mA
IDD4W	Operating burst write current; All banks open, Continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		200	180	170	160	mA

IDD Specifications & Test Conditions (continued)

Symbol	Conditions	-25D/-25E	-3D	-37C	-5B	Units
		DDR2-800D/800E	DDR2-667D	DDR2-533C	DDR2-400B	
IDD4R	Operating burst read current; All banks open, Continuous burst reads, IOUT = 0 mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	180	160	150	140	mA
IDD5B	Burst refresh current; tCK = tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH, CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	180	170	160	150	mA
IDD6	Self refresh current; CK and CK at 0 V; CKE ≤ 0.2 V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	10	10	10	10	mA
IDD7	Operating bank interleave read current; All bank interleaving reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = tRCD(IDD) - 1 x tCK(IDD); tCK = tCK(IDD), tRC = tRC(IDD), tRRD = tRRD(IDD), tRCD = 1 x tCK(IDD); CKE is HIGH, CS is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R	260	240	220	200	mA

Notes:
1. IDD specifications are tested after the device is properly initialized
2. Input slew rate is specified by AC Parametric Test Condition
3. IDD parameters are specified with ODT disabled.
4. Data bus consists of DQ, DM, DQS, $\overline{\text{DQS}}$, RDQS, $\overline{\text{RDQS}}$, LDQS, $\overline{\text{LDQS}}$, UDQS, and $\overline{\text{UDQS}}$. IDD values must be met with all combinations of EMR(1) bits 10 and 11.
5. For DDR2-667/800 testing, tCK in the Conditions should be interpreted as tCK(avg)
6. Definitions for IDD

LOW = Vin ≤ VILAC(max)
HIGH = Vin ≥ VIHAC(min)
STABLE = inputs stable at a HIGH or LOW level
FLOATING = inputs at VREF = VDDQ/2
SWITCHING = inputs changing between HIGH and LOW every other clock cycle (once per two clocks) for address and control signals, and inputs changing between HIGH and LOW every other data transfer (once per clock) for DQ signals not including masks or strobes.

7. The -25E, -37C, and-5B device specifications are shown for reference only.

IDD testing parameters

Speed	DDR2-800D	DDR2-667D	Units
Bin(CL-tRCD-tRP)	5-5-5	5-5-5	
CL(IDD)	5	5	tCK
tRCD(IDD)	12.5	15	ns
tRC(IDD)	55	55	ns
tRRD(IDD) x8	7.5	7.5	ns
tRRD(IDD) x16	10	10	ns
tCK(IDD)	2.5	3	ns
tRASmin(IDD)	40	40	ns
tRASmax(IDD)	70	70	µs
tRP(IDD)	12.5	15	ns
tRFC(IDD)	105	105	ns

Input/Output Capacitance:

Parameter	Symbol	DDR2-400 DDR2-553		DDR2-667		DDR2-800		Units
		Min.	Max.	Min.	Max	Min.	Max.	
Input capacitance, CK and $\overline{CK}$	CCK	1.0	2.0	1.0	2.0	1.0	2.0	pF
Input capacitance delta, CK and $\overline{CK}$	CDCK	–	0.25	–	0.25	–	0.25	pF
Input capacitance, all other input-only pins	CI	1.0	2.0	1.0	2.0	1.0	1.75	pF
Input capacitance delta, all other input-only pins	CDI	–	0.25	–	0.25	–	0.25	pF
Input/output capacitance, DQ, DM, DQS, $\overline{DQS}$	CIO	2.5	4.0	2.5	3.5	2.5	3.5	pF
Input/output capacitance delta, DQ, DM, DQS, $\overline{DQS}$	CDIO	–	0.5	–	0.5	–	0.5	pF

Electrical Characteristics & AC Timing Specifications

Refresh parameters (TOPER; VDDQ = 1.8 V +/- 0.1 V; VDD = 1.8 V +/- 0.1 V)

Parameter	Symbol			Units	Notes
Refresh to active/Refresh command time	tRFC		127.5	ns	1
Average periodic refresh interval	tREFI	-40°C ≤ Tc < 0°C	7.8	µs	1,2
		0°C ≤ Tc ≤ 85°C	7.8	µs	1
		85°C < Tc ≤ 95°C	3.9	µs	1,2
		95°C < Tc ≤ 105°C	3.9	µs	1,2,3

Notes:
1. If refresh timing is violated, data corruption may occur and the data must be re-written with valid data before a valid READ can be executed.
2. Specified for Industrial and Automotive grade only; not applicable for Commercial grade. TOPER may not be violated.
3. Specified for Automotive grade (A2) only; not applicable for any other grade. TOPER may not be violated.

Key Timing Parameters by Speed Grade

	-25D	-25E	-3D	-37C	-5B
Speed bin (JEDEC)	DDR2-800D	DDR2-800E	DDR2-667D	DDR2-533C	DDR2-400B
CL-tRCD-tRP	5-5-5	6-6-6	5-5-5	4-4-4	3-3-3
tRCD	12.5	15	15	15	15
tRP	12.5	15	15	15	15
tRC	55	55	55	55	55
tRAS	40	40	40	40	40
tCK(avg)@CL=3	5	5	5	5	5
tCK(avg)@CL=4	3.75	3.75	3.75	3.75	5
tCK(avg)@CL=5	2.5	3	3	–	–
tCK(avg)@CL=6	2.5	2.5	–	–	–

Note:
Each of the -25D and -3D speed options is individually backward compatible with all the timing specifications for slower options (ie. -25D complies with specifications for -25D, -25E, -3D, -37C, -5B). -25E, -37C, and -5B shown for reference only.

Timing Parameters by Speed Grade (DDR2-400 and DDR2-533)

(For information related to the entries in this table, refer to both the Guidelines and the Specific Notes following this Table.)

Parameter	Symbol	DDR2-400		DDR2-553		Units	Notes
		Min.	Max.	Min.	Max		
Clock cycle time, CL=x	tCK	5	8	3.75	8	ns	15
CK HIGH pulse width	tCH	0.45	0.55	0.45	0.55	tCK	
CK LOW pulse width	tCL	0.45	0.55	0.45	0.55	tCK	
DQS latching rising transitions to associated clock edges	tDQSS	- 0.25	0.25	- 0.25	0.25	tCK	
DQS falling edge to CK setup time	tDSS	0.2	–	0.2	–	tCK	
DQS falling edge hold time from CK	tDSH	0.2	–	0.2	–	tCK	
DQS input HIGH pulse width	tDQSH	0.35	–	0.35	–	tCK	
DQS input LOW pulse width	tDQSL	0.35	–	0.35	–	tCK	
Write preamble	tWPRE	0.35	–	0.35	–	tCK	
Write postamble	tWPST	0.4	0.6	0.4	0.6	tCK	10
Address and control input setup time	tIS(base)	350	–	250	–	ps	5, 7, 9, 22
Address and control input hold time	tIH(base)	475	–	375	–	ps	5, 7, 9, 23
Control & Address input pulse width for each input	tIPW	0.6	–	0.6	–	tCK	
DQ and DM input setup time (differential strobe)	tDS(base)	150	–	100	–	ps	6, 7, 8, 20, 28
DQ and DM input hold time (differential strobe)	tDH(base)	275	–	225	–	ps	6, 7, 8, 21, 28
DQ and DM input setup time (single-ended strobe)	tDS1(base)	25	–	- 25	–	ps	6, 7, 8, 25
DQ and DM input hold time (single-ended strobe)	tDH1(base)	25	–	- 25	–	ps	6, 7, 8, 26
DQ and DM input pulse width for each input	tDIPW	0.35	–	0.35	–	tCK	
DQ output access time from CK/$\overline{CK}$	tAC	- 600	+ 600	- 500	+ 500	ps	
DQS output access time from CK/ $\overline{CK}$	tDQSCK	- 500	+ 500	- 450	+ 450	ps	
Data-out high-impedance time from CK/ $\overline{CK}$	tHZ	–	tAC max	–	tAC max	ps	18
DQS($\overline{DQS}$) low-impedance time from CK/ $\overline{CK}$	tLZ(DQS)	tAC min	tAC max	tAC min	tAC max	ps	18
DQ low-impedance time from CK/ $\overline{CK}$	tLZ(DQ)	2 x tAC min	tAC max	2 x tAC min	tAC max	ps	18
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	–	350	–	300	ps	13
CK half pulse width	tHP	min (tCL, tCH)	–	min (tCL, tCH)	–	ps	11,12
DQ hold skew factor	tQHS	–	450	–	400	ps	12
DQ/DQS output hold time from DQS	tQH	tHP - tQHS	–	tHP - tQHS	–	ps	
Read preamble	tRPRE	0.9	1.1	0.9	1.1	tCK	19
Read postamble	tRPST	0.4	0.6	0.4	0.6	tCK	19

Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) cont'd

(For information related to the entries in this table, refer to both the Guidelines and the Specific Notes following this Table.)

Parameter	Symbol		DDR2-400		DDR2-533		Units	Notes
			Min.	Max.	Min.	Max.		
Active to active command period	tRRD	x8	7.5	–	7.5	–	ns	4
		x16	10	–	10	–		
Four Activate Window	tFAW	x8	37.5	–	37.5	–	ns	
		x16	50	–	50	–	ns	
$\overline{CAS}$ to $\overline{CAS}$ command delay	tCCD		2	–	2	–	tCK	
Write recovery time	tWR		15	–	15	–	ns	
Auto precharge write recovery + precharge time	tDAL		WR + tRP	–	WR + tRP	–	tCK	14
Internal write to read command delay	tWTR		10	–	7.5	–	ns	24
Internal read to precharge command delay	tRTP		7.5	–	7.5	–	ns	3
CKE minimum pulse width (HIGH and LOW pulse width)	tCKE		3	–	3	–	tCK	27
Exit self refresh to a non-read command	tXSNR		tRFC + 10	–	tRFC + 10	–	ns	
Exit self refresh to a read command	tXSRD		200	–	200	–	tCK	
Exit precharge power down to any non-read command	tXP		2	–	2	–	tCK	
Exit active power down to read command	tXARD		2	–	2	–	tCK	1
Exit active power down to read command (slow exit, lower power)	tXARDS		6 - AL	–	6 - AL	–	tCK	1,2
ODT turn-on delay	tAOND		2	2	2	2	tCK	16
ODT turn-on	tAON		tAC(min)	tAC(max)+1	tAC(min)	tAC (max)+1	ns	16
ODT turn-on (Power-Down mode)	tAONPD		tAC(min)+2	2 x tCK + tAC(max)+1	tAC(min) + 2	2 x tCK + tAC(max)+1	ns	
ODT turn-off delay	tAOFD		2.5	2.5	2.5	2.5	tCK	17, 44
ODT turn-off	tAOF		tAC(min)	tAC(max) + 0.6	tAC(min)	tAC(max) + 0.6	ns	17, 44
ODT turn-off (Power-Down mode)	tAOFPD		tAC(min)+2	2.5 x tCK + tAC(max)+1	tAC(min)+2	2.5 x tCK+ tAC(max)+1	ns	
ODT to power down entry latency	tANPD		3	–	3	–	tCK	
ODT power down exit latency	tAXPD		8	–	8	–	tCK	
Mode register set command cycle time	tMRD		2	–	2	–	tCK	
MRS command to ODT update delay	tMOD		0	12	0	12	ns	
OCD drive mode output delay	tOIT		0	12	0	12	ns	
Minimum time clocks remains ON after CKE asynchronously drops LOW	tDelay		tIS+tCK+tIH	–	tIS+tCK+tIH	–	ns	15

Timing Parameters by Speed Grade (DDR2-667 and DDR2-800)

(For information related to the entries in this table, refer to both the Guidelines and the Specific Notes following this Table.)

Parameter	Symbol	DDR2-667		DDR2-800		Units	Notes
		Min.	Max.	Min.	Max		
Average clock period	tCK(avg)	3	8	2.5	8	ns	35,36
Average clock HIGH pulse width	tCH(avg)	0.45	0.55	0.45	0.55	tCK(avg)	35,36
Average clock LOW pulse width	tCL(avg)	0.45	0.55	0.45	0.55	tCK(avg)	35,36
DQS latching rising transitions to associated clock edges	tDQSS	- 0.25	0.25	- 0.25	0.25	tCK(avg)	30
DQS falling edge to CK setup time	tDSS	0.2	–	0.2	–	tCK(avg)	30
DQS falling edge hold time from CK	tDSH	0.2	–	0.2	–	tCK(avg)	30
DQS input HIGH pulse width	tDQSH	0.35	–	0.35	–	tCK(avg)	
DQS input LOW pulse width	tDQSL	0.35	–	0.35	–	tCK(avg)	
Write preamble	tWPRE	0.35	–	0.35	–	tCK(avg)	
Write postamble	tWPST	0.4	0.6	0.4	0.6	tCK(avg)	10
Address and control input setup time	tIS(base)	200	–	175	–	ps	5, 7, 9, 22, 29
Address and control input hold time	tIH(base)	275	–	250	–	ps	5, 7, 9, 23, 29
Control & Address input pulse width for each input	tIPW	0.6	–	0.6	–	tCK(avg)	
DQ and DM input setup time	tDS(base)	50	–	50	–	ps	6, 7, 8, 20, 28, 31
DQ and DM input hold time	tDH(base)	175	–	125	–	ps	6, 7, 8, 21, 28, 31
DQ and DM input pulse width for each input	tDIPW	0.35	–	0.35	–	tCK(avg)	
DQ output access time from CK/CK	tAC	- 450	450	- 400	400	ps	40
DQS output access time from CK/CK	tDQSCK	- 400	400	- 350	350	ps	40
Data-out high-impedance time from CK/CK	tHZ	–	tAC,max	–	tAC, max	ps	18,40
DQS/DQS low-impedance time from CK/CK	tLZ(DQS)	tAC,min	tAC,max	tAC,min	tAC, max	ps	18,40
DQ low-impedance time from CK/CK	tLZ(DQ)	2 x tAC,min	tAC,max	2 x tAC,min	tAC, max	ps	18,40
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	–	240	–	200	ps	13
CK half pulse width	tHP	Min(tCH(abs), tCL(abs))	–	Min(tCH(abs), tCL(abs))	–	ps	37
DQ hold skew factor	tQHS	–	340	–	300	ps	38
DQ/DQS output hold time from DQS	tQH	tHP - tQHS	–	tHP - tQHS	–	ps	39
Read preamble	tRPRE	0.9	1.1	0.9	1.1	tCK(avg)	19,41
Read postamble	tRPST	0.4	0.6	0.4	0.6	tCK(avg)	19,42

Timing parameters by speed grade (DDR2-667 and DDR2-800) cont'd

(For information related to the entries in this table, refer to both the Guidelines and the Specific Notes following this Table.)

Parameter	Symbol		DDR2-667		DDR2-800		Units	Notes
			Min.	Max	Min.	Max.		
Activate to activate command period	tRRD	x8	7.5	–	7.5	–	ns	4,32
		x16	10	–	10	–		
$\overline{CAS}$ to $\overline{CAS}$ command delay	tCCD		2	–	2	–	nCK	
Write recovery time	tWR		15	–	15	–	ns	32
Auto precharge write recovery + precharge time	tDAL		WR + tnRP	–	WR + tnRP	–	nCK	33
Internal write to read command delay	tWTR		7.5	–	7.5	–	ns	24, 32
Internal read to precharge command delay	tRTP		7.5	–	7.5	–	ns	3, 32
CKE minimum pulse width (HIGH and LOW pulse width)	tCKE		3	–	3	–	nCK	27
Exit self refresh to a non-read command	tXSNR		tRFC + 10	–	tRFC + 10	–	ns	32
Exit self refresh to a read command	tXSRD		200	–	200	–	nCK	
Exit precharge power down to any command	tXP		2	–	2	–	nCK	
Exit active power down to read command	tXARD		2	–	2	–	nCK	1
Exit active power down to read command (slow exit, lower power)	tXARDS		7 - AL	–	8 - AL	–	nCK	1, 2
ODT turn-on delay	tAOND		2	2	2	2	nCK	16
ODT turn-on	tAON		tAC, min	tAC,max + 0.7	tAC,min	tAC,max + 0.7	ns	6, 16, 40
ODT turn-on (Power-Down mode)	tAONPD		tAC, min + 2	2 x tCK(avg) + tAC,max + 1	tAC,min + 2	2 x tCK(avg) + tAC,max + 1	ns	
ODT turn-off delay	tAOFD		2.5	2.5	2.5	2.5	nCK	17, 45
ODT turn-off	tAOF		tAC, min	tAC,max + 0.6	tAC,min	tAC,max + 0.6	ns	17, 43, 45
ODT turn-off (Power-Down mode)	tAOFPD		tAC, min+2	2.5 x tCK(avg) + tAC,max + 1	tAC,min+2	2.5 x tCK(avg) + tAC,max + 1	ns	
ODT to power down entry latency	tANPD		3	–	3	–	nCK	
ODT Power Down Exit Latency	tAXPD		8	–	8	–	nCK	
Mode register set command cycle time	tMRD		2	–	2	–	nCK	
OCD drive mode output delay	tOIT		0	12	0	12	ns	32
Minimum time clocks remains ON after CKE asynchronously drops LOW	tDelay		tIS + tCK(avg) + tIH	–	tIS + tCK(avg) + tIH	–	ns	15

Guidelines for AC Parameters

1. DDR2 SDRAM AC Timing Reference Load

Figure "AC Timing Reference Load" represents the timing reference load used in defining the relevant timing parameters of the part. It is not intended to be either a precise representation of the typical system environment or a depiction of the actual load presented by a production tester. System designers will use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions (generally a coaxial transmission line terminated at the tester electronics).

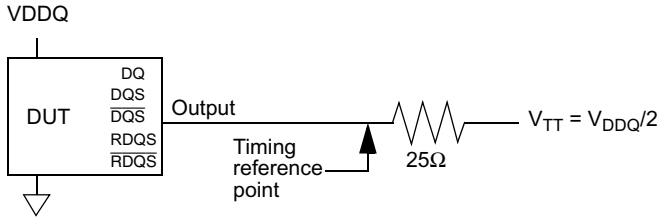


Figure - AC Timing Reference Load

The output timing reference voltage level for single ended signals is the crosspoint with VTT. The output timing reference voltage level for differential signals is the crosspoint of the true (e.g. DQS) and the complement (e.g. DQS) signal.

2. Slew Rate Measurement Levels

a) Output slew rate for falling and rising edges is measured between VTT - 250 mV and VTT + 250 mV for single ended signals. For differential signals (e.g. DQS - $\overline{DQS}$) output slew rate is measured between DQS - $\overline{DQS}$ = - 500 mV and DQS - $\overline{DQS}$ = + 500 mV. Output slew rate is guaranteed by design, but is not necessarily tested on each device.

b) Input slew rate for single ended signals is measured from Vref(dc) to VIH(ac),min for rising edges and from Vref(dc) to VIL(ac),max for falling edges.

For differential signals (e.g. CK - $\overline{CK}$) slew rate for rising edges is measured from CK - $\overline{CK}$ = - 250 mV to CK - $\overline{CK}$ = + 500 mV (+ 250 mV to - 500 mV for falling edges).

c) VID is the magnitude of the difference between the input voltage on CK and the input voltage on CK, or between DQS and $\overline{DQS}$ for differential strobe.

3. DDR2 SDRAM output slew rate test load

Output slew rate is characterized under the test conditions as shown in Figure "Slew Rate Test Load".

4. Differential data strobe

DDR2 SDRAM pin timings are specified for either single ended mode or differential mode depending on the setting of the EMRS “Enable DQS” mode bit; timing advantages of differential mode are realized in system design. The method by which the DDR2 SDRAM pin timings are measured is mode dependent. In single ended mode, timing relationships are measured relative to the rising or falling edges of DQS crossing at VREF. In differential mode, these timing

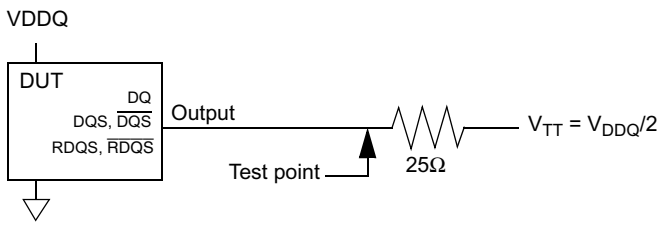
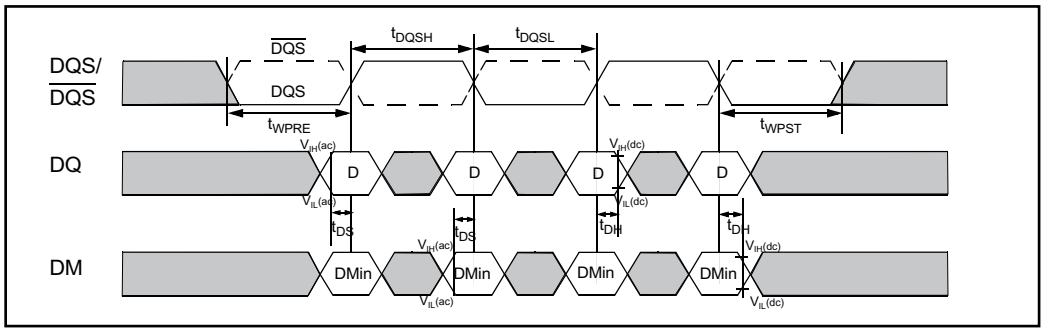
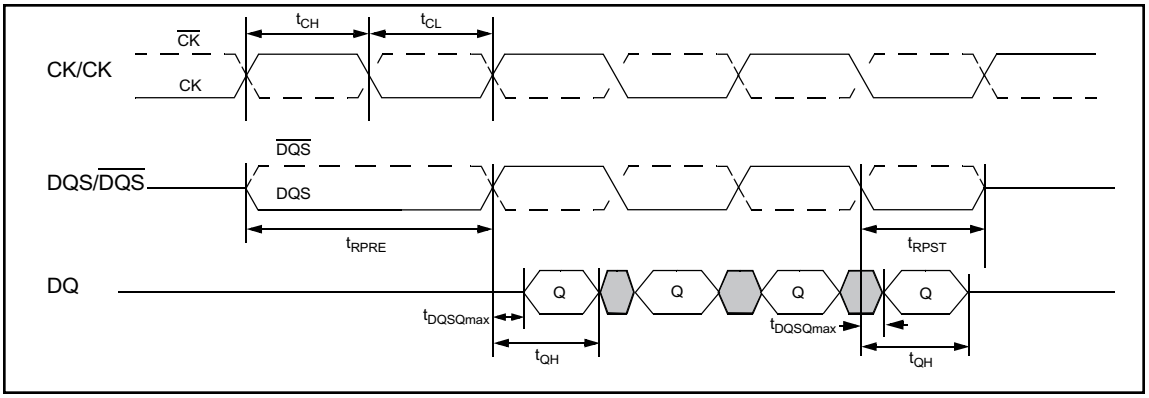


Figure - Slew Rate Test Load

relationships are measured relative to the crosspoint of DQS and its complement, $\overline{DQS}$. This distinction in timing methods is guaranteed by design and characterization. Note that when differential data strobe mode is disabled via the EMRS, the complementary pin, $\overline{DQS}$, must be tied externally to VSS through a 20 Ω to 10 kΩ resistor to insure proper operation.



Data Input (Write) Timing



Data Output (Read) Timing

5. AC timings are for linear signal transitions. See Specific Notes on derating for other signal transitions.

6. All voltages are referenced to VSS.

7. These parameters guarantee device behavior, but they are not necessarily tested on each device They may be guaranteed by device design or tester correlation.

8. Tests for AC timing, IDD, and electrical (AC and DC) characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.

Specific Notes for Dedicated AC Parameters

1. User can choose which active power down exit timing to use via Mode Register Set [A12]. tXARD is expected to be used for fast active power down exit timing. tXARDS is expected to be used for slow active power down exit timing.

2. AL = Additive Latency.

3. This is a minimum requirement. Minimum read to precharge timing is AL + BL / 2 provided that the tRTP and tRAS(min) have been satisfied.

4. A minimum of two clocks (2 x tCK or 2 x nCK) is required irrespective of operating frequency.

5. Timings are specified with command/address input slew rate of 1.0 V/ns. See Specific Notes on derating for other slew rate values.

6. Timings are specified with DQs, DM, and DQS's (DQS/RDQS in single ended mode) input slew rate of 1.0V/ns. See Specific Notes on derating for other slew rate values.

7. Timings are specified with CK/CK differential slew rate of 2.0 V/ns. Timings are guaranteed for DQS signals with a differential slew rate of 2.0 V/ns in differential strobe mode and a slew rate of 1 V/ns in single ended mode. See Specific Notes on derating for other slew rate values.

8. Data setup and hold time derating (t_{DS}, t_{DH}).

ΔtDS, ΔtDH derating values for DDR2-400, DDR2-553 (All units in 'ps'; the note applies to the entire table)																			
		DQS, $\overline{DQS}$ Differential Slew Rate																	
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns		0.8 V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew rate V/ns	2.0	125	45	125	45	125	45	-	-	-	-	-	-	-	-	-	-	-	-
	1.5	83	21	83	21	83	21	95	33	-	-	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	12	12	24	24	-	-	-	-	-	-	-	-
	0.9	-	-	-11	-14	-11	-14	1	-2	13	10	25	22	-	-	-	-	-	-
	0.8	-	-	-	-	-25	-31	-13	-19	-1	-7	11	5	23	17	-	-	-	-
	0.7	-	-	-	-	-	-	-31	-42	-19	-30	-7	-18	5	-6	17	6	-	-
	0.6	-	-	-	-	-	-	-	-	-43	-59	-31	-47	-19	-35	-7	-23	5	-11
	0.5	-	-	-	-	-	-	-	-	-	-	-74	-89	-62	-77	-50	-65	-38	-53
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-127	-140	-115	-128	-103	-116

DDR2-400/533 tDS/tDH derating with differential data strobe

ΔtDS, ΔtDH derating values for DDR2-667, DDR2-800 (All units in 'ps'; the note applies to the entire table)																			
		DQS, $\overline{DQS}$ Differential Slew Rate																	
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns		0.8 V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew rate V/ns	2.0	100	45	100	45	100	45	-	-	-	-	-	-	-	-	-	-	-	-
	1.5	67	21	67	21	67	21	79	33	-	-	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	12	12	24	24	-	-	-	-	-	-	-	-
	0.9	-	-	-5	-14	-5	-14	7	-2	19	10	31	22	-	-	-	-	-	-
	0.8	-	-	-	-	-13	-31	-1	-19	11	-7	23	5	35	17	-	-	-	-
	0.7	-	-	-	-	-	-	-10	-42	2	-30	14	-18	26	-6	38	6	-	-
	0.6	-	-	-	-	-	-	-	-	-10	-59	2	-47	14	-35	26	-23	38	-11
	0.5	-	-	-	-	-	-	-	-	-	-	-24	-89	-12	-77	0	-65	12	-53
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-52	-140	-40	-128	-28	-116

DDR2-667/800 tDS/tDH derating with differential data strobe

ΔtDS1, ΔtDH1 derating values for DDR2-400, DDR2-533 (All units in 'ps'; the note applies to the entire table)																			
		DQS, Single-ended Slew Rate																	
		2.0 V/ns		1.5 V/ns		1.0 V/ns		0.9 V/ns		0.8 V/ns		0.7 V/ns		0.6 V/ns		0.5 V/ns		0.4 V/ns	
		ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1
DQ Slew rate V/ns	2.0	188	167	145	125	63	-	-	-	-	-	-	-	-	-	-	-	-	-
	1.5	146	167	125	125	83	42	81	43	-	-	-	-	-	-	-	-	-	-
	1.0	63	125	42	83	0	0	-2	1	-7	-13	-	-	-	-	-	-	-	-
	0.9	-	-	31	69	-11	-14	-13	-13	-18	-27	-29	-45	-	-	-	-	-	-
	0.8	-	-	-	-	-25	-31	-27	-30	-32	-44	-43	-62	-60	-86	-	-	-	-
	0.7	-	-	-	-	-	-	-45	-53	-50	-67	-61	-85	-78	-109	-108	-152	-	-
	0.6	-	-	-	-	-	-	-	-	-74	-96	-85	-114	-102	-138	-132	-181	-183	-246
	0.5	-	-	-	-	-	-	-	-	-	-	-128	-156	-145	-180	-175	-223	-226	-288
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-210	-243	-240	-286	-291	-351

DDR2-400/533 tDS1/tDH1 derating with single-ended data strobe

For all input signals the total tDS (setup time) and tDH (hold time) required is calculated by adding the data sheet tDS(base) and tDH(base) value to the ΔtDS and ΔtDH derating value respectively. Example: tDS (total setup time) = tDS(base) + ΔtDS.

Setup (tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of Vih(ac)min. Setup (tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of Vil(ac)max. If the actual signal is always earlier than the nominal slew rate line between shaded 'VREF(dc) to ac region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded 'VREF(dc) to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value.

Hold (tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of Vil(dc)max and the first crossing of VREF(dc). Hold (tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of Vih(dc)min and the first crossing of VREF(dc). If the actual signal is always later than the nominal slew rate line between shaded 'dc level to VREF(dc) region', use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to VREF(dc) region', the slew rate of a tangent line to the actual signal from the dc level to VREF(dc) level is used for derating value.

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached VIH/IL(ac) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach VIH/IL(ac).

For slew rates in between the values listed in the "Data Setup and Hold Time Derating" tables, the derating values may obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.

9. Input Setup and Hold Time Derating (tIS, tIH)

tIS, tIH Derating Values for DDR2-400, DDR2-533									
CK, /CK Differential Slew Rate									
		2.0 V/ns		1.5 V/ns		1.0 V/ns		Units	Notes
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH		
Command/ Address Slew rate (V/ns)	4.0	187	94	217	124	247	154	ps	1
	3.5	179	89	209	119	239	149	ps	1
	3	167	83	197	113	227	143	ps	1
	2.5	150	75	180	105	210	135	ps	1
	2.0	125	45	155	75	185	105	ps	1
	1.5	83	21	113	51	143	81	ps	1
	1.0	0	0	30	30	60	60	ps	1
	0.9	-11	-14	19	16	49	46	ps	1
	0.8	-25	-31	5	-1	35	29	ps	1
	0.7	-43	-54	-13	-24	17	6	ps	1
	0.6	-67	-83	-37	-53	-7	-23	ps	1
	0.5	-110	-125	-80	-95	-50	-65	ps	1
	0.4	-175	-188	-145	-158	-115	-128	ps	1
	0.3	-285	-292	-255	-262	-225	-232	ps	1
	0.25	-350	-375	-320	-345	-290	-315	ps	1
	0.2	-525	-500	-495	-470	-465	-440	ps	1
	0.15	-800	-708	-770	-678	-740	-648	ps	1
	0.1	-1450	-1125	-1420	-1095	-1390	-1065	ps	1

ΔtIS and ΔtIH Derating Values for DDR2-667, DDR2-800									
CK,CK Differential Slew Rate									
		2.0 V/ns		1.5 V/ns		1.0 V/ns		Units	Notes
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH		
Command/ Address Slew rate (V/ns)	4	150	94	180	124	210	154	ps	1
	3.5	143	89	173	119	203	149	ps	1
	3	133	83	163	113	193	143	ps	1
	2.5	120	75	150	105	180	135	ps	1
	2	100	45	130	75	160	105	ps	1
	1.5	67	21	97	51	127	81	ps	1
	1	0	0	30	30	60	60	ps	1
	0.9	-5	-14	25	16	55	46	ps	1
	0.8	-13	-31	17	-1	47	29	ps	1
	0.7	-22	-54	8	-24	38	6	ps	1
	0.6	-34	-83	-4	-53	26	-23	ps	1
	0.5	-60	-125	-30	-95	0	-65	ps	1
	0.4	-100	-188	-70	-158	-40	-128	ps	1
	0.3	-168	-292	-138	-262	-108	-232	ps	1
	0.25	-200	-375	-170	-345	-140	-315	ps	1
	0.2	-325	-500	-295	-470	-265	-440	ps	1
	0.15	-517	-708	-487	-678	-457	-648	ps	1
	0.1	-1000	-1125	-970	-1095	-940	-1065	ps	1

For all input signals the total tIS (setup time) and tIH (hold time) required is calculated by adding the data sheet tIS(base) and tIH(base) value to the ΔtIS and ΔtIH derating value respectively. Example: tIS (total setup time) = tIS(base) + ΔtIS

Setup (tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of Vih(ac)min. Setup (tIS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of Vil(ac)max. If the actual signal is always earlier than the nominal slew rate line between shaded 'VREF(dc) to ac region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded 'VREF(dc) to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value.

Hold (tIH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of Vil(dc)max and the first crossing of VREF(dc). Hold (tIH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of Vih(dc)min and the first crossing of VREF(dc). If the actual signal is always later than the nominal slew rate line between shaded 'dc to VREF(dc) region', use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to VREF(dc) region', the slew rate of a tangent line to the actual signal from the dc level to VREF(dc) level is used for derating value.

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached VIH/IL(ac) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach VIH/IL(ac).

For slew rates in between the values listed in the "Input Setup and Hold Time Derating" tables, the derating values may obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.

10. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.

11. MIN (tCL, tCH) refers to the smaller of the actual clock LOW time and the actual clock HIGH time as provided to the device (i.e. this value can be greater than the minimum specification limits for tCL and tCH). For example, tCL and tCH are = 50% of the period, less the half period jitter (tJIT(HP)) of the clock source, and less the half period jitter due to crosstalk (tJIT(crosstalk)) into the clock traces.

12. tQH = tHP – tQHS, where:

tHP = minimum half clock period for any given cycle and is defined by clock HIGH or clock LOW (tCH, tCL). tQHS accounts for:

1) The pulse duration distortion of on-chip clock circuits; and

2) The worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are, separately, due to data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.

13. tDQSQ: Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers as well as output slew rate mismatch between DQS / DQS and associated DQ in any given cycle.

14. tDAL = WR + RU{ tRP[ns] / tCK[ns] }, where RU stands for round up.

WR refers to the tWR parameter stored in the MRS. For tRP, if the result of the division is not already an integer, round up to the next highest integer. tCK refers to the application clock period.

Example: For DDR533 at tCK = 3.75ns with WR programmed to 4 clocks.

tDAL = 4 + (15 ns / 3.75 ns) clocks = 4 + (4) clocks = 8 clocks.

15. The clock frequency is allowed to change during self–refresh mode or precharge power-down mode. In case of clock frequency change during precharge power-down, a specific procedure is required as described in section 3.13.

16. ODT turn on time min is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measured from tAOND, which is interpreted differently per speed bin. For DDR2-400/533, tAOND is 10 ns (= 2 x 5 ns) after the clock edge that registered a first ODT HIGH if tCK = 5 ns. For DDR2-667/800, tAOND is 2 clock cycles after the clock edge that registered a first ODT HIGH counting the actual input clock edges.

17. ODT turn off time min is when the device starts to turn off ODT resistance. ODT turn off time max is when the bus is in high impedance. Both are measured from tAOFD, which is interpreted differently per speed bin. For DDR2-400/533, tAOFD is 12.5 ns (= 2.5 x 5 ns) after the clock edge that registered a first ODT LOW if tCK = 5 ns. For DDR2-667/800, if tCK(avg) = 3 ns is assumed, tAOFD is 1.5 ns (= 0.5 x 3 ns) after the second trailing clock edge counting from the clock edge that registered a first ODT LOW and by counting the actual input clock edges.

18. tHZ and tLZ transitions occur in the same access time as valid data transitions. These parameters are referenced to a specific voltage level which specifies when the device output is no longer driving (tHZ), or begins driving (tLZ) . One method to calculate the point when device is no longer driving (tHZ), or begins driving (tLZ) is by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. tLZ(DQ) refers to tLZ of the DQ's and tLZ(DQS) refers to tLZ of the (U/L/R)DQS and (U/L/R)DQS each treated as single-ended signal.

19. tRPST end point and tRPRE begin point are not referenced to a specific voltage level but specify when the device output is no longer driving (tRPST), or begins driving (tRPRE). One method to calculate these points when the device is no longer driving (tRPST), or begins driving (tRPRE) is by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.

20. Input waveform timing tDS with differential data strobe enabled is referenced from the input signal crossing at the VIH(ac) level to the differential data strobe crosspoint for a rising signal, and from the input signal crossing at the VIL(ac) level to the differential data strobe crosspoint for a falling signal applied to the device under test. DQS, DQS signals must be monotonic between Vil(dc)max and Vih(dc)min.

21. Input waveform timing tDH with differential data strobe enabled is referenced from the differential data strobe crosspoint to the input signal crossing at the VIH(dc) level for a falling signal and from the differential data strobe crosspoint to the input signal crossing at the VIL(dc) level for a rising signal applied to the device under test. DQS, DQS signals must be monotonic between Vil(dc)max and Vih(dc)min.

22. Input waveform timing is referenced from the input signal crossing at the VIH(ac) level for a rising signal and VIL(ac) for a falling signal applied to the device under test.

23. Input waveform timing is referenced from the input signal crossing at the VIL(dc) level for a rising signal and VIH(dc) for a falling signal applied to the device under test.

24. tWTR is at lease two clocks (2 x tCK or 2 x nCK) independent of operation frequency.

25. Input waveform timing with single-ended data strobe enabled, is referenced from the input signal crossing at the VIH(ac) level to the single-ended data strobe crossing VIH/L(dc) at the start of its transition for a rising signal, and from the input signal crossing at the VIL(ac) level to the single-ended data strobe crossing VIH/L(dc) at the start of its transition for a falling signal applied to the device under test. The DQS signal must be monotonic between Vil(dc)max and Vih(dc)min.

26. Input waveform timing with single-ended data strobe enabled, is referenced from the input signal crossing at the VIH(dc) level to the single-ended data strobe crossing VIH/L(ac) at the end of its transition for a rising signal, and from the input signal crossing at the VIL(dc) level to the single-ended data strobe crossing VIH/L(ac) at the end of its transition for a falling signal applied to the device under test. The DQS signal must be monotonic between Vil(dc)max and Vih(dc)min.

27. tCKEmin of 3 clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the 3 clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of tIS + 2 x tCK + tIH.

28. If tDS or tDH is violated, data corruption may occur and the data must be re-written with valid data before a valid READ can be executed.

29. These parameters are measured from a command/address signal (CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, ODT, BA0, A0, A1, etc.) transition edge to its respective clock signal (CK/$\overline{CK}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.

30. These parameters are measured from a data strobe signal ((L/U/R)DQS/$\overline{DQS}$) crossing to its respective clock signal (CK/$\overline{CK}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.

31. These parameters are measured from a data signal ((L/U)DM, (L/U)DQ0, (L/U)DQ1, etc.) transition edge to its respective data strobe signal ((L/U/R)DQS/ $\overline{DQS}$) crossing.

32. For these parameters, the DDR2 SDRAM device is characterized and verified to support tnPARAM = RU{tPARAM / tCK(avg)}, which is in clock cycles, assuming all input clock jitter specifications are satisfied.

For example, the device will support tnRP = RU{tRP / tCK(avg)}, which is in clock cycles, if all input clock jitter specifications are met. This means: For DDR2-667 5-5-5, of which tRP = 15ns, the device will support tnRP = RU{tRP / tCK(avg)} = 5, i.e. as long as the input clock jitter specifications are met, Precharge command at Tm and Active command at Tm+5 is valid even if (Tm+5 - Tm) is less than 15ns due to input clock jitter.

33. tDAL [nCK] = WR [nCK] + tnRP [nCK] = WR + RU {tRP [ps] / tCK(avg) [ps] }, where WR is the value programmed in the mode register set.

34. New units, 'tCK(avg)' and 'nCK', are introduced in DDR2-667 and DDR2-800.

Unit 'tCK(avg)' represents the actual tCK(avg) of the input clock under operation.

Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges.

Note that in DDR2-400 and DDR2-533, 'tCK' is used for both concepts.

ex) tXP = 2 [nCK] means; if Power Down exit is registered at Tm, an Active command may be registered at Tm+2, even if (Tm+2 - Tm) is 2 x tCK(avg) + tERR(2per),min.

35. Input clock jitter spec parameter. These parameters and the ones in the table below are referred to as 'input clock jitter spec parameters' and these parameters apply to DDR2-667 and DDR2-800 only. The jitter specified is a random jitter meeting a Gaussian distribution.

Parameter	Symbol	DDR2-667		DDR2-800		Units	Notes
		min	max	min	max		
Clock period jitter	tJIT(per)	-125	125	-100	100	ps	35
Clock period jitter during DLL locking period	tJIT(per,lck)	-100	100	-80	80	ps	35
Cycle to cycle clock period jitter	tJIT(cc	-250	250	-200	200	ps	35
Cycle to cycle clock period jitter during DLL locking period	tJIT(cc,lck)	-200	200	-160	160	ps	35
Cumulative error across 2 cycles	tERR(2per)	-175	175	-150	150	ps	35
Cumulative error across 3 cycles	tERR(3per)	-225	225	-175	175	ps	35
Cumulative error across 4 cycles	tERR(4per)	-250	250	-200	200	ps	35
Cumulative error across 5 cycles	tERR(5per)	-250	250	-200	200	ps	35
Cumulative error across n cycles, n = 6 ... 10, inclusive	tERR(6-10per)	-350	350	-300	300	ps	35
Cumulative error across n cycles, n = 11 ... 50, inclusive	tERR(11-50per)	-450	450	-450	450	ps	35
Duty cycle jitter	tJIT(duty)	-125	125	-100	100	ps	35

36. These parameters are specified per their average values, however it is understood that the following relationship between the average timing and the absolute instantaneous timing holds at all times. (Min and max of SPEC values are to be used for calculations in the table below.)

Parameter	Symbol	min	max	Units
Absolute clock period	tCK(abs)	tCK(avg),min + tJIT(per),min	tCK(avg),max + tJIT(per),max	ps
Absolute clock HIGH pulse width	tCH(abs)	tCH(avg),min x tCK(avg),min + tJIT(duty),min	tCH(avg),max x tCK(avg),max + tJIT(duty),max	ps
Absolute clock LOW pulse width	tCL(abs)	tCL(avg),min x tCK(avg),min + tJIT(duty),min	tCL(avg),max x tCK(avg),max + tJIT(duty),max	ps

Example: For DDR2-667, tCH(abs),min = (0.48 x 3000 ps) - 125 ps = 1315 ps

37. tHP is the minimum of the absolute half period of the actual input clock. tHP is an input parameter but not an input specification parameter. It is used in conjunction with tQHS to derive the DRAM output timing tQH.

The value to be used for tQH calculation is determined by the following equation;

tHP = Min (tCH(abs), tCL(abs)),

where,

tCH(abs) is the minimum of the actual instantaneous clock HIGH time;

tCL(abs) is the minimum of the actual instantaneous clock LOW time;

38. tQHS accounts for:

1) The pulse duration distortion of on-chip clock circuits, which represents how well the actual tHP at the input is transferred to the output; and

2) The worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are independent of each other, due to data pin skew, output pattern effects, and pchannel to n-channel variation of the output drivers

39. tQH = tHP – tQHS, where:

tHP is the minimum of the absolute half period of the actual input clock; and

tQHS is the specification value under the max column.

{The less half-pulse width distortion present, the larger the tQH value is; and the larger the valid data eye will be.}

Examples:

1) If the system provides tHP of 1315 ps into a DDR2-667 SDRAM, the DRAM provides tQH of 975 ps minimum.

2) If the system provides tHP of 1420 ps into a DDR2-667 SDRAM, the DRAM provides tQH of 1080 ps minimum.

40. When the device is operated with input clock jitter, this parameter needs to be derated by the actual tERR(6-10per) of the input clock. (output deratings are relative to the SDRAM input clock.)

For example, if the measured jitter into a DDR2-667 SDRAM has tERR(6-10per),min = - 272 ps and tERR(6-10per),max = + 293 ps, then tDQSCK,min(derated) = tDQSCK,min - tERR(6-10per),max = - 400 ps - 293 ps = - 693 ps and tDQSCK,max(derated) = tDQSCK,max - tERR(6-10per),min = 400 ps + 272 ps = + 672 ps. Similarly, tLZ(DQ) for DDR2-667 derates to tLZ(DQ),min(derated) = - 900 ps - 293 ps = - 1193 ps and tLZ(DQ),max(derated) = 450 ps + 272 ps = + 722 ps. (Caution on the min/max usage!)

41. When the device is operated with input clock jitter, this parameter needs to be derated by the actual tJIT(per) of the input clock. (output deratings are relative to the SDRAM input clock.)

For example, if the measured jitter into a DDR2-667 SDRAM has tJIT(per),min = - 72 ps and tJIT(per),max = + 93 ps, then tRPRE,min(derated) = tRPRE,min + tJIT(per),min = 0.9 x tCK(avg) - 72 ps = + 2178 ps and tRPRE,max(derated) = tRPRE,max + tJIT(per),max = 1.1 x tCK(avg) + 93 ps = + 2843 ps. (Caution on the min/max usage!)

42. When the device is operated with input clock jitter, this parameter needs to be derated by the actual tJIT(duty) of the input clock. (output deratings are relative to the SDRAM input clock.)

For example, if the measured jitter into a DDR2-667 SDRAM has tJIT(duty),min = - 72 ps and tJIT(duty),max = + 93 ps, then tRPST,min(derated) = tRPST,min + tJIT(duty),min = 0.4 x tCK(avg) - 72 ps = + 928 ps and tRPST,max(derated) = tRPST,max + tJIT(duty),max = 0.6 x tCK(avg) + 93 ps = + 1592 ps. (Caution on the min/max usage!)

43. When the device is operated with input clock jitter, this parameter needs to be derated by { -tJIT(duty),max - tERR(6-10per),max } and { - tJIT(duty),min - tERR(6-10per),min } of the actual input clock. (output deratings are relative to the SDRAM input clock.)

For example, if the measured jitter into a DDR2-667 SDRAM has tERR(6-10per),min = - 272 ps, tERR(6-10per),max = + 293 ps, tJIT(duty),min = - 106 ps and tJIT(duty),max = + 94 ps, then tAOF,min(derated) = tAOF,min + { - tJIT(duty),max - tERR(6-10per),max } = - 450 ps + { - 94 ps - 293 ps} = - 837 ps and tAOF,max(derated) = tAOF,max + { - tJIT(duty),min - tERR(6-10per),min } = 1050 ps + { 106 ps + 272 ps } = + 1428 ps. (Caution on the min/max usage!)

44. For tAOFD of DDR2-400/533, the 1/2 clock of tCK in the 2.5 x tCK assumes a tCH, input clock HIGH pulse width of 0.5 relative to tCK. tAOF,min and tAOF,max should each be derated by the same amount as the actual amount of tCH offset present at the DRAM input with respect to 0.5. For example, if an input clock has a worst case tCH of 0.45, the tAOF,min should be derated by subtracting 0.05 x tCK from it, whereas if an input clock has a worst case tCH of 0.55, the tAOF,max should be derated by adding 0.05 x tCK to it. Therefore, we have;

tAOF,min(derated) = tAC,min - [0.5 - Min(0.5, tCH,min)] x tCK

tAOF,max(derated) = tAC,max + 0.6 + [Max(0.5, tCH,max) - 0.5] x tCK

or

tAOF,min(derated) = Min(tAC,min, tAC,min - [0.5 - tCH,min] x tCK)

tAOF,max(derated) = 0.6 + Max(tAC,max, tAC,max + [tCH,max - 0.5] x tCK)

where tCH,min and tCH,max are the minimum and maximum of tCH actually measured at the DRAM input balls.

45. For tAOFD of DDR2-667/800, the 1/2 clock of nCK in the 2.5 x nCK assumes a tCH(avg), average input clock HIGH pulse width of 0.5 relative to tCK(avg). tAOF,min and tAOF,max should each be derated by the same amount as the actual amount of tCH(avg) offset present at the DRAM input with respect to 0.5. For example, if an input clock has a worst case tCH(avg) of 0.48, the tAOF,min should be derated by subtracting 0.02 x tCK(avg) from it, whereas if an input clock has a worst case tCH(avg) of 0.52, the tAOF,max should be derated by adding 0.02 x tCK(avg) to it. Therefore, we have;

tAOF,min(derated) = tAC,min - [0.5 - Min(0.5, tCH(avg),min)] x tCK(avg)

tAOF,max(derated) = tAC,max + 0.6 + [Max(0.5, tCH(avg),max) - 0.5] x tCK(avg)

or

tAOF,min(derated) = Min(tAC,min, tAC,min - [0.5 - tCH(avg),min] x tCK(avg))

tAOF,max(derated) = 0.6 + Max(tAC,max, tAC,max + [tCH(avg),max - 0.5] x tCK(avg))

where tCH(avg),min and tCH(avg),max are the minimum and maximum of tCH(avg) actually measured at the DRAM input balls.

Note that these deratings are in addition to the tAOF derating per input clock jitter, i.e. tJIT(duty) and tERR(6-10per). However tAC values used in the equations shown above are from the timing parameter table and are not derated.

Thus the final derated values for tAOF are;

tAOF,min(derated_final) = tAOF,min(derated) + { - tJIT(duty),max - tERR(6-10per),max }

tAOF,max(derated_final) = tAOF,max(derated) + { - tJIT(duty),min - tERR(6-10per),min }

46. Flexibility is provided for the absolute refresh interval. A maximum of 8 Refresh commands can be posted to the DRAM, meaning that the maximum absolute interval between any refresh command and the next Refresh command is 9x tREFI.

FUNCTIONAL DESCRIPTION

Power-up and Initialization

DDR2 SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. For DDR2 SDRAMs, both bits BA0 and BA1 must be decoded for Mode/ Extended Mode Register Set (MRS/EMRS) commands. Users must initialize all four Mode Registers. The registers may be initialized in any order.

Power-up and Initialization Sequence

The following sequence is required for Power-up and Initialization.

a) Either one of the following sequence is required for Power-up.

a1) While applying power, attempt to maintain CKE below 0.2 x VDDQ and ODT*1 at a LOW state (all other inputs may be undefined.) The VDD voltage ramp time must be no greater than 200 ms from when VDD ramps from 300 mV to VDD min; and during the VDD voltage ramp, |VDD-VDDQ| ≤ 0.3 volts. Once the ramping of the supply voltages is complete (when VDDQ crosses VDDQ min), the supply voltage specifications provided in "Recommended DC operating conditions" (SSTL_1.8), prevail.

- VDD, VDDL and VDDQ are driven from a single power converter output, AND
- VTT is limited to 0.95V max, AND
- VREF tracks VDDQ/2, VREF must be within +/- 300mV with respect to VDDQ/2 during supply ramp time.
- VDDQ ≥ VREF must be met at all times.

a2) While applying power, attempt to maintain CKE below 0.2 x VDDQ and ODT*1 at a LOW state, all other inputs may be undefined, voltage levels at I/Os and outputs must be less than VDDQ during voltage ramp time to avoid DRAM latch-up. During the ramping of the supply voltages, VDD ≥ VDDL ≥ VDDQ must be maintained and is applicable to both AC and DC levels until the ramping of the supply voltages is complete, which is when VDDQ crosses VDDQ min. Once the ramping of the supply voltages is complete, the supply voltage specifications provided in "Recommended DC operating conditions" (SSTL_1.8), prevail.

- Apply VDD/VDDL before or at the same time as VDDQ.
- VDD/VDDL voltage ramp time must be no greater than 200ms from when VDD ramps from 300mV to VDD min
- Apply VDDQ before or at the same time as VTT.
- The VDDQ voltage ramp time from when VDD min is achieved on VDD to when VDDQ min is achieved on VDDQ must be no greater than 500ms.
  (Note: While VDD is ramping, current may be supplied from VDD through the DRAM to VDDQ.)
- VREF must track VDDQ/2, VREF must be within +/- 300mv with respect to VDDQ/2 during supply ramp time.

- VDDQ ≥ VREF must be met at all times.

- Apply VTT.

- The VTT voltage ramp time from when VDDQ min is achieved on VDDQ to when VTT min is achieved on VTT must be no greater than 500ms.

b) Start clock and maintain stable condition.

c) For the minimum of 200µs after stable power (VDD, VDDL, VDDQ, VREF and VTT are between their minimum and maximum values as stated in "Recommended DC operating conditions" (SSTL_1.8)) and stable clock (CK, CK), then apply NOP or Deselect & take CKE HIGH.

d) Wait minimum of 400ns then issue precharge all command. NOP or Deselect applied during 400 ns period.

e) Issue an EMRS command to EMR(2).

Power-up and Initialization Sequence (cont'd)

f) Issue an EMRS command to EMR(3).

g) Issue EMRS to enable DLL.

h) Issue a Mode Register Set command for DLL reset.

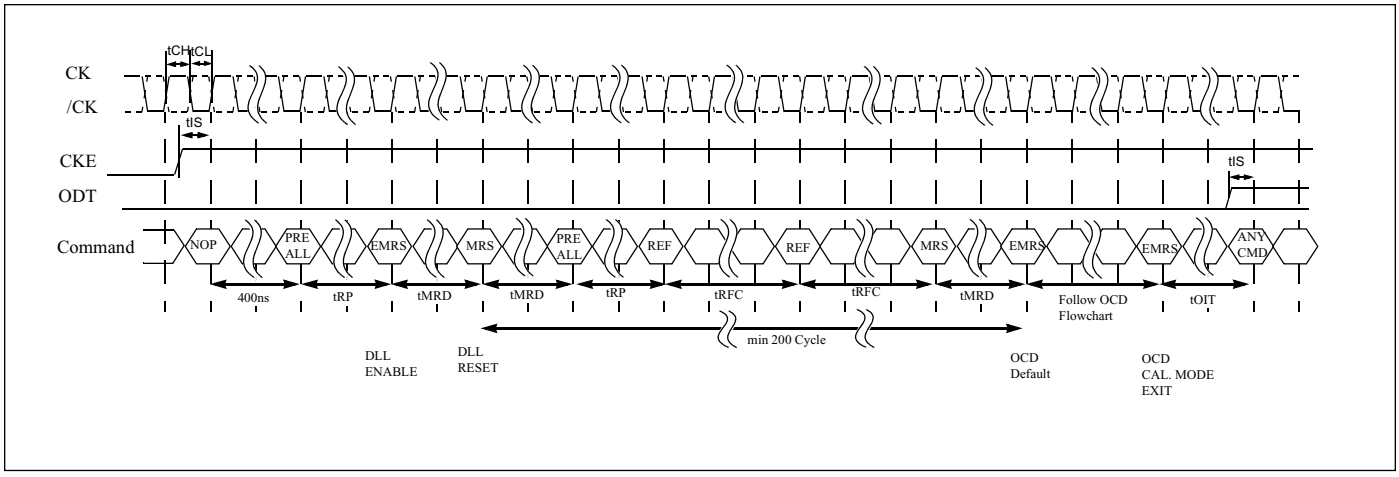
i) Issue a precharge all command.

j) Issue 2 or more auto-refresh commands.

k) Issue a MRS command with LOW to A8 to initialize device operation. (i.e. to program operating parameters without resetting the DLL.)

l) At least 200 clocks after step h, execute OCD Calibration. This is done by EMRS to EMR(1) to set OCD Calibration Default (A9=A8=A7=HIGH) followed by EMRS to EMR(1) to exit OCD Calibration Mode (A9=A8=A7=LOW) must be issued with other operating parameters of EMR(1).

m) The DDR2 SDRAM is now ready for normal operation.



Initialization Sequence after Power-Up

Programming the Mode and Extended Mode Registers

For application flexibility, burst length, burst type, CAS latency, DLL reset function, write recovery time (WR) are user defined variables and must be programmed with a Mode Register Set (MRS) command. Additionally, DLL disable function, driver impedance, additive CAS latency, ODT (On Die Termination), single-ended strobe, and OCD (off chip driver impedance adjustment) are also user defined variables and must be programmed with an Extended Mode Register Set (EMRS) command. Contents of the Mode Register or Extended Mode Registers can be altered by re-executing the MRS or EMRS Commands. Even if the user chooses to modify only a subset of the MR, or EMR(1), EMR(2), or EMR(3) variables, all variables within the addressed register must be redefined when the MRS or EMRS commands are issued.

MRS, EMRS and Reset DLL do not affect memory array contents, which means re-initialization including those can be executed at any time after power-up without affecting memory array contents.

Mode Register (MR)

The mode register stores the data for controlling the various operating modes of the DDR2 SDRAM. It controls CAS latency, burst length, burst sequence, test mode, DLL reset, and Write Recovery time (WR) to make DDR2 SDRAM useful for various applications. The default value of the mode register is not defined, therefore the mode register must be programmed during initialization for proper operation. The mode register is written by asserting LOW on CS, RAS, CAS, WE, BA0, BA1 and BA2, while controlling the state of address pins A0-A13(x8) or A0-A12(x16). The DDR2 SDRAM should be in all bank precharge state with CKE already HIGH prior to writing into the mode register. The mode register set command cycle time (tMRD) is required to complete the write operation to the mode register. The mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state. The mode register is divided into various fields depending on functionality. Burst length is defined by A0 - A2 with options of 4 and 8 bit burst lengths. The burst length decodes are compatible with DDR SDRAM. Burst address sequence type is defined by A3, CAS latency is defined by A4 - A6. The DDR2 does not support half clock latency mode. A7 is a mode bit and must be set to LOW for normal MRS operation. A8 is used for DLL reset. Write recovery time WR is defined by A9 - A11. Refer to the table for specific codes.

DDR2 SDRAM Mode Register Set (MRS)

Address Field	Mode Register
BA1	**0**
BA0	**0**
A13	0
A12	PD
A11	WR
A10	WR
A9	WR
A8	DLL
A7	TM
A6	CAS Latency
A5	CAS Latency
A4	CAS Latency
A3	BT
A2	Burst Length
A1	Burst Length
A0	Burst Length

A12	Active power down exit time
0	Fast exit (use tXARD)
1	Slow exit(use tXARDS)

A11	A10	A9	WR(cycles)[1]
0	0	0	Reserved
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

A8	DLL Reset
0	No
1	Yes

A7	Mode
0	Normal
1	Reserved

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	3[2]
1	0	0	4[2]
1	0	1	5[2]
1	1	0	6[2]
1	1	1	7[2]

A3	Burst Type
0	Sequential
1	Interleave

A2	A1	A0	BL
0	1	0	4
0	1	1	8

Notes:
1. For DDR2-400/533, WR (write recovery for autoprecharge) min is determined by tCK max and WR max is determined by tCK min. WR in clock cycles is calculated by dividing tWR (in ns) by tCK (in ns) and rounding up to the next integer (WR[cycles] = RU{ tWR[ns] / tCK[ns] }, where RU stands for round up). For DDR2-667/800, WR min is determined by tCK(avg) max and WR max is determined by tCK(avg) min. WR[cycles] = RU{ tWR[ns] / tCK(avg)[ns] }, where RU stands for round up. The mode register must be programmed to this value. This is also used with tRP to determine tDAL.
2. Speed bin determined. Refer to Key Timing Parameter table.
3. A13, only applicable for x8.

Burst mode operation

Burst mode operation is used to provide a constant flow of data to memory locations (write cycle), or from memory locations (read cycle). The parameters that define how the burst mode will operate are burst sequence and burst length. DDR2 SDRAM supports 4 bit burst and 8 bit burst modes only. For 8 bit burst mode, full interleave address ordering is supported, however, sequential address ordering is nibble based for ease of implementation. The burst type, either sequential or interleaved, is programmable and defined by MR[A3], which is similar to the DDR SDRAM operation. Seamless burst read or write operations are supported. Unlike DDR devices, interruption of a burst read or write cycle during BL = 4 mode operation is prohibited. However in case of BL = 8 mode, interruption of a burst read or write operation is limited to two cases, reads interrupted by a read, or writes interrupted by a write. Therefore the Burst Stop command is not supported on DDR2 SDRAM devices.

Burst Length and Sequence

Burst Length	Starting Address (A1, A0)	Sequential Addressing (decimal)	Interleave Addressing (decimal)
4	0 0	0, 1, 2, 3	0, 1, 2, 3
	0 1	1, 2, 3, 0	1, 0, 3, 2
	1 0	2, 3, 0, 1	2, 3, 0, 1
	1 1	3, 0, 1, 2	3, 2, 1, 0

Burst Length	Starting Address (A2, A1, A0)	Sequential Addressing (decimal)	Interleave Addressing (decimal)
8	0 0 0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	0 0 1	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6
	0 1 0	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5
	0 1 1	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4
	1 0 0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	1 0 1	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2
	1 1 0	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1
	1 1 1	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0

Extended Mode Registers (EMR)

Extended Mode Register 1 (EMR1)

The EMR(1) stores the data for enabling or disabling the DLL, output driver strength, additive latency, ODT, DQS disable, OCD program, RDQS enable. The default value of the EMR(1) is not defined, therefore the extended mode register must be programmed during initialization for proper operation. The EMR(1) is written by asserting LOW on CS, RAS, CAS, WE, HIGH on BA0 and LOW on BA1 and BA2, while controlling the states of address pins A0 - A13. The DDR2 SDRAM should be in all bank precharge with CKE already HIGH prior to writing into the extended mode register. The mode register set command cycle time (tMRD) must be satisfied to complete the write operation to the extended mode register. Mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state.

DLL enable/disable

The DLL must be enabled for normal operation. DLL enable is required during power-up and initialization, and upon returning to normal operation after having the DLL disabled. The DLL is automatically disabled when entering self refresh operation and is automatically re-enabled upon exit of self refresh operation. Any time the DLL is enabled (and subsequently reset), 200 clock cycles must occur before a Read command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the tAC or tDQSCK parameters.

Address Field	Mode Register
BA2	**0**
BA1	**0**
BA0	**1**
A13[4]	0
A12	Qoff
A11	RDQS[*1]
A10	/DQS
A9	OCD Program
A8	
A7	
A6	Rtt
A5	Additive Latency
A4	
A3	
A2	Rtt
A1	D.I.C
A0	DLL

A12	Qoff[*3]
0	Output buffer enabled
1	Ouput buffer disabled

A11[*1]	RDQS Enable
0	Disable
1	Enable

A10	/DQS
0	Enable
1	Disable

A11[*1] (RDQS)	A10 (/DQS)	Strobe Function Marix RDQS/DM	/RDQS	DQS	/DQS
0	**0**	DM	Hi-z	**DQS**	**/DQS**
0	**1**	DM	Hi-z	**DQS**	**Hi-z**
1	0	RDQS	/RDQS	DQS	/DQS
1	1	RDQS	Hi-z	DQS	Hi-z

A9	A8	A7	OCD Calibration Program
0	0	0	OCD Calibration mode exit; maintain setting
0	0	1	Reserved
0	1	0	Reserved
1	0	0	Reserved
1	1	1	OCD Calibration default[*2]

A5	A4	A3	Additive Latency
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	Reserved

A6	A2	Rtt(NOMINAL)
0	0	ODT Disabled
0	1	75 ohm
1	0	150 ohm
1	1	50 ohm

A1	Output Drive Impedance Control
0	Full Strength
1	Reduced strength

A0	DLL enable
0	Enable
1	Disable

EMR(1)

Notes:
1. x16 doesn't support RDQS option; this must be set to 0 when programming the EMR(1).
2. After setting to default, OCD calibration mode needs to be exited by setting A9-A7 to 000.
3. Output disabled - DQs, DQSs, $\overline{\text{DQS}}$s, RDQS and $\overline{\text{RDQS}}$. This feature is used in conjunction with DIMM IDD measurements when IDDQ is not desired to be included.
4. A13 is only applicable for x8.

Extended Mode Register 2 (EMR2)

The Extended Mode Register 2 controls refresh related features. The default value of the EMR(2) is not defined, therefore the mode register must be programmed during initialization for proper operation. The EMR(2) is written by asserting LOW on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, HIGH on BA1 and LOW on BA0 and BA2, while controlling the states of address pins A0 - A13. The DDR2 SDRAM should be in all bank precharge state with CKE already HIGH prior to writing into the EMR(2). The mode register set command cycle time (tMRD) must be satisfied to complete the write operation to the EMR(2). Mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state.

Address Field	Mode Register
BA2	**0**
BA1	**1**
BA0	**0**
A13[*1,3]	**0**
A12[*1]	**0**
A11[*1]	**0**
A10[*1]	**0**
A9[*1]	**0**
A8[*1]	**0**
A7	SRF
A6[*1]	**0**
A5[*1]	**0**
A4[*1]	**0**
A3[*1]	**0**
A2[*1]	**0**
A1[*1]	**0**
A0[*1]	**0**

A7	High Temperature Self-Refresh Rate Enable
0	Disable
1	Enable[*2]

EMR(2)

Notes:
1. A0-A6, A8-A13 are reserved for future use and must be set to 0 when programming the EMR(2).
2. Only Industrial and Automotive grade devices support the high temperature Self-Refresh Mode. The controller can set the EMR (2) [A7] bit to enable this self-refresh rate if Tc > 85°C while in self-refresh operation. TOPER may not be violated.
3. A13 is only applicable for x8.

DDR2 SDRAM Extended Mode Register 3 (EMR3)

No function is defined in Extended Mode Register (3). The default value of the EMR(3) is not defined, therefore the EMR(3) must be programmed during initialization for proper operation.

All bits in EMR(3) except BA0, BA1 and BA2 are reserved for future use and must be set to 0 when programming this mode register.

Address Field	BA2	BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode Register	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TRUTH TABLES

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the speechified initialization sequence before normal operation can continue.

Command Truth Table

Function	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA2 - BA0	A13-A11	A10	A9-A0	Notes
	Previous Cycle	Current Cycle									
(Extended) Mode Register Set (Load Mode)	H	H	L	L	L	L	BA	OP Code			1, 2
Refresh (REF)	H	H	L	L	L	H	X	X	X	X	1
Self Refresh Entry	H	L	L	L	L	H	X	X	X	X	1, 8
Self Refresh Exit	L	H	H	X	X	X	X	X	X	X	1, 7, 8
			L	H	H	H					
Single Bank Precharge	H	H	L	L	H	L	BA	X	L	X	1, 2
Precharge all Banks	H	H	L	L	H	L	X	X	H	X	1
Bank Activate	H	H	L	L	H	H	BA	Row Address			1,2,10
Write	H	H	L	H	L	L	BA	X	L	Column	1, 2, 3
Write with Auto Precharge	H	H	L	H	L	L	BA	X	H	Column	1, 2, 3
Read	H	H	L	H	L	H	BA	X	L	Column	1, 2, 3
Read with Auto-Precharge	H	H	L	H	L	H	BA	X	H	Column	1, 2, 3
No Operation	H	X	L	H	H	H	X	X	X	X	1
Device Deselect	H	X	H	X	X	X	X	X	X	X	1
Power Down Entry	H	L	H	X	X	X	X	X	X	X	1, 4
			L	H	H	H					
Power Down Exit	L	H	H	X	X	X	X	X	X	X	1, 4
			L	H	H	H					

Notes:
1. All DDR2 SDRAM commands are defined by states of $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and CKE at the rising edge of the clock.
2. Bank addresses BA0, BA1 and BA2 (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.
3. Burst reads or writes at BL=4 cannot be terminated or interrupted. See sections "Reads interrupted by a Read" and "Writes interrupted by a Write" for details.
4. The Power Down Mode does not perform any refresh operations. The duration of Power Down is therefore limited by the refresh requirements
5. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh. See section 3.4.4.
6. “X” means “H or L (but a defined logic level)”
7. Self refresh exit is asynchronous.
8. VREF must be maintained during Self Refresh operation.
9. BAx and Axx refers to the MSBs of bank addresses and addresses, respectively.
10. For x16 option, A13 is "Don't Care" (X) for Activate.

Clock Enable (CKE) Truth Table

Current State[2]	CKE		Command (N)[3]	Action (N)[3]	Notes
	Previous Cycle[1] (N-1)	Current Cycle[1] (N)	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$		
Power Down	L	L	X	Maintain Power-Down	11, 13, 15
	L	H	DESELECT or NOP	Power Down Exit	4, 8, 11, 13
Self Refresh	L	L	X	Maintain Self Refresh	11, 15,16
	L	H	DESELECT or NOP	Self Refresh Exit	4, 5, 9, 16
Bank(s) Active	H	L	DESELECT or NOP	Active Power Down Entry	4, 8, 10, 11, 13
All Banks Idle	H	L	DESELECT or NOP	Precharge Power Down Entry	4, 8, 10, 11,13
	H	L	REFRESH	Self Refresh Entry	6, 9, 11,13
	H	H	Refer to the Command Truth Table		7

Notes:
1. CKE (N) is the logic state of CKE at clock edge N; CKE (N–1) was the state of CKE at the previous clock edge.
2. Current state is the state of the DDR2 SDRAM immediately prior to clock edge N.
3. COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N).
4. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
5. On Self Refresh Exit DESELECT or NOP commands must be issued on every clock edge occurring during the tXSNR period. Read commands may be issued only after tXSRD (200 clocks) is satisfied.
6. Self Refresh mode can only be entered from the All Banks Idle state.
7. Must be a legal command as defined in the Command Truth Table.
8. Valid commands for Power Down Entry and Exit are NOP and DESELECT only.
9. Valid commands for Self Refresh Exit are NOP and DESELECT only.
10. Power Down and Self Refresh cannot be entered while Read or Write operations, (Extended) Mode Register Set operations or Precharge operations are in progress.
11. tCKEmin of 3 clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the 3 clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of tIS + 2 x tCK + tIH.
12. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
13. The Power Down does not perform any refresh operations. The duration of Power Down Mode is therefore limited by the refresh requirements outlined in this datasheet.
14. CKE must be maintained HIGH while the DDRII SDRAM is in OCD calibration mode .
15. “X” means “don’t care (including floating around VREF)” in Self Refresh and Power Down. However ODT must be driven HIGH or LOW in Power Down if the ODT function is enabled (Bit A2 or A6 set to “1” in EMR(1)).
16. VREF must be maintained during Self Refresh operation.

Data Mask Truth Table

Name (Functional)	DM	DQs	Note
Write enable	L	Valid	1
Write inhibit	H	X	1

Note:
1. Used to mask write data, provided coincident with the corresponding data

DESELECT

The DESELECT function ($\overline{CS}$ HIGH) prevents new commands from being executed by the DDR2 SDRAM. The DDR2 SDRAM is effectively deselected. Operations already in progress are not affected. DESELECT is also referred to as COMMAND INHIBIT.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to instruct the selected DDR2 SDRAM to perform a NOP ($\overline{CS}$ is LOW; $\overline{RAS}$, $\overline{CAS}$, and WE are HIGH). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

MODE REGISTER SET (MRS or EMRS)

The mode registers are loaded via bank address and address inputs. The bank address balls determine which mode register will be programmed. See sections on Mode Register and Extended Mode Register. The MRS and EMRS commands can only be issued when all banks are idle, and a subsequent executable command cannot be issued until tMRD is met.

ACTIVATE

The ACTIVATE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the bank address inputs determines the bank, and the address inputs select the row. This row remains active (or open) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

READ

The READ command is used to initiate a burst read access to an active row. The value on the bank address inputs determine the bank, and the address provided on address inputs A0–A9 selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the READ burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

DDR2 SDRAM also supports the AL feature, which allows a READ or WRITE command to be issued prior to tRCD (MIN) by delaying the actual registration of the READ/WRITE command to the internal device by AL clock cycles.

WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the bank select inputs selects the bank, and the address provided on inputs A0–A9 selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the WRITE burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

DDR2 SDRAM also supports the AL feature, which allows a READ or WRITE command to be issued prior to tRCD (MIN) by delaying the actual registration of the READ/WRITE command to the internal device by AL clock cycles.

Input data appearing on the DQ is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered LOW, the corresponding data will be written to memory; if the DM signal is registered HIGH, the corresponding data inputs will be ignored, and a WRITE will not be executed to that byte/column location.

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row activation a specified time (tRP) after the PRECHARGE command is issued, except in the case of concurrent auto precharge, where a READ or WRITE command to a different bank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. After a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command is allowed if there is no open row in that bank (idle state) or if the previously open row is already in the process of precharging. However, the precharge period will be determined by the last PRECHARGE command issued to the bank.

REFRESH

REFRESH is used during normal operation of the DDR2 SDRAM and is analogous to $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ (CBR) REFRESH. All banks must be in the idle mode prior to issuing a REFRESH command. This command is nonpersistent, so it must be issued each time a refresh is required. The addressing is generated by the internal refresh controller. This makes the address bits a “Don’t Care” during a REFRESH command.

Flexibility is provided for the absolute refresh interval. A maximum of 8 Refresh commands can be posted to the DRAM, meaning that the maximum absolute interval between any Refresh command and the next Refresh command is 9x tREFI.

SELF REFRESH

The SELF REFRESH command can be used to retain data in the DDR2 SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the DDR2 SDRAM retains data without external clocking. All power supply inputs (including VREF) must be maintained at valid levels upon entry/exit and during SELF REFRESH operation.

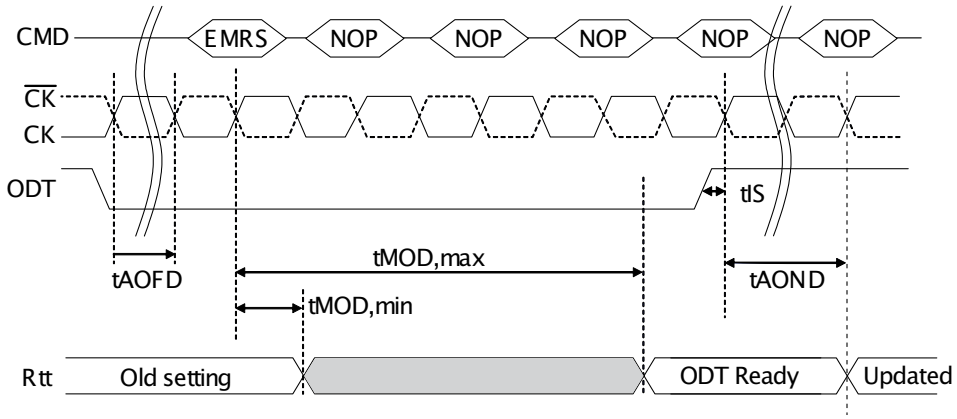
The SELF REFRESH command is initiated like a REFRESH command except CKE is LOW. The DLL is automatically disabled upon entering self refresh and is automatically enabled upon exiting self refresh.

ODT (On-Die Termination)

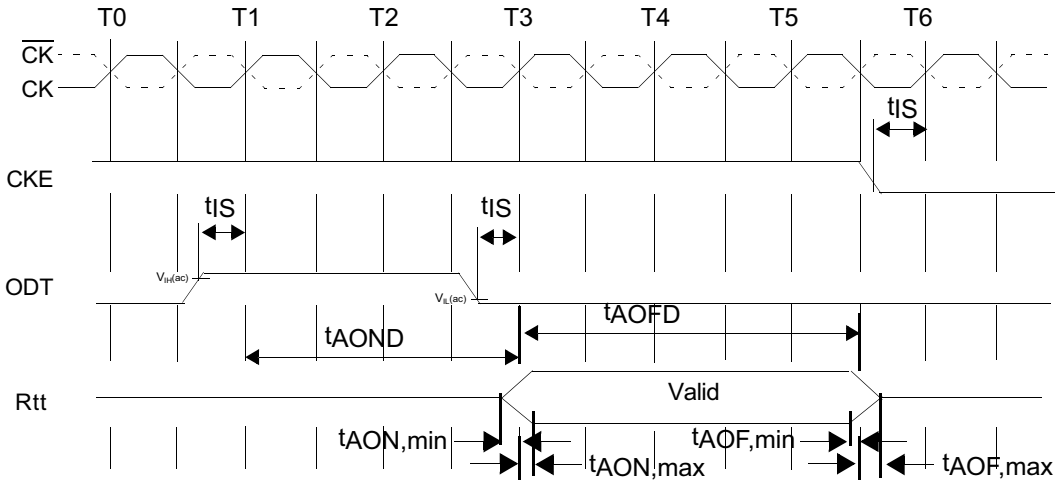
The On-Die Termination feature allows the DDR2 SDRAM to easily implement a termination resistance (Rtt) for each DQ, DQS, $\overline{\text{DQS}}$, RDQS, and $\overline{\text{RDQS}}$ signal. The ODT feature can be configured with the Extended Mode Register Set (EMRS) command, and turned on or off using the ODT input signal. Before and after the EMRS is issued, the ODT input must be received with respect to the timings of tAOFD, tMOD(max), tAOND; and the CKE input must be held HIGH throughout the duration of tMOD(max).

The DDR2 SDRAM supports the ODT on and off functionality in Active, Standby, and Power Down modes, but not in Self Refresh mode. ODT timing diagrams follow for Active/Standby mode and Power Down mode.

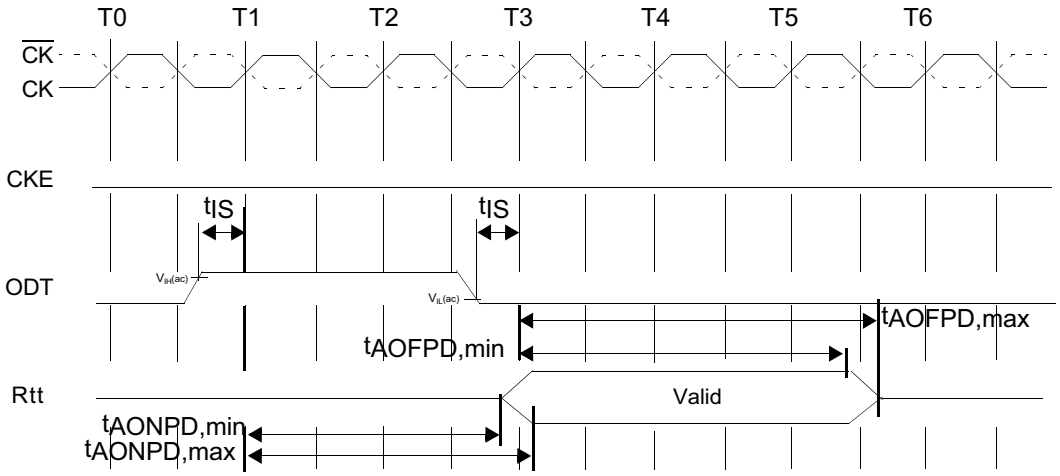
EMRS to ODT Update Delay



ODT On/Off Timing for Active/Standby mode



ODT On/Off Timing for Power-Down mode



ORDERING INFORMATION: x8

Commercial Range: Tc = 0°C to +85°C

Clock (MHz)	Speed Grade	CL-tRCD-tRP	Order Part No.	Package
400	DDR2-800D	5-5-5	IS43DR81280C-25DBL	60 Ball BGA, Lead-free
333	DDR2-667D	5-5-5	IS43DR81280C-3DBL	60 Ball BGA, Lead-free

Industrial Range: Tc = -40°C to +95°C, Ta = -40°C to +85°C

Clock (MHz)	Speed Grade	CL-tRCD-tRP	Order Part No.	Package
400	DDR2-800D	5-5-5	IS43DR81280C-25DBLI	60 Ball BGA, Lead-free
333	DDR2-667D	5-5-5	IS43DR81280C-3DBLI	60 Ball BGA, Lead-free

Automotive Range, A1: Tc = -40°C to +95°C, Ta = -40°C to +85°C

Clock (MHz)	Speed Grade	CL-tRCD-tRP	Order Part No.	Package
400	DDR2-800D	5-5-5	IS46DR81280C-25DBLA1	60 Ball BGA, Lead-free
333	DDR2-667D	5-5-5	IS46DR81280C-3DBLA1	60 Ball BGA, Lead-free

Automotive Range, A2: Tc = -40°C to +105°C, Ta = -40°C to +105°C

Clock (MHz)	Speed Grade	CL-tRCD-tRP	Order Part No.	Package
400	DDR2-800D	5-5-5	IS46DR81280C-25DBLA1	60 Ball BGA, Lead-free
333	DDR2-667D	5-5-5	IS46DR81280C-3DBLA1	60 Ball BGA, Lead-free

Notes:
1. Please contact ISSI for availability of leaded options.
2. The -3D, and -25D speed options are backward compatible with all the timing specifications for slower grades.

ORDERING INFORMATION: x16

Commercial Range: Tc = 0°C to +85°C

Clock (MHz)	Speed Grade	CL-tRCD-tRP	Order Part No.	Package
400	DDR2-800D	5-5-5	IS43DR16640C-25DBL	84 Ball BGA, Lead-free
333	DDR2-667D	5-5-5	IS43DR16640C-3DBL	84 Ball BGA, Lead-free

Industrial Range: Tc = -40°C to +95°C, Ta = -40°C to +85°C

Clock (MHz)	Speed Grade	CL-tRCD-tRP	Order Part No.	Package
400	DDR2-800D	5-5-5	IS43DR16640C-25DBLI	84 Ball BGA, Lead-free
333	DDR2-667D	5-5-5	IS43DR16640C-3DBLI	84 Ball BGA, Lead-free

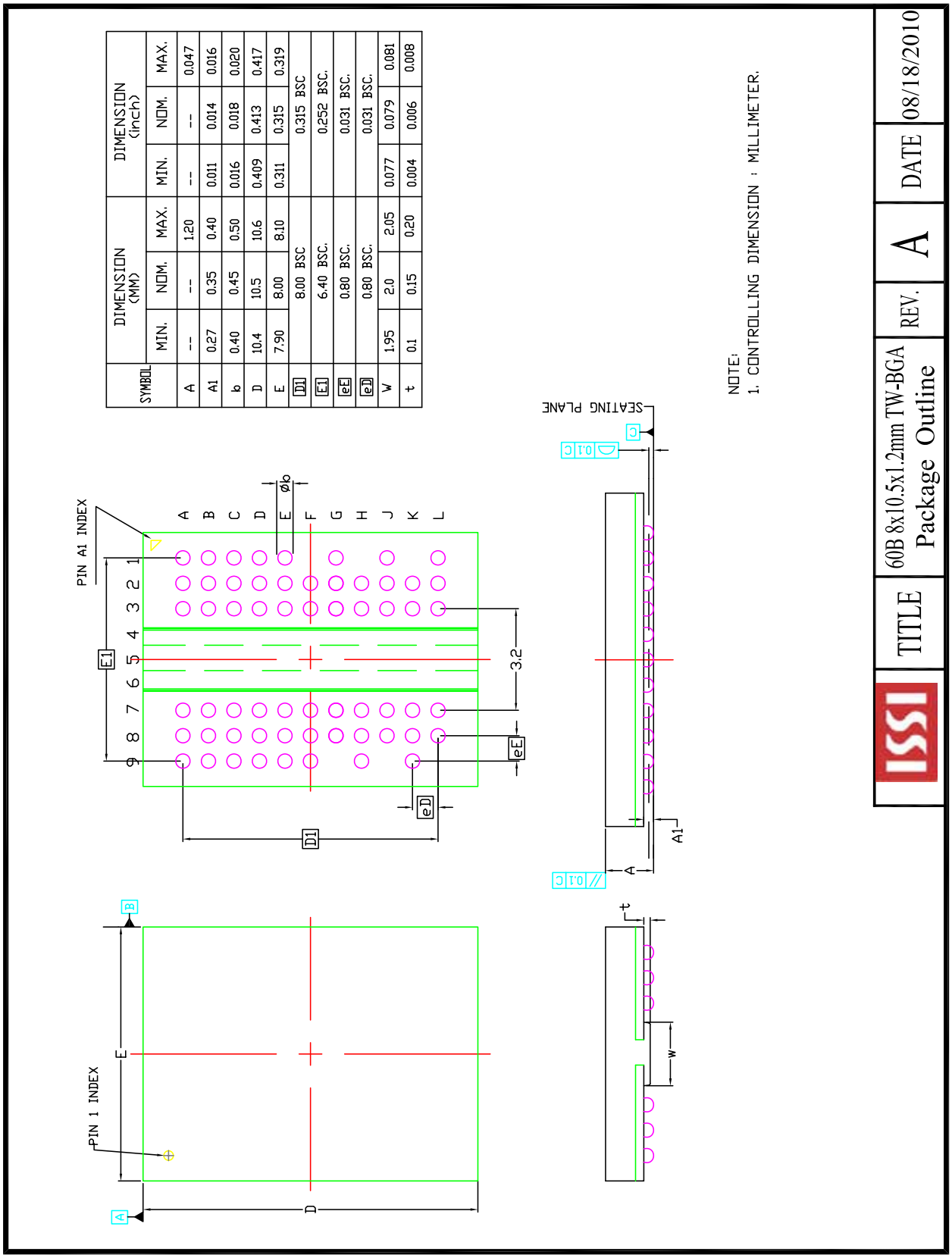
Automotive Range, A1: Tc = -40°C to +95°C, Ta = -40°C to +85°C

Clock (MHz)	Speed Grade	CL-tRCD-tRP	Order Part No.	Package
400	DDR2-800D	5-5-5	IS46DR16640C-25DBLA1	84 Ball BGA, Lead-free
333	DDR2-667D	5-5-5	IS46DR16640C-3DBLA1	84 Ball BGA, Lead-free

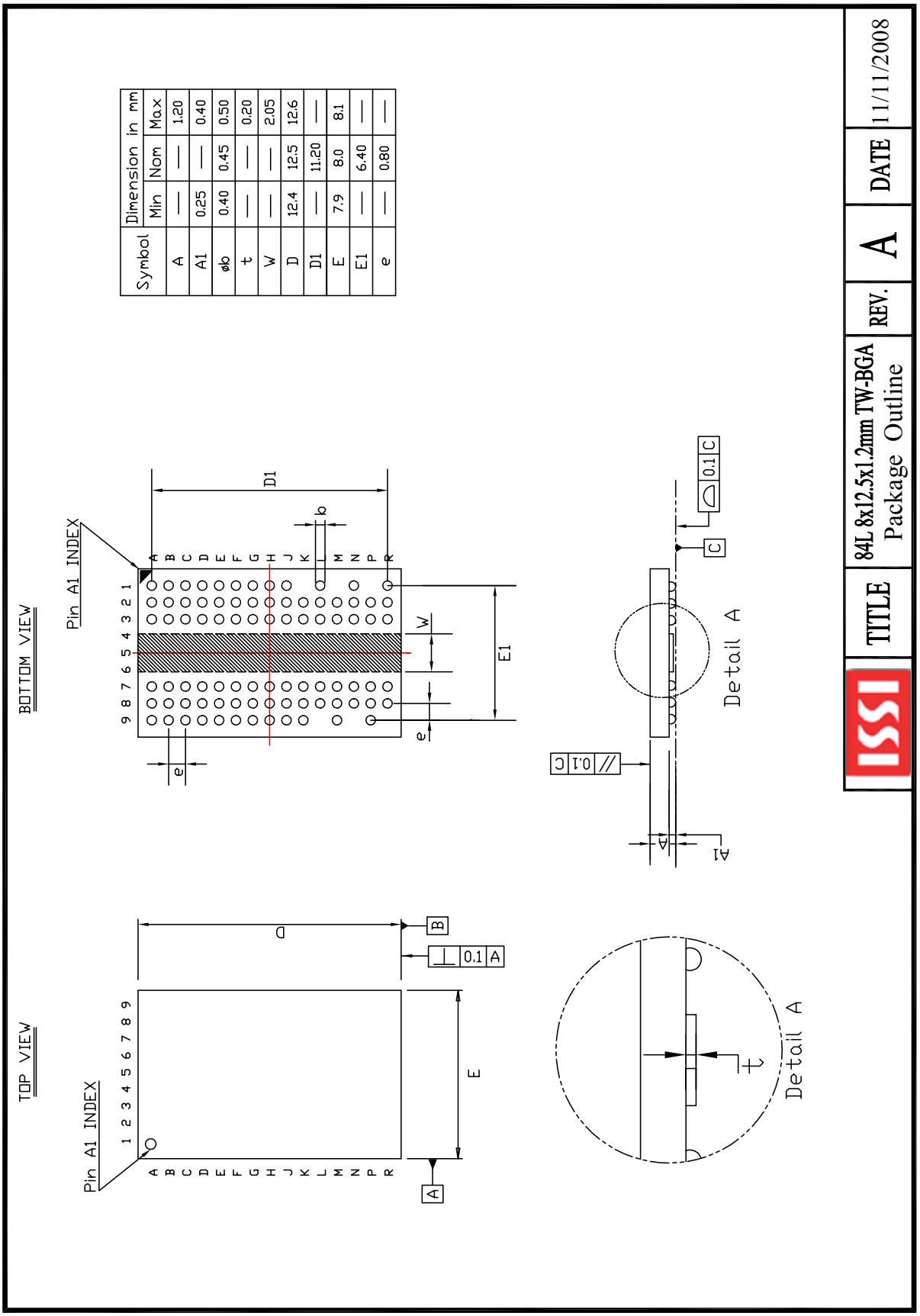
Automotive Range, A2: Tc = -40°C to +105°C, Ta = -40°C to +105°C

Clock (MHz)	Speed Grade	CL-tRCD-tRP	Order Part No.	Package
400	DDR2-800D	5-5-5	IS46DR16640C-25DBLA2	84 Ball BGA, Lead-free
333	DDR2-667D	5-5-5	IS46DR16640C-3DBLA2	84 Ball BGA, Lead-free

Notes:
1. Please contact ISSI for availability of leaded options.
2. The -3D, and -25D speed options are backward compatible with all the timing specifications for slower grades.



SYMBOL	DIMENSION (MM)			DIMENSION (inch)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	--	--	1.20	--	--	0.047
A1	0.27	0.35	0.40	0.011	0.014	0.016
b	0.40	0.45	0.50	0.016	0.018	0.020
D	10.4	10.5	10.6	0.409	0.413	0.417
E	7.90	8.00	8.10	0.311	0.315	0.319
D1		8.00 BSC			0.315 BSC	
E1		6.40 BSC.			0.252 BSC.	
eE		0.80 BSC.			0.031 BSC.	
eD		0.80 BSC.			0.031 BSC.	
W	1.95	2.0	2.05	0.077	0.079	0.081
t	0.1	0.15	0.20	0.004	0.006	0.008



Symbol	Dimension in mm		
	Min	Nom	Max
A	—	—	1.20
A1	0.25	—	0.40
øb	0.40	0.45	0.50
t	—	—	0.20
W	—	—	2.05
D	12.4	12.5	12.6
D1	—	11.20	—
E	7.9	8.0	8.1
E1	—	6.40	—
e	—	0.80	—