

## CURRENT SENSING SINGLE CHANNEL DRIVER

### Features

- Floating channel designed for bootstrap operation  
 Fully operational to +600V  
 Tolerant to negative transient voltage dV/dt immune
- Application- specific gate drive range:  
 Motor Drive: 12 to 20V (IR2127/IR2128)  
 Automotive: 9 to 20V (IR21271)
- Undervoltage lockout
- 3.3V, 5V and 15V input logic compatible
- FAULT lead indicates shutdown has occurred
- Output in phase with input (IR2127/IR21271)
- Output out of phase with input (IR2128)
- Available in Lead-Free

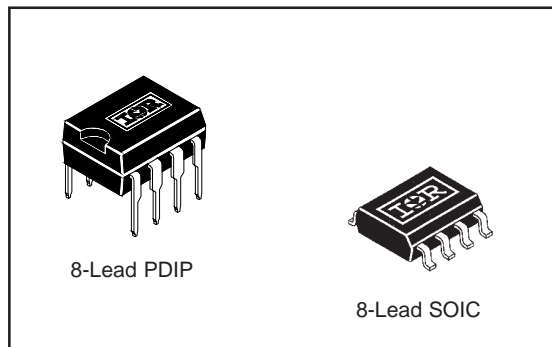
### Description

The IR2127/IR2128/IR21271(S) is a high voltage, high speed power MOSFET and IGBT driver. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL outputs, down to 3.3V. The protection circuitry detects over-current in the driven power transistor and terminates the gate drive voltage. An open drain FAULT signal is provided to indicate that an over-current shutdown has occurred. The output driver features a high pulse current buffer stage designed for minimum cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side or low side configuration which operates up to 600 volts.

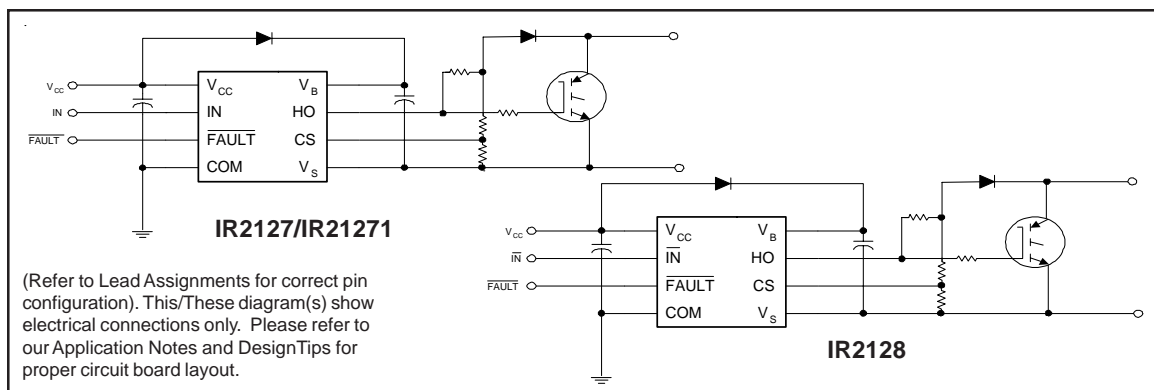
### Product Summary

<b>V<sub>OFFSET</sub></b>	<b>600V max.</b>	
<b>I<sub>O+/-</sub></b>	<b>200 mA / 420 mA</b>	
<b>V<sub>OUT</sub></b>	<b>12 - 20V</b> (IR2127/IR2128)	<b>9 - 20V</b> (IR21271)
<b>V<sub>csth</sub></b>	<b>250 mV or 1.8V</b>	
<b>t<sub>on/off</sub> (typ.)</b>	<b>200 &amp; 150 ns</b>	

### Packages



### Typical Connection



### Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
V <sub>B</sub>	High Side Floating Supply Voltage	-0.3	625	V
V <sub>S</sub>	High Side Floating Offset Voltage	V <sub>B</sub> - 25	V <sub>B</sub> + 0.3	
V <sub>HO</sub>	High Side Floating Output Voltage	V <sub>S</sub> - 0.3	V <sub>B</sub> + 0.3	
V <sub>CC</sub>	Logic Supply Voltage	-0.3	25	
V <sub>IN</sub>	Logic Input Voltage	-0.3	V <sub>CC</sub> + 0.3	
V <sub>FLT</sub>	$\overline{\text{FAULT}}$ Output Voltage	-0.3	V <sub>CC</sub> + 0.3	
V <sub>CS</sub>	Current Sense Voltage	V <sub>S</sub> - 0.3	V <sub>B</sub> + 0.3	
dV <sub>S</sub> /dt	Allowable Offset Supply Voltage Transient	—	50	V/ns
P <sub>D</sub>	Package Power Dissipation @ T <sub>A</sub> ≤ +25°C (8 Lead DIP)	—	1.0	W
	(8 Lead SOIC)	—	0.625	
R <sub>thJA</sub>	Thermal Resistance, Junction to Ambient (8 Lead DIP)	—	125	°C/W
	(8 Lead SOIC)	—	200	
T <sub>J</sub>	Junction Temperature	—	150	°C
T <sub>S</sub>	Storage Temperature	-55	150	
T <sub>L</sub>	Lead Temperature (Soldering, 10 seconds)	—	300	

### Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V<sub>S</sub> offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V <sub>B</sub>	High Side Floating Supply Voltage (IR2127/IR2128)	V <sub>S</sub> + 12	V <sub>S</sub> + 20	V
	(IR21271)	V <sub>S</sub> + 9	V <sub>S</sub> + 20	
V <sub>S</sub>	High Side Floating Offset Voltage	Note 1	600	
V <sub>HO</sub>	High Side Floating Output Voltage	V <sub>S</sub>	V <sub>B</sub>	
V <sub>CC</sub>	Logic Supply Voltage	10	20	
V <sub>IN</sub>	Logic Input Voltage	0	V <sub>CC</sub>	
V <sub>FLT</sub>	$\overline{\text{FAULT}}$ Output Voltage	0	V <sub>CC</sub>	
V <sub>CS</sub>	Current Sense Signal Voltage	V <sub>S</sub>	V <sub>S</sub> + 5	
T <sub>A</sub>	Ambient Temperature	-40	125	°C

Note 1: Logic operational for V<sub>S</sub> of -5 to +600V. Logic state held for V<sub>S</sub> of -5V to -V<sub>BS</sub>. (Please refer to the Design Tip DT97-3 for more details).

## Dynamic Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 15V,  $C_L$  = 1000 pF and  $T_A$  = 25°C unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in Figure 3.

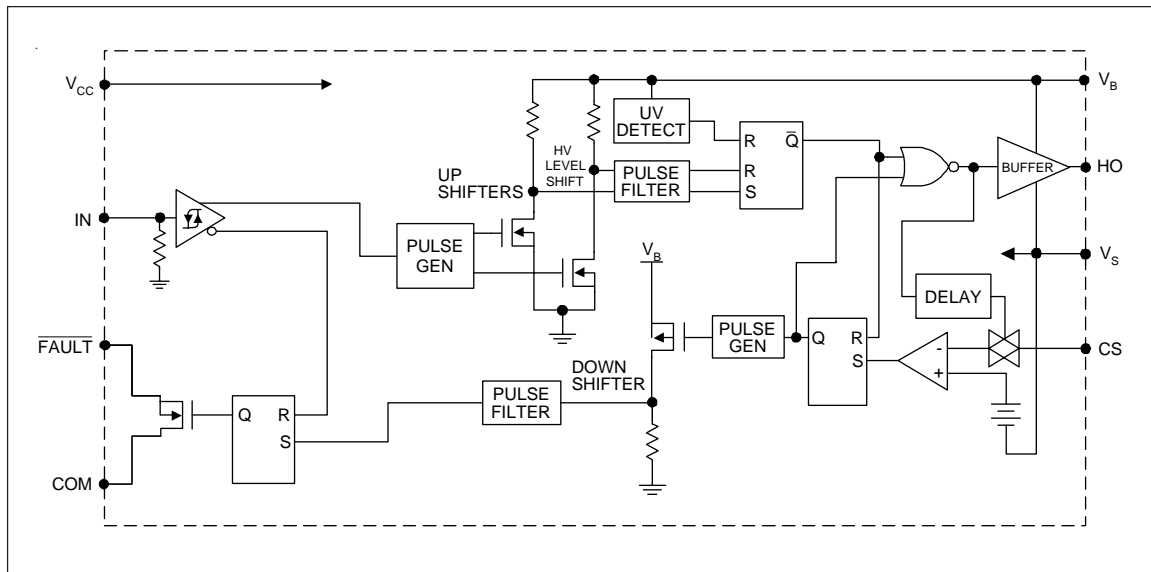
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$t_{on}$	Turn-On Propagation Delay	—	200	250	ns	$V_S = 0V$
$t_{off}$	Turn-Off Propagation Delay	—	150	200		$V_S = 600V$
$t_r$	Turn-On Rise Time	—	80	130		
$t_f$	Turn-Off Fall Time	—	40	65		
$t_{bl}$	Start-Up Blanking Time	500	700	900		
$t_{cs}$	CS Shutdown Propagation Delay	—	240	360		
$t_{fit}$	CS to FAULT Pull-Up Propagation Delay	—	340	510		

## Static Electrical Characteristics

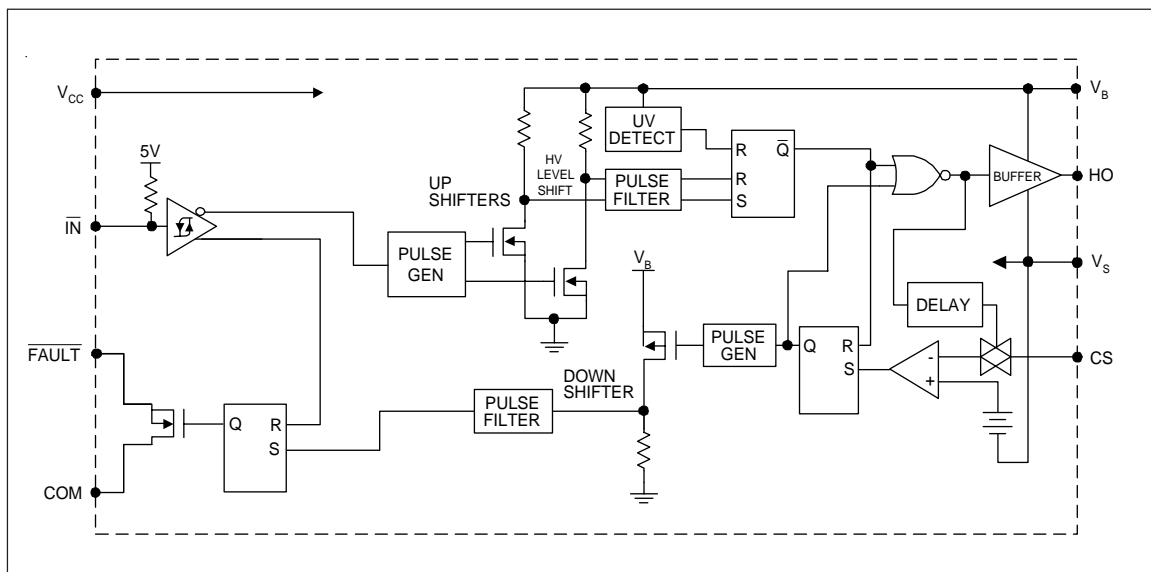
$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 15V and  $T_A$  = 25°C unless otherwise specified. The  $V_{IN}$ ,  $V_{TH}$  and  $I_{IN}$  parameters are referenced to COM. The  $V_O$  and  $I_O$  parameters are referenced to  $V_S$ .

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$V_{IH}$	Logic "1" Input Voltage (IR2127/IR21271)	3.0	—	—	V	$V_{CC} = 10V$ to 20V
$V_{IL}$	Logic "0" Input Voltage (IR2128)	—	—	0.8		
$V_{IL}$	Logic "0" Input Voltage (IR2127/IR21271)	—	—	0.8	mV	
$V_{CS+}$	Logic "1" Input Voltage (IR2128)	—	—	0.8		
$V_{CSTH+}$	CS Input Positive Going Threshold (IR2127/IR2128)	180	250	320	V	
$V_{CSTH+}$	CS Input Positive Going Threshold (IR21271)	—	1.8	—		
$V_{OH}$	High Level Output Voltage, $V_{BIAS} - V_O$	—	—	100	mV	$I_O = 0A$
$V_{OL}$	Low Level Output Voltage, $V_O$	—	—	100		$I_O = 0A$
$I_{LK}$	Offset Supply Leakage Current	—	—	50	$\mu A$	$V_B = V_S = 600V$
$I_{QBS}$	Quiescent $V_{BS}$ Supply Current	—	200	400		$V_{IN} = 0V$ or 5V
$I_{QCC}$	Quiescent $V_{CC}$ Supply Current	—	60	120		$V_{IN} = 5V$
$I_{IN+}$	Logic "1" Input Bias Current	—	7.0	15		$V_{IN} = 0V$
$I_{IN-}$	Logic "0" Input Bias Current	—	—	1.0		$V_{CS} = 3V$
$I_{CS+}$	"High" CS Bias Current	—	—	1.0		$V_{CS} = 0V$
$I_{CS-}$	"High" CS Bias Current	—	—	1.0		
$V_{BSUV+}$	$V_{BS}$ Supply Undervoltage Positive Going Threshold (IR2127/IR2128)	8.8	10.3	11.8		V
$V_{BSUV+}$	$V_{BS}$ Supply Undervoltage Positive Going Threshold (IR21271)	6.3	7.2	8.2		
$V_{BSUV-}$	$V_{BS}$ Supply Undervoltage Negative Going Threshold (IR2127/IR2128)	7.5	9.0	10.6	V	
$V_{BSUV-}$	$V_{BS}$ Supply Undervoltage Negative Going Threshold (IR21271)	6.0	6.8	7.7		
$I_{O+}$	Output High Short Circuit Pulsed Current	200	250	—	mA	$V_O = 0V$ , $V_{IN} = 5V$ $PW \leq 10 \mu s$
$I_{O-}$	Output Low Short Circuit Pulsed Current	420	500	—		$V_O = 15V$ , $V_{IN} = 0V$ $PW \leq 10 \mu s$
Ron, FLT	FAULT - Low on Resistance	—	125	—	$\Omega$	

**Functional Block Diagram IR2127/IR21271**



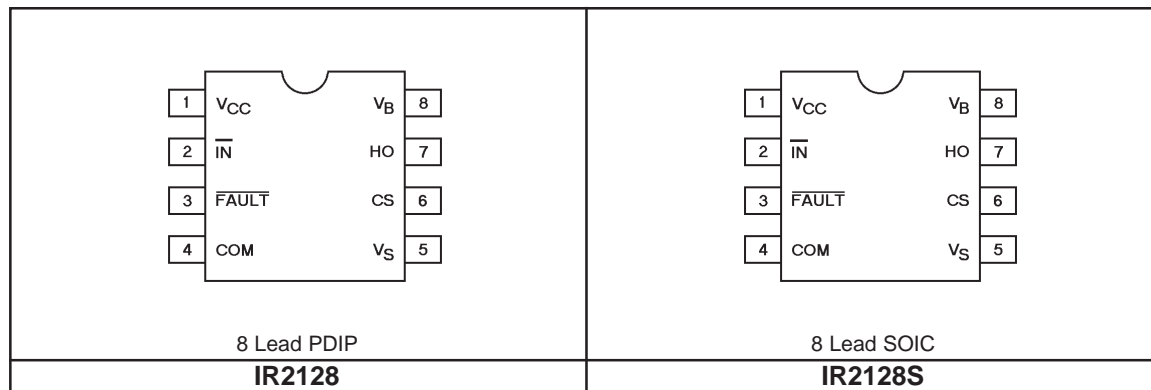
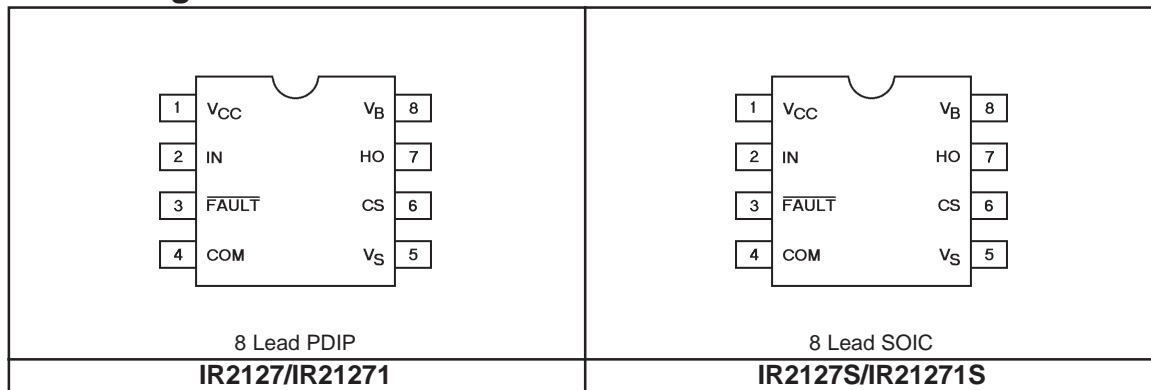
**Functional Block Diagram IR2128**



**Lead Definitions**

Symbol	Description
V <sub>CC</sub>	Logic and gate drive supply
IN	Logic input for gate driver output (HO), in phase with HO (IR2127/IR21271) out of phase with HO (IR2128)
$\overline{\text{FAULT}}$	Indicates over-current shutdown has occurred, negative logic
COM	Logic ground
V <sub>B</sub>	High side floating supply
HO	High side gate drive output
V <sub>S</sub>	High side floating supply return
CS	Current sense input to current sense comparator

**Lead Assignments**



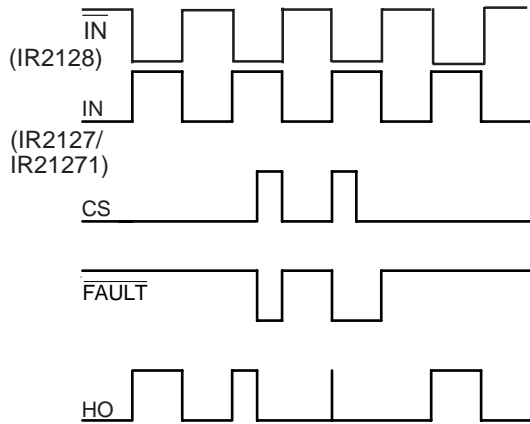


Figure 1. Input/Output Timing Diagram

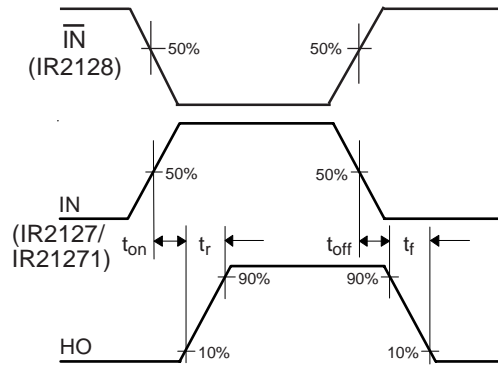


Figure 2. Switching Time Waveform Definition

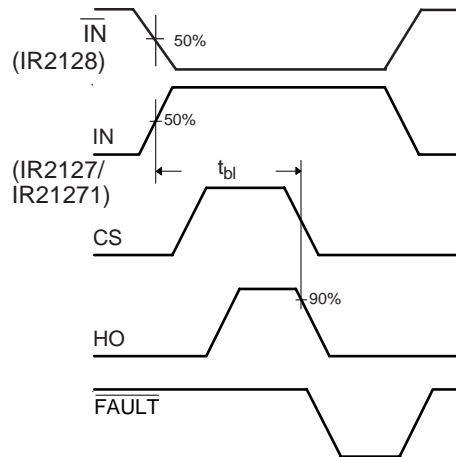


Figure 3. Start-up Blanking Time Waveform Definitions

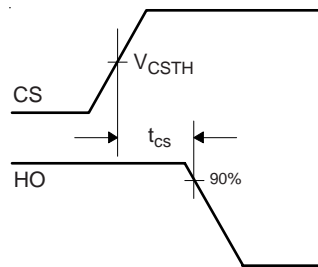


Figure 4. CS Shutdown Waveform Definitions

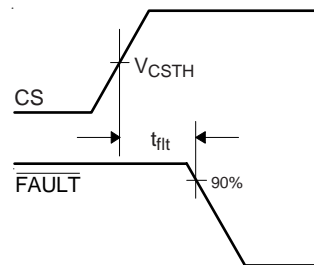


Figure 5. CS to FAULT Waveform Definitions

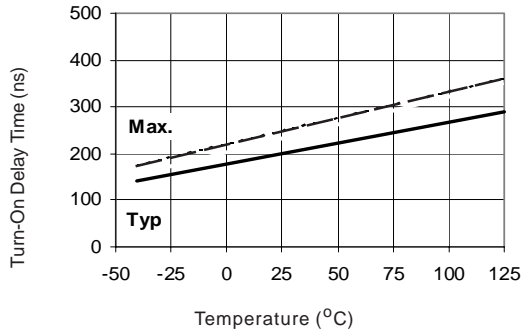


Figure 10A Turn-On Time vs. Temperature

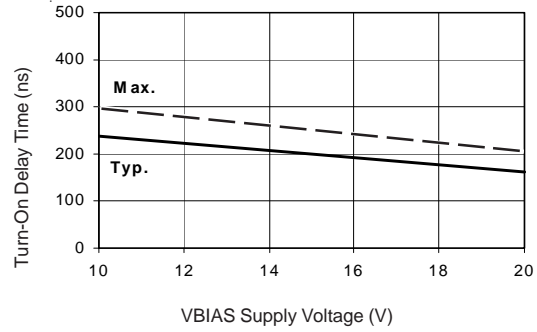


Figure 10B Turn-On Time vs. Supply Voltage

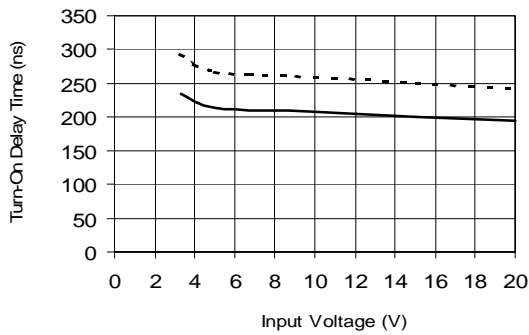


Figure 10C Turn-On Time vs. Input Voltage

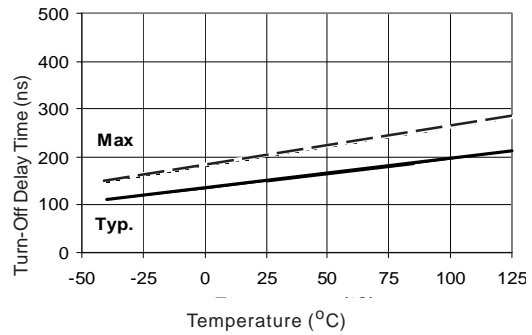


Figure 11A Turn-Off Time vs. Temperature



Figure 11B Turn-Off Time vs. Supply Voltage

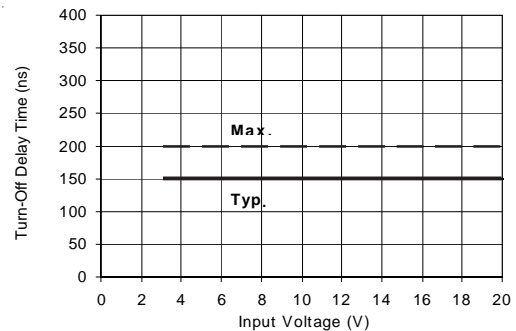


Figure 11C Turn-Off Time vs. Input Voltage



Figure 12A Turn-On Rise Time vs. Temperature

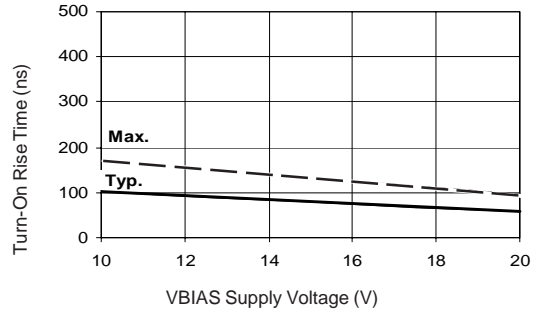


Figure 12B Turn-On Rise Time vs. Supply Voltage

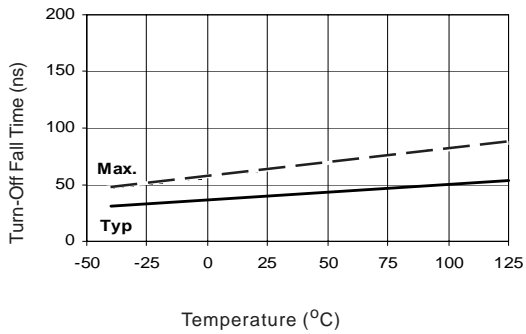


Figure 13A Turn-Off Fall Time vs. Temperature

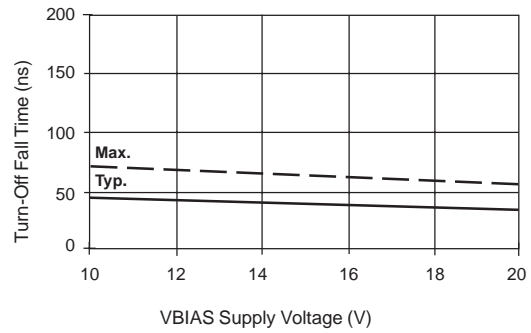


Figure 13B Turn-Off Fall Time vs. Voltage

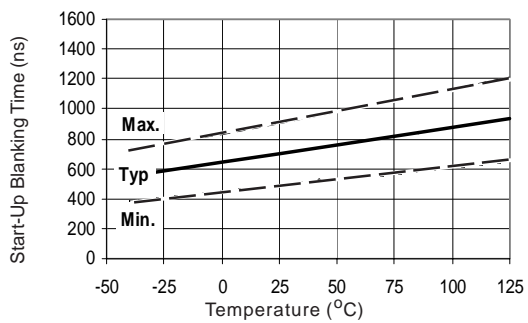


Figure 14A Start-Up Blanking Time vs. Temperature

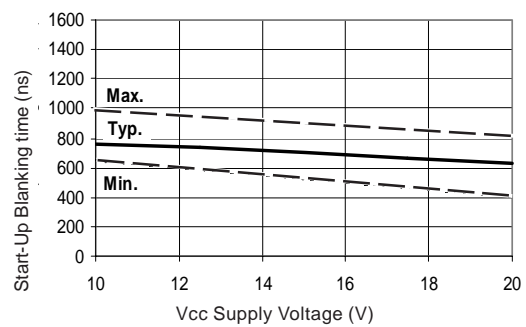


Figure 14B Start-Up Blanking Time vs Voltage



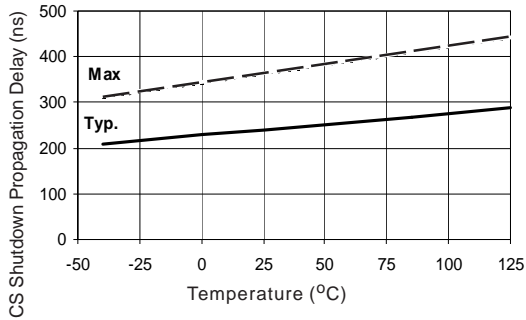


Figure 15A CS Shutdown Propagation Delay vs. Temperature

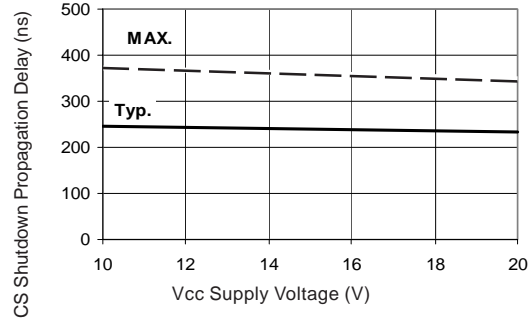


Figure 15B CS Shutdown Propagation Delay vs. Voltage

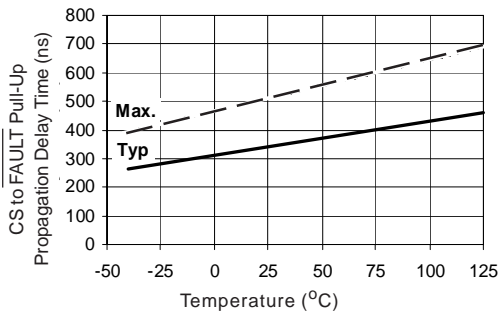


Figure 16A CS to  $\overline{\text{FAULT}}$  Pull-Up Propagation Delay vs. Temperature

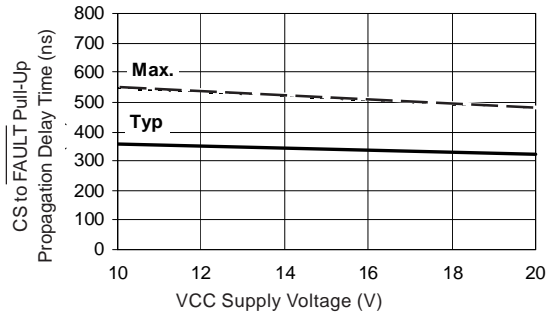


Figure 16B CS to  $\overline{\text{FAULT}}$  Pull-Up Propagation Delay vs. Voltage

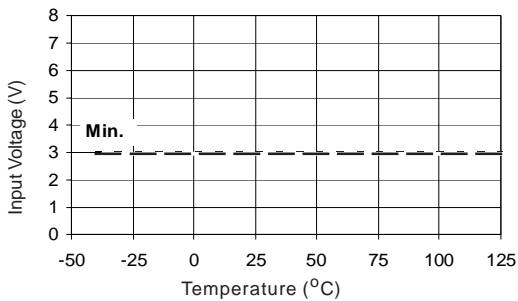


Figure 17A Logic "1" Input Voltage (IR2127)  
 Logic "0" Input Voltage (IR2128)  
 vs Temperature

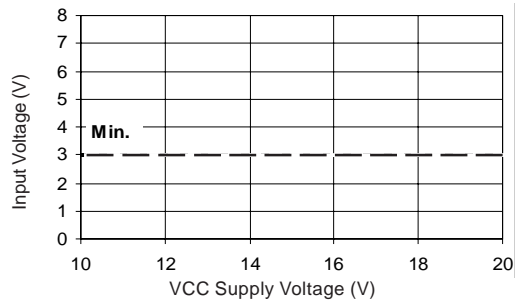
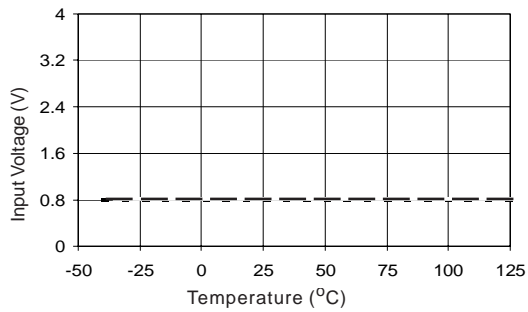
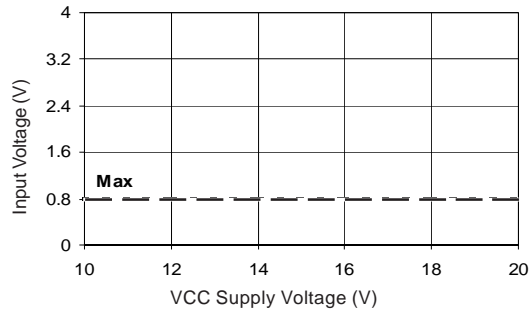


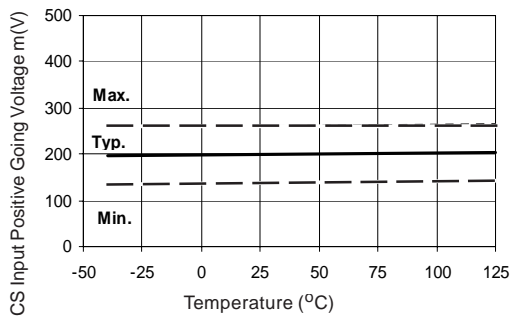
Figure 17B Logic "1" Input Voltage (IR2127)  
 Logic "0" Input Voltage (IR2128)  
 vs Voltage



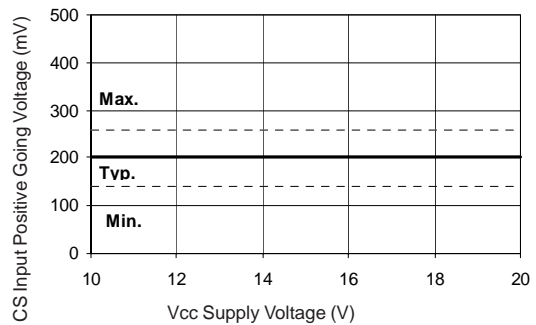
**Figure 18A Logic "0" Input Voltage (IR2127)  
 Logic "1" Input Voltage (IR2128)  
 vs Temperature**



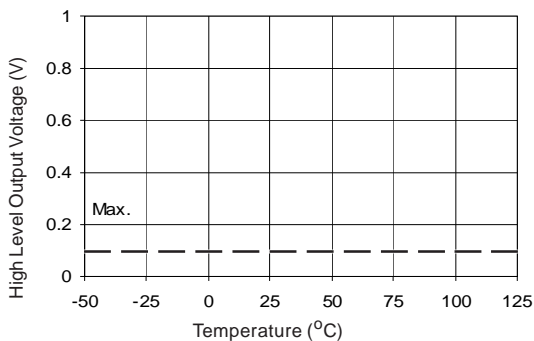
**Figure 18B Logic "0" Input Voltage (IR2127)  
 Logic "1" Input Voltage (IR2128)  
 vs Voltage**



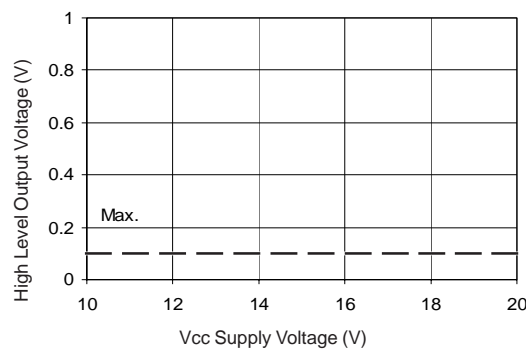
**Figure 19A CS Input Positive Going Voltage  
 vs Temperature (IR2127/IR2128)**



**Figure 19B CS Input Positive Going Voltage  
 vs Voltage (IR2127/IR2128)**



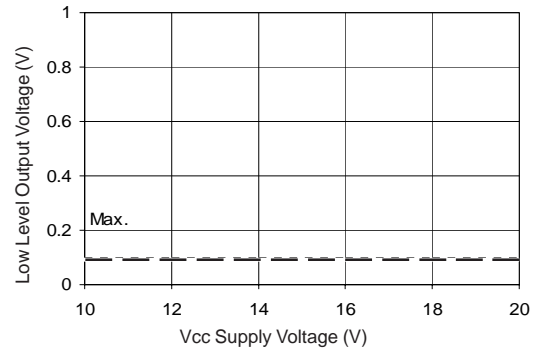
**Figure 20A High Level Output vs Temperature**



**Figure 20B High Level Output vs Voltage**



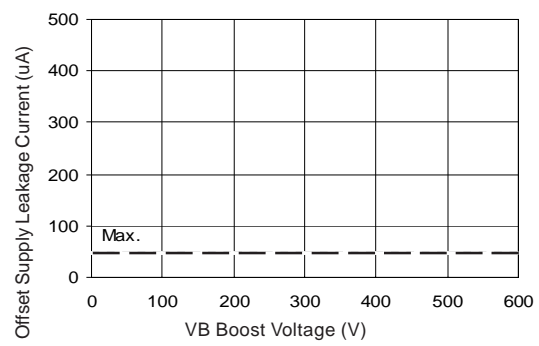
**Figure 21A Low Level Output vs Temperature**



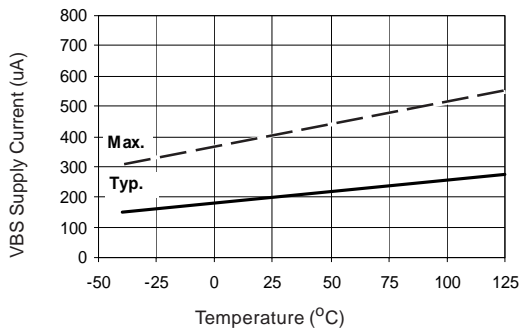
**Figure 21B Low Level Output vs Voltage**



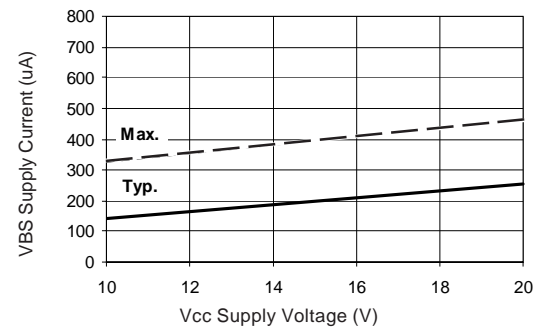
**Figure 22A Offset Supply Current vs Temperature**



**Figure 22B Offset Supply Current vs Voltage**



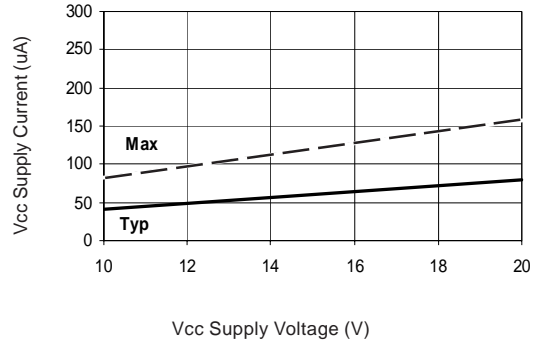
**Figure 23A VBS Supply Current vs Temperature**



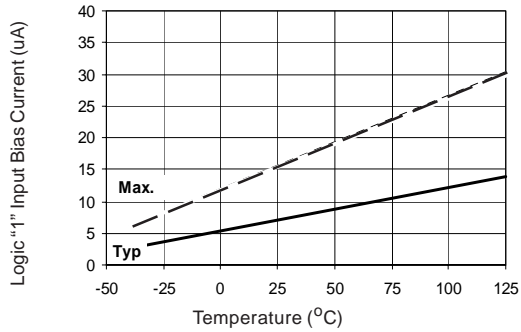
**Figure 23B VBS Supply Current vs Voltage**



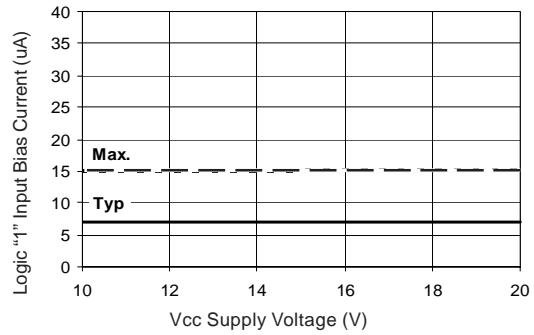
**Figure 24A Vcc Supply Current vs Temperature**



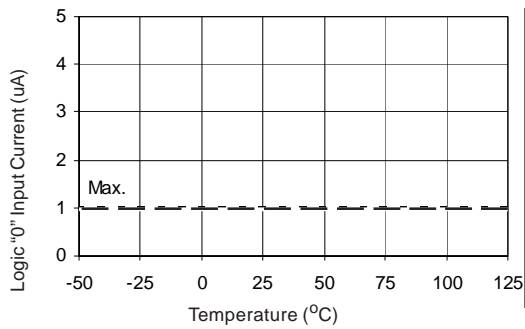
**Figure 24B Vcc Supply Current vs Voltage**



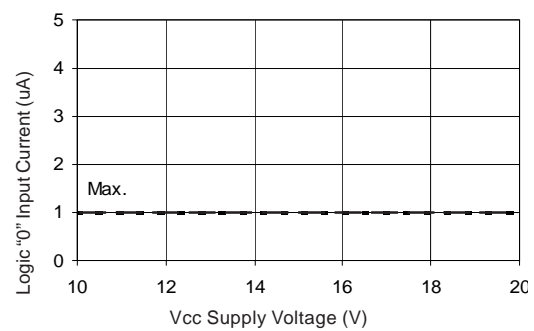
**Figure 25A Logic "1" Input Current vs Temperature**



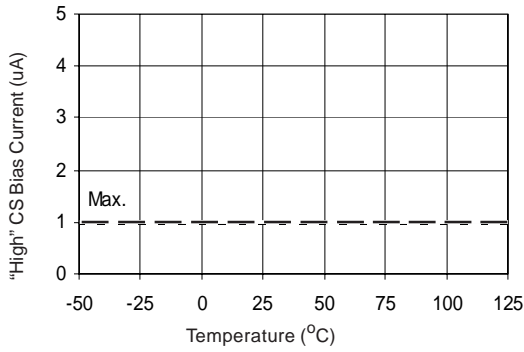
**Figure 25B Logic "1" Input Current vs Voltage**



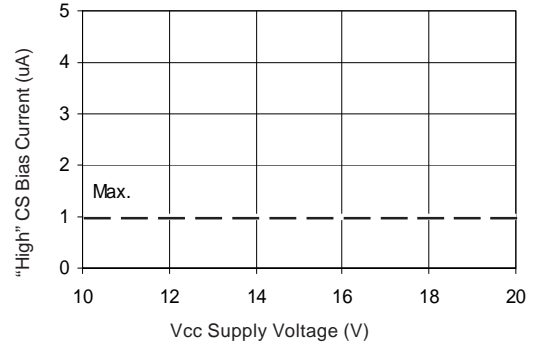
**Figure 26A Logic "0" Input Current vs Temperature**



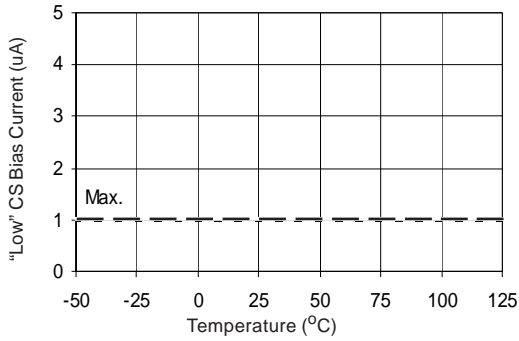
**Figure 26B Logic "0" Input Current vs Voltage**



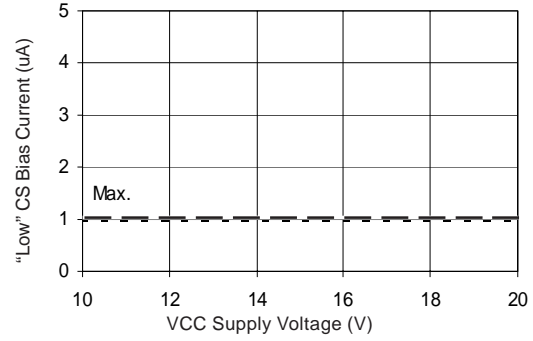
**Figure 27A "High" CS Bias Current vs Temperature**



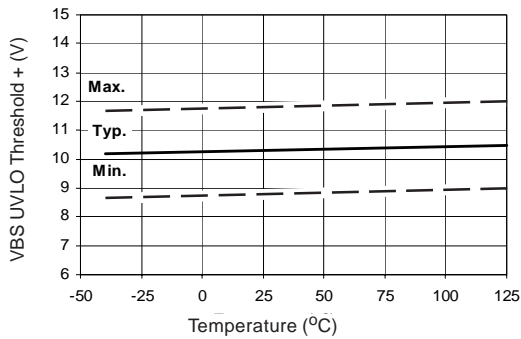
**Figure 27B "High" CS Bias Current vs Voltage**



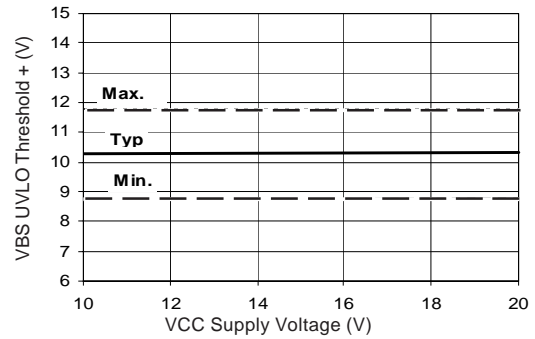
**Figure 28A "Low" CS Bias Current vs Temperature**



**Figure 28B "Low" CS Bias Current vs Voltage**



**Figure 29A VBS Undervoltage Threshold (+) vs Temperature (IR2127/IR2128)**



**Figure 29B VBS Undervoltage Threshold (+) vs Voltage (IR2127/IR2128)**

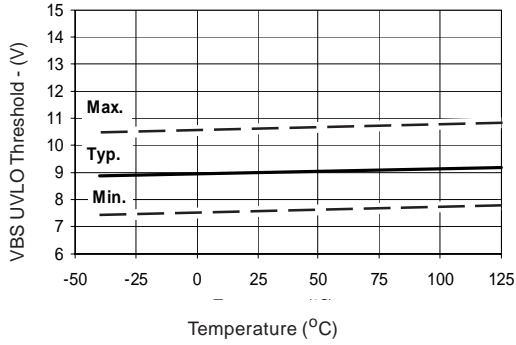


Figure 30A VBS Undervoltage Threshold (-) vs Temperature (IR2127/IR2128)

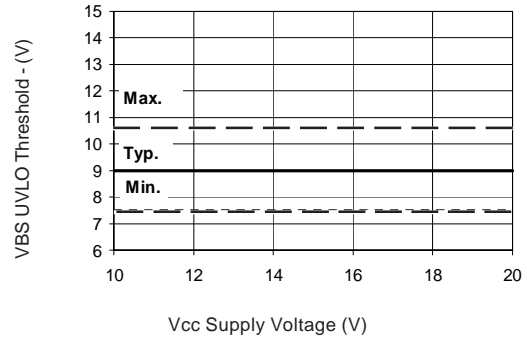


Figure 30B VBS Undervoltage Threshold (-) vs Voltage (IR2127/IR2128)

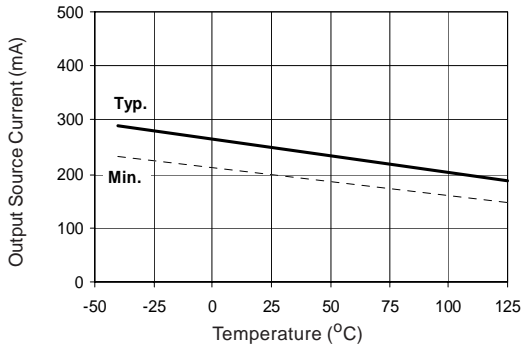


Figure 31A Output Source Current vs Temperature



Figure 31B Output Source Current vs Voltage

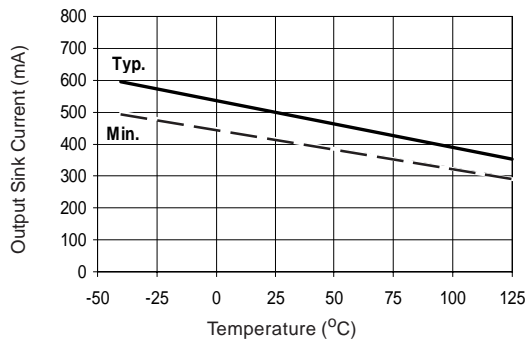


Figure 32A Output Sink Current vs Temperature

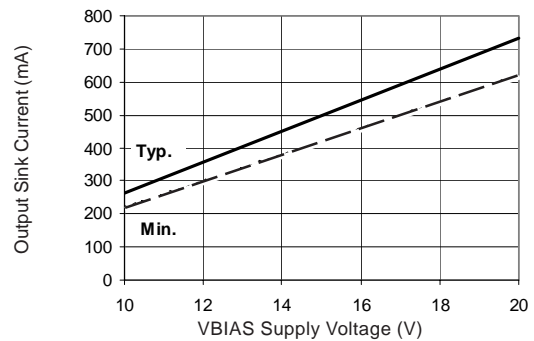
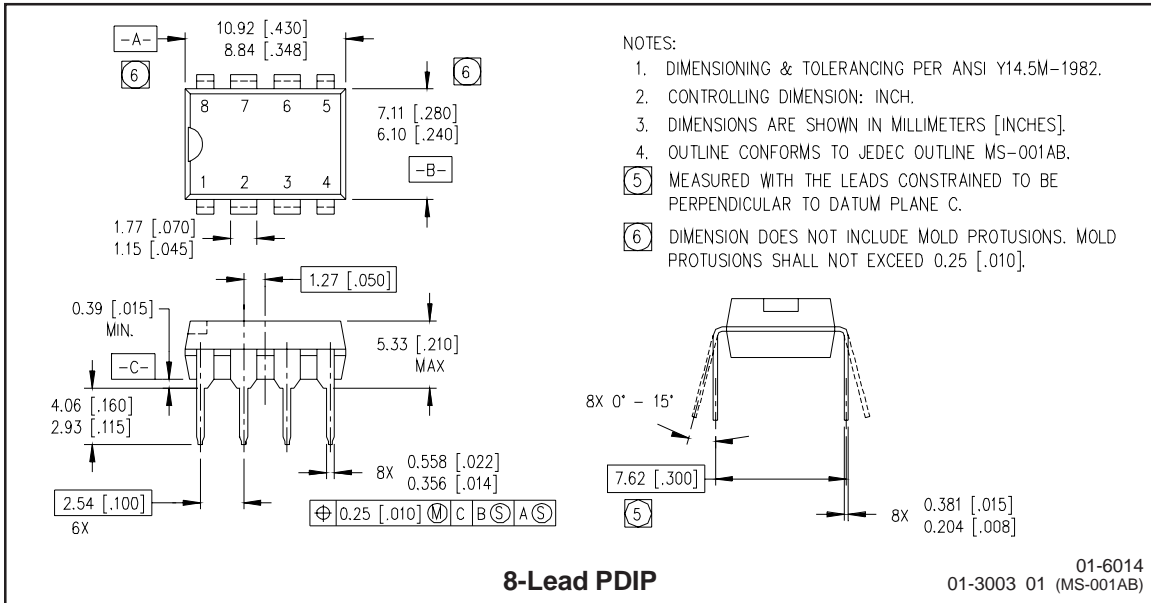
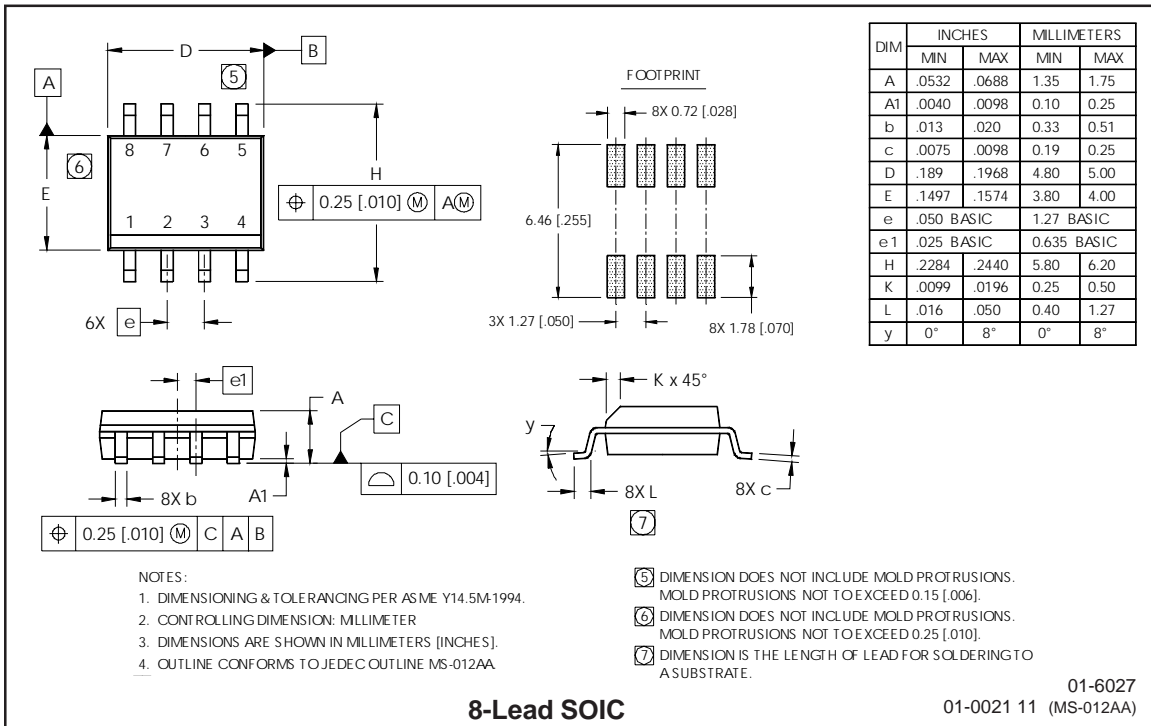


Figure 32B Output Sink Current vs Voltage

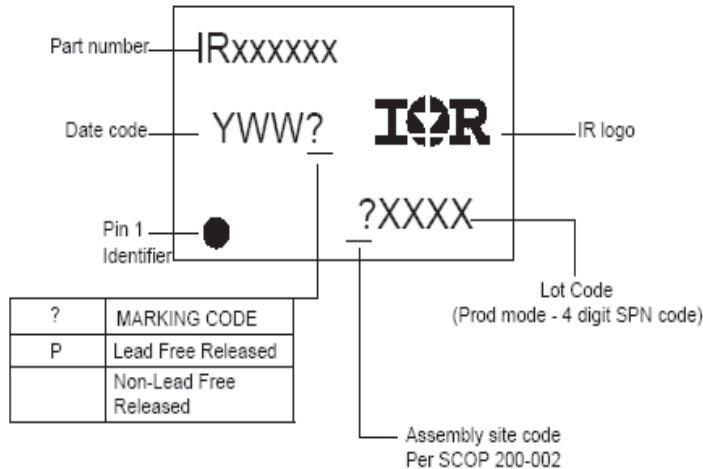
**Case outlines**



- NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
  4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AB.
  - ⑤ MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
  - ⑥ DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].



**LEADFREE PART MARKING INFORMATION**



**ORDER INFORMATION**

**Basic Part (Non-Lead Free)**

8-Lead PDIP IR2127 order IR2127  
 8-Lead SOIC IR2127S order IR2127S  
 8-Lead PDIP IR21271 order IR21271  
 8-Lead SOIC IR21271S order IR21271S  
 8-Lead PDIP IR2128 order IR2128  
 8-Lead SOIC IR2128S order IR2128S

**Lead-Free Part**

8-Lead PDIP IR2127 order IR2127PbF  
 8-Lead SOIC IR2127S order IR2127SPbF  
 8-Lead PDIP IR21271 order IR21271PbF  
 8-Lead SOIC IR21271S order IR21271SPbF  
 8-Lead PDIP IR2128 order IR2128PbF  
 8-Lead SOIC IR2128S order IR2128SPbF