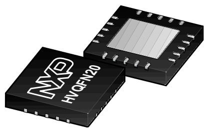


BGA3131

DOCSIS 3.1 upstream amplifier

Rev. 1 — 13 May 2016 **Product data sheet**

1. General description

The BGA3131 is an upstream amplifier meeting the Data Over Cable Service Interface Specifications (DOCSIS 3.1). It is designed for cable modem, CATV set top box and VoIP modem applications. The device operates from 5 MHz to 205 MHz. The BGA3131 provides 58 dB gain control range in 1 dB increments with high incremental accuracy. Its maximum gain setting delivers 37 dB voltage gain and a superior linear performance.

It supports the DOCSIS 3.1 output power levels while meeting the stringent ACLR requirements.

The BGA3131 operates at 5 V supply. The gain is controlled via a 3-wire serial interface (SPI-Bus). The current consumption can be reduced in 4 steps via the serial interface. This interface enables the user to optimize between DC power efficiency and linearity. In addition, the current is automatically reduced at lower gain settings while preserving the linearity performance. In disable mode, the device draws typically 25 mA while it can be still programmed to new gain and current settings.

The BGA3131 is housed in 20 pins 5 mm × 5 mm leadless HVQFN package.

2. Features and benefits

- 58 dB gain control range in 1 dB steps using a 3-wire serial interface
- 5 MHz to 205 MHz frequency operating range
- ± 0.4 dB incremental gain step accuracy
- Maximum voltage gain 37 dB
- Excellent IMD3 of –60 dBc at 68 dBmV total output power
- Excellent second harmonic level of –60 dBc at 68 dBmV total output power
- Excellent third harmonic level of –60 dBc at 68 dBmV total output power
- Excellent noise figure of 6.5 dB at maximum gain
- Capable of transmitting modulated carriers while meeting the DOCSIS 3.1 ACLR specification. At an output power of 65 dBmV at the F-connector (assuming 3 dB of output loss), the typical ACLR is–64 dBc
- 5 V single supply operation
- Excellent ESD protection at all pins
- Unconditionally stable
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

3. Applications

- DOCSIS 3.1 and 3.0 cable modems
- VoIP modems
- Set-top boxes

4. Quick reference data

Table 1. Quick reference data

Typical values at V_{CC} = 5 V; current setting = 3 mA; gain setting 50 up to and including 63; T_{case} = 25 °C; $Z_{i(dif)}$ = 200 Ω; $Z_{o(se)}$ = 75 Ω; voltage gain does include loss due to output transformer; unless otherwise specified. All RF parameters are measured on an application board with the circuit as shown in Figure 12 and components implemented as listed in Table 15.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}	supply current	transmit-enable mode; TX_EN = HIGH	610	660	720	mA
		transmit-disable mode; TX_EN = LOW	-	25	-	mA
G_v	voltage gain	gain code = 111111 [1][2]	-	37	-	dB
NF	noise figure	transmit-enable mode; gain code = 111111	-	6.5	-	dB
α_{2H}	second harmonic level	transmit-enable mode; gain code = 111111; P_i(RMS) = 31.0 dBmV; P_L(RMS) = 68.0 dBmV into 75 Ω impedance	-	−65	-	dBc
α_{3H}	third harmonic level	transmit-enable mode; gain code = 111111; P_i(RMS) = 31.0 dBmV; P_L(RMS) = 68.0 dBmV into 75 Ω impedance	-	−65	-	dBc
IMD3	third-order intermodulation distortion	transmit-enable mode; gain code = 111111; P_L(RMS) = 65.0 dBmV per tone into 75 Ω impedance	-	−60	-	dBc
$P_{L(1dB)}$	output power at 1 dB gain compression	CW input signal RMS value; frequency = 205 MHz	-	78	-	dBmV

[1] P_i <= 30 dBmV.

[2] Excluding 5.7 dB loss of resistive matching circuit, to match 75 Ω to 50 Ω.

Table 2. ACLR quick reference data

Typical values at V_{CC} = 5 V; current setting = 3 mA; Gain setting 60; T_{case} = 25 °C; $Z_{i(dif)}$ = 200 Ω; $Z_{o(se)}$ = 75 Ω; channel bandwidth = 192 MHz; integration bandwidth = 9.6 MHz; f = 5 MHz to 205 MHz; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DOCSIS 3.1						
ACLR	adjacent channel leakage ratio	P_i(RMS) = 34 dBmV; P_L(RMS) = 68 dBmV. Channel configuration: channel bandwidth is 192 MHz, with exclusion band at 147.5 MHz; with a bandwidth of 9.6 MHz. Input signal with a PAPR of 13 dB	-	−64	−58	dBc

5. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BGA3131	HVQFN20	plastic thermal enhanced very thin quad flat package; no leads; 20 terminals; body 5 × 5 × 0.85 mm	SOT662-1

6. Functional diagram

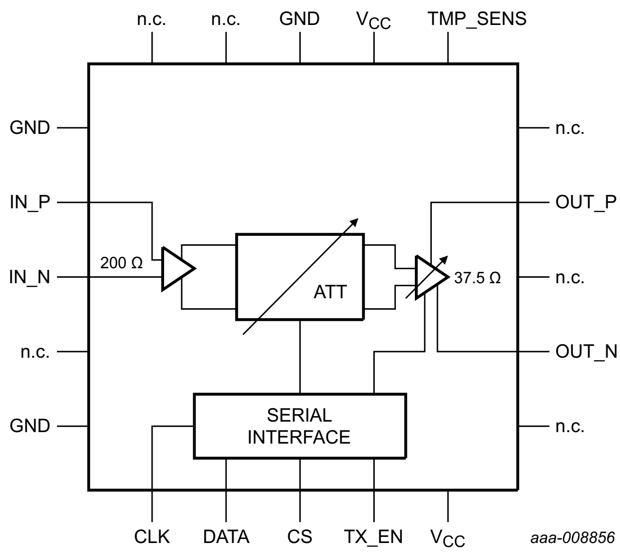


Fig 1. Functional diagram

7. Pinning information

7.1 Pinning

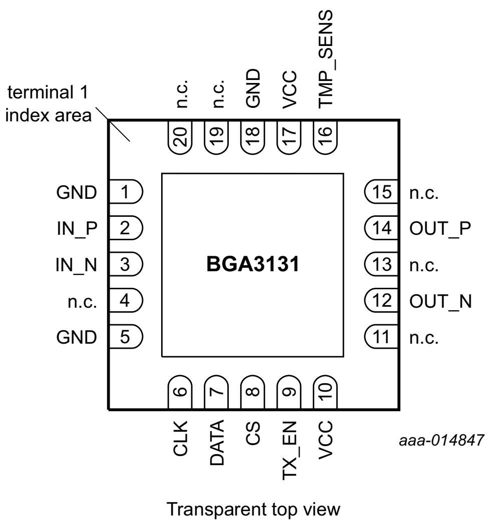


Fig 2. Pin configuration

7.2 Pin description

Table 4. Pin description

Symbol	Pin	Description
GND	1	ground
IN_P	2	amplifier input +
IN_N	3	amplifier input –
n.c. [1]	4	not connected
GND	5	ground
CLK	6	clock
DATA	7	data
CS	8	chip select
TX_EN	9	transmit enable active high
V_{CC}	10	supply voltage
n.c. [1]	11	not connected
OUT_N	12	amplifier output –
n.c. [1]	13	not connected, pin can be left open, grounded or connected to the center tap voltage in the application
OUT_P	14	amplifier output +
n.c. [1]	15	not connected
TMP_SENS	16	temperature sense
V_{CC}	17	supply voltage
GND	18	ground
n.c. [1]	19	not connected
n.c. [1]	20	not connected
GND	die paddle	ground

[1] not connected pins can either be left open or grounded in the application.

8. Functional description

8.1 Logic programming

The programming word is set through a shift register. It uses the data of the SPI bus (pin name DATA), clock (pin name CLK), and enable (pin name TX_EN) lines. By default, the data is entered in order with the most significant bit (MSB) first and the least significant bit (LSB) last. The Chip Select line (CS) must be low during the data entry, then set high to sample the shift register. The rising edge of the clock pulse shifts each data value into the shift register. When the register is programmed, the new settings take effect:

- on the rising, edge of CS, IF TX_EN is HIGH
- on the rising, edge of TX_EN if TX_EN is LOW

Table 5. Programming register

Data bit	11	10	9	8	7	6	5	4	3	2	1	0
Function	**Register address**				**Current settings[1]**		**attenuation (gain) settings[2]**					
Settings	0	0	0	0	C[1]	C[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]
Initialize	0	0	0	1	Soft reset (mirror)	LSB first (mirror)	ASC address (mirror)	16b mode (mirror)	16b mode	ASC address	LSB first	Soft reset
Reserved	0	0	1	0	0	0	0	0	0	0	0	0
Reserved	0	0	1	1	0	0	0	0	0	0	0	0

[1] For current bit settings, see Table 7.

[2] For gain bit settings, see Table 6.

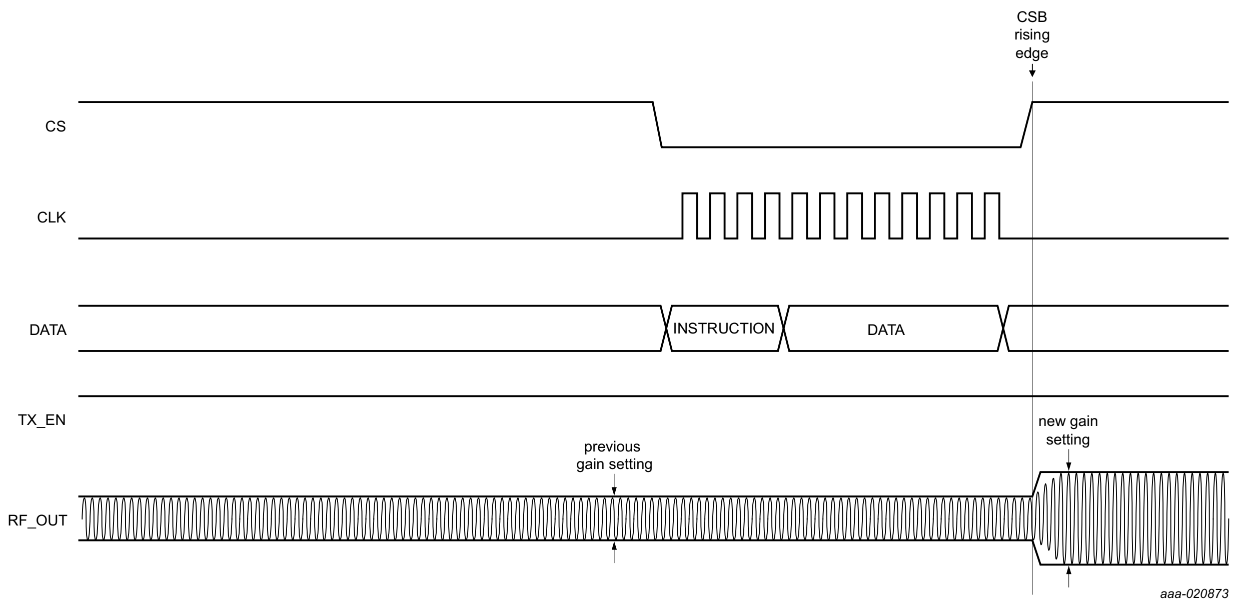


Fig 3. Serial data input timing when TX_EN is HIGH

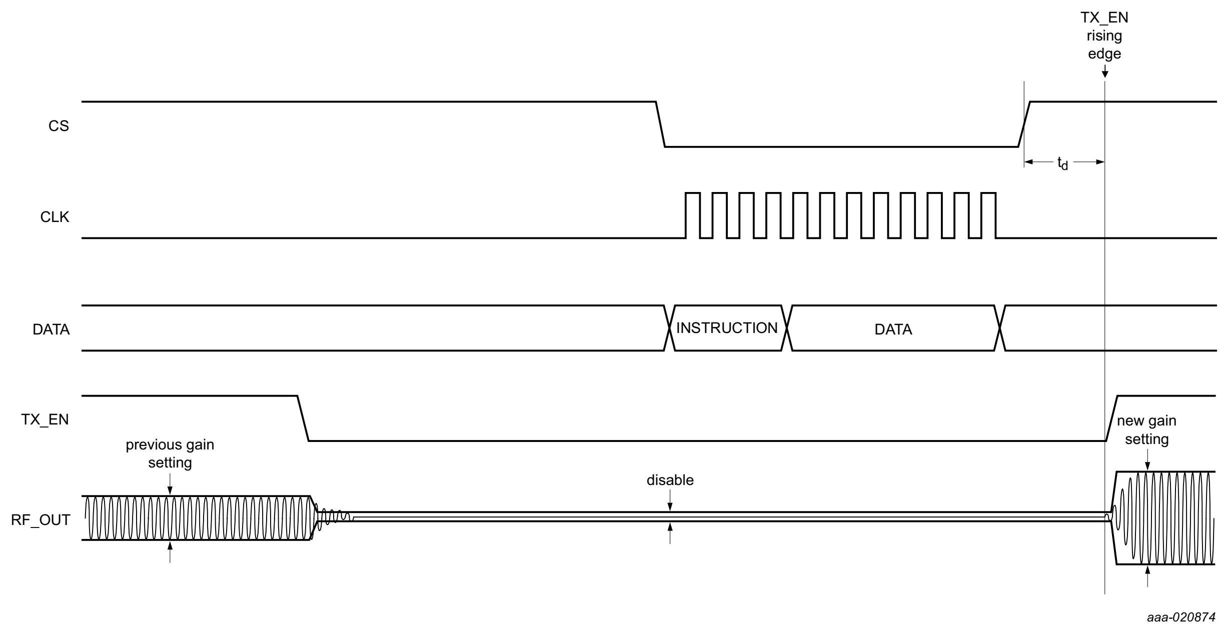


Fig 4. Serial data input timing when TX_EN is LOW

8.2 Register settings

8.2.1 Register address

Only addresses 0000 to 0011 are used. Using any other addresses do not affect the VGA. Address 0000 is used to configure attenuation and current parameters of the device. Address 0001 is used to configure the SPI interface specifically. Addresses 0010 and 0011 are reserved, and must be kept at value 0.

8.2.2 Gain/attenuator setting

The gain shall be controlled via the SPI bus. Data bits D0 through D5 set the gain/attenuator level, with 111111 being the min attenuation setting, and 000101 being the maximum attenuation setting. A new gain/attenuator setting can be loaded while the VGA is on (transmit-enable).

Table 6. Gain settings

Gain setting G[5:0][1]		Typical gain
binary notation	decimal notation	(dB)
000000 to 000101	0 to 5	–21
000110	6	–20
111110	62	36
111111	63	37

[1] With every increment of the gain setting between 000101 (5) and 111111 (63), the typical gain increases accordingly.

8.2.3 Output stage current setting

The current (of the output stage) shall be controlled via the 3-wire bus. Data bits D6 and D7 set the current. Setting 11 sets the maximum current for maximum linearity. The current can be lowered for improved efficiency at lower output power levels, or lower linearity requirements. Setting 00 sets the minimum current. A new current setting can be loaded while the VGA is on (transmit-enable).

Table 7. Supply current settings

At gain setting 63.

Current setting C[1:0]		Typical supply current
binary notation	**decimal notation**	**(mA)**
00	0	350
01	1	410
10	2	480
11	3	660

The current is automatically reduced at lower gain settings while preserving the linearity performance.

Table 8. Device current setting versus gain setting

Gain setting		Typical current (mA)				
Attenuation bit [5.0]	**H value**	**Current setting C[1:0] = 00**	**Current setting C[1:0] = 01**	**Current setting C[1:0] = 10**	**Current setting C[1:0] = 11**	**Comments**
111111	0x3F	315	410	480	660	Max.gain (code = 63)
110001	0x31	280	315	345	370	Gain code = 49
101011	0x2B	290	320	350	375	Gain code = 43
100101	0x25	240	260	260	330	Gain code = 37
011001	0x19	220	235	235	250	Gain code = 25

8.2.4 SPI Initialize register

The SPI receiver may be configured in several communication modes. By default, the device is waiting for a 12 bit, MSB first SPI frame. In that case, the address field is 4 bit wide and the data field is 8 bit wide. Using the Initialize register at address 0x01 allows switching the device to different SPI modes. Register 0x01 contains four effective bits, but programmed with the mirror value of the 4 LSBs in the 4 MSBs.

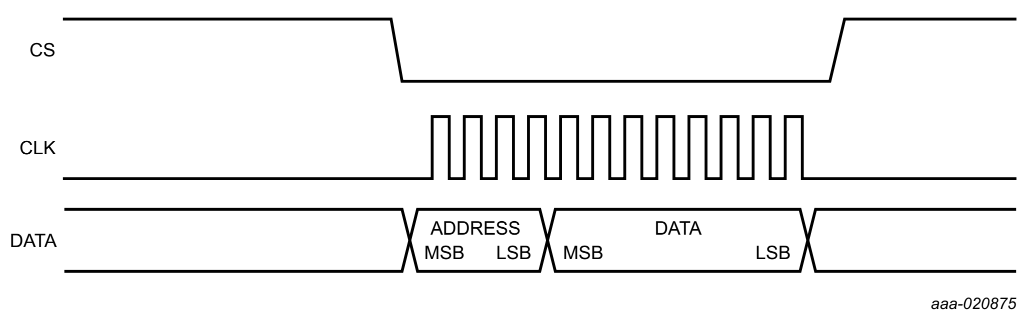


Fig 5. Default SPI frame, 12 bit, MSB first, descending address

8.2.4.1 SPI Soft Reset

By setting bits *Soft_reset AND Soft_reset (mirror)* at address 0x01, the device is set to its default state (maximum gain).

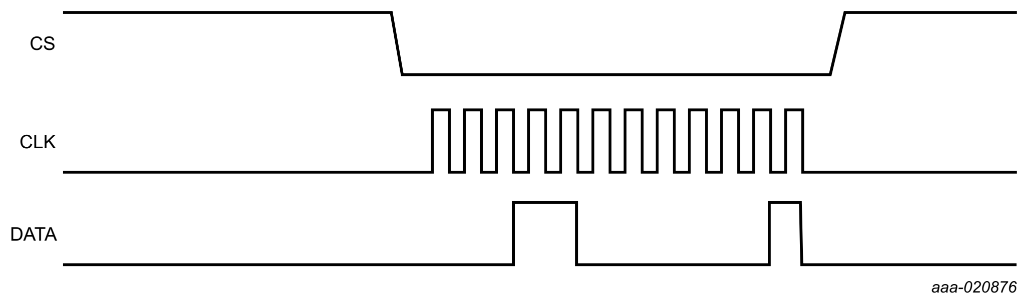


Fig 6. SPI frame for Soft Reset, 12 bit, MSB first, descending address

8.2.4.2 SPI 16-bit mode

By default, the SPI frame is made of 4 bits for address and a multiple of 8 bits for data. By setting bits 16b_mode AND 16b_mode (mirror) at address 0x01, the device is configured such that the next SPI command will be a 16-bit command. Address is sent on 8 bits, whereas data is a multiple of 8 bits.

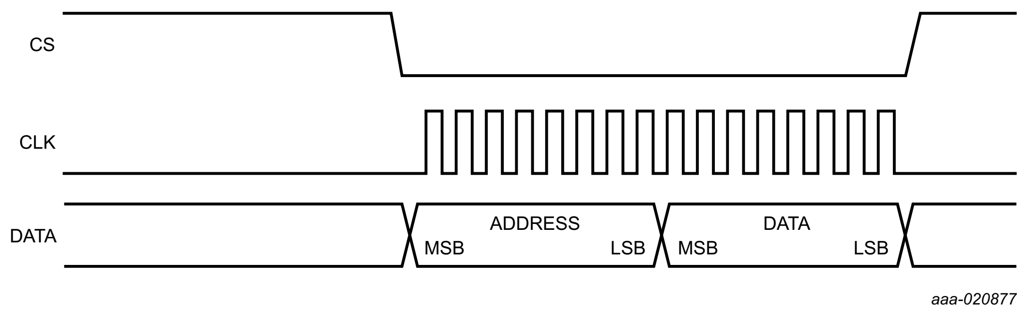


Fig 7. Default SPI frame, 16 bit, MSB first, descending address

8.2.4.3 SPI ascending address

By default, the SPI slave can be programmed with a single SPI frame. The SPI contains a start address and several data bytes to be written at the start address. It has an auto decrementing mechanism to store data in the corresponding register. By setting bits *asc_addr* AND *asc_addr (mirror)* at address 0x01, the device is configured so that the internal addresses are auto-incremented instead of auto-decremented.

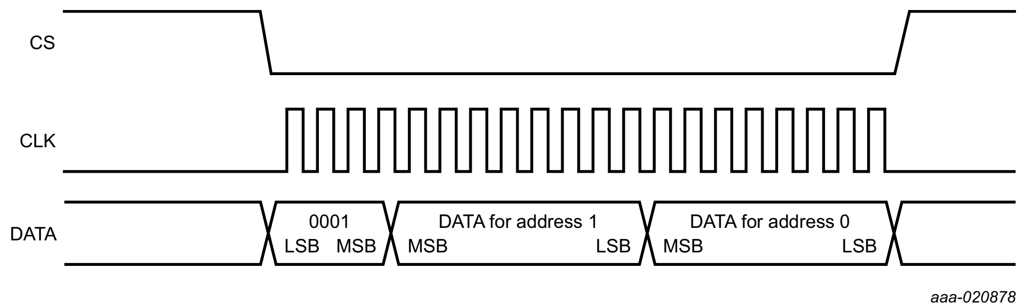


Fig 8. Burst SPI frame, 12 bit, MSB first, descending address

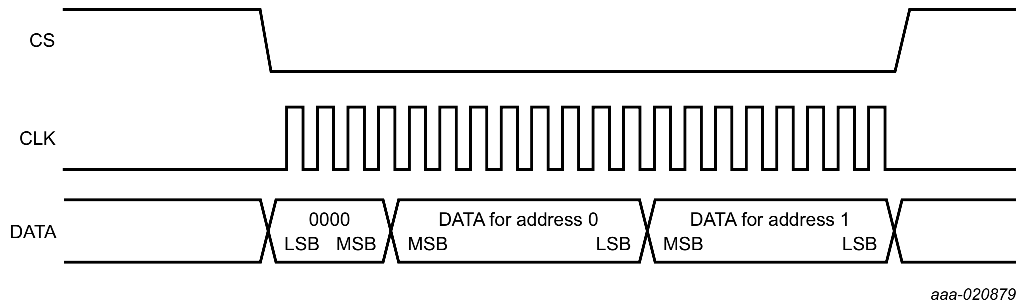


Fig 9. Burst SPI frame, 12 bit, MSB first, ascending address

8.2.4.4 SPI LSB first

By default, the SPI slave waits for the MSB data first. By setting bits *lsb_first* AND *lsb_first (mirror)* at address 0x01, the device is configured. The first bit received is considered as the LSB of each field (address and data).

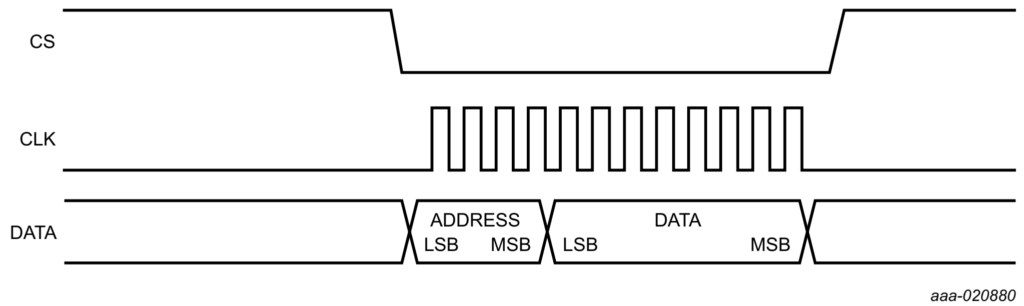


Fig 10. Burst SPI frame, 12 bit, MSB first, descending address

8.3 TX enable / TX disable

The amplifier can be disabled or enabled by making TX_EN (pin 9) LOW or HIGH. A LOW to HIGH TX enable transition enables new programmed settings. If no new settings are programmed, the last programmed setting is reactivated.

9. Limiting values

Table 9. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).
Absolute maximum ratings are given as limiting values of stress conditions during operation, that must not be exceeded under the worst probable conditions.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-	6.0	V
I_i	input current	on pin TMP_SENS		-	1	mA
V_i	input voltage	on pin IN_P		–0.5	+6.0	V
		on pin IN_N		–0.5	+6.0	V
		on pin CLK	[1]	–0.5	+6.0	V
		on pin DATA	[1]	–0.5	+6.0	V
		on pin CS	[1]	–0.5	+6.0	V
		on pin TX_EN	[1]	–0.5	+6.0	V
		on pin OUT_N		–0.5	+6.0	V
		on pin OUT_P		–0.5	+6.0	V
$P_{i(max)}$	maximum input power			-	60	dBmV
T_{stg}	storage temperature			–55	+150	°C
T_j	junction temperature			-	150	°C
V_{ESD}	electrostatic discharge voltage	Human Body Model (HBM); according to JEDEC standard 22-A114E	[2]	-	±4	kV
		Charged Device Model (CDM); according to JEDEC standard 22-C101B	[2]	-	±2	kV
f_{SPI}	SPI frequency	Master writes to slave; load on DATA line 30 pF maximum. Under nominal V_{IL} and V_{IH} levels		-	25	MHz

[1] All digital pins must not exceed V_{CC} as the internal ESD circuit can be damaged. To prevent this damage, it is recommended that control pins are limited to a maximum of 5 mA.

[2] Stressed with pulses of 200 ms in duration.

10. Thermal characteristics

Table 10. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-bop)}$	thermal resistance from junction to bottom of package	Still air, natural convection	[1]	6.1	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Still air, natural convection	[1]	29.3	K/W
$\Psi_{(j-top)}$	thermal characterization parameter from junction to top of package	Still air, natural convection	[1]	9.9	K/W

[1] Simulated using final element method model resembling the device mounted on the application board. See Figure 13.

For more thermal details, refer to the BGA3131 *Thermal management guidelines AN11753* at www.nxp.com.

10.1 Thermal compact model

Compact thermal model parameters (Delphi compact model), definitions according to Figure 11

Table 11. Delphi model parameters[1]

R_{th} (K/W)	junction	top inner	top outer	bottom inner	bottom outer	sides	leads	surface areas [mm^2]
junction		201		6.17				
top inner			1207	543	1330			4.27
top outer				114	60.4		222	20.7
bottom inner					53.8	315	311	9.53
bottom outer							37.8	12.6
sides							101	17.0
leads								2.85

[1] Cells are intentionally left empty.

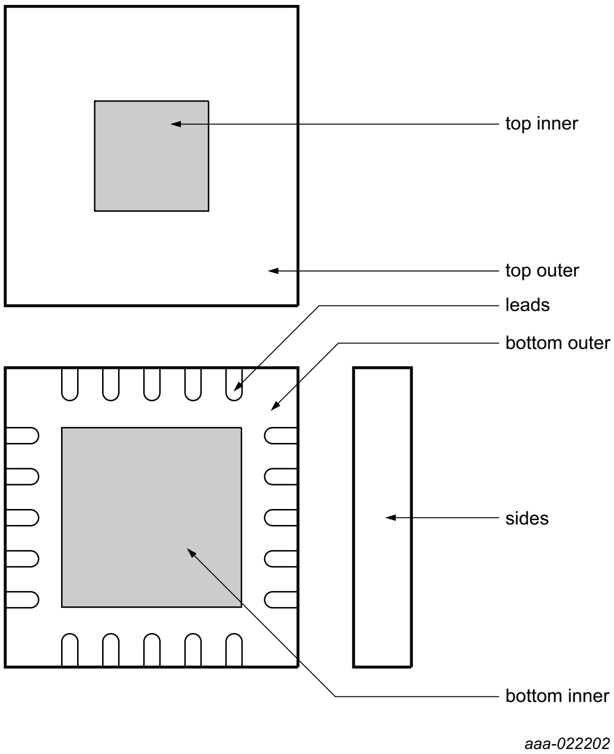


Fig 11. Delphi compact model definition

11. Static characteristics

Table 12. Characteristics

Typical values at V_{CC} = 5 V; current setting = 3 mA; gain setting 50 up to and including 63; T_{case} = 25 °C; $Z_{i(dif)}$ = 200 Ω; $Z_{o(se)}$ = 75 Ω; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.75	5.0	5.25	V
I_{CC}	supply current	transmit-enable mode; TX_EN = HIGH	610	660	720	mA
		transmit-disable mode; TX_EN = LOW	-	25	-	mA
V_{IH}	HIGH-level input voltage	[1]	1.8	-	V_{CC} + 0.6	V
V_{IL}	LOW-level input voltage	[1]	0	-	0.8	V
P	power dissipation		-	3.3		W

[1] Voltage on the control pins.

12. Dynamic characteristics

Table 13. Characteristics

Typical values at V_{CC} = 5 V; current setting = 3 mA; gain setting 15 up to and including 63; T_{case} = 25 °C; $Z_{i(dif)}$ = 200 Ω; $Z_{o(se)}$ = 75 Ω; voltage gain does include loss due to output transformer; unless otherwise specified. All RF parameters are measured on an application board with the circuit as shown in Figure 12 and components implemented as listed in Table 15.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_v	voltage gain	gain code = 111111 [1][2]	-	37	-	dB
		gain code = 001111 [1][2]	-	–11	-	dB
G_{flat}	gain flatness	f = 5 MHz to 205 MHz [1]	-	± 0.5	-	dB
RL_{out}	output return loss	transmit mode enable over all gain settings, measured in 75 Ω system	-	14	-	dB
		transmit mode disable over all gain settings, measured in 75 Ω system	-	12	-	dB
RL_{in}	input return loss	transmit mode enable overall gain settings, measured in 200 Ω system	-	20	-	dB
		transmit modes disable overall gain settings, measured in 200 Ω system	-	20	-	dB
G_{step}	gain step	[1]	-	1.0	-	dB
$E_{G(dif)}$	differential gain error	[1]	-	± 0.4	-	dB
$R_{i(dif)}$	differential input resistance		-	200	-	Ω
$R_{o(dif)}$	differential output resistance		-	37.5	-	Ω
f_{range}	frequency range		5	-	205	MHz
α_{isol}	isolation	transmit-disable mode; TX_EN = LOW; f = 205 MHz	-	60	-	dB
NF	noise figure	transmit mode; gain code = 111111	-	6.5	-	dB
		transmit mode; gain code = 100110	-	15	-	dB
$t_{sw(G)}$	gain switch time	transmit-disable/transmit-enable transient duration	-	3.0	-	µs
		transmit-enable/transmit-disable transient duration	-	0.5	-	µs

Table 13. Characteristics *...continued*

Typical values at V_{CC} = 5 V; current setting = 3 mA; gain setting 15 up to and including 63; T_{case} = 25 °C; $Z_{i(dif)}$ = 200 Ω; $Z_{o(se)}$ = 75 Ω; voltage gain does include loss due to output transformer; unless otherwise specified. All RF parameters are measured on an application board with the circuit as shown in Figure 12 and components implemented as listed in Table 15.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{trt}	transient voltage	transmit-disable/transmit-enable transient step size; peak value					
		≥ 58 dBmV output power	[3][4]	-	45	-	mV
		52 dBmV output power	[3][4]	-	15	-	mV
		46 dBmV output power	[3][4]	-	10	-	mV
		40 dBmV output power	[3][4]	-	5	-	mV
		≤ 34 dBmV output power	[3][4]	-	3	-	mV
α_{2H}	second harmonic level	transmit-enable mode; gain code = 111111; P_i = 31.0 dBmV(rms); P_L = 68.0 dBmV(rms) into 75 Ω impedance		-	–65	-	dBc
α_{3H}	third harmonic level	transmit-enable mode; gain code = 111111; P_i = 31.0 dBmV(rms); P_L = 68.0 dBmV(rms) into 75 Ω impedance		-	–65	-	dBc
IMD3	third-order intermodulation distortion	transmit-enable mode; gain code = 111111; P_L = 65 dBmV(rms) per tone into 75 Ω impedance		-	–60	-	dBc
$P_{L(1dB)}$	output power at 1 dB gain compression	CW input signal RMS value; frequency = 205 MHz		-	78	-	dBmV

[1] $P_i \leq$ 30 dBmV.

[2] Excluding loss of resistive matching circuit, to match 75Ω to 50 Ω.

[3] Measured at the output of the output balun.

[4] Assume 3 dB loss between by output of the balun and F-connector in the final application.

Table 14. ACLR characteristics

Typical values at V_{CC} = 5 V; current setting = 3 mA; Gain setting 60; T_{case} = 25 °C; $Z_{i(dif)}$ = 200 Ω: $Z_{o(se)}$ = 75 Ω; channel bandwidth = 192 MHz; integration bandwidth = 9.6 MHz; f = 5 MHz to 205 MHz; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DOCSIS 3.1						
ACLR	adjacent channel leakage ratio	P_i(RMS) = 34 dBmV; P_L(RMS) = 68 dBmV. Channel configuration: channel bandwidth is 192 MHz, with exclusion band at 147.5 MHz; with a bandwidth of 9.6 MHz. Input signal with a PAPR of 13 dB	-	–64	–58	dBc

13. External components

Matching the balanced output of the chip to a single-ended 75 Ω load is accomplished using a 1: 2 ratio transformer. For measurements in a 50 Ω system, R5 and R6 are added for impedance transformation from 75 Ω to 50 Ω. R5 and R6 are not required in the final application.

The transformer also cancels even mode distortion products and common mode signals, such as the voltage transients that occur while enabling and disabling the amplifiers.

External capacitors are needed for the functionality of the circuit, the pins are internal nodes in the output amplifier. The measured voltage on the temperature sense pin 16 at an input current of 1 mA, is related to the die temperature.

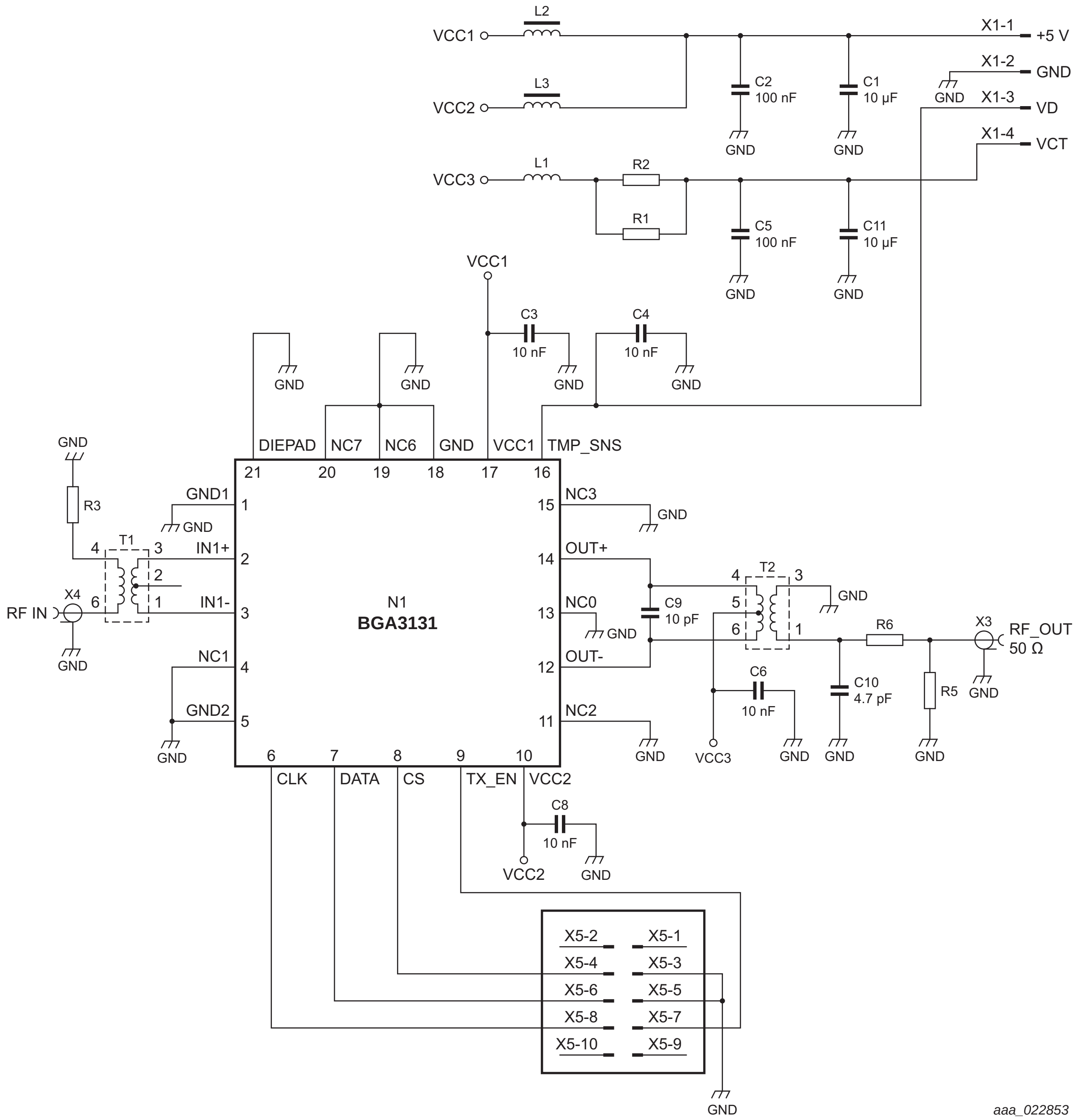


Fig 12. Schematic components

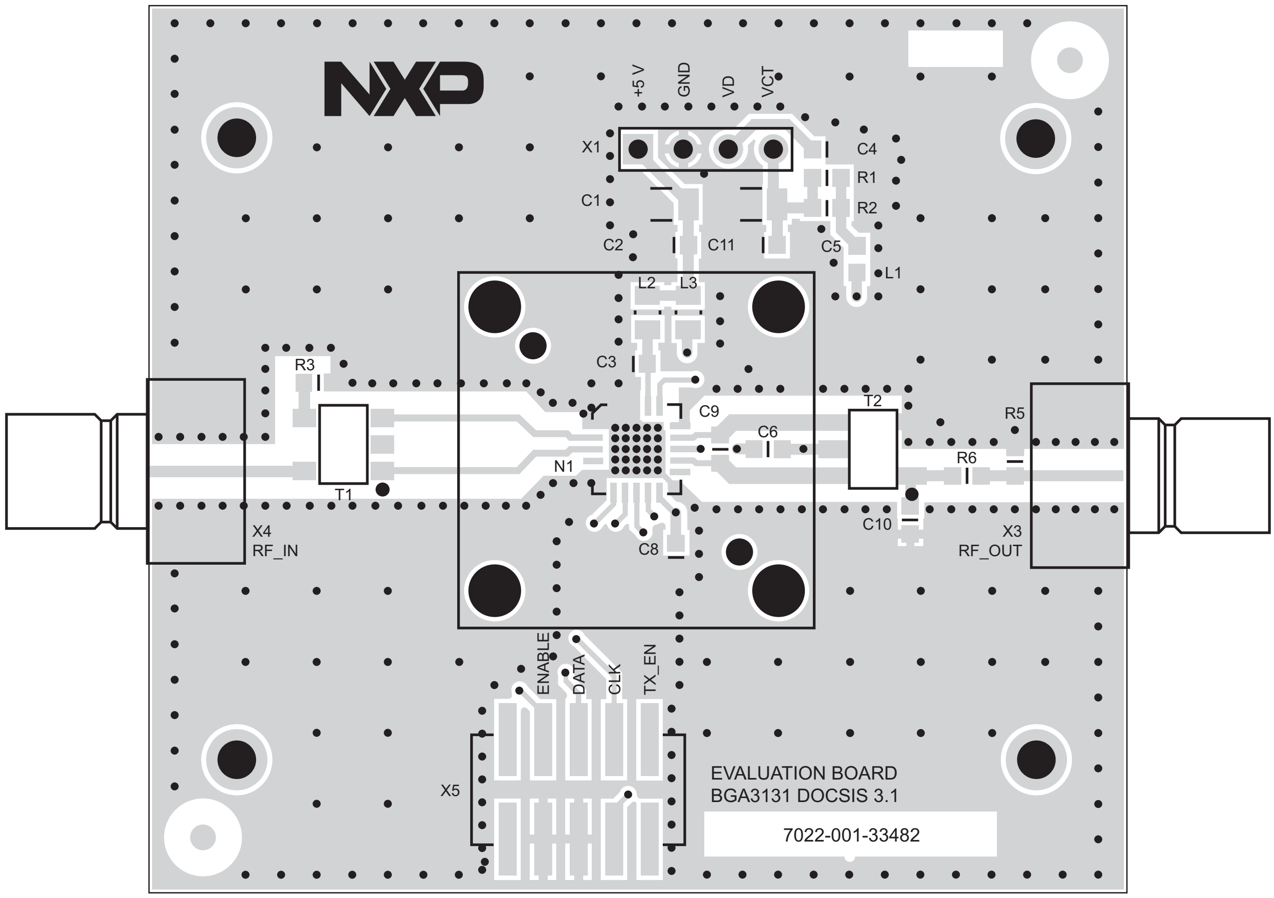


Fig 13. Layout

Table 15. List of components

For application diagram, see Figure 12.

Component	Description	Value	Size	Supplier: Part No.
C1, C11	capacitor	10 µF	SMD 1206	
C2, C5	capacitor	100 nF	SMD 0603	
C3, C4, C6, C8	capacitor	10 nF	SMD 0603	
C9	capacitor	10 pF	SMD 0603	
C10	capacitor	4.7 pF	SMD 0603	
L1	place holder for optional inductor	-	-	on EVB 0 Ω mounted
L2, L3	place holder for option chokes	-	-	on EVB 0 Ω mounted
N1	amplifier	-	-	NXP: BGA3131
R1, R2	resistor	0 Ω	SMD 0603	
R3	resistor	0 Ω	SMD 0603	
R5	resistor	86.6 Ω	SMD 0603	75 Ω to 50 Ω conversion for measurement purpose only
R6	resistor	43.2 Ω	SMD 0603	75 Ω to 50 Ω conversion for measurement purpose only

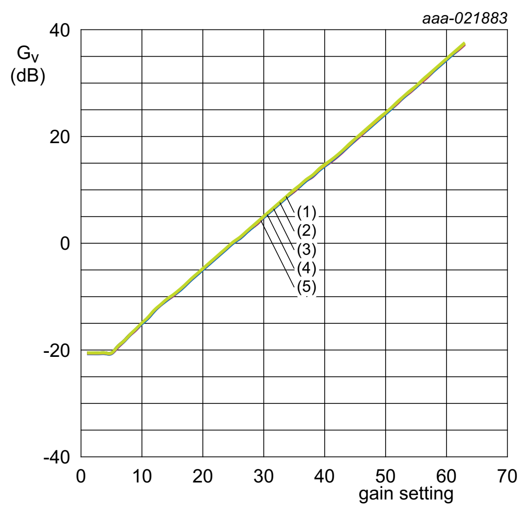
Table 15. List of components *...continued*

For application diagram, see Figure 12.

Component	Description	Value	Size	Supplier: Part No.
T1	transformer	-	-	TOKO: #617PT-1664
T2	transformer	-	-	MACOM: MABA-011056
X1	header, 4P	-	-	
X3, X4	SMA connector	-	-	
X5	header, 10P	-	-	

14. Application information

14.1 Graphics



V_{CC} = 5 V; current setting = 3; T_{amb} = 25 °C

(1) frequency = 5 MHz

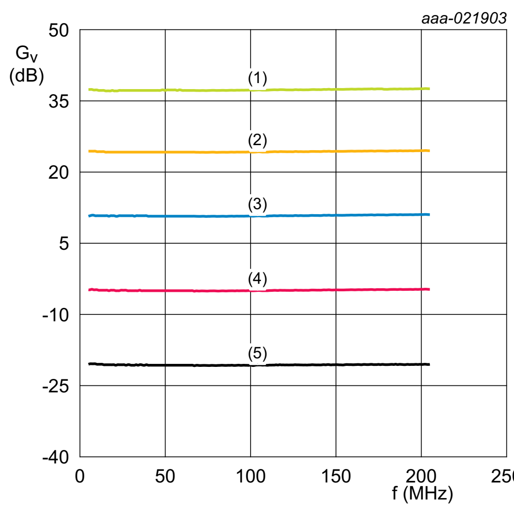
(2) frequency = 50 MHz

(3) frequency = 100 MHz

(4) frequency = 150 MHz

(5) frequency = 205 MHz

Fig 14. G_v as function of gain setting, typical values



V_{CC} = 5 V; current setting = 3; T_{amb} = 25 °C

(1) gs = 63

(2) gs = 50

(3) gs = 36

(4) gs = 20

(5) gs = 5

Fig 15. G_v as function of frequency, typical values

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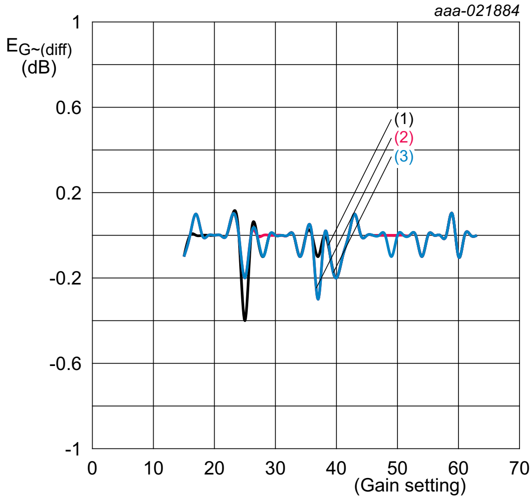


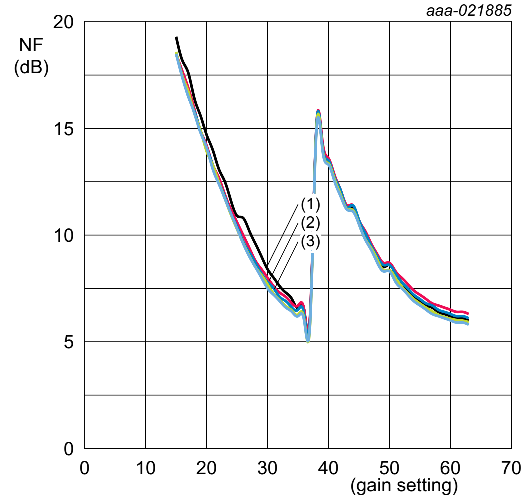
V_{CC} = 5 V; current setting = 3; T_{amb} = 25 °C

(1) frequency = 5 MHz

(2) frequency = 100 MHz

(3) frequency = 200 MHz

Fig 16. Differential gain error as function of gain setting; typical values



V_{CC} = 5 V; current setting = 3; T_{amb} = 25 °C

(1) frequency = 5 MHz

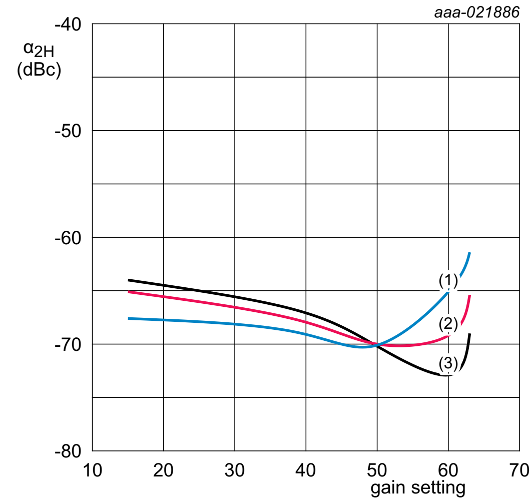
(2) frequency = 50 MHz

(3) frequency = 100 MHz

(4) frequency = 150 MHz

(5) frequency = 205 MHz

Fig 17. Noise figure as function of gain setting; typical values



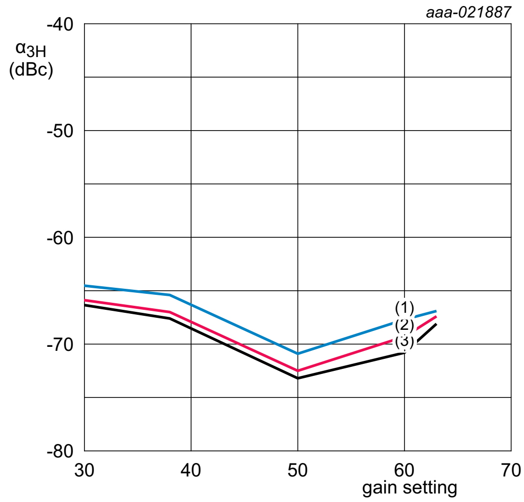
V_{CC} = 5 V; current setting = 3; T_{amb} = 25 °C;
P_L = 68 dBmV; fundamental frequency = 102 MHz;
Measurement frequency = 204 MHz

(1) T_{amb} = –40 °C

(2) T_{amb} = +25 °C

(3) T_{amb} = +85 °C

Fig 18. Second order harmonic level as function of gain setting; typical values



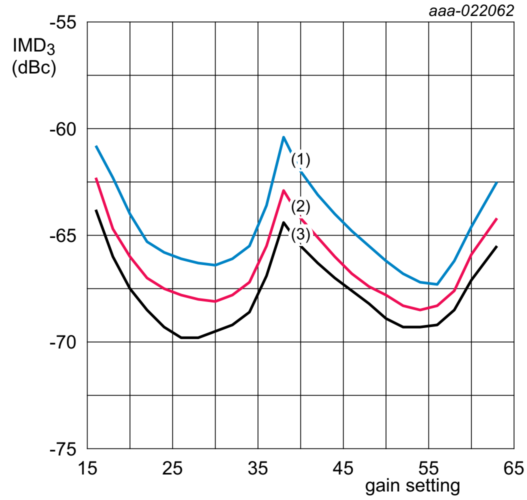
V_{CC} = 5 V; current setting = 3; T_{amb} = 25 °C;
P_L = 68 dBmV; fundamental frequency = 68 MHz;
Measurement frequency = 204 MHz

(1) T_{amb} = –40 °C

(2) T_{amb} = +25 °C

(3) T_{amb} = +85 °C

Fig 19. Third order harmonic level as function of gain setting; typical values



V_{CC} = 5 V; current setting = 3; T_{amb} = 25 °C;

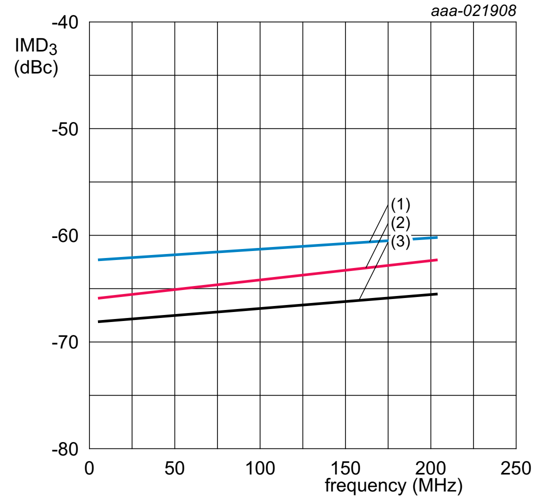
P_L per tone = 65 dBmV

(1) frequency = 204 MHz

(2) frequency = 100 MHz

(3) frequency = 5 MHz

Fig 20. Third order intermodulation distortion as a function of gain setting; typical values



V_{CC} = 5 V; current setting = 3; T_{amb} = 25 °C;

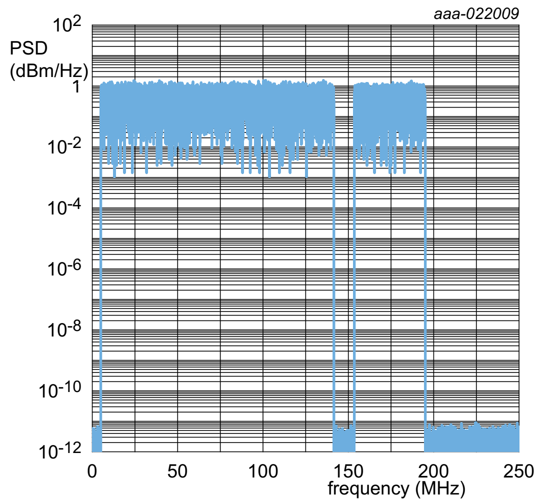
P_L per tone = 65 dBmV; gs = 60

(1) T_{amb} = –40 °C

(2) T_{amb} = +25 °C

(3) T_{amb} = +85 °C

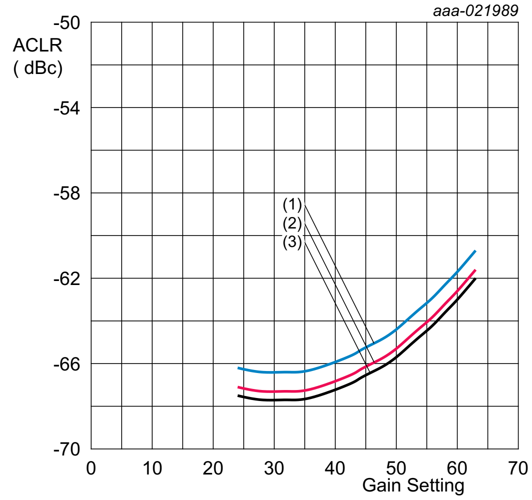
Fig 21. Third order intermodulation distortion as function of temperature; typical values



OFDM input signal for ACLR measurements, total bandwidth = 192 MHz; exclusion band @147.5 MHz, all with a bandwidth of 9.6 MHz.

Peak-to-average (PAR) ratio of the signal = 13 dB.

Fig 22. Power Spectral Density of input signal used for ACLR measurements.



V_{CC} = 5 V; current setting = 3;

Pin = 34 dBmV up to gs = 60

At gs = 61; 62 and 63; P_{out} = 68 dBmV

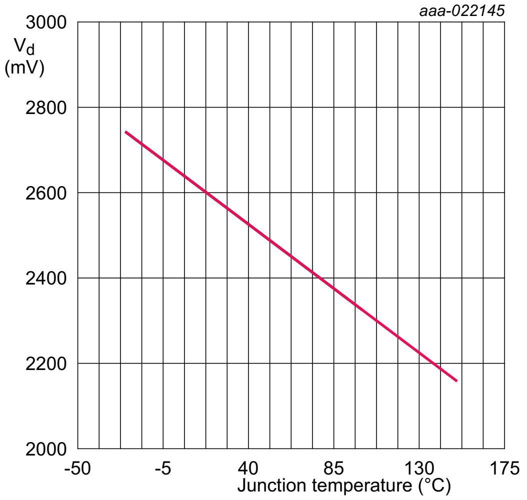
Input signal applied as described in Fig.22

(1) T_{amb} = –40 °C

(2) T_{amb} = +25 °C

(3) T_{amb} = +85 °C

Fig 23. Adjacent channel leakage ratio as function of temperature; typical values.

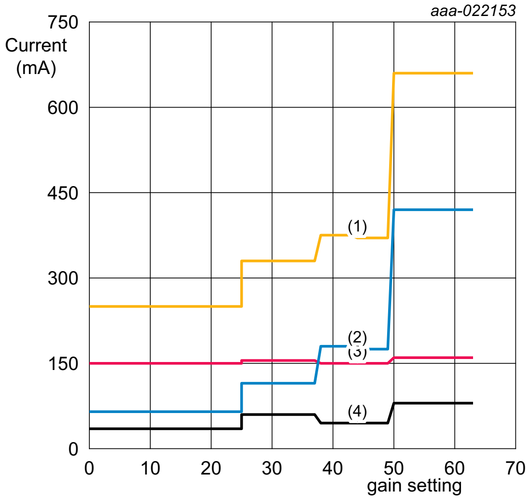


V_{CC} = 5 V; current setting = 3

TMP_SENS; DC current = 1 mA

gs = 63

Fig 24. Thermal diode voltage as function of junction temperature; typical values.



V_{CC} = 5 V; current setting = 3; T_{amb} = 25 °C;

(1) total current; I_{CC1} + I_{CC2} + ICT

(2) ICT; output balun center tap current

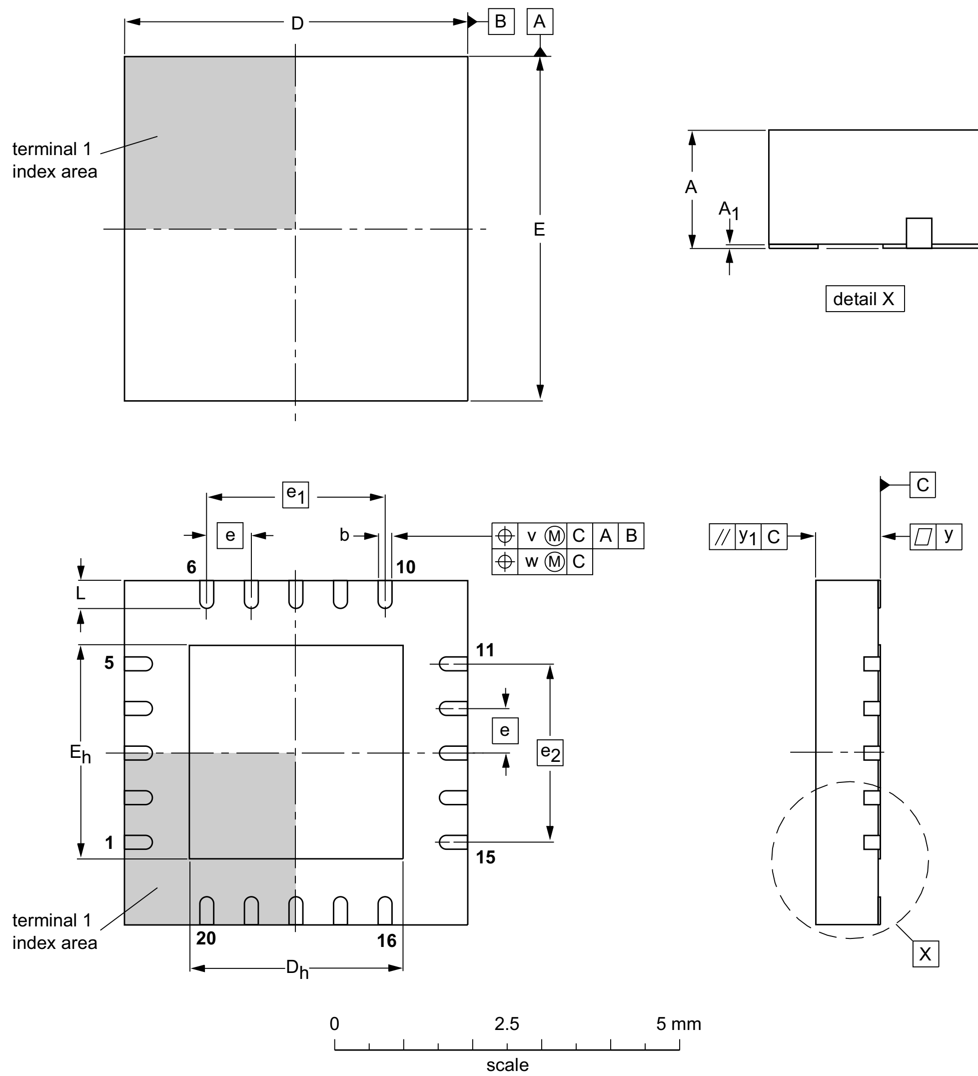
(3) I_{CC1}; current through Pin #17 (V_{CC1})

(4) I_{CC2}; current through Pin #16 (V_{CC2})

Fig 25. DC-current as function of gain setting; typical values.

15. Package outline

HVQFN20: plastic thermal enhanced very thin quad flat package; no leads; 20 terminals; body 5 x 5 x 0.85 mm **SOT662-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.38 0.23	0.2	5.1 4.9	3.25 2.95	5.1 4.9	3.25 2.95	0.65	2.6	2.6	0.75 0.50	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT662-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-22

Fig 26. Package outline SOT662-1 (HVQFN20)

16. Handling information

16.1 Moisture sensitivity

Table 16. Moisture sensitivity level

Test methodology	Class
JESD-22-A113	MSL 1

17. Abbreviations

Table 17. Abbreviations

Acronym	Description
ACLR	Adjacent Channel Leakage Ratio
CATV	Community Antenna Television
CW	Continuous Wave
ESD	ElectroStatic Discharge
HVQFN	Heat sink Very thin Quad Flat pack No leads
OFDM	Orthogonal Frequency Division Multiplexing
PAPR	Peak-to-Average Power Ratio
SMA	Sub-Miniature version A
SMD	Surface-Mounted Device
TX	Transmission
VoIP	Voice over Internet Protocol

18. Revision history

Table 18. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BGA3131 v.1	20160513	Product data sheet	-	-

19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term ‘short data sheet’ is explained in section “Definitions”.

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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