NXP Semiconductors
Technical Data

Document Number: MHT1108N
Rev. 0, 03/2017

RF Power LDMOS Transistor

N-Channel Enhancement-Mode Lateral MOSFET

This 12.5 W CW high efficiency RF power transistor is designed for consumer and commercial cooking applications operating in the 2450 MHz ISM band.

Typical Performance: V_{DD} = 28 Vdc, I_{DQ} = 110 mA

Frequency (MHz)	Signal Type	G_{ps} (dB)	PAE (%)	P_{out} (W)
2400	CW	18.5	55.7	12.5
2450		18.6	56.3	12.5
2500		18.1	54.2	12.5

Load Mismatch/Ruggedness

Frequency (MHz)	Signal Type	VSWR	P_{in} (dBm)	Test Voltage	Result
2450	CW	> 10:1 at all Phase Angles	26 (3 dB Overdrive)	32	No Device Degradation

Features

- Characterized with series equivalent large-signal impedance parameters and common source S-parameters
- Qualified for operation at 32 Vdc
- Integrated ESD protection
- 150°C case operating temperature
- 150°C die temperature capability

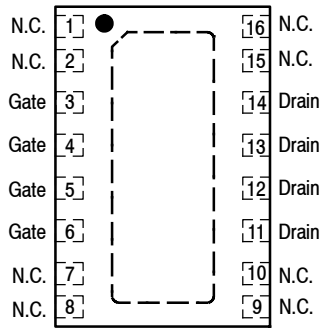
Target Applications

- Consumer cooking as PA driver
- Commercial cooking as PA driver

MHT1108N

2450 MHz, 12.5 W CW, 28 V
RF POWER LDMOS TRANSISTOR
FOR CONSUMER AND
COMMERCIAL COOKING

DFN 4 × 6
PLASTIC



(Top View)

Note: Exposed backside of the package is the source terminal for the transistor.

Figure 1. Pin Connections

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	–0.5, +65	Vdc
Gate–Source Voltage	V_{GS}	–6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–40 to +150	°C
Operating Junction Temperature Range (1,2)	T_J	–40 to +150	°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	32.9 0.26	W W/°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 97°C, 12.6 W CW, 28 Vdc, I_{DQ} = 110 mA, 2450 MHz	$R_{\theta JC}$	3.8	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22–A114)	1C, passes 1000 V
Charge Device Model (per JESD22–C101)	C3, passes 1000 V

Table 4. Moisture Sensitivity Level (MSL)

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22–A113, IPC/JEDEC J–STD–020	3	260	°C

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 14.3 μAdc)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, I_D = 90 mAdc)	$V_{GS(Q)}$	—	1.8	—	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 143 mAdc)	$V_{DS(on)}$	0.1	0.2	0.3	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.nxp.com/RF/calculators.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.nxp.com/RF and search for AN1955.

Table 6. Typical Performance

In NXP Reference Circuit, 50 ohm system, V_{DD} = 28 Vdc, I_{DQ} = 110 mA

Frequency	G_{ps} (dB)	PAE (%)	P_{out} (W)
2400 MHz	18.5	55.7	12.5
2450 MHz	18.6	56.3	12.5
2500 MHz	18.1	54.2	12.5

Table 7. Load Mismatch/Ruggedness

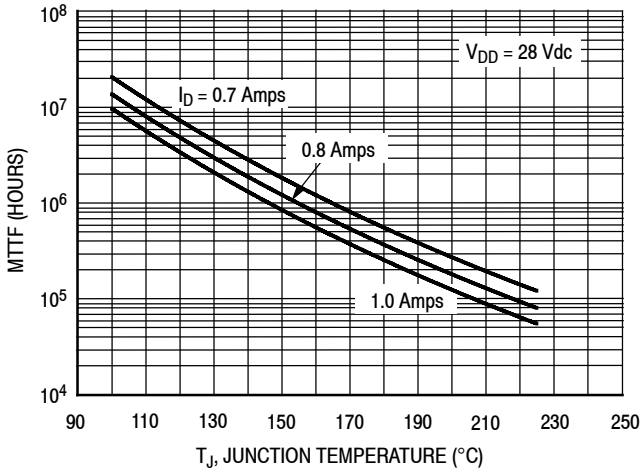
In NXP Reference Circuit, 50 ohm system, I_{DQ} = 110 mA

Frequency (MHz)	Signal Type	VSWR	P_{in} (dBm)	Test Voltage, V_{DD}	Result
2450	CW	>10:1 at all Phase Angles	26 (3 dB Overdrive)	32	No Device Degradation

Table 8. Ordering Information

Device	Tape and Reel Information	Package
MHT1108NT1	T1 Suffix = 1,000 Units, 16 mm Tape Width, 7–inch Reel	DFN 4 × 6

TYPICAL CHARACTERISTICS



Note: MTTF value represents the total cumulative operating time under indicated test conditions.

MTTF calculator available at http://www.nxp.com/RF/calculators.

Figure 2. MTTF versus Junction Temperature – CW

Table 9. Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, I_{DQ} = 110 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Output Power					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	PAE (%)
2400	1.13 – j2.48	0.77 + j2.04	5.21 + j1.81	19.6	42.2	17	60.0	59.5
2450	1.03 – j2.77	0.74 + j2.24	5.37 + j1.51	19.1	42.2	16	58.4	57.7
2500	1.02 – j2.93	0.84 + j2.47	5.02 + j1.34	19.1	42.1	16	58.0	57.3

			Max Output Power					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	PAE (%)
2400	1.13 – j2.48	0.75 + j2.25	6.22 + j1.32	17.3	43.0	20	59.4	58.4
2450	1.03 – j2.77	0.71 + j2.43	6.08 + j1.21	16.9	42.9	19	58.6	57.2
2500	1.02 – j2.93	0.84 + j2.68	5.76 + j0.92	16.9	42.8	19	57.8	56.6

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

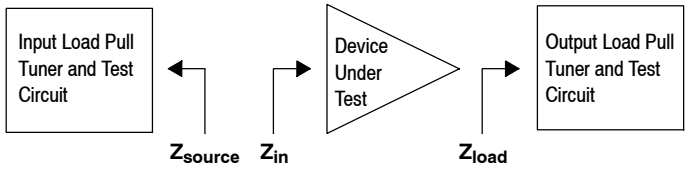
Table 10. Load Pull Performance — Maximum Efficiency Tuning

V_{DD} = 28 Vdc, I_{DQ} = 110 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Efficiency					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	PAE (%)
2400	1.13 – j2.48	0.65 + j2.01	3.94 + j3.57	20.9	41.5	14	65.8	65.2
2450	1.03 – j2.77	0.63 + j2.20	3.84 + j3.50	20.5	41.3	14	64.4	63.8
2500	1.02 – j2.93	0.70 + j2.42	3.32 + j3.15	20.6	41.1	13	63.5	63.0

			Max Efficiency					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	PAE (%)
2400	1.13 – j2.48	0.63 + j2.19	4.12 + j3.59	18.9	42.1	16	65.6	64.7
2450	1.03 – j2.77	0.62 + j2.37	4.24 + j3.10	18.1	42.2	17	63.9	63.0
2500	1.02 – j2.93	0.73 + j2.63	4.05 + j3.04	18.4	42.0	16	63.2	62.9

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P3dB – TYPICAL LOAD PULL CONTOURS — 2450 MHz

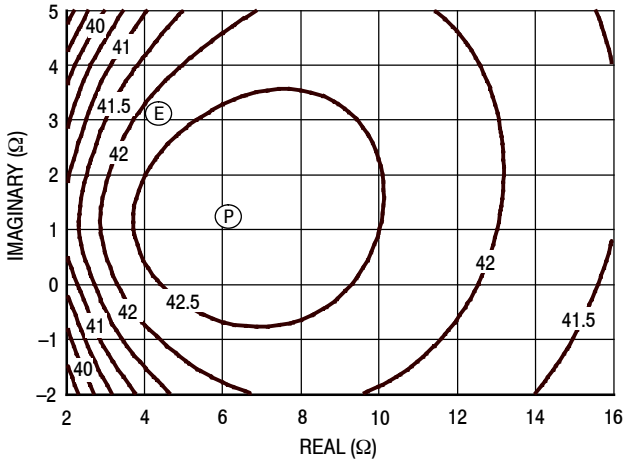


Figure 3. P3dB Load Pull Output Power Contours (dBm)

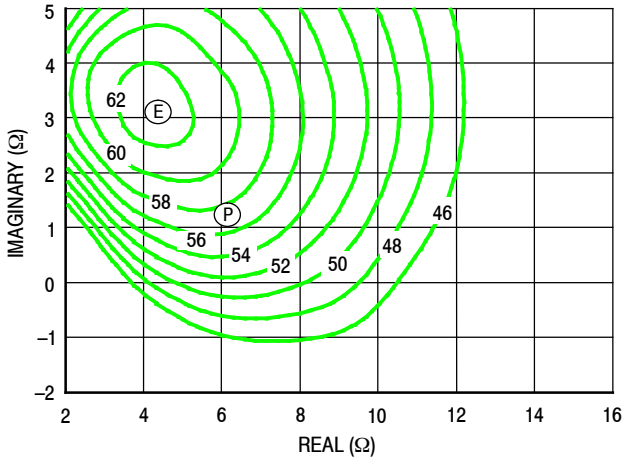


Figure 4. P3dB Load Pull PAE Contours (%)

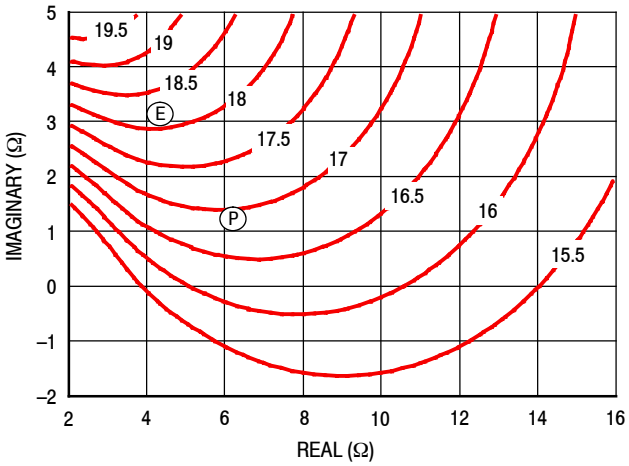


Figure 5. P3dB Load Pull Gain Contours (dB)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Power Added Efficiency

Gain

Power Added Efficiency

Output Power

2450 MHz REFERENCE CIRCUIT — 3″ × 5″ (7.6 cm × 12.7 cm)

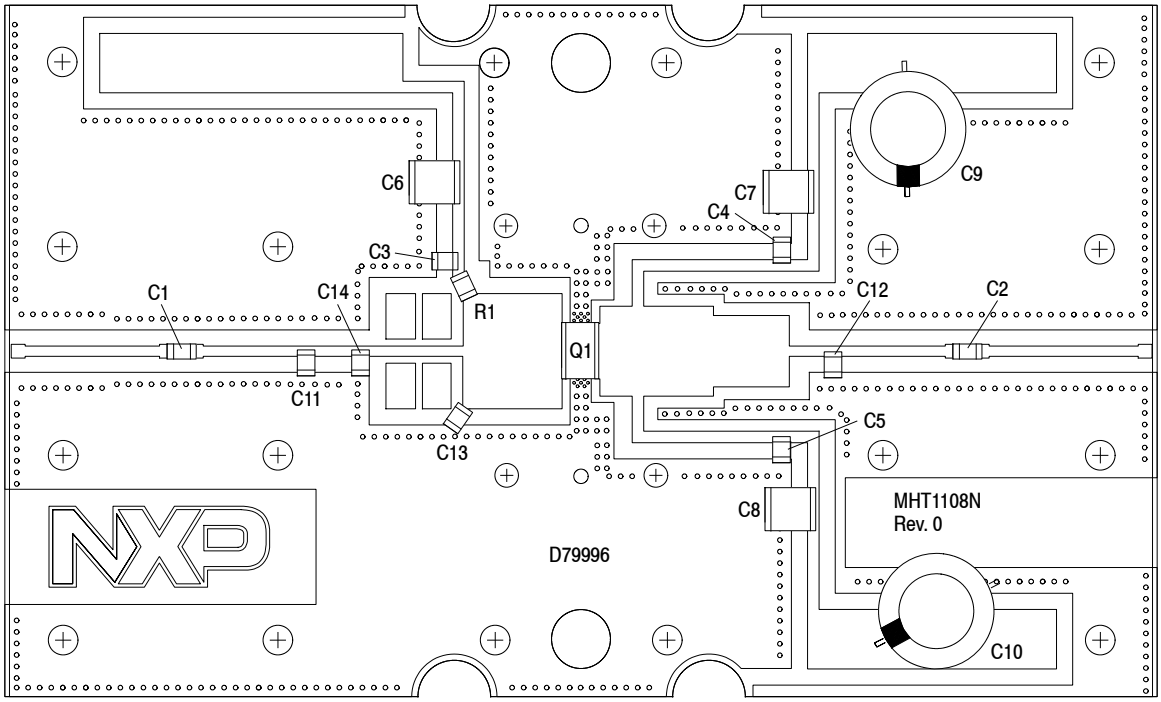


Figure 6. MHT1108N Reference Circuit Component Layout — 2450 MHz

Table 11. MHT1108N Reference Circuit Component Designations and Values — 2450 MHz

Part	Description	Part Number	Manufacturer
C1, C2, C3, C4, C5	6.2 pF Chip Capacitor	ATC100B6R2FW1500XT	ATC
C6, C7, C8	10 μF Chip Capacitor	C5750X7S2A106M	TDK
C9, C10	220 μF, 50 V Electrolytic Capacitor	227CKS050M	Illinois Capacitor
C11	0.6 pF Chip Capacitor	ATC100B0R6FW1500XT	ATC
C12, C13	1.0 pF Chip Capacitor	ATC100B1R3FW1500XT	ATC
C14	0.3 pF Chip Capacitor	ATC100B0R3FW1500XT	ATC
Q1	RF Power LDMOS Transistor	MHT1108N	NXP Semiconductors
R1	4.7 Ω, 1/4 W Chip Resistor	CRCW12064R70FKEA	Vishay
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D79996	MTL

TYPICAL CHARACTERISTICS — 2450 MHz REFERENCE CIRCUIT

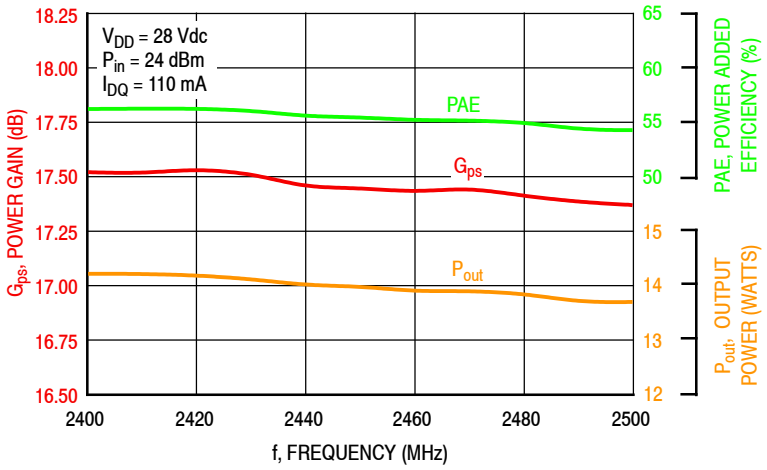


Figure 7. Power Gain, Power Added Efficiency and Output Power versus Frequency at a Constant Input Power

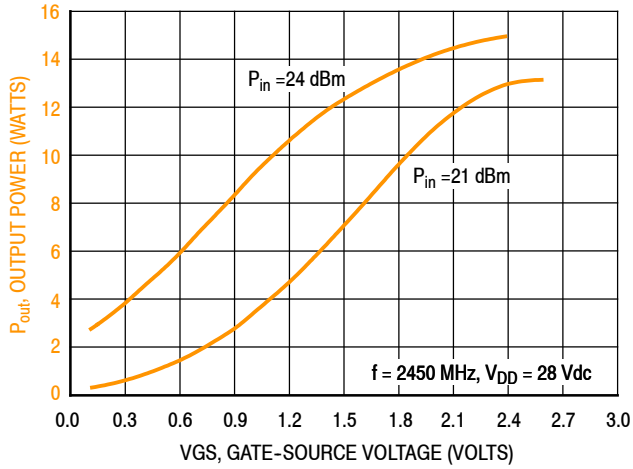


Figure 8. Output Power versus Gate-Source Voltage

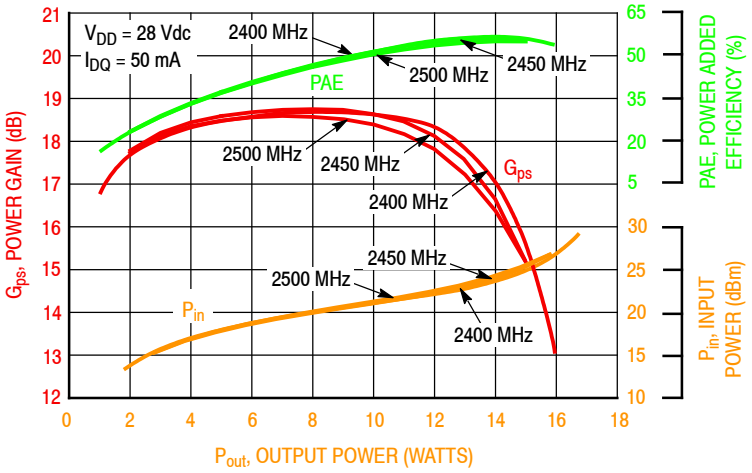


Figure 9. Power Gain, Power Added Efficiency and Input Power versus Output Power and Frequency

TYPICAL CHARACTERISTICS — 2450 MHz REFERENCE CIRCUIT

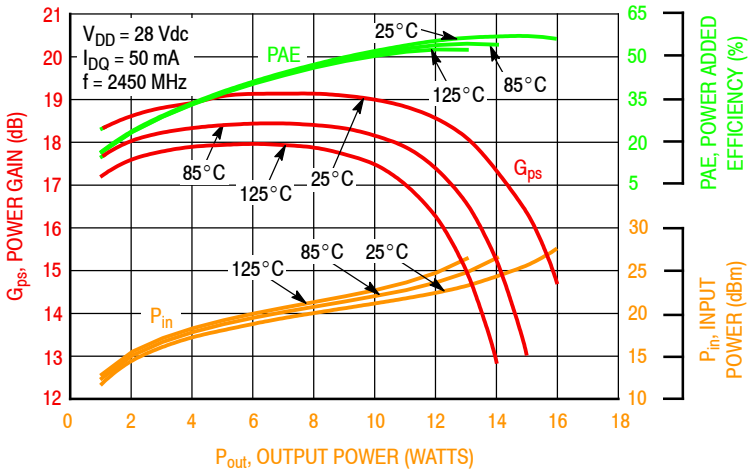


Figure 10. Power Gain, Power Added Efficiency and Input Power versus Output Power and Temperature

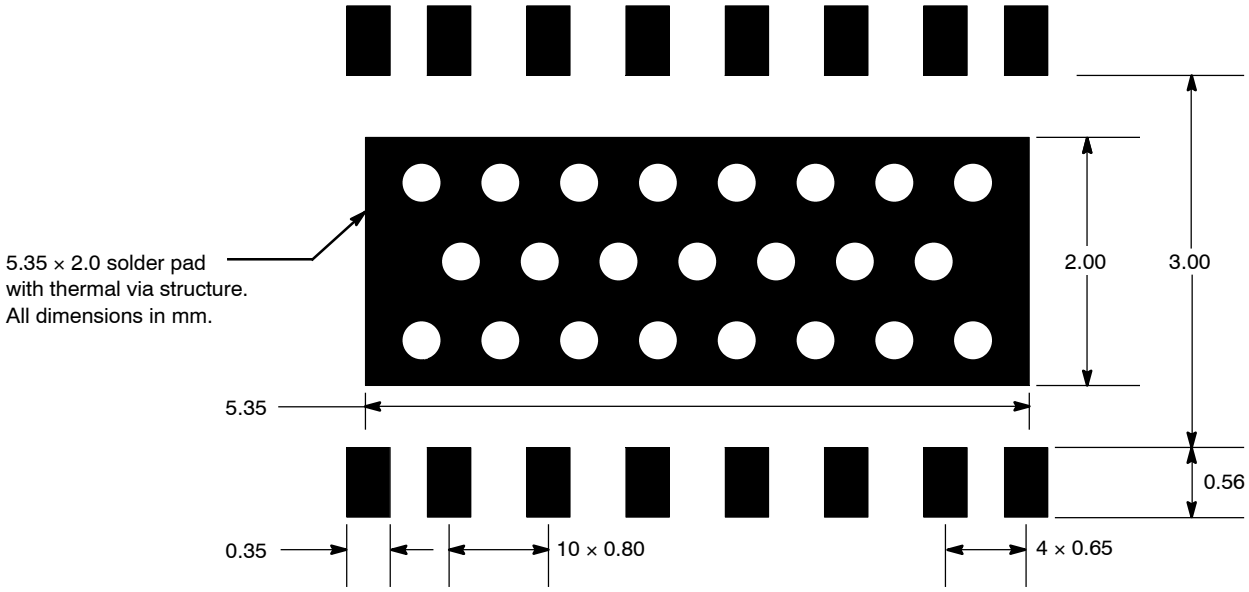
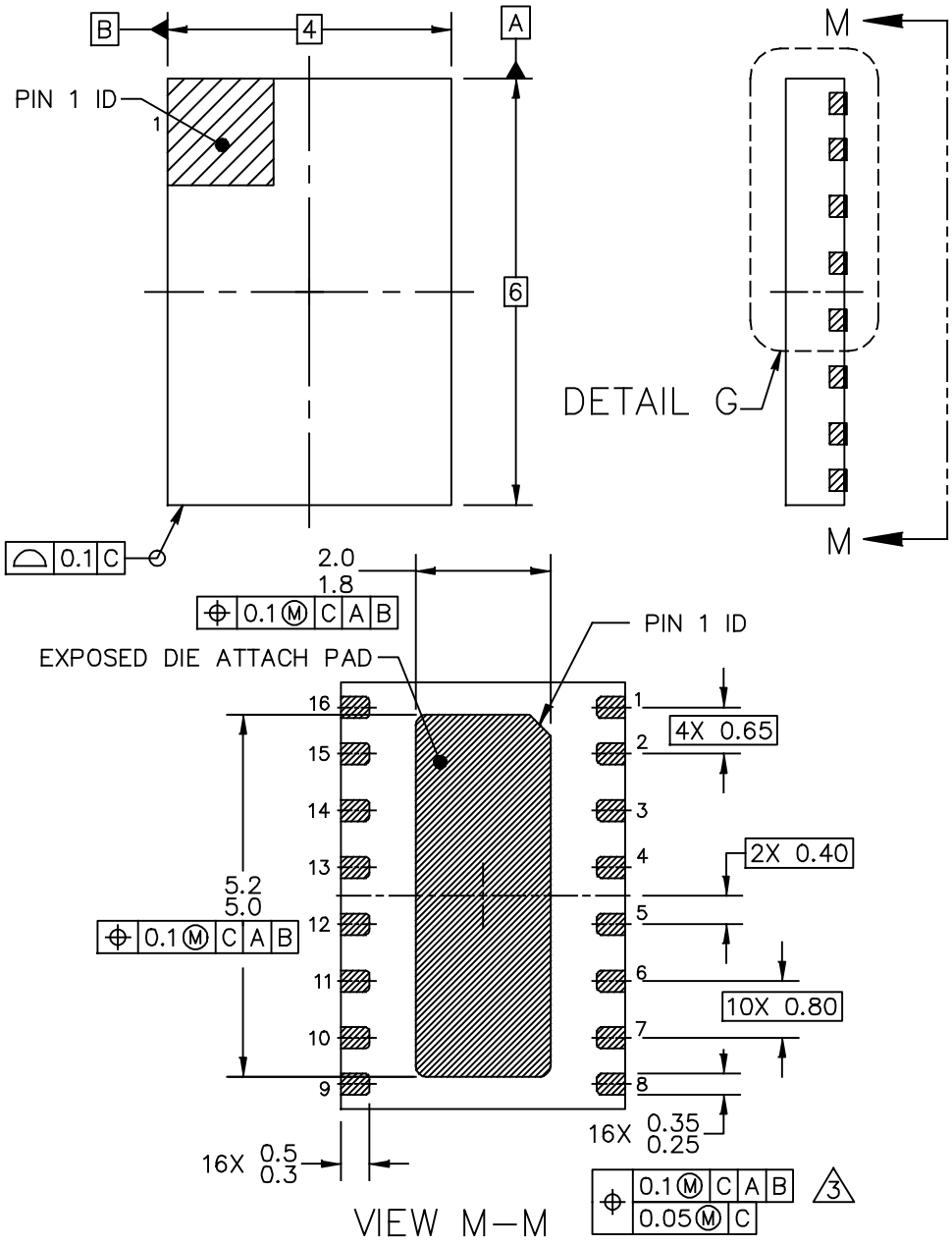


Figure 11. PCB Pad Layout for 16-Lead DFN 4 × 6

Figure 12. Product Marking

PACKAGE DIMENSIONS



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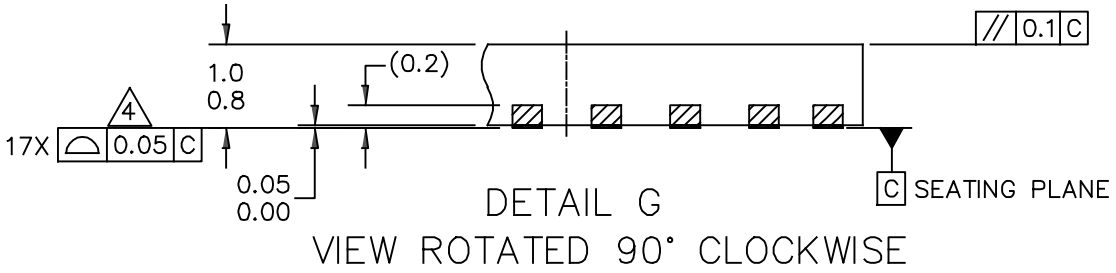
TITLE: DFN, THERMALLY ENHANCED 4 X 6 X 0.9, 0.8 & 0.65 PITCH, 16 TERMINAL	DOCUMENT NO: 98ASA00868D	REV: B
	STANDARD: NON–JEDEC	
	SOT1862–1	27 JUL 2016



DETAIL G
VIEW ROTATED 90° CLOCKWISE

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	STANDARD: NON–JEDEC	
	SOT1862–1	27 JUL 2016

NOTES:

1. DIMENSIONING & TOLERANCING CONFIRM TO ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. THIS DIMENSION APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 MM AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED HEAT SLUG AS WELL AS THE TERMINALS.

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	STANDARD: NON–JEDEC
	SOT1862–1 27 JUL 2016

PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the resources to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Over-Molded Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model

Development Tools

- Printed Circuit Boards

To Download Resources Specific to a Given Part Number:

1. Go to http://www.nxp.com/RF
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Mar. 2017	• Initial Release of Data Sheet

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