**REVISION HISTORY**

| Revision | Description | Issue Date |
|---|---|---|
| Rev. 1.0 | Initial Issue | February 2007 |
| Rev. 1.1 | Revision of Supply current  ISB1 – page 3<br>Commercial temp 20 µA<br>Industrial temp 30 µA | March 26, 2013 |
|  | Revision of Alliance Memory address | March 26, 2013 |
| Rev 1.2 | Further Revision of Supply current  - page 3<br>Commercial temp 15 µA<br>Industrial temp 30 µA | March 23, 2016 |
|  | IdR (data-retention current) to be 20uA - page 7 |  |

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# 32K X 8 BIT LOW POWER CMOS SRAM

## FEATURES

- Access time : 55ns
- Low power consumption:
  Operation current :
       15mA (TYP.), $V_{CC}$ = 3.0V
  Standby current :
       1μA (TYP.), $V_{CC}$ = 3.0V
- Wide range power supply : 2.7 ~ 5.5V
- Fully Compatible with all Competitors 5V product
- Fully Compatible with all Competitors 3.3V product
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data retention voltage :1.5V (MIN.)
- **All products ROHS Compliant**
- Package : 28-pin 600 mil PDIP
             28-pin 330 mil SOP
             28-pin 8mm x 13.4mm sTSOP

## GENERAL DESCRIPTION

The AS6C62256 is a 262,144-bit low power CMOS static random access memory organized as 32,768 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

The AS6C62256 is well designed for low power application, and particularly well suited for battery back-up nonvolatile memory application.

The AS6C62256 operates with wide range power supply 2.7 ~ 5.5V
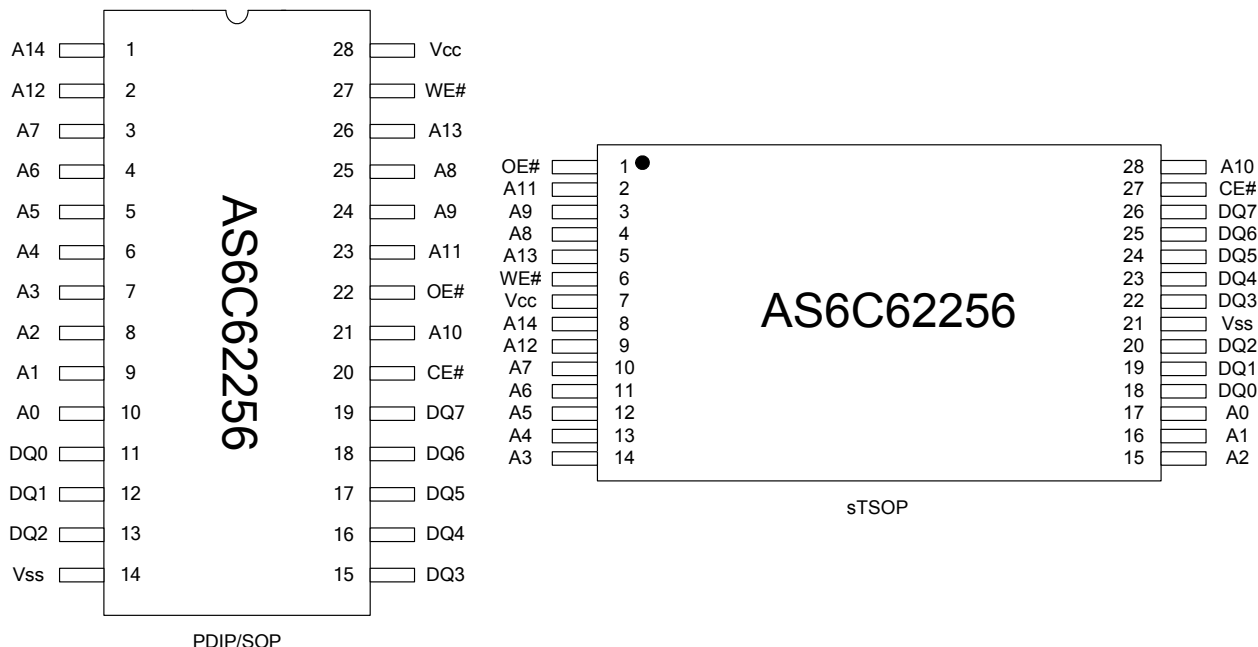
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## FUNCTIONAL BLOCK DIAGRAM
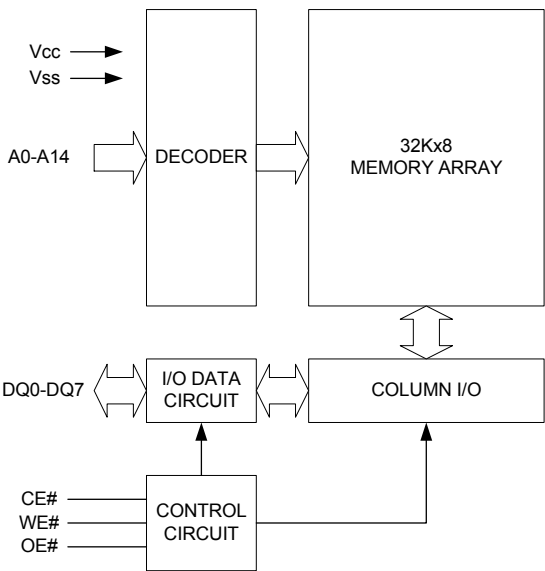


## PIN DESCRIPTION

| SYMBOL | DESCRIPTION |
|---|---|
| A0 - A14 | Address Inputs |
| DQ0 – DQ7 | Data Inputs/Outputs |
| CE# | Chip Enable Input |
| WE# | Write Enable Input |
| OE# | Output Enable Input |
| $V_{CC}$ | Power Supply |
| $V_{SS}$ | Ground |

**32K X 8 BIT LOW POWER CMOS SRAM**

## PIN CONFIGURATION

```
        A14 ▭  1        28 ▭ Vcc
        A12 ▭  2        27 ▭ WE#
        A7  ▭  3        26 ▭ A13
        A6  ▭  4        25 ▭ A8
        A5  ▭  5        24 ▭ A9
        A4  ▭  6        23 ▭ A11
        A3  ▭  7        22 ▭ OE#
        A2  ▭  8        21 ▭ A10
        A1  ▭  9        20 ▭ CE#
        A0  ▭ 10        19 ▭ DQ7
        DQ0 ▭ 11        18 ▭ DQ6
        DQ1 ▭ 12        17 ▭ DQ5
        DQ2 ▭ 13        16 ▭ DQ4
        Vss ▭ 14        15 ▭ DQ3
              PDIP/SOP
```
(AS6C62256)

```
   OE# ▭  1 ●            28 ▭ A10
   A11 ▭  2             27 ▭ CE#
   A9  ▭  3             26 ▭ DQ7
   A8  ▭  4             25 ▭ DQ6
   A13 ▭  5             24 ▭ DQ5
   WE# ▭  6             23 ▭ DQ4
   Vcc ▭  7   AS6C62256 22 ▭ DQ3
   A14 ▭  8             21 ▭ Vss
   A12 ▭  9             20 ▭ DQ2
   A7  ▭ 10             19 ▭ DQ1
   A6  ▭ 11             18 ▭ DQ0
   A5  ▭ 12             17 ▭ A0
   A4  ▭ 13             16 ▭ A1
   A3  ▭ 14             15 ▭ A2
              sTSOP
```

## ABSOLUTE MAXIMUM RATINGS*

| PARAMETER | SYMBOL | RATING | UNIT |
|---|---|---|---|
| Terminal Voltage with Respect to Vss | $V_{TERM}$ | -0.5 to 7.0 | V |
| Operating Temperature | $T_A$ | 0 to 70(C grade) | °C |
| | | | |
| | | -40 to 85(I grade) | °C |
| Storage Temperature | $T_{STG}$ | -65 to 150 | |
| Power Dissipation | $P_D$ | 1 | W |
| DC Output Current | $I_{OUT}$ | 50 | mA |
| Soldering Temperature (under 10 sec) | $T_{SOLDER}$ | 260 | °C |

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

## TRUTH TABLE

| MODE | CE# | OE# | WE# | I/O OPERATION | SUPPLY CURRENT |
|---|---|---|---|---|---|
| Standby | H | X | X | High-Z | $I_{SB}, I_{SB1}$ |
| Output Disable | L | H | H | High-Z | $I_{CC}, I_{CC1}$ |
| Read | L | L | H | $D_{OUT}$ | $I_{CC}, I_{CC1}$ |
| Write | L | X | L | $D_{IN}$ | $I_{CC}, I_{CC1}$ |

Note:   H = $V_{IH}$, L = $V_{IL}$, X = Don't care.

## DC ELECTRICAL CHARACTERISTICS

| PARAMETER | SYMBOL | TEST CONDITION | | MIN. | TYP. [5] | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | | | 2.7 | 3.3 | 5.5 | V |
| Input High Voltage | $V_{IH}$[1] | | | 2.4 V | - | $V_{CC}$+0.5 | V |
| Input Low Voltage | $V_{IL}$[2] | | | - 0.5 | - | 0.6 | V |
| Input Leakage Current | $I_{LI}$ | $V_{CC} \geq V_{IN} \geq V_{SS}$ | | - 1 | - | 1 | µA |
| Output Leakage Current | $I_{LO}$ | $V_{CC} \geq V_{OUT} \geq V_{SS}$, Output Disabled | | - 1 | - | 1 | µA |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -1mA | | 2.4 | 3.0 | - | V |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 2mA | | - | - | 0.4 | V |
| Average Operating Power supply Current | $I_{CC}$ | Cycle time = Min. CE# = $V_{IL}$ , $I_{I/O}$ = 0mA | -55 | - | 15 | 45 | mA . |
| | $I_{CC1}$ | Cycle time = 1µs CE#$\leqq$0.2V and $I_{I/O}$ = 0mA other pins at 0.2V or $V_{CC}$-0.2V | | - | 3 | 10 | mA |
| Standby Power Supply Current | $I_{SB}$ | CE# = $V_{IH}$ | | - | 1 | 3 | mA |
| | $I_{SB1}$ | CE# >=$V_{CC}$ - 0.2V Others at 0.2V or $V_{CC}$-0.2V | -C | - | 1 | 15[4] | µA |
| | | | -I | - | 1 | 30[4] | µA |

Notes: C = Commercial Temperature   I = Industrial Temperature
1. $V_{IH}$(max) = $V_{CC}$ + 3.0V for pulse width less than 10ns.
2. $V_{IL}$(min) = $V_{SS}$ - 3.0V for pulse width less than 10ns.
3. Over/Undershoot specifications are characterized, not 100% tested.
4. 10µA for special request
5. Typical values are included for reference only and are not guaranteed or tested.
   Typical valued are measured at $V_{CC}$ = $V_{CC}$(TYP.) and $T_A$ = 25ºC

## CAPACITANCE  ($T_A$ = 25℃, f = 1.0MHz)

| PARAMETER | SYMBOL | MIN. | MAX | UNIT |
|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | - | 6 | pF |
| Input/Output Capacitance | $C_{I/O}$ | - | 8 | pF |

Note : These parameters are guaranteed by device characterization, but not production tested.

## AC TEST CONDITIONS

| | |
|---|---|
| Input Pulse Levels | 0.2V to $V_{CC}$ - 0.2V |
| Input Rise and Fall Times | 3ns |
| Input and Output Timing Reference Levels | 1.5V |
| Output Load | $C_L$ = 50pF + 1TTL, $I_{OH}$/$I_{OL}$ = -1mA/2mA |

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**32K X 8 BIT LOW POWER CMOS SRAM**

## AC ELECTRICAL CHARACTERISTICS

### (1) READ CYCLE

| PARAMETER | SYM | | | AS6C62256-55 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX. | | | |
| Read Cycle Time | $t_{RC}$ | | | 55 | - | | | ns |
| Address Access Time | $t_{AA}$ | | | - | 55 | | | ns |
| Chip Enable Access Time | $t_{ACE}$ | | | - | 55 | | | ns |
| Output Enable Access Time | $t_{OE}$ | | | - | 30 | | | ns |
| Chip Enable to Output in Low-Z | $t_{CLZ}$* | | | 10 | - | | | ns |
| Output Enable to Output in Low-Z | $t_{OLZ}$* | | | 5 | - | | | ns |
| Chip Disable to Output in High-Z | $t_{CHZ}$* | | | - | 20 | | | ns |
| Output Disable to Output in High-Z | $t_{OHZ}$* | | | - | 20 | | | ns |
| Output Hold from Address Change | $t_{OH}$ | | | 10 | - | | | ns |

### (2) WRITE CYCLE

| PARAMETER | SYM | | | AS6C62256-55 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | | | |
| Write Cycle Time | $t_{WC}$ | | | 55 | - | | | ns |
| Address Valid to End of Write | $t_{AW}$ | | | 50 | - | | | ns |
| Chip Enable to End of Write | $t_{CW}$ | | | 50 | - | | | ns |
| Address Set-up Time | $t_{AS}$ | | | 0 | - | | | ns |
| Write Pulse Width | $t_{WP}$ | | | 45 | - | | | ns |
| Write Recovery Time | $t_{WR}$ | | | 0 | - | | | ns |
| Data to Write Time Overlap | $t_{DW}$ | | | 25 | - | | | ns |
| Data Hold from End of Write Time | $t_{DH}$ | | | 0 | - | | | ns |
| Output Active from End of Write | $t_{OW}$* | | | 5 | - | | | ns |
| Write to Output in High-Z | $t_{WHZ}$* | | | - | 20 | | | ns |

*These parameters are guaranteed by device characterization, but not production tested.

## TIMING WAVEFORMS

**READ CYCLE 1** (Address Controlled) (1,2)
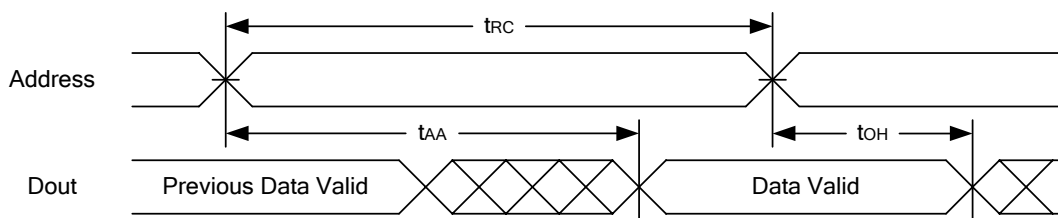


**READ CYCLE 2** (CE# and OE# Controlled) (1,3,4,5)
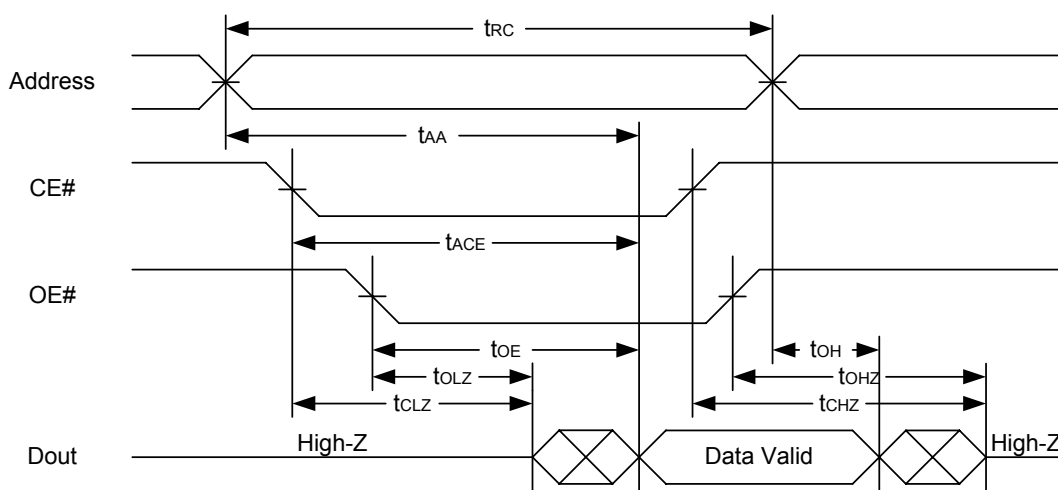


Notes :
1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low.
3. Address must be valid prior to or coincident with CE# = low,; otherwise $t_{AA}$ is the limiting parameter.
4. $t_{CLZ}$, $t_{OLZ}$, $t_{CHZ}$ and $t_{OHZ}$ are specified with $C_L$ = 5pF. Transition is measured ±500mV from steady state.
5. At any given temperature and voltage condition, $t_{CHZ}$ is less than $t_{CLZ}$ , $t_{OHZ}$ is less than $t_{OLZ}$.

**WRITE CYCLE 1** (WE# Controlled) (1,2,3,5,6)
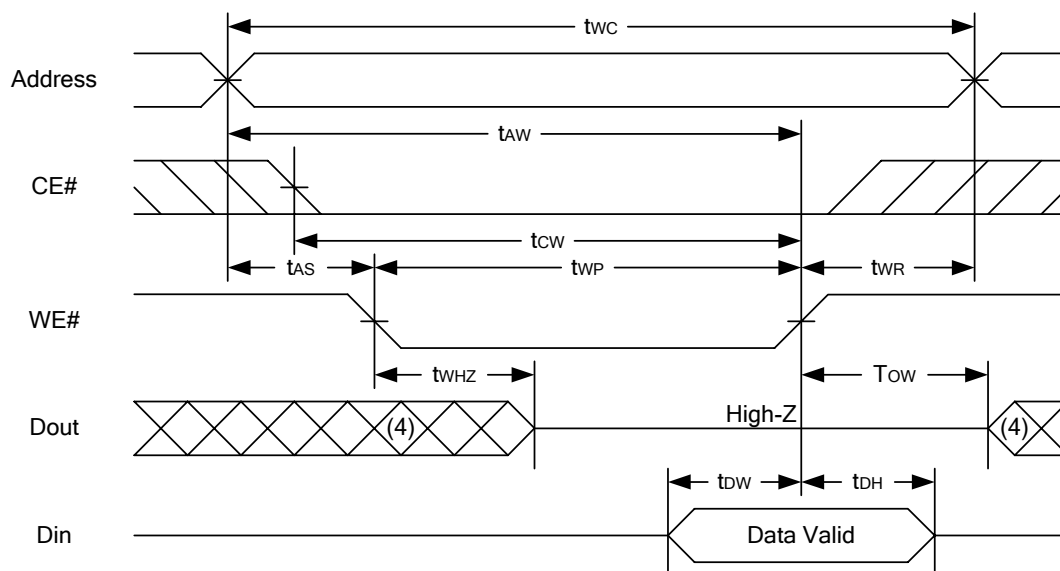


**WRITE CYCLE 2** (CE# Controlled) (1,2,5,6)
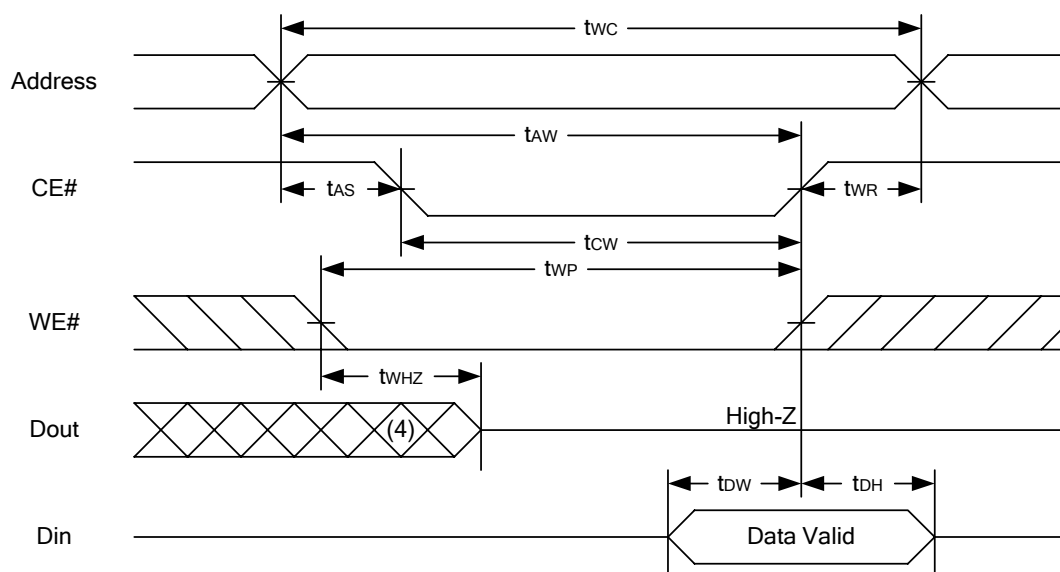


Notes :
1.WE#, CE# must be high during all address transitions.
2.A write occurs during the overlap of a low CE#, low WE#.
3.During a WE# controlled write cycle with OE# low, $t_{WP}$ must be greater than $t_{WHZ}$ + $t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
4.During this period, I/O pins are in the output state, and input signals must not be applied.
5.If the CE# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
6.$t_{OW}$ and $t_{WHZ}$ are specified with $C_L$ = 5pF. Transition is measured ±500mV from steady state.

**32K X 8 BIT LOW POWER CMOS SRAM**

## DATA RETENTION CHARACTERISTICS

| PARAMETER | SYMBOL | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|-----------|--------|----------------|------|------|------|------|
| $V_{CC}$ for Data Retention | $V_{DR}$ | CE# $\geq$ $V_{CC}$ - 0.2V | 1.5 | - | 5.5 | V |
| Data Retention Current | $I_{DR}$ | $V_{CC}$ = 2.0V<br>CE# $\geq$ $V_{CC}$ - 0.2V | - | 0.5 | 20 | µA |
| Chip Disable to Data Retention Time | $t_{CDR}$ | See Data Retention Waveforms (below) | 0 | - | - | ns |
| Recovery Time | $t_R$ | | $t_{RC*}$ | - | - | ns |

$t_{RC*}$ = Read Cycle Time
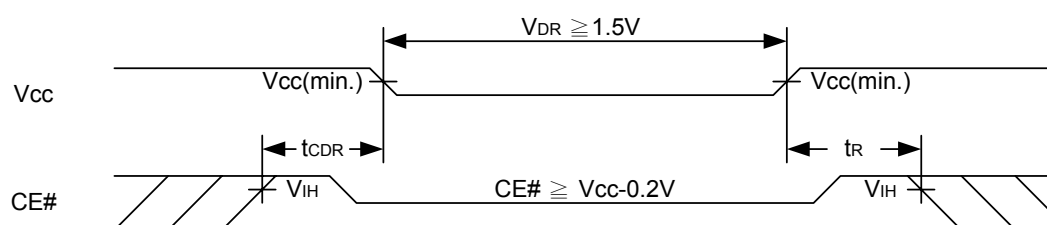
## DATA RETENTION WAVEFORM

## PACKAGE OUTLINE DIMENSION

**28 pin 600 mil PDIP Package Outline Dimension**
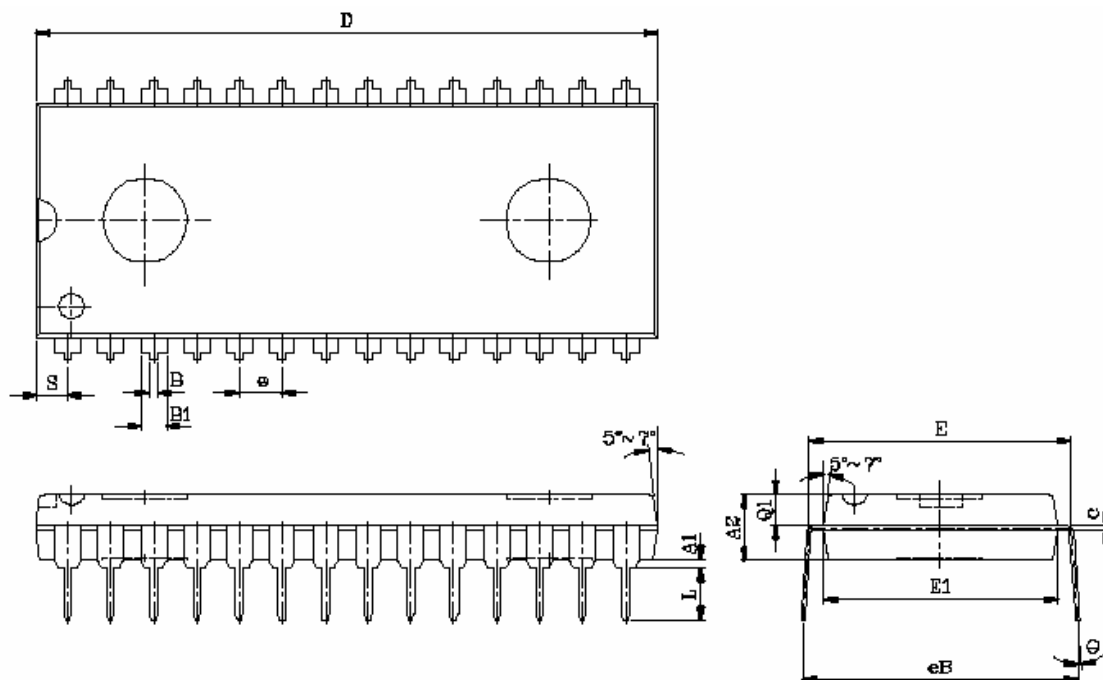


| UNIT SYM. | INCH.(BASE) | MM(REF) |
|---|---|---|
| A1 | 0.010 (MIN) | 0.254 (MIN) |
| A2 | 0.150±0.005 | 3.810±0.127 |
| B | 0.020 (MAX) | 0.508(MAX) |
| B1 | 0.055 (MAX) | 1.397(MAX) |
| c | 0.012 (MAX) | 0.304 (MAX) |
| D | 1.430 (MAX) | 36.322 (MAX) |
| E | 0.6 (TYP) | 15.24 (TYP) |
| E1 | 0.52 (MAX) | 13.208 (MAX) |
| e | 0.100 (TYP) | 2.540(TYP) |
| eB | 0.625 (MAX) | 15.87 (MAX) |
| L | 0.180(MAX) | 4.572(MAX) |
| S | 0.06 (MAX) | 1.524 (MAX) |
| Q1 | 0.08(MAX) | 2.032(MAX) |
| Θ | $15^{o}$(MAX) | $15^{o}$(MAX) |

**28 pin 330 mil SOP Package Outline Dimension**
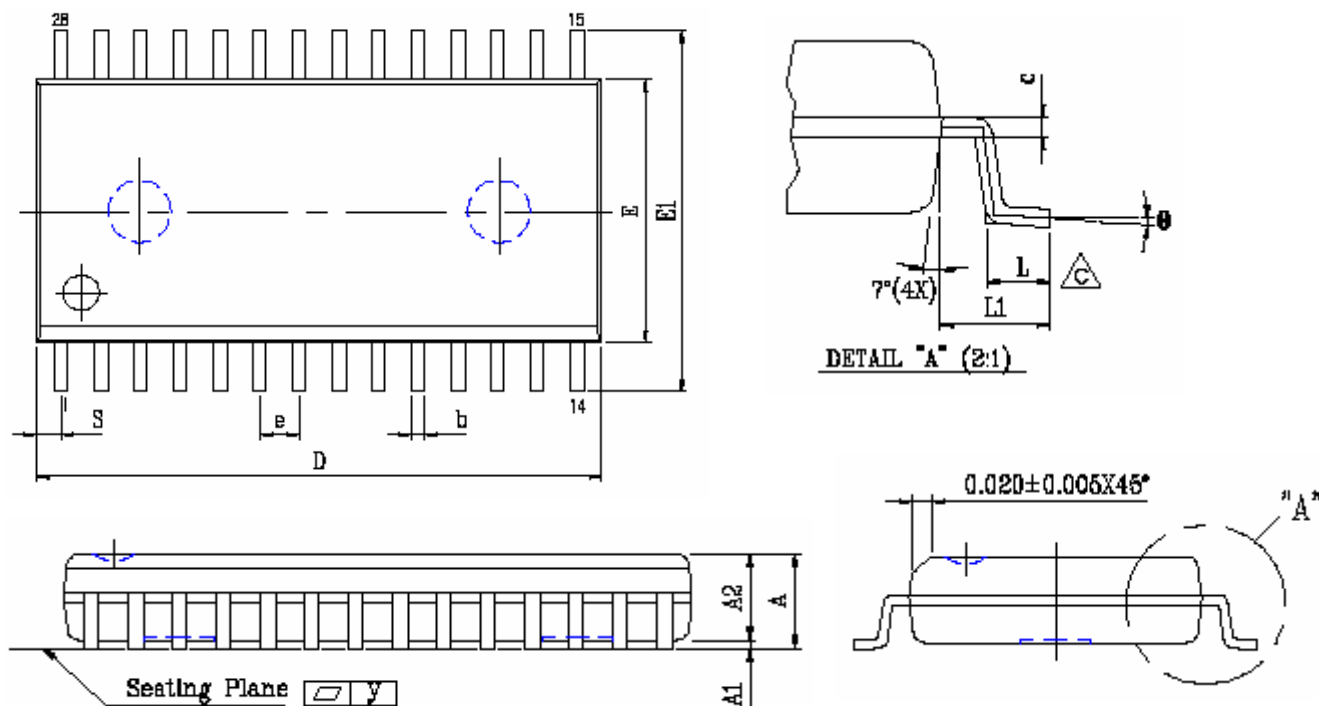


| UNIT<br>SYM. | INCH(BASE) | MM(REF) |
|---|---|---|
| A | 0.120 (MAX) | 3.048 (MAX) |
| A1 | 0.002(MIN) | 0.05(MIN) |
| A2 | 0.098±0.005 | 2.489±0.127 |
| b | 0.016 (TYP) | 0.406(TYP) |
| c | 0.010 (TYP) | 0.254(TYP) |
| D | 0.728 (MAX) | 18.491 (MAX) |
| E | 0.340 (MAX) | 8.636 (MAX) |
| E1 | 0.465±0.012 | 11.811±0.305 |
| e | 0.050 (TYP) | 1.270(TYP) |
| L | 0.05 (MAX) | 1.270 (MAX) |
| L1 | 0.067±0.008 | 1.702 ±0.203 |
| S | 0.047 (MAX) | 1.194 (MAX) |
| y | 0.003(MAX) | 0.076(MAX) |
| Θ | 0°∼10° | 0°∼10° |

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**32K X 8 BIT LOW POWER CMOS SRAM**

**28 pin 8mm x 13.4mm sTSOP Package Outline Dimension**
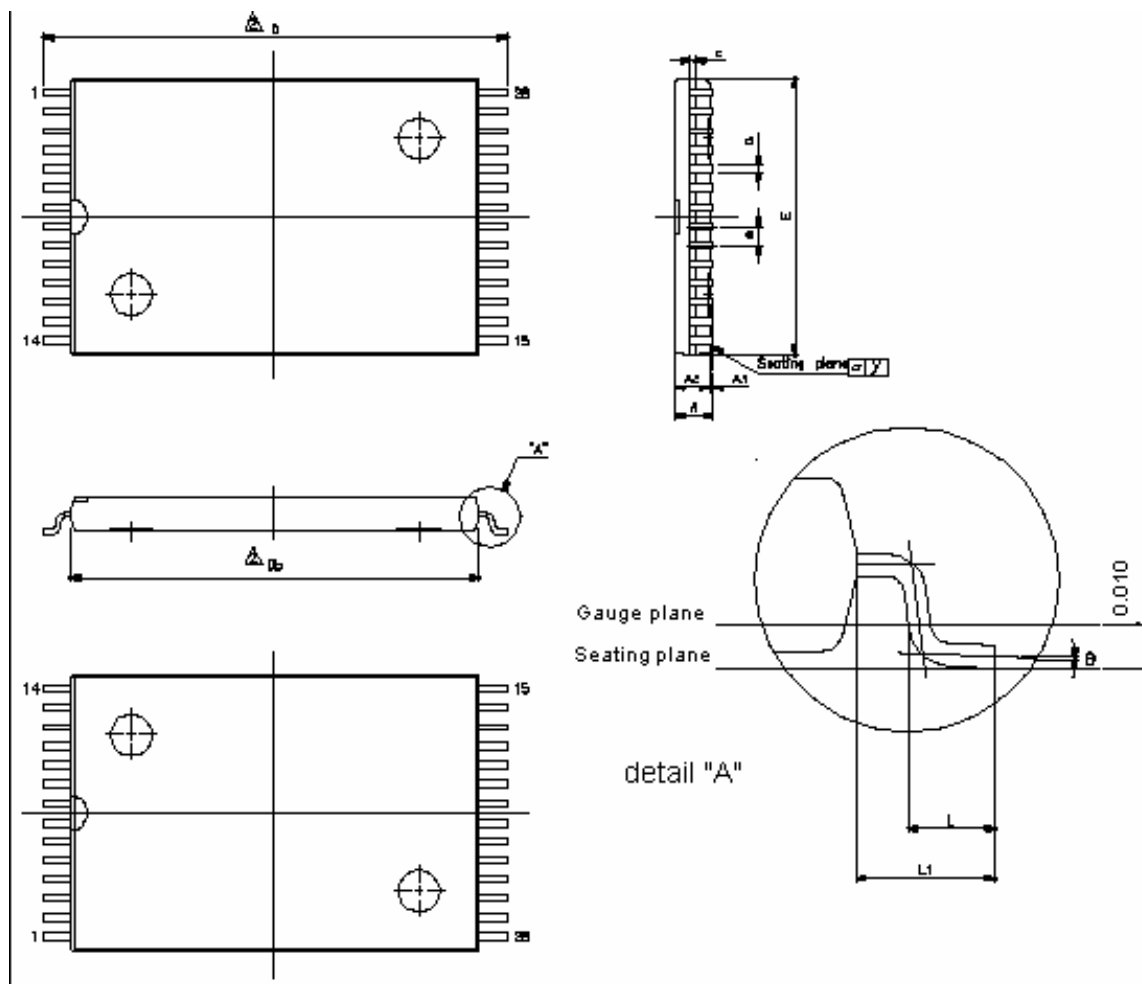


| UNIT SYM. | INCH(BASE) | MM(REF) |
|---|---|---|
| A | 0.047 (MAX) | 1.20 (MAX) |
| A1 | 0.004±0.002 | 0.10±0.05 |
| A2 | 0.039±0.002 | 1.00±0.05 |
| b | 0.006 (TYP) | 0.15(TYP) |
| c | 0.010 (TYP) | 0.254(TYP) |
| Db | 0.465±0.004 | 11.80±0.10 |
| E | 0.315±0.004 | 8.00±0.10 |
| e | 0.022 (TYP) | 0.55(TYP) |
| D | 0.528±0.008 | 13.40±0.20 |
| L | 0.020±0.004 | 0.50±0.10 |
| L1 | 0.0315±0.004 | 0.80±0.10 |
| y | 0.08(MAX) | 0.003(MAX) |
| Θ | 0°～5° | 0°～5° |

Note：E dimension is not including end flash. The total of both sides' end flash is not above 0.3mm.

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**32K X 8 BIT LOW POWER CMOS SRAM**

## ORDERING INFORMATION

Ordering Codes

| Alliance | Organization | VCC range | Package | Operating Temp | Speed ns |
|---|---|---|---|---|---|
| **AS6C62256-55PCN** | 32k x 8 | 2.7-5.5V | 28pin 600mil PDIP | Commercial ~ 0º C to 70º C | 55 |
| **AS6C62256-55SCN** | 32k x 8 | 2.7-5.5V | 28pin 330mil SOP | Commercial ~ 0º C to 70º C | 55 |
| **AS6C62256-55SIN** | 32k x 8 | 2.7-5.5V | 28pin 330mil SOP | Industrial ~ -40ºC to 85º C | 55 |
| **AS6C62256-55STCN** | 32k x 8 | 2.7-5.5V | 28pin sTSOP  (8 x 13.4 mm) | Commercial ~ 0º C to 70º C | 55 |
| **AS6C62256-55STIN** | 32k x 8 | 2.7-5.5V | 28pin sTSOP  (8 x 13.4 mm) | Industrial ~ -40ºC to 85º C | 55 |

Part numbering system

| AS6C | 62256 | - 55 | X | X | N |
|---|---|---|---|---|---|
| low power SRAM prefix | Device Number 62256 | Access Time | Package Options: P = 28 pin 600 mil P-DIP S = 28 pin 330 mil SOP ST = 28 pin sTSOP (8mm x 13.4 mm) | Temperature Range: C = Commercial (0ºC to +70º C) I = Industrial (-40º to +85º C) | N = Lead Free ROHS Compliant Part |

**Rev 1.2**
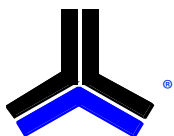
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Part Number: AS6C62256

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