MAX7319

I²C Port Expander with Eight Inputs and Maskable Transition Detection

General Description

The MAX7319 2-wire serial-interfaced peripheral fea-tures eight input ports with selectable internal pullups, overvoltage protection to +6V, and transition detection with interrupt output.

All input ports are continuously monitored for state changes (transition detection). Transitions are latched, allowing detection of transient changes. Any combination of inputs can be selected using the interrupt mask to assert the $\overline{INT}$ output. When the MAX7319 is subsequently accessed through the serial interface, any pending interrupt is cleared.

The +5.5V tolerant $\overline{RST}$ input clears the serial interface, terminating any I²C communication to or from the MAX7319.

The MAX7319 uses two address inputs with four-level logic to allow 16 I²C slave addresses. The slave address also enables or disables internal 40kΩ pullups in groups of four ports.

The MAX7319 supports hot insertion. All eight input ports, the serial interface SDA, SCL, AD0, AD2, $\overline{INT}$, and $\overline{RST}$ remain high impedance in power-down (V+ = 0) with up to +6V asserted on them.

The MAX7319 is one device in a family of pin-compatible port expanders with a choice of input ports, open-drain I/O ports, and push-pull output ports (see Table 1).

The MAX7319 is available in 16-pin QSOP and 16-pin TQFN packages, and is specified over the automotive temperature range (-40°C to +125°C).

Applications

- Cell Phones
- SAN/NAS
- Servers
- Notebooks
- Satellite Radio

Features

- 400kHz, +5.5V-Tolerant I²C Serial Interface
- +1.71V to +5.5V Operating Voltage
- Eight Input Ports with Maskable, Latching Transition Detection
- Input Ports are Overvoltage Protected to +6V
- Transient Changes are Latched, Allowing Detection Between Read Operations
- INT Output Alerts Change on Any Selection of Inputs
- AD0 and AD2 Inputs Select from 16 Slave Addresses
- Low 0.6µA (typ) Standby Current
- -40°C to +125°C Operating Temperature Range

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX7319AEE+	-40° TO +125°C	16 QSOP	—
MAX7319ATE+	-40° TO +125°C	16 TQFN-EP*	ADA

+Denotes a lead(Pb)-free/RoHS-compliant package.
*EP = Exposed pad.

Pin Configurations, Typical Application Circuit, and Functional Diagram appear at end of data sheet.

Selector Guide

PART	INPUTS	INTERRUPT MASK	OPEN-DRAIN OUTPUTS	PUSH-PULL OUTPUTS
MAX7319	8	Yes	—	—
MAX7320	—	—	—	8
MAX7321	Up to 8	—	Up to 8	—
MAX7322	4	Yes	—	4
MAX7323	Up to 4	—	Up to 4	4
MAX7328*	Up to 8	—	Up to 8	—
MAX7329**		—		—

*Second source to PCF8574.
**Second source to PCF8574A.

maxim integrated™

I²C Port Expander with Eight Inputs and Maskable Transition Detection

Absolute Maximum Ratings

(All voltages referenced to GND.)

Supply Voltage V+ ....-0.3V to +6V
SCL, SDA, AD0, AD2, RST, INT, I0–I7 ....-0.3V to +6V
SDA Input Current 10mA
INT Input Current..10mA
Total V+ Current 50mA
Total GND Current 100mA

Continuous Power Dissipation (TA = +70°C)
   16-Pin QSOP (derate 8.3mW/°C over +70°C)............667mW
   16-Pin TQFN (derate 15.6mW/°C over +70°C) 1250mW
Operating Temperature Range......................... -40°C to +125°C
Junction Temperature...+150°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V+ = +1.71V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V+ = +3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage	V+		1.71		5.50	V
Power-On Reset Voltage	V_{POR}				1.6	V
Standby Current (Interface Idle)	I_{STB}	SCL and SDA and other digital inputs at V+		0.6	1.5	µA
Supply Current (Interface Running)	I+	f_{SCL} = 400kHz; other digital inputs at V+		23	55	µA
Input High Voltage SDA, SCL, AD0, AD2, RST, I0–I7	V_{IH}	V_+ < 1.8V	0.8 x V+			V
		V_+ ≥ 1.8V	0.7 x V+			
Input Low Voltage SDA, SCL, AD0, AD2, RST, I0–I7	V_{IL}	V_+ < 1.8V			0.2 x V+	V
		V_+ ≥ 1.8V			0.3 x V+	
Input Leakage Current SDA, SCL, AD0, AD2, RST, I0–I7	I_{IH}, I_{IL}	SDA, SCL, AD0, AD2, RST, I0–I7 at V+ or GND	-0.2		+0.2	µA
Input Capacitance SDA, SCL, AD0, AD2, RST, I0–I7				10		pF
Output Low Voltage SDA	V_{OLSDA}	I_{SINK} = 6mA			250	mV
Output Low Voltage INT	$V_{OL\overline{INT}}$	I_{SINK} = 5mA		100	250	mV
Port Input Pullup Resistor	R_{PU}		25	40	55	kΩ

Port and Interrupt $\overline{\text{INT}}$ Timing Characteristics

(V+ = +1.71V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V+ = +3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Port Input Setup Time	t_{PSU}	$C_L \le 100pF$	0			µs
Port Input Hold Time	t_{PH}	$C_L \le 100pF$	4			µs
$\overline{\text{INT}}$ Input Data Valid Time	t_{IV}	$C_L \le 100pF$			4	µs
$\overline{\text{INT}}$ Reset Delay Time from STOP	t_{IP}	$C_L \le 100pF$			4	µs
$\overline{\text{INT}}$ Reset Delay Time from Acknowledge	t_{IR}	$C_L \le 100pF$			4	µs

Timing Characteristics

(V+ = +1.71V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V+ = +3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial-Clock Frequency	f_{SCL}				400	kHz
Bus Free Time Between a STOP and a START Condition	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD, STA}$		0.6			µs
Repeated START Condition Setup Time	$t_{SU, STA}$		0.6			µs
STOP Condition Setup Time	$t_{SU, STO}$		0.6			µs
Data Hold Time	$t_{HD, DAT}$	(Note 2)			0.9	µs
Data Setup Time	$t_{SU, DAT}$		100			ns
SCL Clock Low Period	t_{LOW}		1.3			µs
SCL Clock High Period	t_{HIGH}		0.7			µs
Rise Time of Both SDA and SCL Signals, Receiving	t_R	(Notes 3, 4)		20 + 0.1C_b	300	ns
Fall Time of Both SDA and SCL Signals, Receiving	t_F	(Notes 3, 4)		20 + 0.1C_b	300	ns
Fall Time of SDA, Transmitting	$t_{F,TX}$	(Notes 3, 4)		20 + 0.1C_b	250	ns
Pulse Width of Spike Suppressed	t_{SP}	(Note 5)		50		ns
Capacitive Load for Each Bus Line	C_b	(Note 3)			400	pF
$\overline{\text{RST}}$ Pulse Width	t_W		500			ns
$\overline{\text{RST}}$ Rising to START Condition Setup Time	$t_{\overline{\text{RST}}}$		1			µs

Note 1: All parameters are tested at T_A = +25°C. Specifications over temperature are guaranteed by design.
Note 2: A master device must provide a hold time of at least 300ns for the SDA signal (referred to V_{IL} of the SCL signal) to bridge the undefined region of SCL's falling edge.
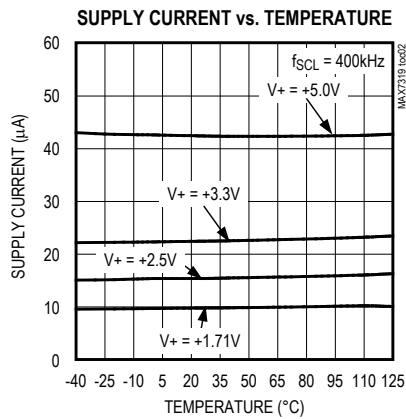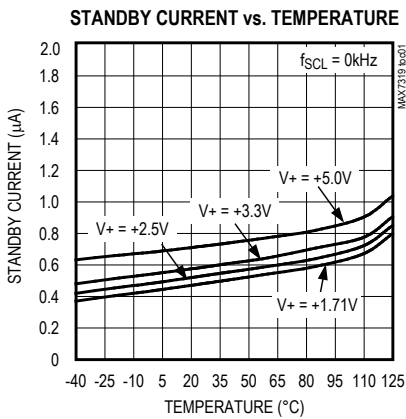**Note 3:** Guaranteed by design.
Note 4: C_b = total capacitance of one bus line in pF. t_R and t_F measured between 0.3 x V+ and 0.7 x V+, $I_{SINK} \le 6mA$.
Note 5: Input filters on the SDA and SCL inputs suppress noise spikes less than 50ns.

Typical Operating Characteristics

(T$_A$ = +25°C, unless otherwise noted.)

STANDBY CURRENT vs. TEMPERATURE

f$_{SCL}$ = 0kHz

V+ = +5.0V
V+ = +3.3V
V+ = +2.5V
V+ = +1.71V

STANDBY CURRENT (µA)
TEMPERATURE (°C)

MAX7319 toc01

SUPPLY CURRENT vs. TEMPERATURE

f$_{SCL}$ = 400kHz
V+ = +5.0V

V+ = +3.3V
V+ = +2.5V
V+ = +1.71V

SUPPLY CURRENT (µA)
TEMPERATURE (°C)

MAX7319 toc02

Pin Description

PIN		NAME	FUNCTION
QSOP	TQFN		
1, 3	15, 1	AD0, AD2	Address Inputs. Select device slave address with AD0 and AD2. Connect AD0 and AD2 to either GND, V+, SCL, or SDA to give four logic combinations (see Table 3).
2	16	$\overline{RST}$	Reset Input, Active Low. Drive $\overline{RST}$ low to clear the 2-wire interface.
4–7, 9–12	2–5, 7–10	I0–I7	Input Ports. I0 to I7 are CMOS logic inputs protected to +6V.
8	6	GND	Ground
13	11	$\overline{INT}$	Interrupt Output, Active Low. $\overline{INT}$ is an open-drain output rated at +6V.
14	12	SCL	I²C-Compatible Serial Clock Input
15	13	SDA	I²C-Compatible Serial Data I/O
16	14	V+	Positive Supply Voltage. Bypass V+ to GND with a ceramic capacitor of at least 0.047µF.
—	EP	EP	Exposed Pad. Connect exposed pad to GND.

Detailed Description

MAX7319–MAX7329 Family Comparison

The MAX7319–MAX7323 family consists of five pin-compatible, eight-port expanders. Each version is optimized for different applications. The MAX7328 and MAX7329 are second sources to the PCF8574 and PCF8574A.

The MAX7324–MAX7327 family consists of four pin-compatible, 16-port expanders that integrate the functions of the MAX7320 and one of either the MAX7319, MAX7321, MAX7322, or MAX7323.

Functional Overview

The MAX7319 is a general-purpose port expander, operating from a +1.71V to +5.5V supply that provides eight CMOS input ports that are overvoltage protected to +6V independent of supply voltage.

The MAX7319 is set to one of 16 I²C slave addresses (0x60 to 0x6F) using the address-select inputs AD2 and AD0, and is accessed over an I²C serial interface. The $\overline{RST}$ input clears the serial interface in case of a hung bus, terminating any serial transaction to or from the MAX7319.

The input ports offer latching transition detection functionality. All input ports are continuously monitored

Table 1. MAX7319–MAX7329 Family Comparison

PART	I²C SLAVE ADDRESS	INPUTS	INPUT INTERRUPT MASK	OPEN-DRAIN OUTPUTS	PUSH-PULL OUTPUTS	APPLICATION
8-PORT EXPANDERS						
MAX7319	110xxxx	8	Yes	—	—	Input-only versions: Eight input ports with programmable latching transition detection interrupt and selectable pullups. Offers maximum versatility for automatic input monitoring. An interrupt mask selects which inputs cause an interrupt on transitions, and transition flags identify which inputs have changed (even momentarily) since the ports were last read.
MAX7320	101xxxx	—	—	—	8	Output-only versions: Eight push-pull outputs with selectable power-up default levels Push-pull outputs offer faster rise time than open-drain outputs, and require no pullup resistors.
MAX7321	110xxxx	Up to 8	—	Up to 8	—	I/O versions: Eight open-drain I/O ports with latching transition detection interrupt and selectable pullups. Open-drain outputs can level shift the logic-high State to a higher or lower voltage than V+ using external pullup resistors. Any port can be used as an input by setting the open-drain output to logic-high. Transition flags identify which inputs have changed (even momentarily) since the ports were last read.
MAX7322	110xxxx	4	Yes	—	4	Four input-only, four output-only versions: Four input ports with programmable latching transition detection interrupt and selectable pullups. Four push-pull outputs with selectable power-up default levels.

Table 1. MAX7319–MAX7329 Family Comparison (continued)

PART	I²C SLAVE ADDRESS	INPUTS	INPUT INTERRUPT MASK	OPEN-DRAIN OUTPUTS	PUSH-PULL OUTPUTS	APPLICATION
MAX7323	110xxxx	Up to 4	—	Up to 4	4	Four I/O, four output-only versions: Four open-drain I/O ports with latching transition detection interrupt and selectable pullups. Four push-pull outputs with selectable power-up default levels.
MAX7328 MAX7329	0100xxx 0111xxx	Up to 8	—	Up to 8	—	PCF8574-, PCF8574A-compatible versions: Eight open-drain I/O ports with nonlatching transition detection interrupt and pullups on all ports. All ports power up as inputs (or logic-high outputs). Any port can be used as an input by setting the open-drain output to logic-high.
16-PORT EXPANDERS						
MAX7324	101xxxx And 110xxxx	8	Yes	—	8	Software equivalent to a MAX7320 plus a MAX7321.
MAX7325		Up to 8	—	Up to 8	8	Software equivalent to a MAX7320 plus a MAX7319.
MAX7326		4	Yes	—	12	Software equivalent to a MAX7320 plus a MAX7322.
MAX7327		Up to 4	—	Up to 4	12	Software equivalent to a MAX7320 plus a MAX7323.

for changes. An input change sets one of eight flag bits that identify changed input(s). All flags are cleared upon a subsequent read or write transaction to the MAX7319.

A latching interrupt output, $\overline{INT}$, is programmed to flag input data changes on input ports through an interrupt mask register. By default, data changes on any input port force $\overline{INT}$ to a logic-low. The interrupt output, $\overline{INT}$, and all transition flags are cleared when the MAX7319 is next accessed through the serial interface.

Internal pullup resistors to V+ are selected by the address-select inputs, AD0 and AD2. Pullups are enabled on the input ports in groups of four (see Table 3).

Initial Power-Up

On power-up, the transition detection logic is reset, and $\overline{INT}$ is released to a high-impedance state. The interrupt mask register is set to 0xFF, enabling the interrupt output for transitions on all eight input ports. The transition flags are cleared to indicate no data changes.

$\overline{RST}$ Input

The $\overline{RST}$ input voids any I²C transaction involving the MAX7319, forcing the MAX7319 into the I²C STOP condition. A reset does not affect the interrupt output ($\overline{INT}$) or change the contents of the interrupt mask register. $\overline{RST}$ is overvoltage tolerant to +6V.

Standby Mode

When the serial interface is idle, the MAX7319 automatically enters standby mode, drawing minimal supply current.

Slave Address and Input Pullup Selection

Address inputs AD0 and AD2 determine the MAX7319 slave address and select which inputs have pullup resistors. Pullups are enabled on the input ports in groups of four (see Table 3). The MAX7319, MAX7321, MAX7322, and MAX7323 use a different range of slave addresses (110xxxx) than the MAX7320 (101xxxx).

The MAX7319 slave address is determined on each I²C transmission, regardless of whether the transmission is actually addressing the MAX7319. The MAX7319 distinguishes whether address inputs AD2 and AD0 are connected to SDA or SCL instead of fixed logic levels V+ or GND during this transmission. This means that the MAX7319 slave address can be configured dynamically in the application without cycling the device supply.

On initial power-up, the MAX7319 cannot decode the address inputs AD2 and AD0 fully until the first I²C transmission. AD0 and AD2 initially appear to be connected to V+ or GND. This is important because the address selection determines which inputs have pullups applied. However, at power-up, the I²C SDA and SCL bus interface lines are high impedance at the pins of every device (master or slave) connected to the bus, including the MAX7319. This is guaranteed as part

Table 2. Read and Write Access to Eight-Port Expander Family

PART	I2C SLAVE ADDRESS	INPUTS	INTERRUPT MASK	OPEN-RAIN OUTPUTS	PUSH-PULL OUTPUTS	I2C DATA WRITE	I2C DATA READ
MAX7319	110xxxx	8	Yes	—	—	<I7–I0 interrupt mask>	<I7–I0 port inputs> <I7–I0 transition flags>
MAX7320	101xxxx	—	—	—	8	<O7–O0 port outputs>	<O7–O0 port inputs>
MAX7321	110xxxx	Up to 8	—	Up to 8	—	<P7–P0 port outputs>	<P7–P0 port inputs> <P7–P0 transition flags>
MAX7322	110xxxx	4	Yes	—	4	<O7, O6 outputs, I5–I2 interrupt mask, O1, O0 outputs>	<O7, O6, I5–I2, O1, O0 Port inputs> <0, 0, I5–I2 transition flags, 0, 0>
MAX7323	110xxxx	Up to 4	—	Up to 4	4	<port outputs>	<O7, O6, P5–P2, O1, O0 Port inputs> <0, 0, P5–P2 transition flags, 0, 0>
MAX7328	0100xxx	Up to 8	—	Up to 8	—	<P7–P0 port outputs>	<P7–P0 port inputs>
MAX7329	0111xxx	Up to 8	—	Up to 8	—	<P7–P0 port outputs>	<P7–P0 port inputs>

of the I2C specification. Therefore, address inputs AD2 and AD0 that are connected to SDA or SCL normally appear at power-up to be connected to V+. The pullup selection logic uses AD0 to select whether pullups are enabled for ports I3–I0, and uses AD2 to select whether pullups are enabled for ports I7–I4. The rule is that a logic-high SDA or SCL connection selects the pullups, while a logic-low deselects the pullups (Table 3). The pullup configuration is correct on power-up for a standard I2C configuration, where SDA and SCL are pulled up to V+ by the external I2C pullup resistors.

There are circumstances where the assumption that SDA = SCL = V+ on power-up is not true, for example, in true hot-swap applications, in which there is legitimate bus activity during power-up. Also, if SDA and SCL are terminated with pullup resistors to a different supply voltage than the MAX7319's supply voltage, and if that pullup supply rises later than the MAX7319's supply, then SDA or SCL may appear at power-up to be connected to GND. In such applications, use the four address combinations that are selected by connecting address inputs AD2 and AD0 to V+ or GND (shown in bold in Table 3). These selections are guaranteed to be correct at power-up, independent of SDA and SCL

behavior. If one of the other 12 address combinations is used, be aware that an unexpected combination of pullups might be asserted until the first I2C transmission (to any device, not necessarily the MAX7319) is put on the bus.

Port Inputs

Port inputs switch at CMOS logic levels as determined by the expander's supply voltage, and are overvoltage tolerant to +6V, independent of the expander's supply voltage.

Port-Input Transition Detection

All eight input ports are monitored for changes since the expander was last accessed through the serial interface. The state of the input ports is stored in an internal "snapshot" register for transition monitoring. The snapshot is continuously compared with the actual input conditions, and if a change is detected for any port input, an internal transition flag is set for that port. The eight port inputs are sampled (internally latched into the snapshot register) and the old transition flags cleared during the I2C acknowledge of every MAX7319 read and write access. The previous port transition flags are read through the serial interface as the second byte of a 2-byte read sequence.

Table 3. MAX7319 Address Map

PIN CONNECTION		DEVICE ADDRESS							40kΩ INPUT PULLUP ENABLED							
AD2	AD0	A6	A5	A4	A3	A2	A1	A0	I7	I6	I5	I4	I3	I2	I1	I0
SCL	GND	1	1	0	0	0	0	0	Y	Y	Y	Y	—	—	—	—
SCL	V+	1	1	0	0	0	0	1	Y	Y	Y	Y	Y	Y	Y	Y
SCL	SCL	1	1	0	0	0	1	0	Y	Y	Y	Y	Y	Y	Y	Y
SCL	SDA	1	1	0	0	0	1	1	Y	Y	Y	Y	Y	Y	Y	Y
SDA	GND	1	1	0	0	1	0	0	Y	Y	Y	Y	—	—	—	—
SDA	V+	1	1	0	0	1	0	1	Y	Y	Y	Y	Y	Y	Y	Y
SDA	SCL	1	1	0	0	1	1	0	Y	Y	Y	Y	Y	Y	Y	Y
SDA	SDA	1	1	0	0	1	1	1	Y	Y	Y	Y	Y	Y	Y	Y
GND	**GND**	**1**	**1**	**0**	**1**	**0**	**0**	**0**	—	—	—	—	—	—	—	—
GND	**V+**	**1**	**1**	**0**	**1**	**0**	**0**	**1**	—	—	—	—	**Y**	**Y**	**Y**	**Y**
GND	SCL	1	1	0	1	0	1	0	—	—	—	—	Y	Y	Y	Y
GND	SDA	1	1	0	1	0	1	1	—	—	—	—	Y	Y	Y	Y
V+	**GND**	**1**	**1**	**0**	**1**	**1**	**0**	**0**	**Y**	**Y**	**Y**	**Y**	—	—	—	—
V+	**V+**	**1**	**1**	**0**	**1**	**1**	**0**	**1**	**Y**	**Y**	**Y**	**Y**	**Y**	**Y**	**Y**	**Y**
V+	SCL	1	1	0	1	1	1	0	Y	Y	Y	Y	Y	Y	Y	Y
V+	SDA	1	1	0	1	1	1	1	Y	Y	Y	Y	Y	Y	Y	Y

A long read sequence (more than 2 bytes) can be used to poll the expander continuously without the overhead of resending the slave address. If more than 2 bytes are read from the expander, the expander repeatedly returns the input port data followed by the transition flags. The inputs are repeatedly resampled and the transition flags repeatedly reset for each pair of bytes read. All changes that occur during a long read sequence are detected and reported.

The MAX7319 includes an 8-bit interrupt mask register that selects which inputs generate an interrupt upon change. Each input's transition flag is set when its input changes, independent of the interrupt mask register settings. The interrupt mask register allows the processor to be interrupted for critical events, while the inputs and the transition flags can be polled periodically to detect less critical events.

The INT logic ensures that unnecessary interrupts are not asserted, yet data transitions are detected and reported regardless of when the transition occurs. The INT output is not reasserted during a read sequence to avoid recursive reentry into an interrupt service routine. If transition occurs during read sequence, the INT assertion is delayed until the STOP condition, however, INT is not reasserted upon a STOP condition if the changed input data is read before the STOP occurs.

Transition-Detection Masks

The transition-detection logic incorporates a transition flag and an interrupt mask bit for each input port. The eight change flags can be read through the serial interface, and the 8-bit interrupt mask is set through the serial interface.

Each port's transition flag is set when that port's input changes, and the transition flag remains set even if the input returns to its original state. The port's interrupt mask determines whether a transition on that input port generates an interrupt. Enable interrupts for high-priority inputs using the interrupt mask. The interrupt allows the system to respond quickly to changes on these inputs. Poll the MAX7319 periodically to monitor less-important inputs. The transition flags indicate whether a permanent or transient change has occurred on any input since the MAX7319 was last accessed.

Serial Interface

Serial Addressing

The MAX7319 operates as a slave that sends and receives data through an I2C interface. The interface uses a serial data line (SDA) and a serial clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). The master initiates all data transfers to and from the MAX7319 and generates the SCL clock that synchronizes the data transfer (Figure 1).
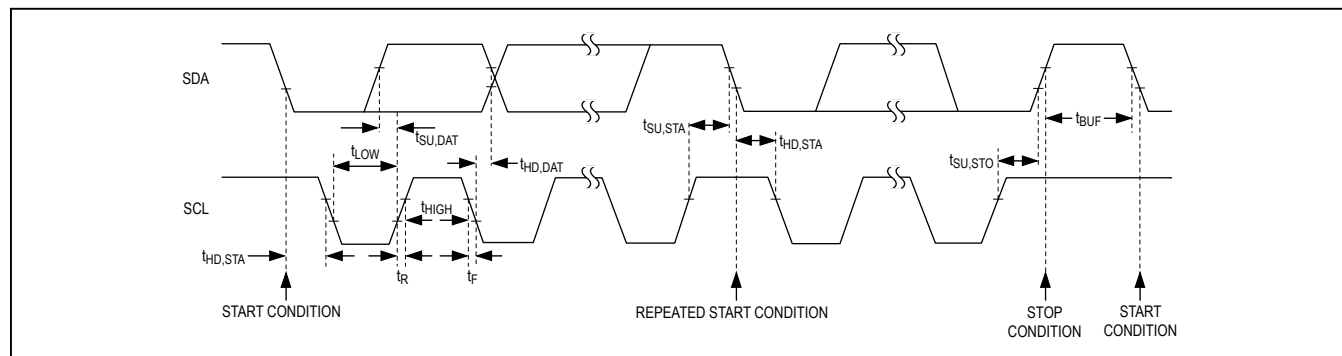
Figure 1. 2-Wire Serial-Interface Timing Details

SDA operates as both an input and an open-drain output. A pullup resistor, typically 4.7kΩ, is required on SDA. SCL operates only as an input. A pullup resistor, typically 4.7kΩ, is required on SCL if there are multiple masters on the 2-wire interface, or if the master in a single-master system has an open-drain SCL output.

Each transmission consists of a START condition sent by a master, followed by the MAX7319's 7-bit slave address plus R/$\overline{W}$ bit, then 1 or more data bytes, and finally a STOP condition (Figure 2).

Start and Stop Conditions
Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, the master issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission (Figure 2).
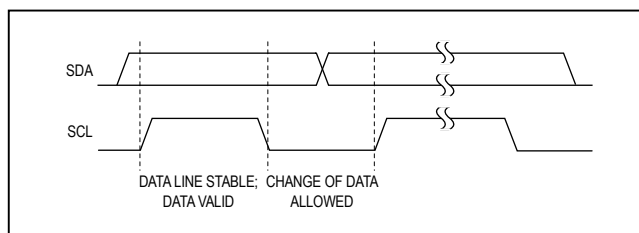
Bit Transfer
One data bit is transferred during each clock pulse. The data on SDA must remain stable while SCL is high (Figure 3).

Acknowledge
The acknowledge bit is a clocked 9th bit the recipient uses to acknowledge receipt of each byte of data (Figure 4). Each byte transferred effectively requires 9 bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse, so the SDA line is stable low during the high period of the clock pulse. When the master is transmitting to the MAX7319, the MAX7319 generates the acknowledge bit because the device is the recipient.

Figure 2. Start and Stop Conditions

Figure 3. Bit Transfer
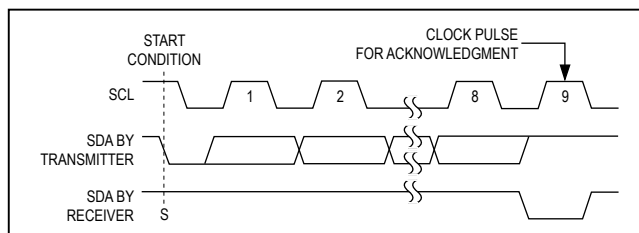
Figure 4. Acknowledge

When the MAX7319 is transmitting to the master, the master generates the acknowledge bit because the master is the recipient.

Slave Address

The MAX7319 has a 7-bit slave address (Figure 5). The 8th bit following the 7-bit slave address is the R/$\overline{W}$ bit. It is low for a write command, and high for a read command.

The 1st (A6), 2nd (A5), and 3rd (A4) bits of the MAX7319 slave address are always 1, 1, and 0. Connect AD2 and AD0 to GND, V+, SDA, or SCL to select slave address bits A3, A2, A1, and A0. The MAX7319 has 16 possible slave addresses (Table 3), allowing up to 16 MAX7319 devices on an I²C bus

Accessing the MAX7319

I²C-interface access to the MAX7319 is summarized as follows (Table 2):

A **single-byte read** from the MAX7319 returns the status of the eight input ports, and clears both the internal transition flags and the $\overline{INT}$ output (Figure 7).

A **2-byte read** returns the status of the eight input ports (as for a single-byte read), followed by the transition flags. The internal transition flags and the $\overline{INT}$ output are cleared when the MAX7319 acknowledges the slave address byte, but the previous transition flag data is sent as the second byte (Figure 8).

A **multibyte read** (more than 2 bytes before the I²C STOP bit) repeatedly returns the input port data, alternating with the transition flags. As the input data is resampled for each transmission, and the transition flags are reset each time, a multibyte read continuously returns the current data and identifies any changing input ports.

If a port input data change occurs during the read sequence, $\overline{INT}$ is reasserted after the I²C STOP bit. The MAX7319 does not generate another interrupt during a single-byte or multibyte read.
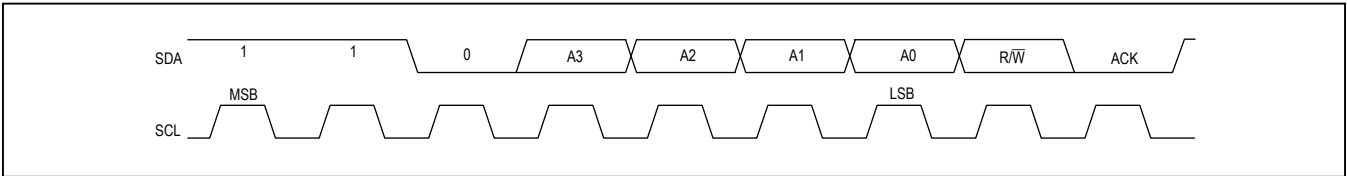
Figure 5. Slave Address
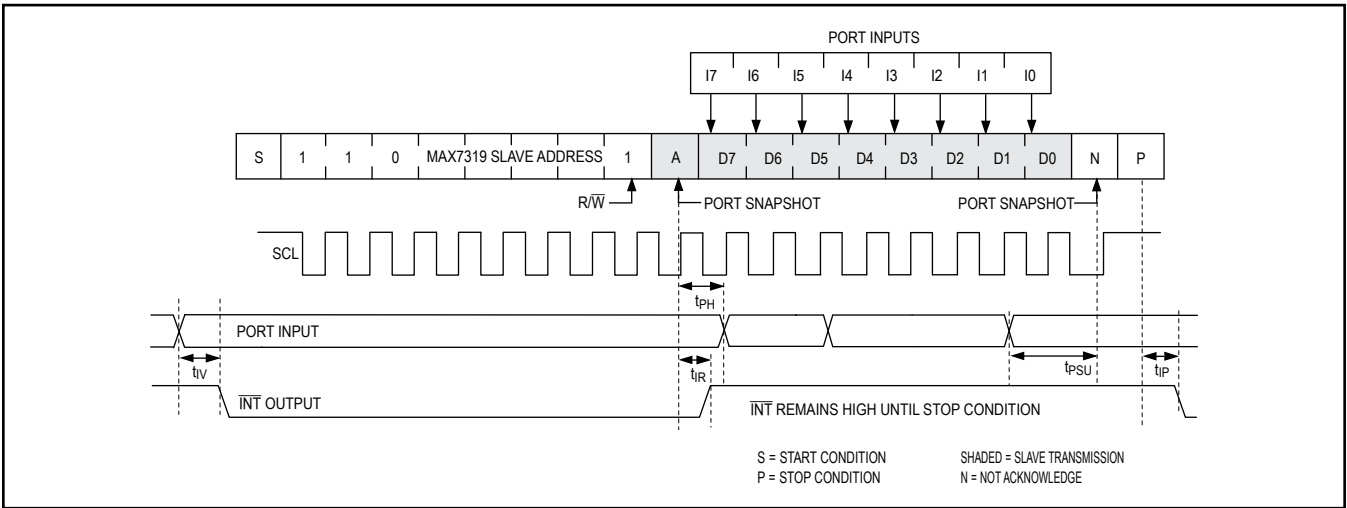
Figure 6. Reading from the MAX7319 (1 Data Byte)

Input port data is sampled during the preceding I²C acknowledge bit (the acknowledge bit for the I²C slave address in the case of a single-byte or 2-byte read).

A **single-byte** write to the MAX7319 sets the interrupt mask register, and clears both the internal transition flags and the INT output.

A **multibyte write** to the MAX7319 sets the interrupt mask register repeatedly.

Reading from the MAX7319

A read from the MAX7319 starts with the master transmitting the MAX7319's slave address with the R/W̄ bit set high. The MAX7319 acknowledges the slave address and samples the input ports during acknowledge bit. INT deasserts during the slave address acknowledge.

Typically, the master reads 1 or 2 bytes from the MAX7319, with each byte, except the last one, being acknowledged by the master upon reception.

When the master reads 1 byte from the MAX7319 and subsequently issues a STOP condition (Figure 6), the MAX7319 transmits the current port data, clears the transition flags, and resets the transition detection. INT deasserts during the slave address acknowledge. The new snapshot data is the current port data transmitted to the master; therefore, port transitions ocurring during the transmission are detected. INT remains high until the STOP condition.

When the master reads 2 bytes from the MAX7319 and subsequently issues a STOP condition (Figure 7), the MAX7319 transmits the current port data, followed by the transition flags. The transition flags are cleared, and transition detection reset. INT deasserts during the slave address acknowledge. The new snapshot data is the current port data transmitted to the master; therefore, port transitions occurring during the transmission are detected. INT remains high until the STOP condition. When the master reads more than 2 bytes, the input port data alternates with the transition flag.
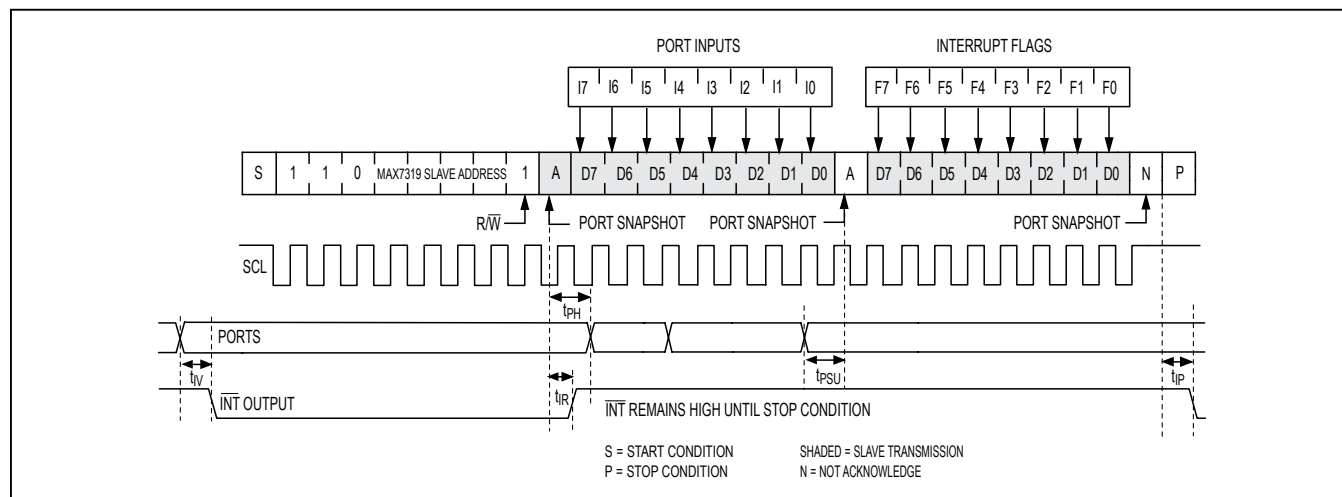

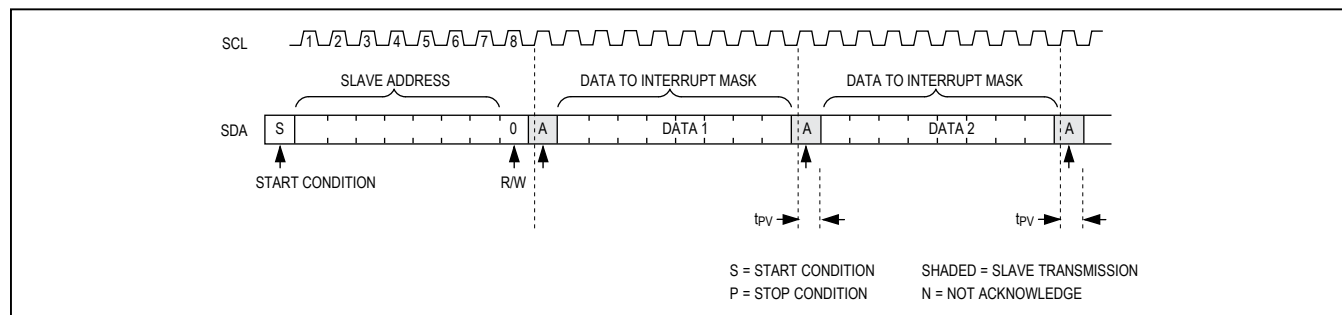*Figure 7. Reading from the MAX7319 (2 Data Bytes)*

Figure 8. Writing to the MAX7319

Writing to the MAX7319

A write to the MAX7319 starts with the master transmitting the MAX7319's slave address with the R/$\overline{W}$ bit set low. The MAX7319 acknowledges the slave address, and samples the input ports during the acknowledge bit. $\overline{INT}$ deasserts during the slave address acknowledge. The master can now transmit 1 or more bytes of data. The MAX7319 acknowledges these subsequent bytes of data and updates the interrupt mask register with each new byte until the master issues a STOP condition (Figure 8).

Applications Information

Port Input and I²C Interface Level Translation from Higher or Lower Logic Voltages

The MAX7319 I2C interface (SDA, SCL, AD0, AD2), reset input $\overline{RST}$, interrupt output $\overline{INT}$, and the eight input ports I0–I7 are overvoltage protected to +6V independent of V+. This allows the MAX7319 to operate from a lower supply voltage, such as +3.3V, while the I2C interface and/or any of the eight input ports are driven from a higher logic level, such as +5V.

The MAX7319 can operate from a higher supply voltage, such as +3V, while the I2C interface and/or some of the input ports I0–I7 are driven from a lower logic level, such as +2.5V. Apply a minimum voltage of 0.7 x V+ to assert a logic-high on any input. For example, a MAX7319 operating from a +5V supply may not recognize a +3.3V nominal logic-high. One solution for input level translation is to drive the MAX7319 inputs from open-drain outputs. Use a pullup resistor to V+ or a higher supply to ensure a high logic voltage of greater than 0.7 x V+.

Hot Insertion

$\overline{RST}$, SCL, SDA, AD0, and AD2 remain high impedance with up to +6V asserted on them when the MAX7319 is powered down (V+ = 0). The MAX7319 can therefore be used in hot-swap applications.

Each of the input ports I0–I7 has a protection diode to GND (Figure 9). When a port input is driven to a voltage lower than GND, the protection diode clamps the voltage to a diode drop below GND.

Each of the input ports I0–I7 also has a 40kΩ (typ) pullup resistor that can be enabled or disabled. When a port input is driven to a voltage higher than V+, the body diode of the pullup enable switch conducts and the 40kΩ pullup resistor is enabled. When the MAX7319 is powered down (V+ = 0), every input port appears as a 40kΩ resistor in series with a diode connected to GND. Input ports are protected to +6V under any of these circumstances (Figure 9).
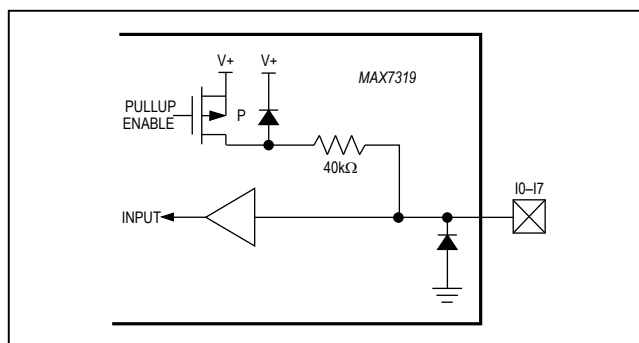

Figure 9. Input Port Structure

Power-Supply Considerations

The MAX7319 operates with a +1.71V to +5.5V supply voltage over the -40°C to +125°C temperature range. Bypass V+ to GND with a ceramic capacitor of at least 0.047µF as close to the device as possible. For the TQFN version, connect the exposed pad to GND.

## Compatibility with MAX6965, MAX7315, and MAX7316

The MAX7319 is subset pin compatible with the MAX6965, MAX7315, and MAX7316. The pin differences are shown in Table 4. The MAX7319 is not software compatible with MAX6965, MAX7315, or MAX7316. In many cases, it is possible to design a PC board to work with all these port expanders, providing design flexibility.

Table 4. MAX7319, MAX6965, MAX7315, and MAX7316 Pin Compatibility

PIN-PACKAGE		PIN FUNCTION		
16 QSOP	16 TQFN	MAX7319	MAX7315	MAX6965 AND MAX7316
1	15	AD0	AD0	BLINK
2	16	$\overline{RST}$	AD1	$\overline{RST}$
3	1	AD2	AD2	AD0

Pin Configurations
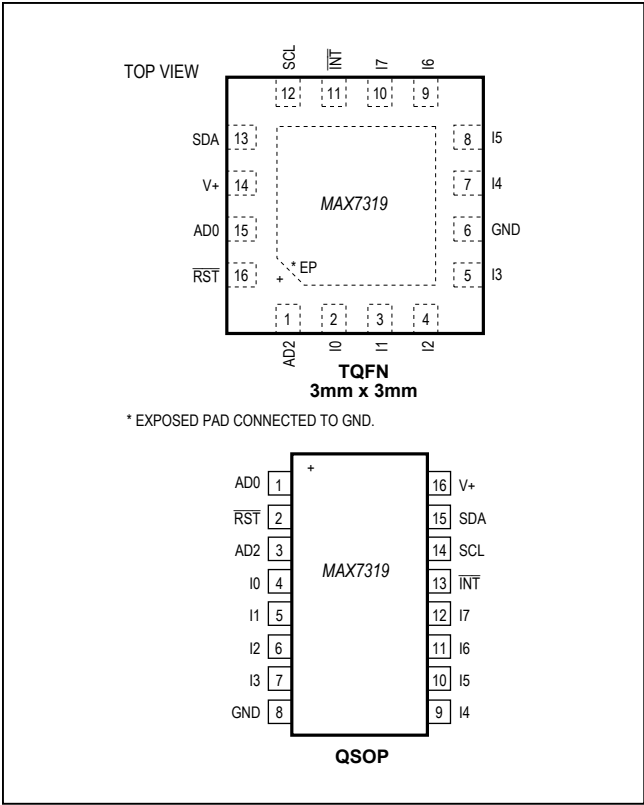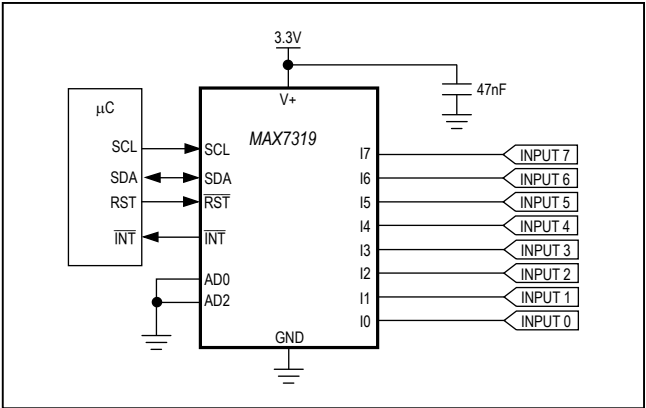
Typical Application Circuit

Functional Diagram
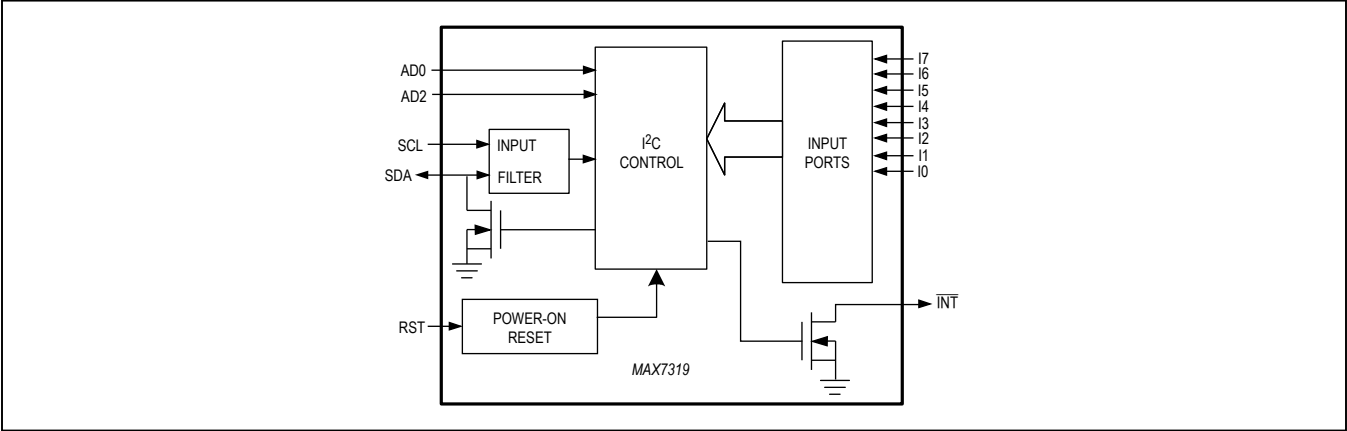
Chip Information

PROCESS: BiCMOS

CONNECT EXPOSED PAD TO GND

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 QSOP	E16+4	**21-0055**	**90-0167**
16 TQFN-EP	T1633+4	**21-0136**	**90-0031**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
2	5/14	No /V OPNs; removed automotive reference from *Applications* section; updated *Packaging Information*	1