MachXO3L Breakout Board Evaluation Kit

User Guide

January 2015
EB94_1.1

Introduction

The MachXO3L Breakout Board Evaluation Kit focuses on providing an environment to evaluate high speed source synchronous interfaces with the Lattice MachXO3L-2100 and MachXO3L-6900 products in both 49-ball WLCSP and 256-ball caBGA packages respectively.

The MachXO3L Breakout Board contains two sections for development. The first section of the board features the MachXO3L-2100 which is optimized for MIPI D-PHY receiver and MIPI D-PHY transmitter interfaces with up to four data lanes and one clock lane each. The second section of the board features the MachXO3L-6900. This section provides a flexible IO evaluation environment for MIPI D-PHY, SubLVDS, FPD-LINK, FPC-LINK as well as other source synchronous type protocols. The IO of the MachXO3L-6900 provides eight high speed data and two high speed clock interfaces in both transmit and receive directions. Connection to these interfaces is available through SMAs for signal integrity and performance evaluation.

Evaluation Kit Contents

- MachXO3L Breakout Board
- Pre-loaded Demo
- Mini USB Cable
- QuickStart Guide

Figure 1. MachXO3L Breakout Board (Top Side)

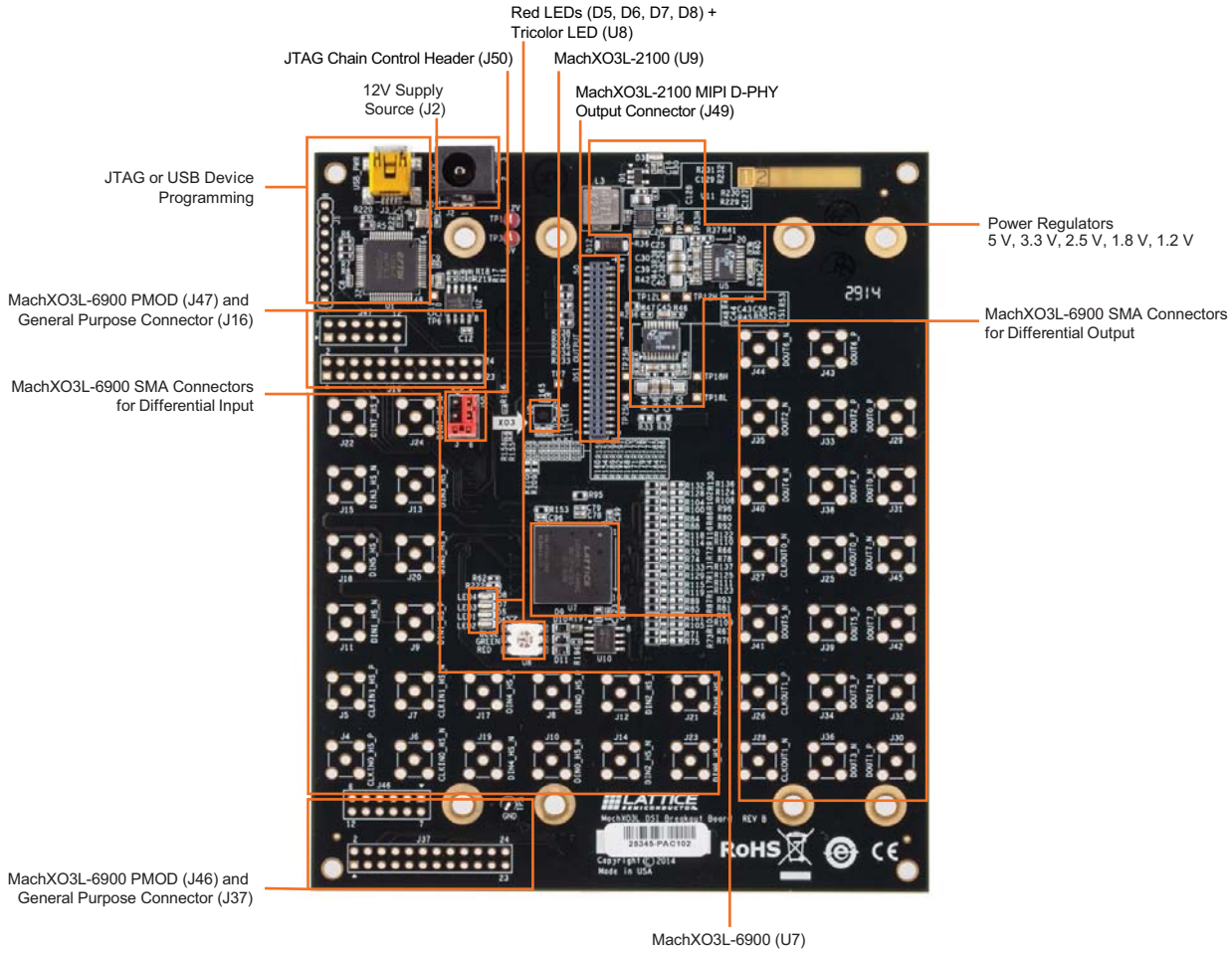
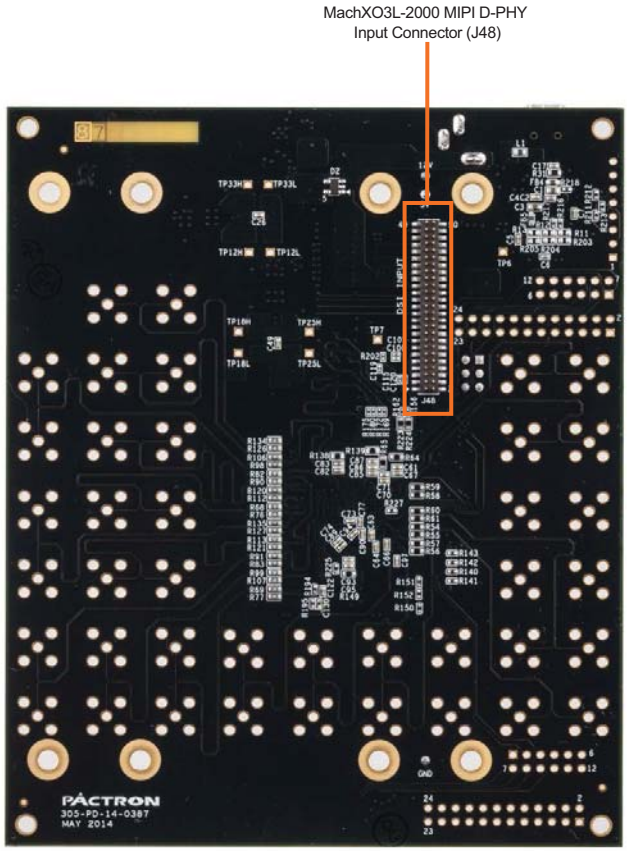


Figure 2. MachXO3L Breakout Board (Bottom Side)

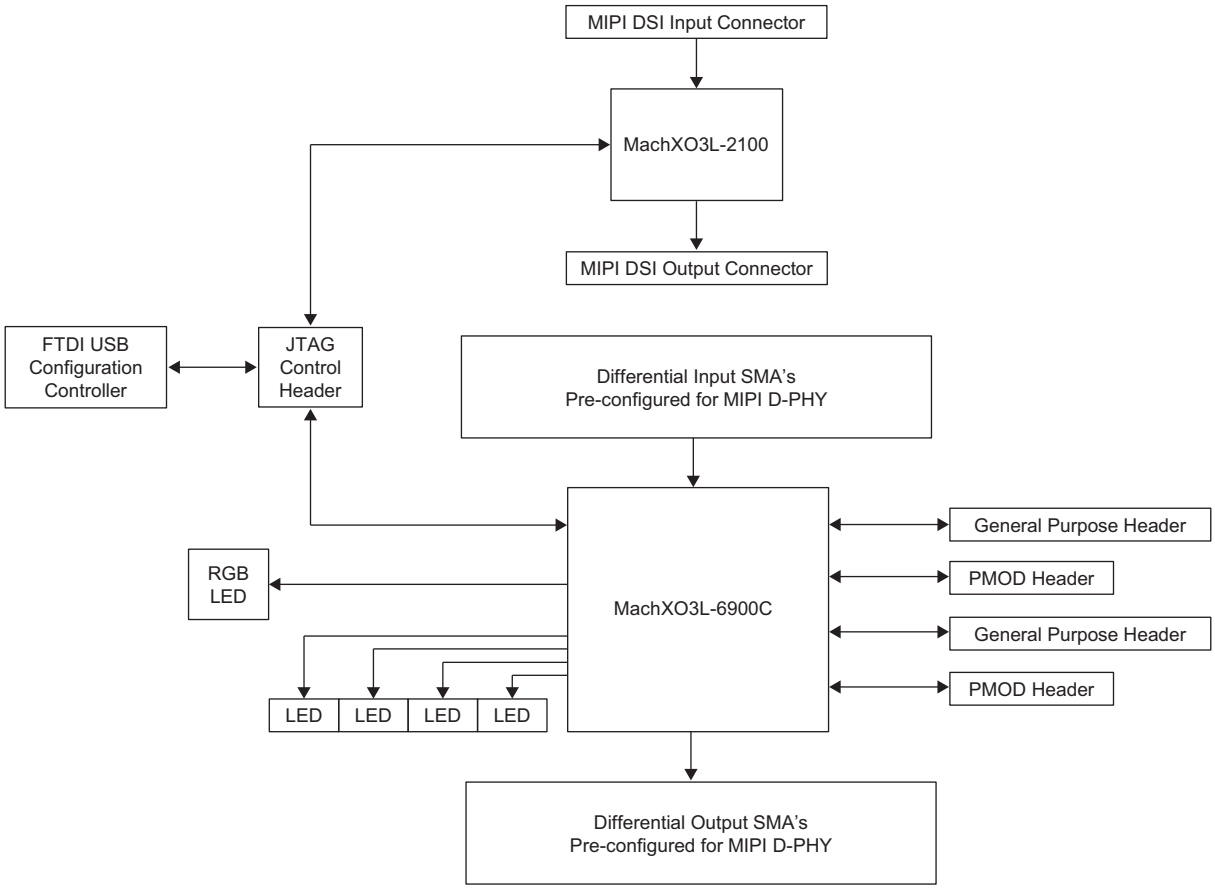


Overview

The MachXO3L Breakout Board allows for multi-device testing and scalability by providing a larger MachXO3L-6900 and a smaller MachXO3L-2100 device. The MachXO3L-6900 has two high speed clock and eight high speed data inputs and outputs. By default these ports are configured for MIPI D-PHY IO support, but can be modified for various IO options, such as LVDS, SubLVDS and CMOS. The MachXO3L-6900 also has four general purpose IO headers, two of which have the ability to connect with Digilent PMOD interface boards. Additionally, the MachXO3L-6900 device has the ability to control four general purpose LEDs and one tri-color RGB LED.

The MachXO3L-2100 is attached to two connectors providing four data and one clock lanes configured for MIPI D-PHY going in to and out of the FPGA. The pinout for the MachXO3L-2100 is optimized for low cost and small form factor by operating only off of 1.2 V and 3.3 V CMOS IO rails.

Figure 3. MachXO3L Breakout Board Functional Block Diagram



MachXO3L Devices

The MachXO3L Breakout Board features both the MachXO3L-6900 in 256-ball caBGA package and the MachXO3L-2100 in 49-ball WLCSP package. These devices feature 2100 and 6900 LUTs and 74 and 240 kbits of embedded block RAM respectively. Both of these devices feature a variety of features and programmability. For more information on the capabilities of each device see DS1047, MachXO3 Family Data Sheet.

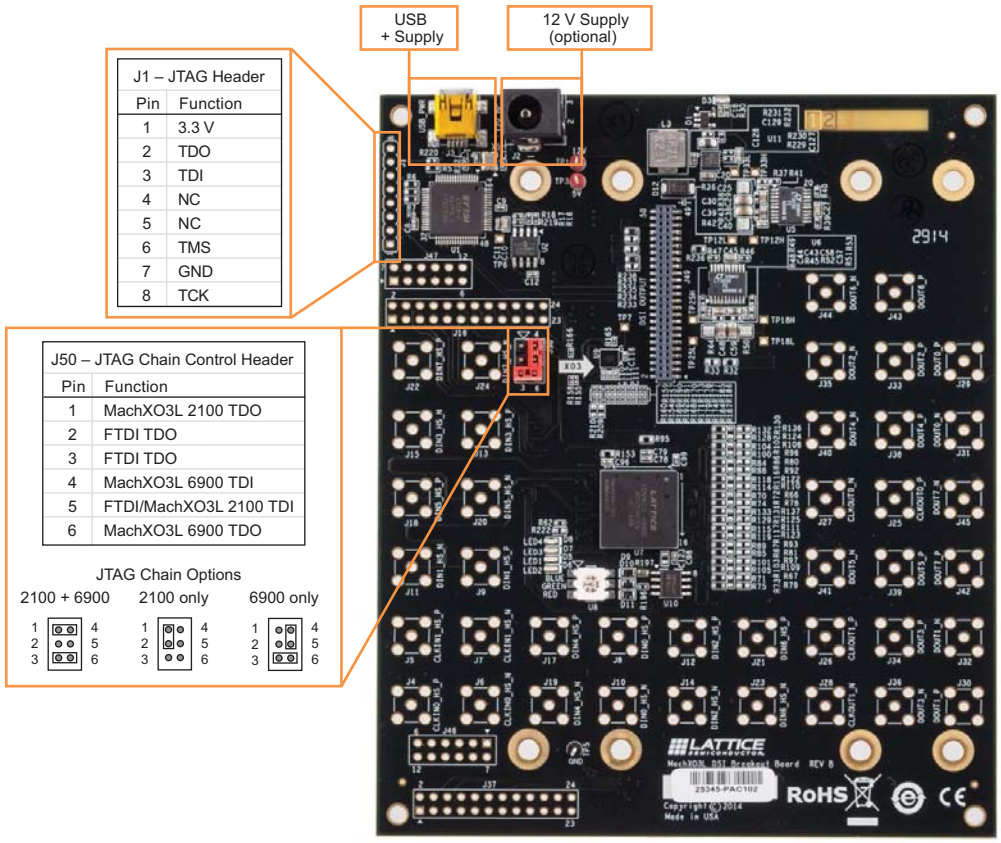
Connector Descriptions

Configuration

The MachXO3L-2100 and MachXO3L-6900 parts can be programmed via JTAG through USB port or standalone JTAG header. The USB path uses a FT2232H FTDI part to convert USB to JTAG. The standalone JTAG header can be used to program the devices using the Lattice Programming Cable. In order to use the stand alone JTAG header R5, R6, R7 and R8 to remove the FTDI part from the JTAG chain.

Power can be supplied to the board via mini USB port, 12 V power supply, from a separate board through the J48 DSI input connector or any combination of the three.

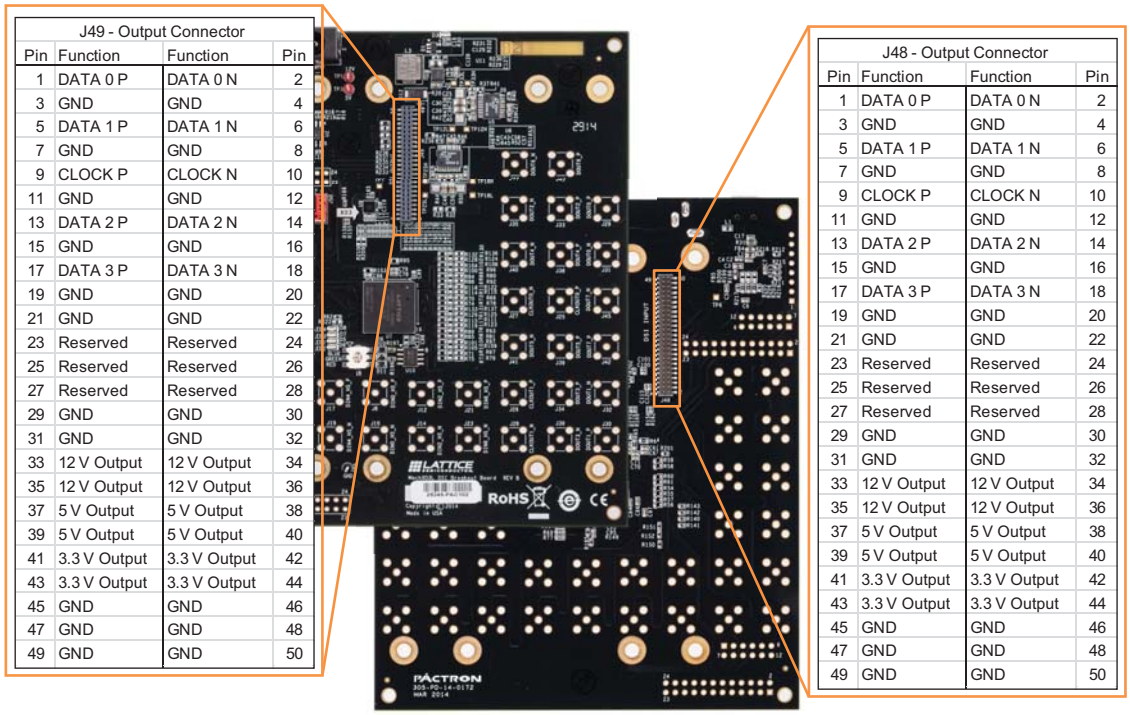
Figure 4. Configuration Connectors



MachXO3L-2100 MIPI D-PHY Connectors

The MachXO3L-2100 has input and output connectors capable of receiving and transmitting MIPI D-PHY, DSI or CSI-2 data. The connectors are also capable of other IO standards with proper board modifications. Power can be supplied to the MachXO3L board from the bottom input connector if desired. Similarly, power can be supplied from the MachXO3L to any attached board through the top output connector.

Figure 5. MachXO3L-2100 MIPI D-PHY Connectors



J49 - Output Connector

Pin	Function	Function	Pin
1	DATA 0 P	DATA 0 N	2
3	GND	GND	4
5	DATA 1 P	DATA 1 N	6
7	GND	GND	8
9	CLOCK P	CLOCK N	10
11	GND	GND	12
13	DATA 2 P	DATA 2 N	14
15	GND	GND	16
17	DATA 3 P	DATA 3 N	18
19	GND	GND	20
21	GND	GND	22
23	Reserved	Reserved	24
25	Reserved	Reserved	26
27	Reserved	Reserved	28
29	GND	GND	30
31	GND	GND	32
33	12 V Output	12 V Output	34
35	12 V Output	12 V Output	36
37	5 V Output	5 V Output	38
39	5 V Output	5 V Output	40
41	3.3 V Output	3.3 V Output	42
43	3.3 V Output	3.3 V Output	44
45	GND	GND	46
47	GND	GND	48
49	GND	GND	50

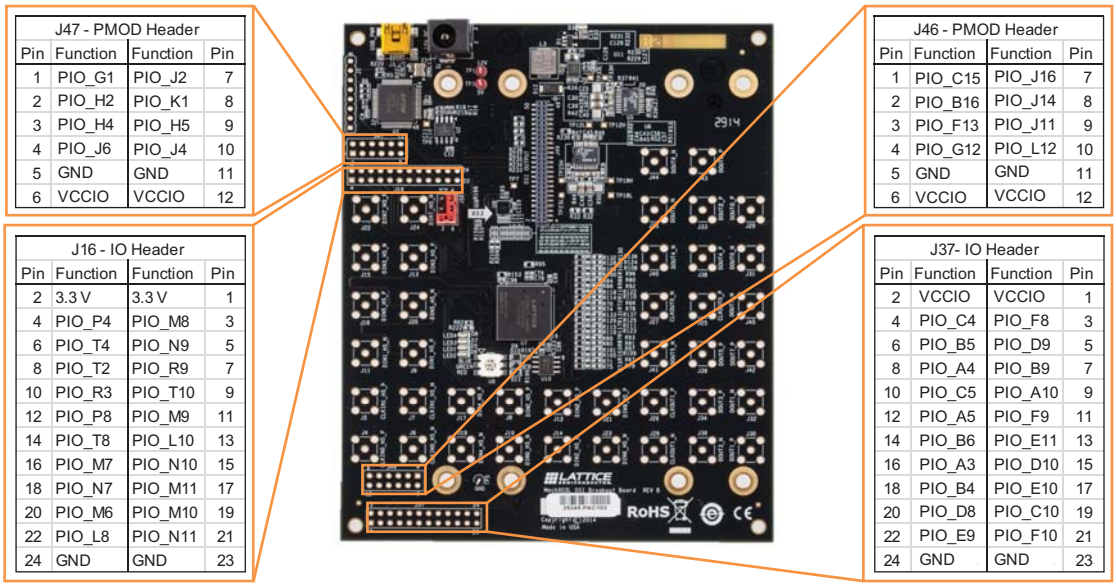
J48 - Output Connector

Pin	Function	Function	Pin
1	DATA 0 P	DATA 0 N	2
3	GND	GND	4
5	DATA 1 P	DATA 1 N	6
7	GND	GND	8
9	CLOCK P	CLOCK N	10
11	GND	GND	12
13	DATA 2 P	DATA 2 N	14
15	GND	GND	16
17	DATA 3 P	DATA 3 N	18
19	GND	GND	20
21	GND	GND	22
23	Reserved	Reserved	24
25	Reserved	Reserved	26
27	Reserved	Reserved	28
29	GND	GND	30
31	GND	GND	32
33	12 V Output	12 V Output	34
35	12 V Output	12 V Output	36
37	5 V Output	5 V Output	38
39	5 V Output	5 V Output	40
41	3.3 V Output	3.3 V Output	42
43	3.3 V Output	3.3 V Output	44
45	GND	GND	46
47	GND	GND	48
49	GND	GND	50

MachXO3L-6900 PMOD and General Purpose Connectors

Two 0.1 inch 24-pin headers are available as general purpose connectors. Two 0.1 inch 12-pin headers are also available either for general purpose or for use with Digilent PMOD boards.

Figure 6. MachXO3L-6900 PMOD and General Purpose Connectors



J47 - PMOD Header

Pin	Function	Function	Pin
1	PIO_G1	PIO_J2	7
2	PIO_H2	PIO_K1	8
3	PIO_H4	PIO_H5	9
4	PIO_J6	PIO_J4	10
5	GND	GND	11
6	VCCIO	VCCIO	12

J46 - PMOD Header

Pin	Function	Function	Pin
1	PIO_C15	PIO_J16	7
2	PIO_B16	PIO_J14	8
3	PIO_F13	PIO_J11	9
4	PIO_G12	PIO_L12	10
5	GND	GND	11
6	VCCIO	VCCIO	12

J16 - IO Header

Pin	Function	Function	Pin
2	3.3 V	3.3 V	1
4	PIO_P4	PIO_M8	3
6	PIO_T4	PIO_N9	5
8	PIO_T2	PIO_R9	7
10	PIO_R3	PIO_T10	9
12	PIO_P8	PIO_M9	11
14	PIO_T8	PIO_L10	13
16	PIO_M7	PIO_N10	15
18	PIO_N7	PIO_M11	17
20	PIO_M6	PIO_M10	19
22	PIO_L8	PIO_N11	21
24	GND	GND	23

J37- IO Header

Pin	Function	Function	Pin
2	VCCIO	VCCIO	1
4	PIO_C4	PIO_F8	3
6	PIO_B5	PIO_D9	5
8	PIO_A4	PIO_B9	7
10	PIO_C5	PIO_A10	9
12	PIO_A5	PIO_F9	11
14	PIO_B6	PIO_E11	13
16	PIO_A3	PIO_D10	15
18	PIO_B4	PIO_E10	17
20	PIO_D8	PIO_C10	19
22	PIO_E9	PIO_F10	21
24	GND	GND	23

MachXO3L-6900 Input and Output SMA Connectors

The MachXO3L-6900 has 10 input SMA's on bank 2 and 10 output SMA's on bank 0. On the input side, two SMA's are connected to edge clock inputs allowing for high speed gearing. On the input side, the additional eight SMA connections are connect to A/B pairs to support 1:8 gearing ratios. The clock and data lanes 0 and 1 have additional 50 ohm resistors connected to the P and N channels. These 50 ohm resistors are connected to bank 3 at 1.2V to support MIPI D-PHY contention detect and termination options.

On the transmit side each of the FPGA to SMA paths contain a resistor divider circuit. By default, the external resistor circuit is configured to support MIPI D-PHY in SLVS-200 and 1.2 V CMOS. The external circuit provides other options such as subLVDS, and AC coupling options by providing additional board component pads for such modifications.

Software Requirements

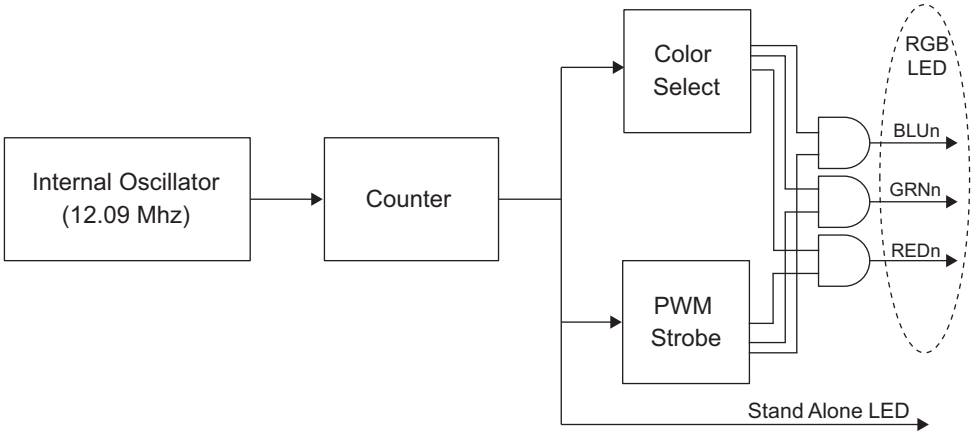
You should install the following software before you begin to develop new designs for the MachXO3L Breakout Board:

- Lattice Diamond® design software
- Diamond Standalone Programmer

Demonstration Design

Lattice provides a simple, pre-programmed demo to illustrate basic operation of the MachXO3L device. The design flashes the red LEDs as well as the RGB LED. The design utilizes the internal oscillator operating at 12.09 MHz. A counter is designed to slow down the clock and light up the individual LEDs. The demonstration design automatically starts on a newly purchased board when power is applied.

Figure 7. Demonstration Design Block Diagram



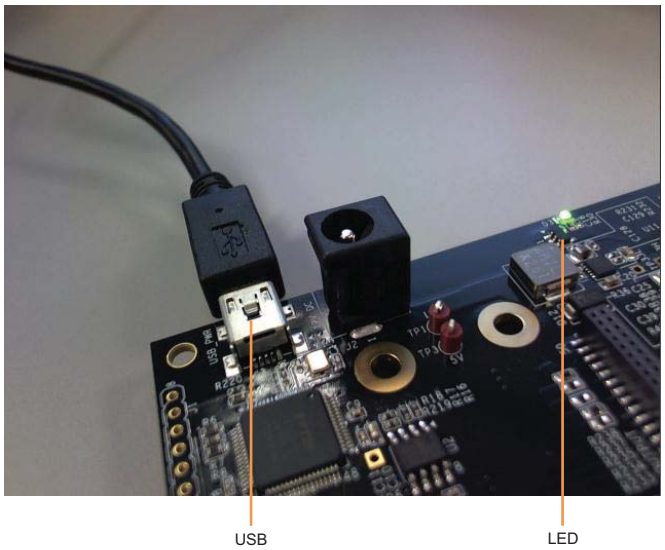
Download Demo Designs

The LED demo is preprogrammed into the Breakout Board, however over time it is likely your board will be loaded with a different design. Lattice distributes source and programming files for demonstration designs compatible with the MachXO3L Breakout Board. The Lattice Diamond project and Verilog source code for the MachXO3L Breakout Board example design can be obtained at www.latticesemi.com.

Programming Demonstration Design

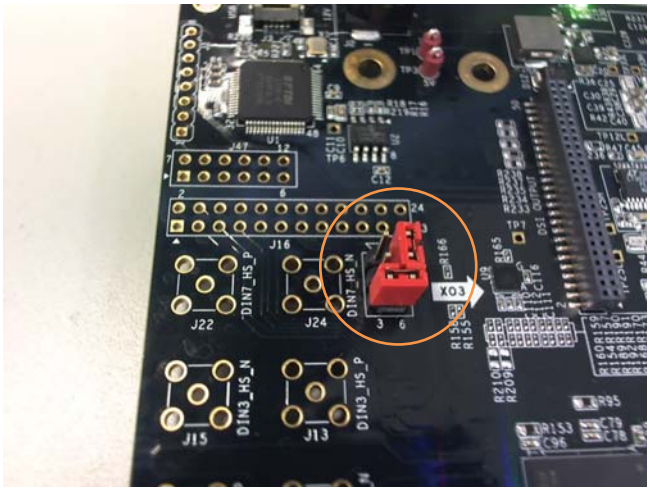
1. Plug in USB Cable to USB J3 connector. Check that D3 LED is *ON*.

Figure 8. USB and D3 LED



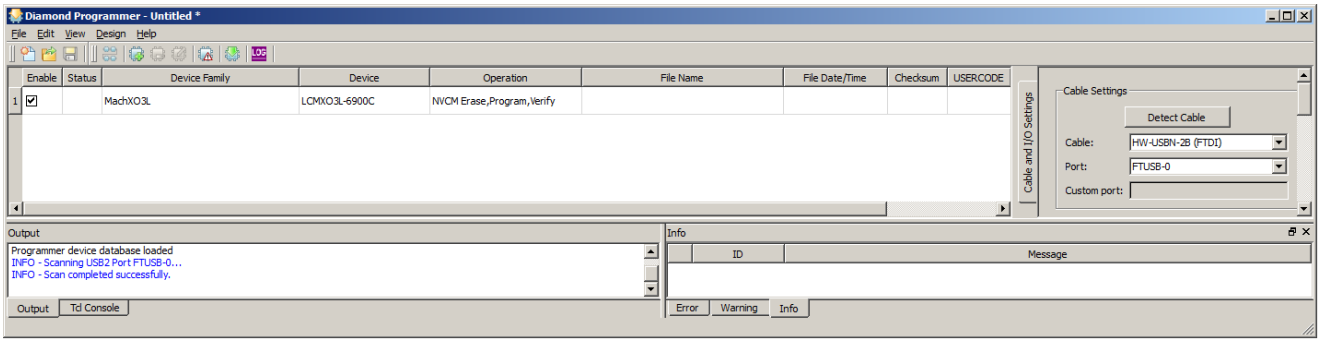
2. Place a jumper on pins 4-5 and another jumper on pins 3-6 of the J50 JTAG header.

Figure 9. Pins 3-6 and J50 JTAG Header



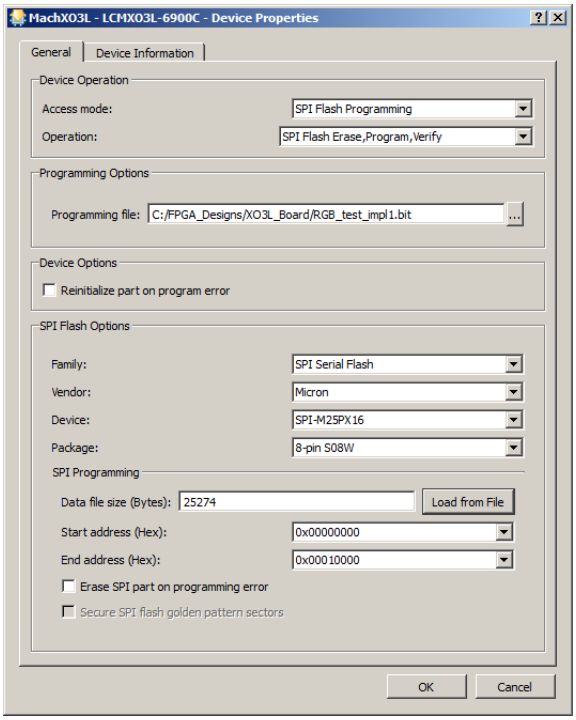
3. Open Diamond Programmer Version 3.2 (or higher) and click **OK**. The board scans and the LCMXO3L-6900C device becomes available for programming.

Figure 10. LCMXO3L-6900C Device for Programming



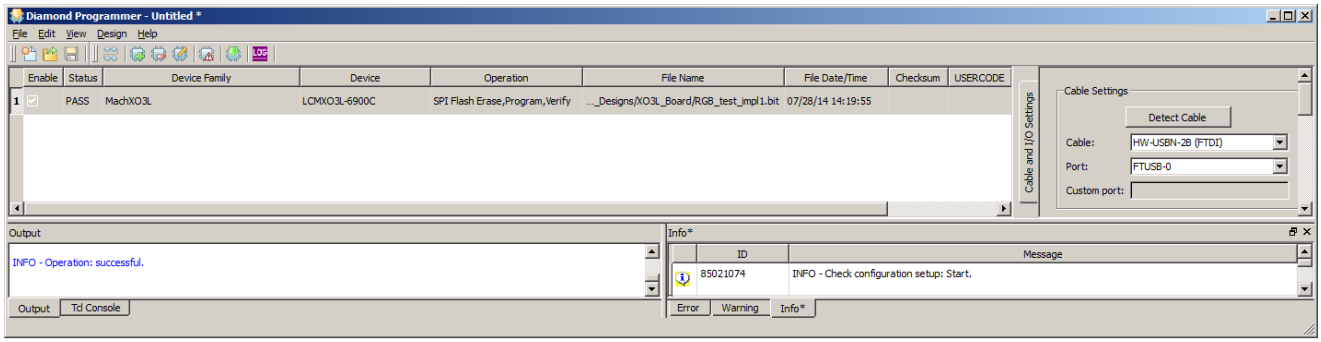
4. Double-click under Operation. The Device Properties dialog box opens.

Figure 11. SPI Flash Programming Access Mode



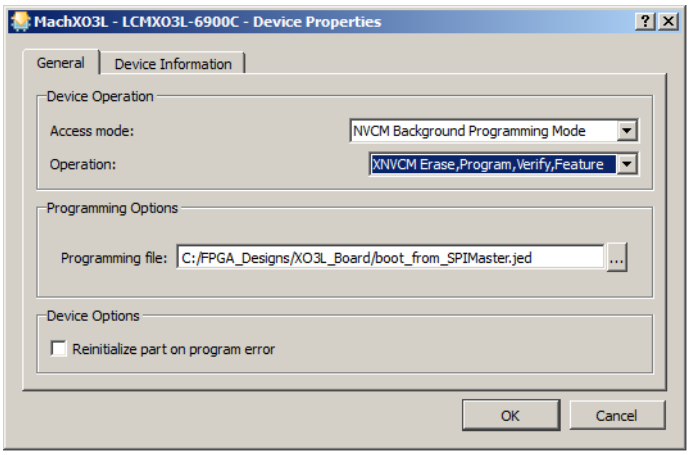
5. Select **SPI Flash Programming** in Access Mode.
6. Select the programming file *RGB_test_impl1.bit*.
7. Set all the SPI Flash Options as seen in Figure 23and click **Load from File** to retrieve the data file size. Then click **OK**.
8. Click **Design> Program**. The External SPI Flash Programming operation completes successfully.

Figure 12. Operation Verified as Successful



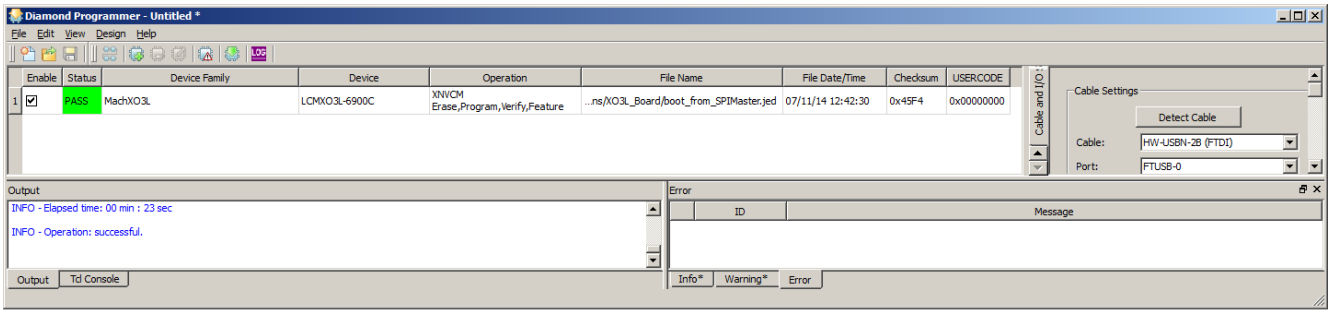
9. Double-click under Operation. The Device Properties dialog box opens.

Figure 13. XNVCM Erase, Program, Verify, Feature Access Mode



10. Select **XNVCM Erase, Program, Verify, Feature** in Access Mode.
11. Select the programming file boot_from_*SPIMaster.jed* and click **OK**.
12. Click **Design> Program**. In the Output pane, verify that *INFO – Operation: successful* is displayed.

Figure 14. Operation Verified as Successful



13. Recycle power by unplugging and re-plugging in the USB cable. The Red LEDs and RGB LEDs start flashing.

Storage and Handling

Static electricity can shorten the lifespan of electronic components. Observe these tips to prevent damage that could occur from electro-static discharge:

- Use anti-static precautions such as operating on an anti-static mat and wearing an anti-static wrist-band.
- Store the evaluation board in the packaging provided.
- Touch a metal USB housing to equalize voltage potential between you and the board.

Ordering Information

The MachXO3L breakout board can be ordered in two different forms. The MachXO3L SMA Breakout Board has all of the SMA's populated and the DSI connectors (J48 and J49) depopulated. The MachXO3L DSI Breakout Board has all of the SMA's de-populated and the DSI connectors (J48 and J49) populated.

Figure 15. MachXO3L SMA Breakout Board

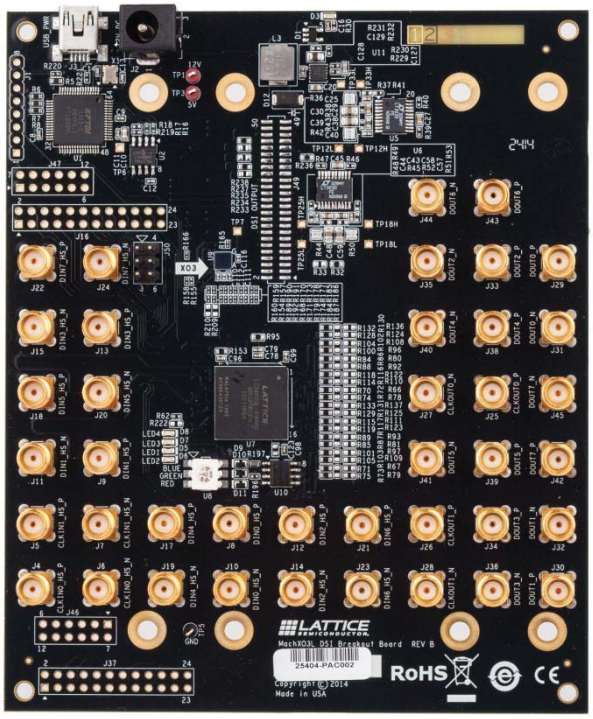
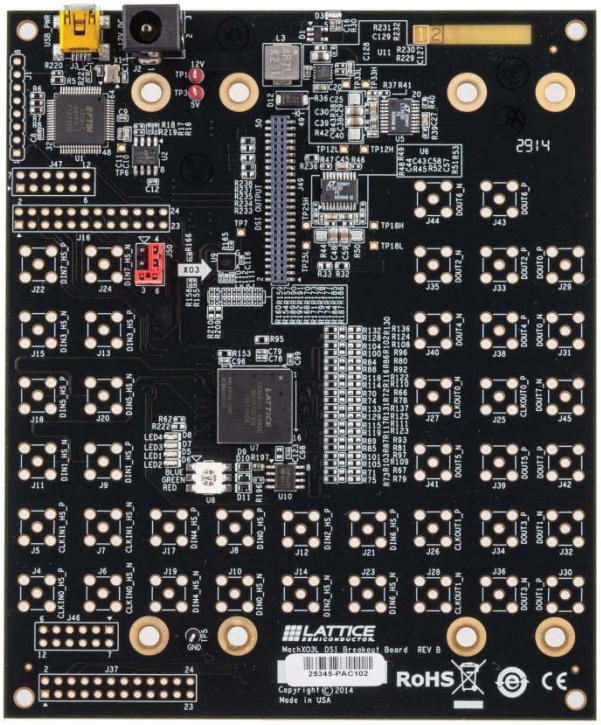


Figure 16. MachXO3L DSI Breakout Board



Description	Ordering Part Number	China RoHS Environment-Friendly Use Period (EFUP)
MachXO3L SMA Breakout Board	LCMXO3L-SMA-EVN	
MachXO3L DSI Breakout Board	LCMXO3L-DSI-EVN	

Technical Support Assistance

e-mail: techsupport@latticesemi.com

Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
January 2015	1.1	Updated Appendix A. Schematic Diagrams. Revised Figure 19, Board Power.
August 2014	1.0	Initial release.

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Appendix A. Schematic Diagrams

Figure 17. Block Diagram

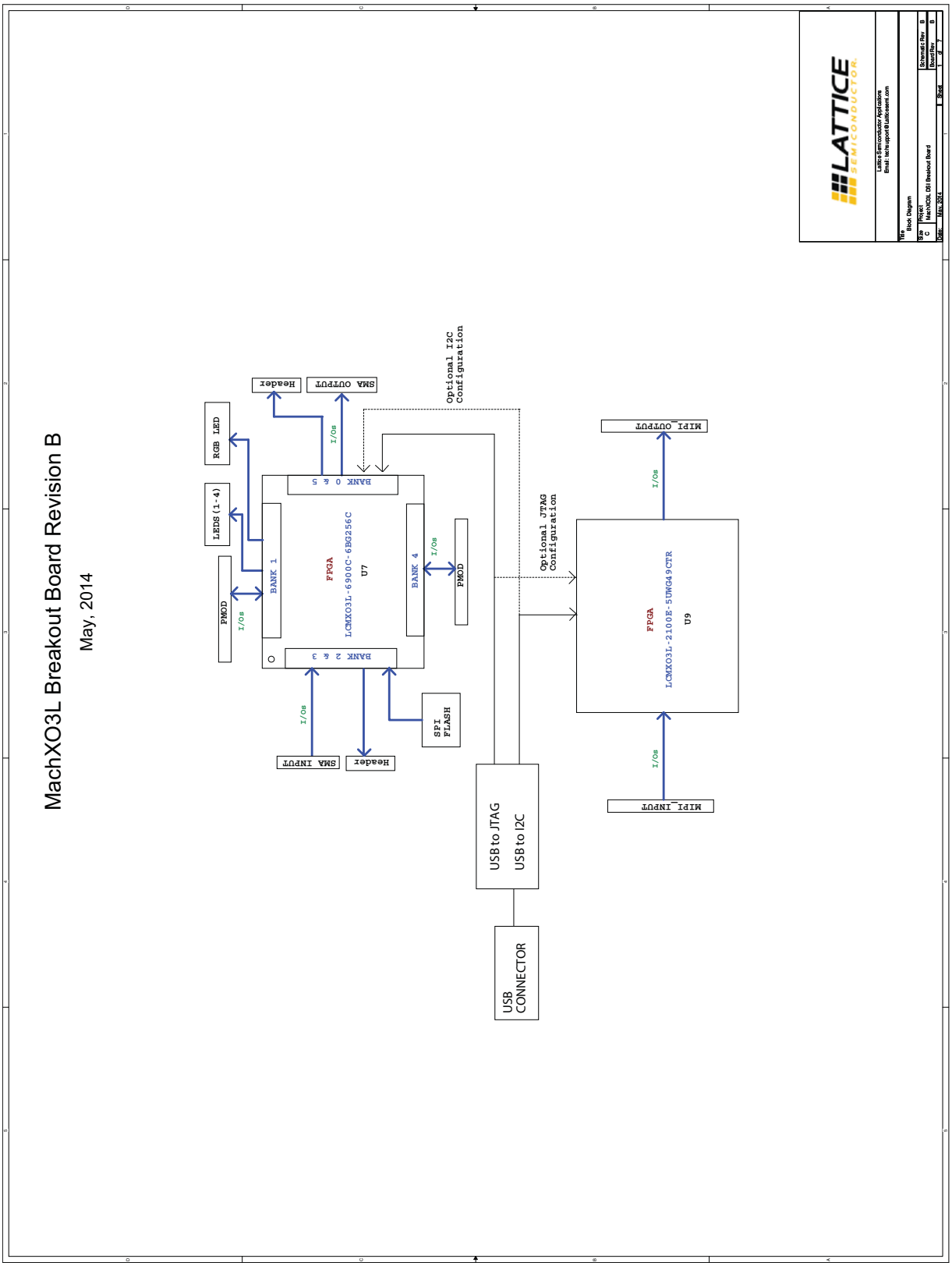

Figure 18. USB to JTAG

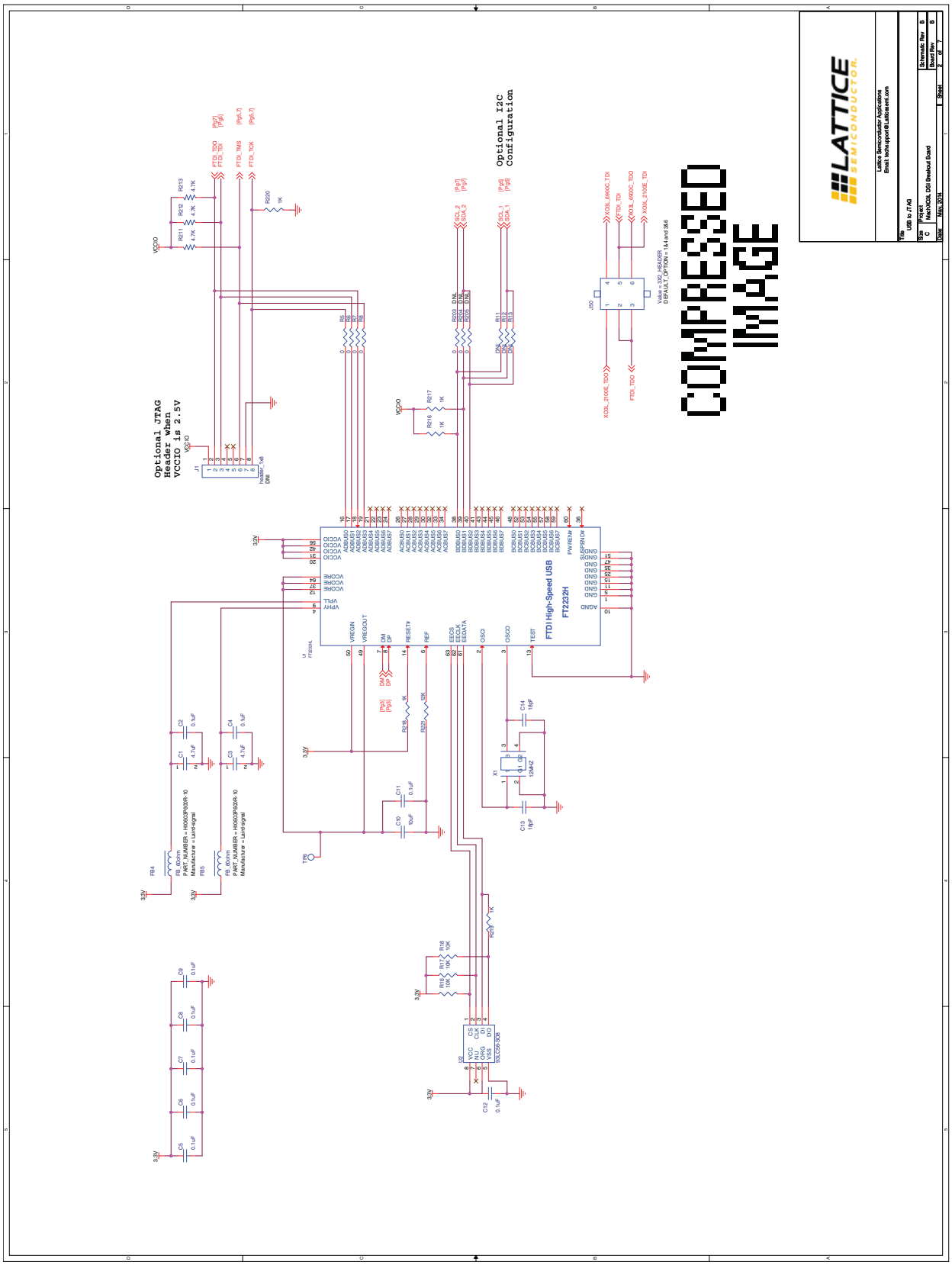

Figure 19. Board Power

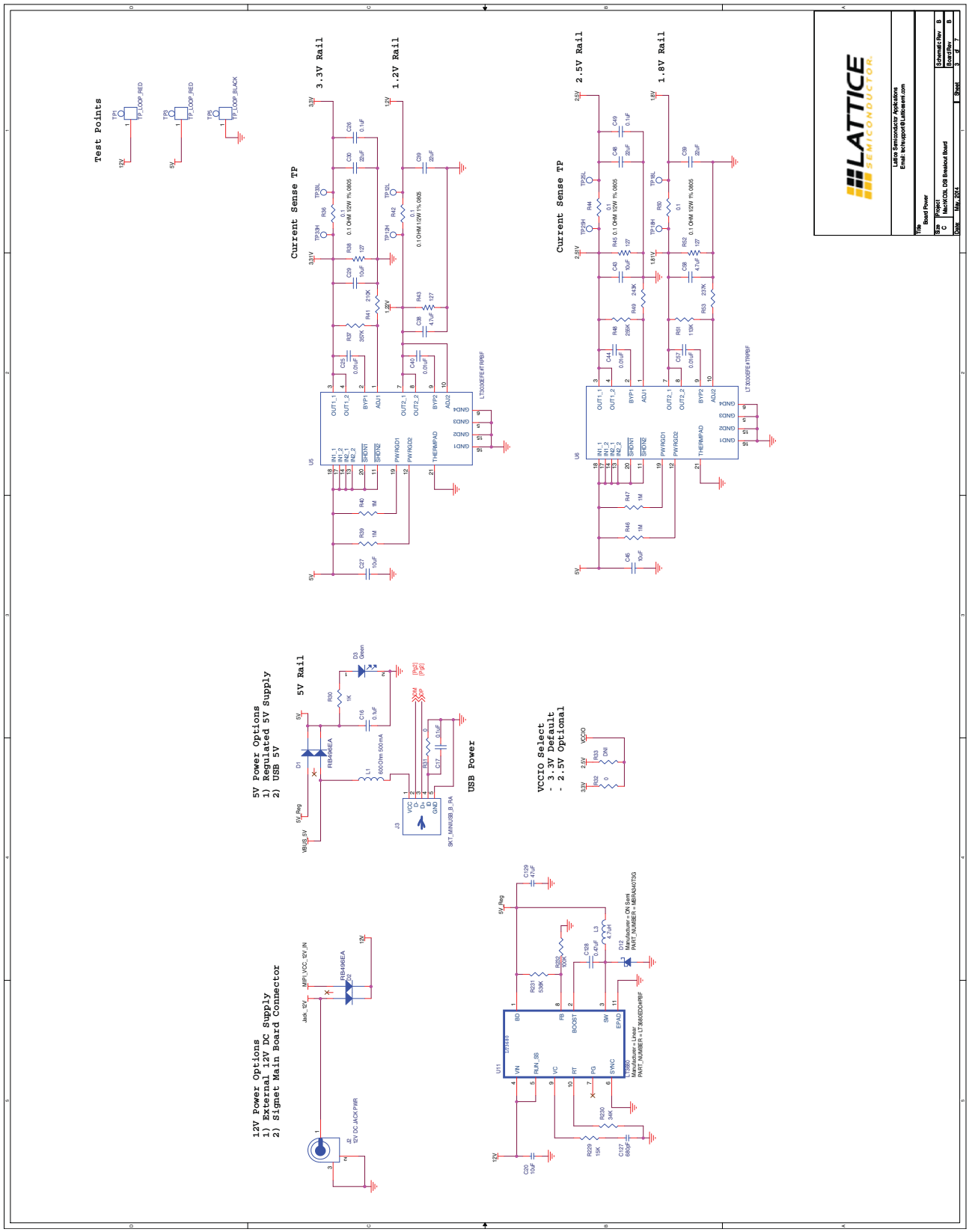

Figure 20. DSI: SMA_INPUT

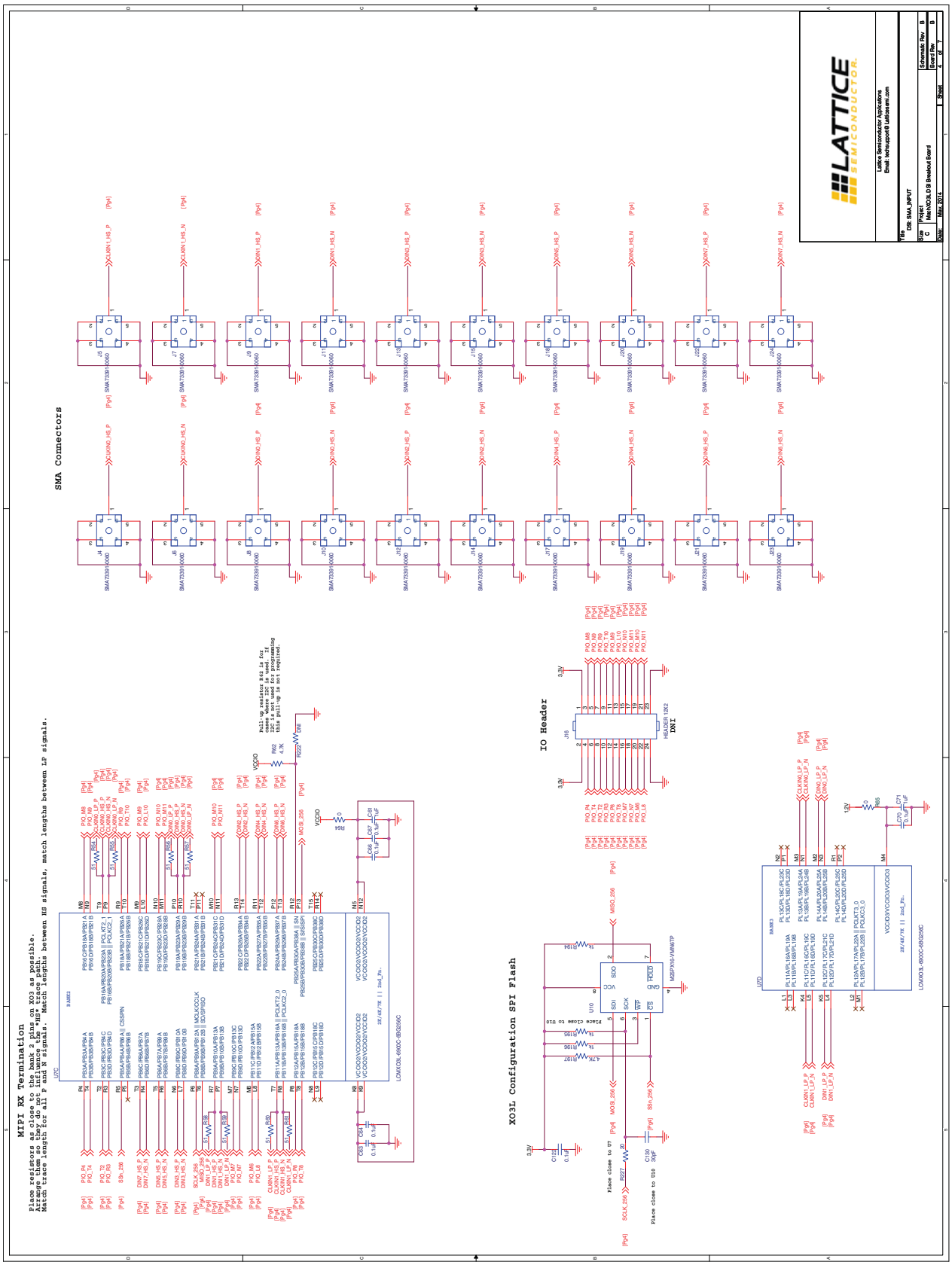

Figure 21. DSI: SMA_OUTPUT

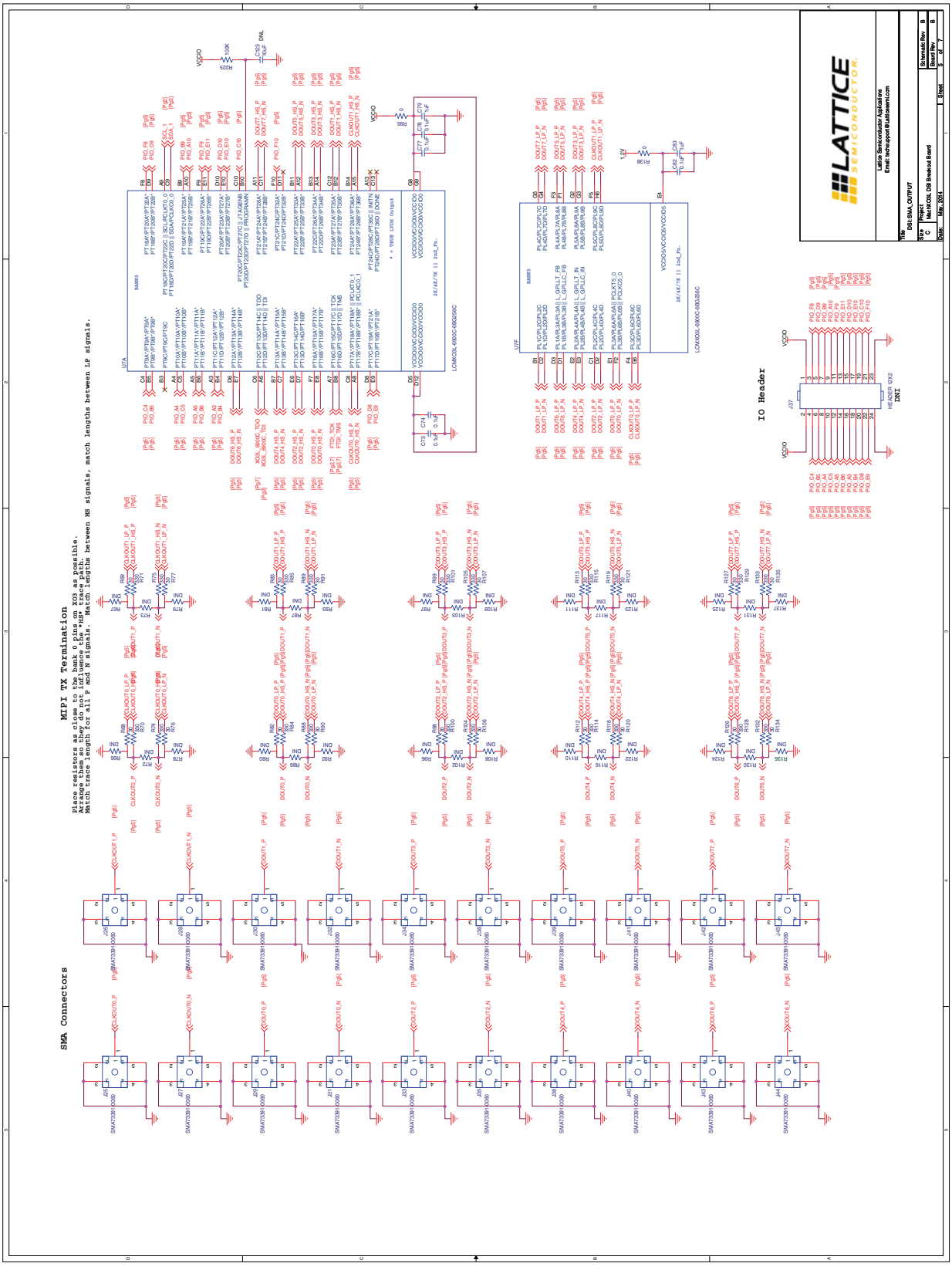

Figure 22. Breakout Connection

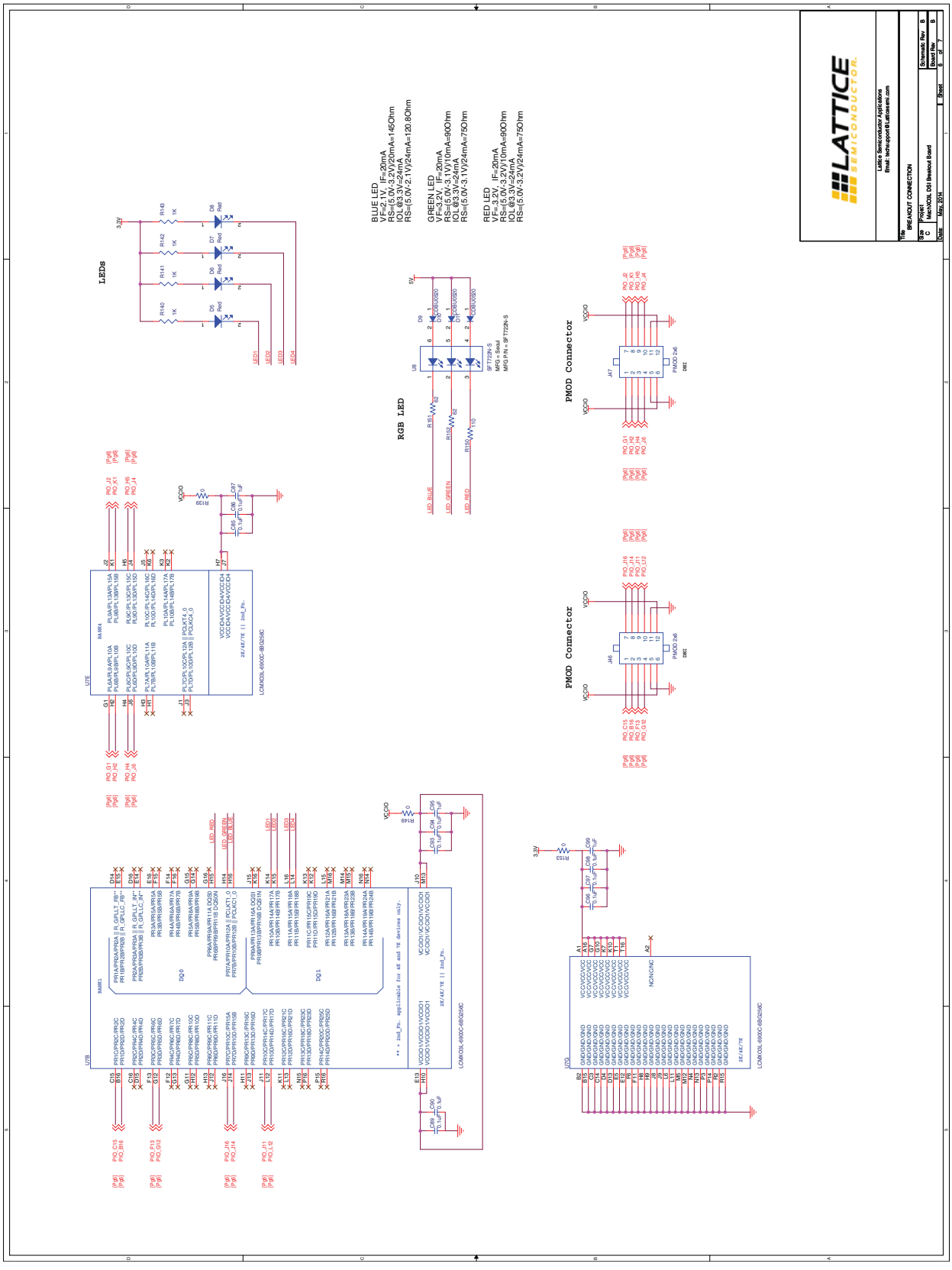

Figure 23. X03 BOB + DSI: LCMX3L-2100E-5WLCSP49