Document Number: A2I09VD050N
Rev. 0, 09/2018

RF LDMOS Wideband Integrated Power Amplifiers

The A2I09VD050N wideband integrated circuit is designed with on-chip matching that makes it usable from 575 to 960 MHz. This multi-stage structure is rated for 48 to 55 V operation and covers all typical cellular base station modulation formats.

900 MHz

- Typical Single-Carrier W-CDMA Characterization Performance: V_{DD} = 48 Vdc, $I_{DQ1(A+B)}$ = 74 mA, $I_{DQ2(A+B)}$ = 240 mA, P_{out} = 6.3 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. (1)

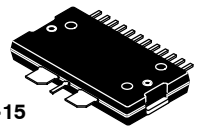
Frequency	G_{ps} (dB)	PAE (%)	ACPR (dBc)
920 MHz	36.8	19.7	–45.5
940 MHz	36.8	19.9	–45.9
960 MHz	36.6	19.8	–45.8

Features

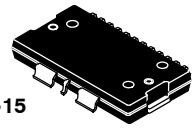
- On-chip matching (50 ohm input, DC blocked)
- Integrated quiescent current temperature compensation with enable/disable function (2)
- Designed for digital predistortion error correction systems
- Optimized for Doherty applications

A2I09VD050NR1
A2I09VD050GNR1

575–960 MHz, 6.3 W AVG., 48 V AIRFAST RF LDMOS WIDEBAND INTEGRATED POWER AMPLIFIERS



TO-270WB-15
PLASTIC
A2I09VD050NR1



TO-270WBG-15
PLASTIC
A2I09VD050GNR1

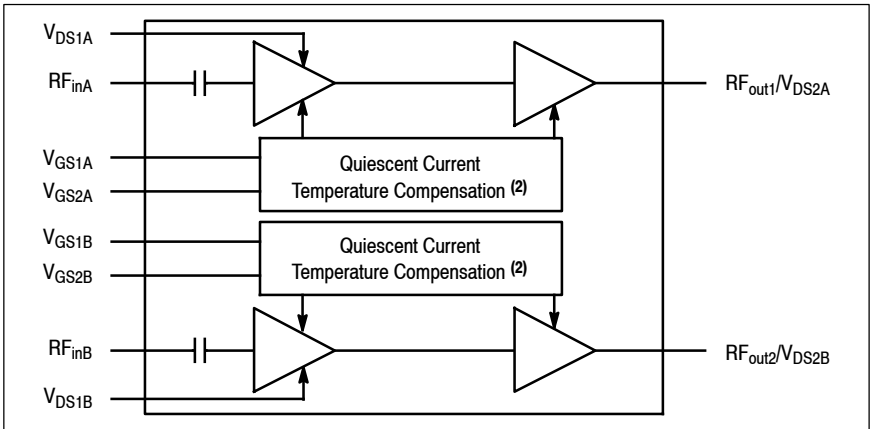
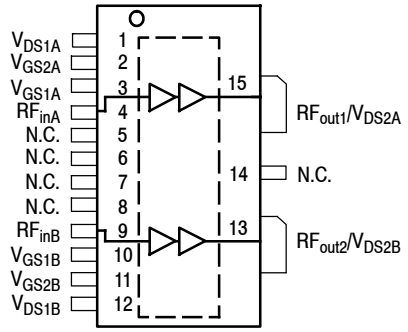


Figure 1. Functional Block Diagram



(Top View)

Note: Exposed backside of the package is the source terminal for the transistor.

Figure 2. Pin Connections

1. All data measured in fixture with device soldered to heatsink.
2. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family*, and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to http://www.nxp.com/RF and search for AN1977 or AN1987.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	–0.5, +105	Vdc
Gate–Source Voltage	V_{GS}	–0.5, +10	Vdc
Operating Voltage	V_{DD}	55, +0	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–40 to +150	°C
Operating Junction Temperature Range (1,2)	T_J	–40 to +225	°C
Input Power	P_{in}	20	dBm

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 73°C, 6.3 W, 940 MHz Stage 1, 48 Vdc, $I_{DQ1(A+B)}$ = 74 mA Stage 2, 48 Vdc, $I_{DQ2(A+B)}$ = 240 mA	$R_{\theta JC}$	 3.2 1.5	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JS–001–2017)	1A
Charge Device Model (per JS–002–2014)	C0B

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22–A113, IPC/JEDEC J–STD–020	3	260	°C

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.nxp.com/RF/calculators.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.nxp.com/RF and search for AN1955.

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Stage 1 - Off Characteristics (1)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 105 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 55 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 1.2 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Stage 1 - On Characteristics					
Gate Threshold Voltage (1) (V_{DS} = 10 Vdc, I_D = 4 μAdc)	$V_{GS(th)}$	1.3	1.7	2.3	Vdc
Gate Quiescent Voltage (V_{DS} = 48 Vdc, $I_{DQ1(A+B)}$ = 74 mAdc)	$V_{GS(Q)}$	—	2.1	—	Vdc
Fixture Gate Quiescent Voltage (V_{DD} = 48 Vdc, $I_{DQ1(A+B)}$ = 74 mAdc, Measured in Functional Test)	$V_{GG(Q)}$	4.6	4.9	5.2	Vdc
Stage 2 - Off Characteristics (1)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 105 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 55 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 1.2 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Stage 2 - On Characteristics					
Gate Threshold Voltage (1) (V_{DS} = 10 Vdc, I_D = 19 μAdc)	$V_{GS(th)}$	1.3	1.7	2.3	Vdc
Gate Quiescent Voltage (V_{DS} = 48 Vdc, $I_{DQ2(A+B)}$ = 240 mAdc)	$V_{GS(Q)}$	—	2.0	—	Vdc
Fixture Gate Quiescent Voltage (V_{DD} = 48 Vdc, $I_{DQ2(A+B)}$ = 240 mAdc, Measured in Functional Test)	$V_{GG(Q)}$	4.0	4.3	4.6	Vdc
Drain-Source On-Voltage (1) (V_{GS} = 10 Vdc, I_D = 190 mAdc)	$V_{DS(on)}$	0.1	0.25	0.5	Vdc

1. Each side of device measured separately.

(continued)

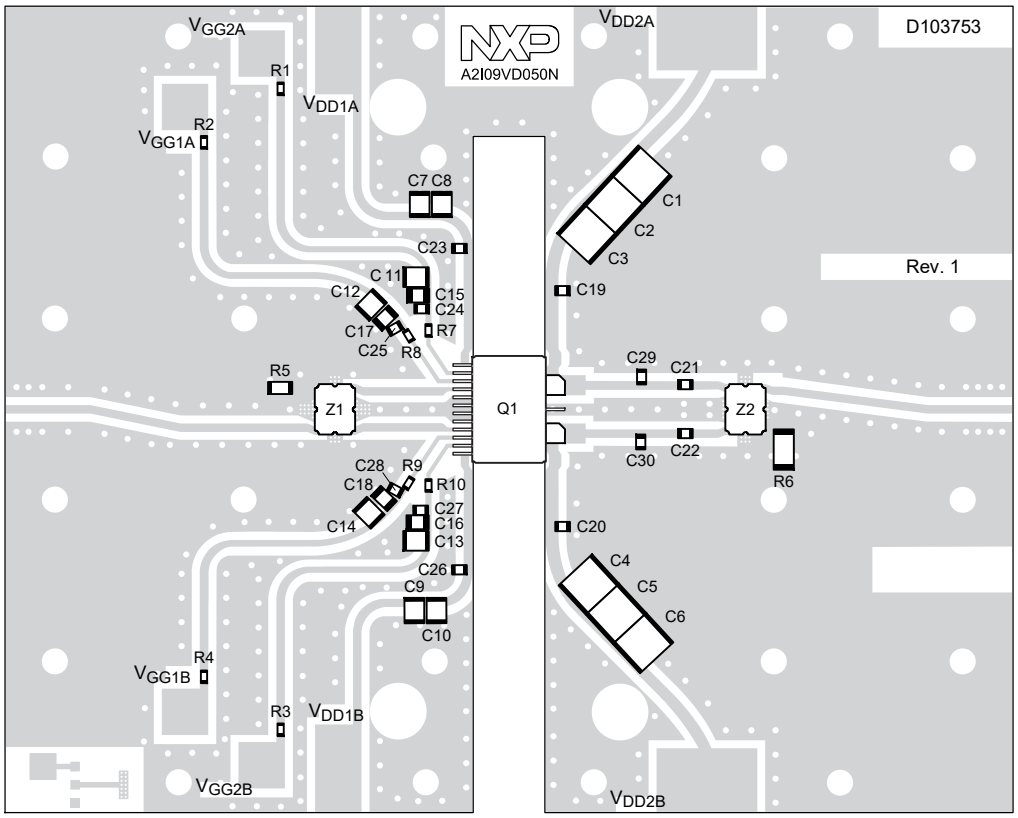
Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests (1,2) (In NXP Production Test Fixture, 50 ohm system) V_{DD} = 48 Vdc, $I_{DQ1(A+B)}$ = 74 mA, $I_{DQ2(A+B)}$ = 240 mA, P_{out} = 6.3 W Avg., f = 920 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	35.0	36.5	38.0	dB
Power Added Efficiency	PAE	18.0	19.8	—	%
Adjacent Channel Power Ratio	ACPR	—	–45.3	–43.0	dBc
P_{out} @ 3 dB Compression Point, CW (I_{DQA} = 50 mA, I_{DQB} = 200 mA)	P3dB	58.9	66.1	—	W
Load Mismatch (In NXP Production Test Fixture, 50 ohm system) $I_{DQ1(A+B)}$ = 74 mA, $I_{DQ2(A+B)}$ = 240 mA, f = 940 MHz					
VSWR 10:1 at 55 Vdc, 70 W CW Output Power (3 dB Input Overdrive from 56 W CW Rated Power)	No Device Degradation				
Typical Performance (3) (In NXP Characterization Test Fixture, 50 ohm system) V_{DD} = 48 Vdc, $I_{DQ1(A+B)}$ = 74 mA, $I_{DQ2(A+B)}$ = 240 mA, 920–960 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	53.7	—	W
P_{out} @ 3 dB Compression Point (4)	P3dB	—	67.6	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 920–960 MHz frequency range.)	Φ	—	–8	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	200	—	MHz
Quiescent Current Accuracy over Temperature (5) with 2 kΩ Gate Feed Resistors (–30 to 85°C) Stage 1 with 2 kΩ Gate Feed Resistors (–30 to 85°C) Stage 2	ΔI_{QT}	 — —	 1.7 2.5	 — —	%
Gain Flatness in 40 MHz Bandwidth @ P_{out} = 6.3 W Avg.	G_F	—	0.3	—	dB
Gain Variation over Temperature (–40°C to +85°C)	ΔG	—	0.031	—	dB/°C
Output Power Variation over Temperature (–40°C to +85°C)	ΔP1dB	—	0.007	—	dB/°C

Table 6. Ordering Information

Device	Tape and Reel Information	Package
A2I09VD050NR1	R1 Suffix = 500 Units, 44 mm Tape Width, 13-inch Reel	TO-270WB-15
A2I09VD050GNR1		TO-270WBG-15

1. Part internally input and output matched.
2. Measurements made with device in straight lead configuration before any lead forming operation is applied. Lead forming is used for gull wing (GN) parts.
3. All data measured in fixture with device soldered to heatsink.
4. P3dB = P_{avg} + 7.0 dB where P_{avg} is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.
5. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family*, and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to http://www.nxp.com/RF and search for AN1977 or AN1987.



Note: All data measured in fixture with device soldered to heatsink. Production fixture does not include device soldered to heatsink.

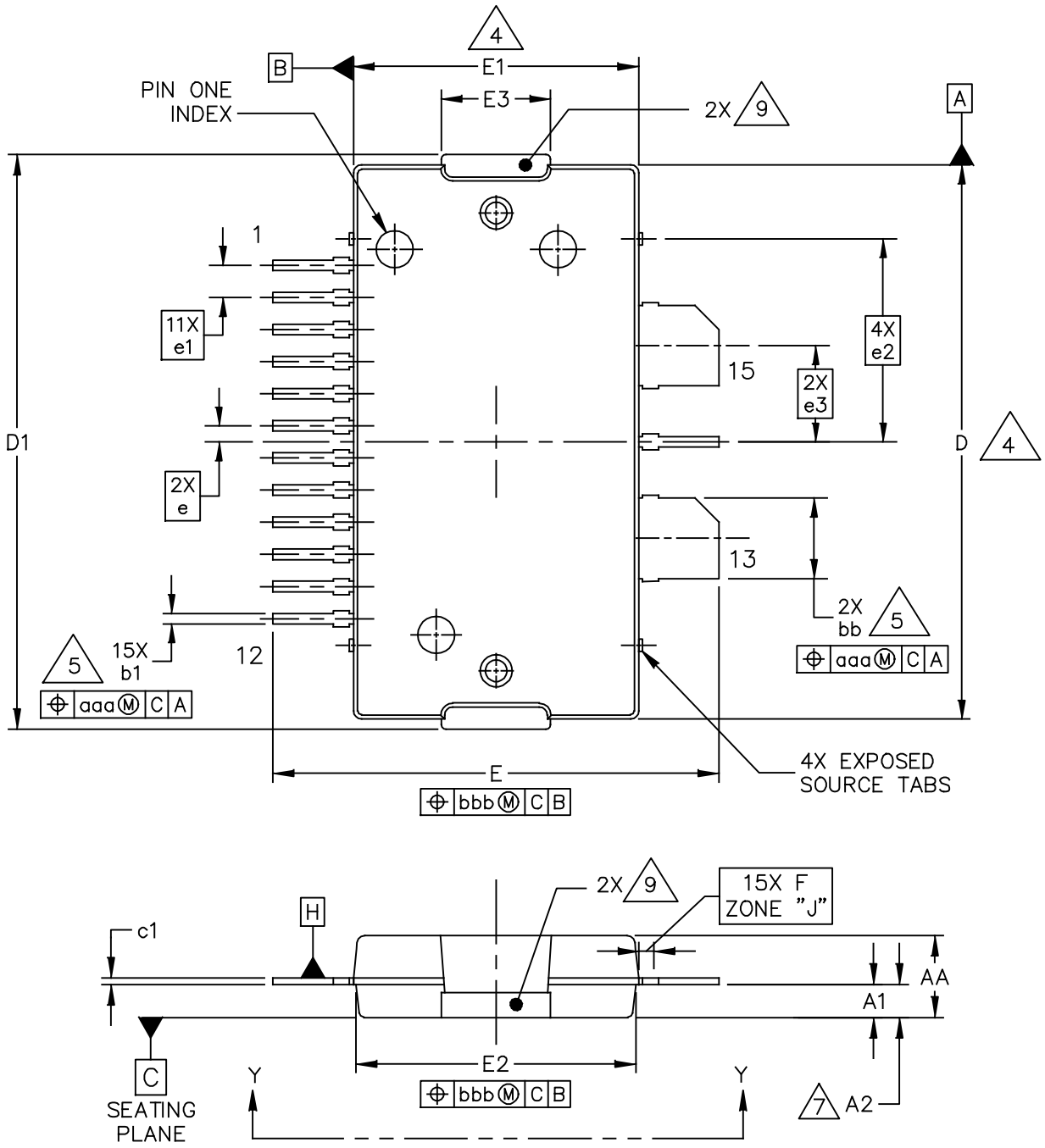
aaa-031569

Figure 3. A2I09VD050NR1 Test Circuit Component Layout

Table 7. A2I09VD050NR1 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2, C3, C4, C5, C6	10 μF Chip Capacitor	C5750X7S2A106M230KB	TDK
C7, C8, C9, C10	4.7 μF Chip Capacitor	C4532X7S2A475M230KB	TDK
C11, C12, C13, C14	10 μF Chip Capacitor	C3225X7S1H106M250AB	TDK
C15, C16, C17, C18	0.01 μF Chip Capacitor	C0805C103K5RAC	Kemet
C19, C20, C21, C22, C23, C24, C25, C26, C27, C28	47 pF Chip Capacitor	ATC600S470JT250XT	ATC
Q1	RF Power LDMOS Amplifier	A2I09VD050N	NXP
R1, R2, R3, R4	2.2 kΩ, 1/8 W Chip Resistor	CRCW08052K20JNEA	Vishay
R5	50 Ω, 8 W Termination Chip Resistor	C8A50Z4B	Anaren
R6	50 Ω, 20 W Termination Chip Resistor	C20A50Z4	Anaren
R7, R8, R9, R10	10 Ω, 1/8 W Chip Resistor	CRCW080510R0FKEA	Vishay
Z1, Z2	800–1000 MHz Band, 90°, 3 dB Hybrid Coupler	X3C09P1-03S	Anaren
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D103753	MTL

PACKAGE DIMENSIONS



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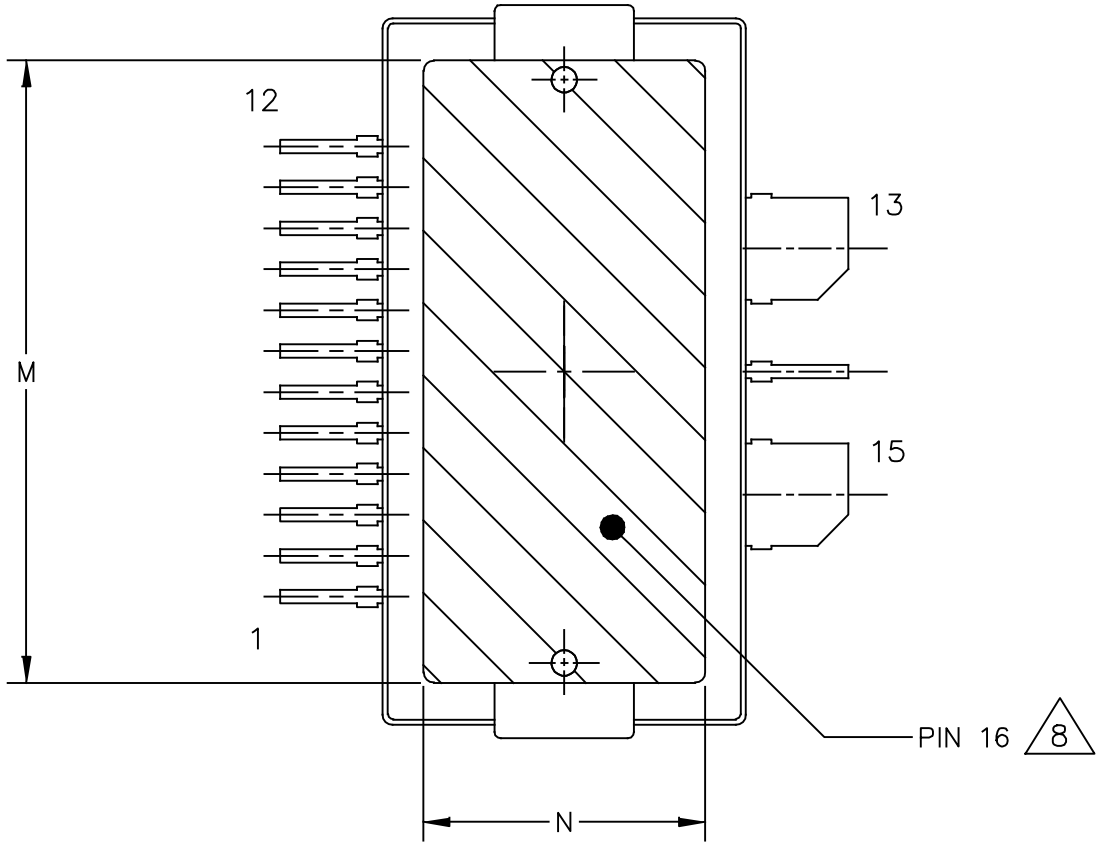
	SOT1722−1	21 JAN 2016



VIEW Y–Y

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	SOT1722–1	21 JAN 2016

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUM PLANE H IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 INCH (0.15 MM) PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

5. DIMENSIONS bb AND b1 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13 MM) TOTAL IN EXCESS OF THE bb AND b1 DIMENSIONS AT MAXIMUM MATERIAL CONDITION.

6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

7. DIMENSION A2 APPLIES WITHIN ZONE J ONLY.

8. HATCHING REPRESENTS THE EXPOSED AND SOLDERABLE AREA OF THE HEAT SLUG. DIMENSIONS M AND N REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF THE HEAT SLUG.

9. THESE SURFACES OF THE HEAT SLUG ARE NOT PART OF THE SOLDERABLE SURFACES AND MAY REMAIN UNPLATED.

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
AA	.099	.105	2.51	2.67	M	.600	----	15.24	----
A1	.039	.043	0.99	1.09	N	.270	----	6.86	----
A2	.040	.042	1.02	1.07	bb	.097	.103	2.46	2.62
D	.688	.692	17.48	17.58	b1	.010	.016	0.25	0.41
D1	.712	.720	18.08	18.29	c1	.007	.011	0.18	0.28
E	.551	.559	14.00	14.20	e	.020 BSC		0.51 BSC	
E1	.353	.357	8.97	9.07	e1	.040 BSC		1.02 BSC	
E2	.346	.350	8.79	8.89	e2	.253 INFO ONLY		6.43 INFO ONLY	
E3	.132	.140	3.35	3.56	e3	.120 BSC		3.05 BSC	
F	.025 BSC		0.64 BSC		aaa	.004		0.10	
					bbb	.008		0.20	

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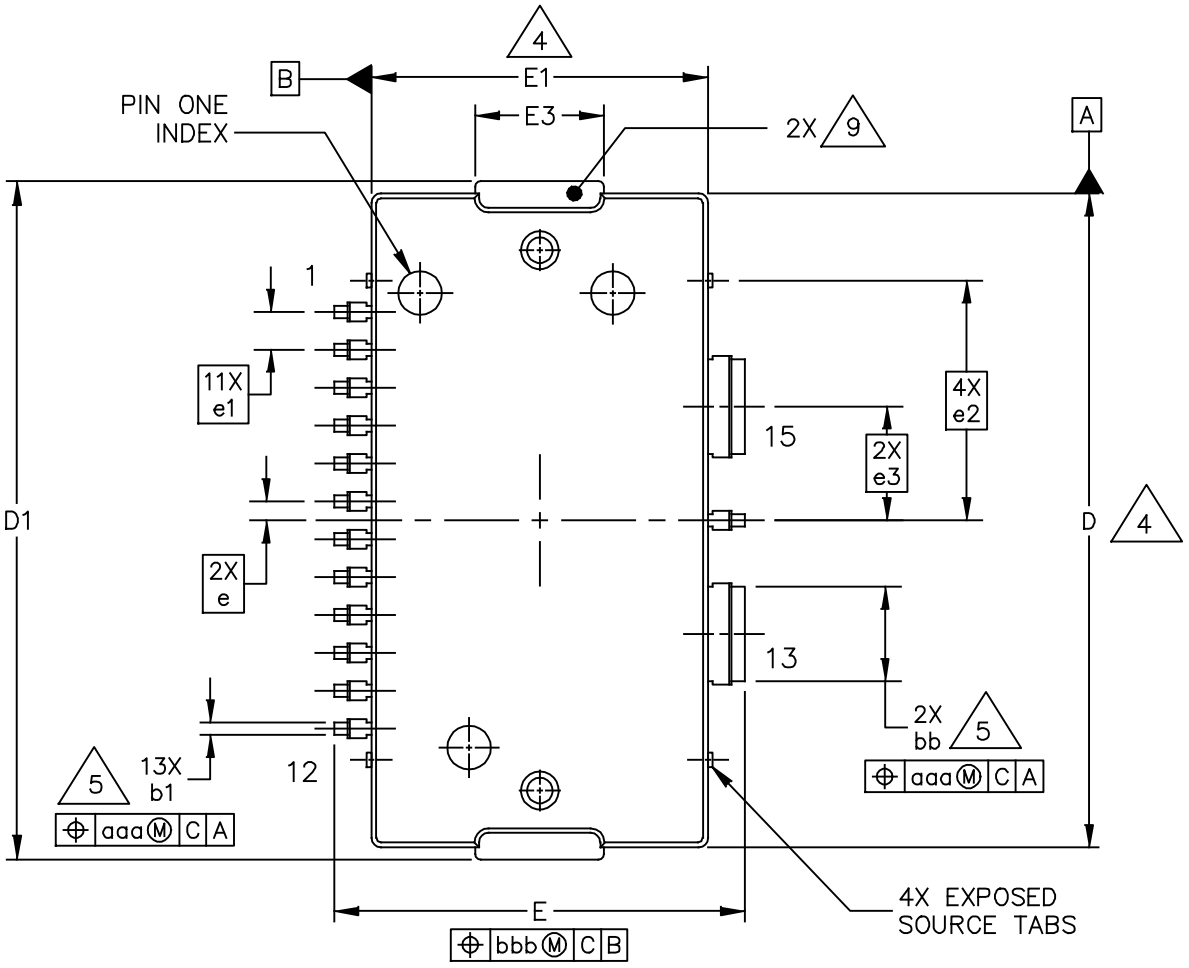

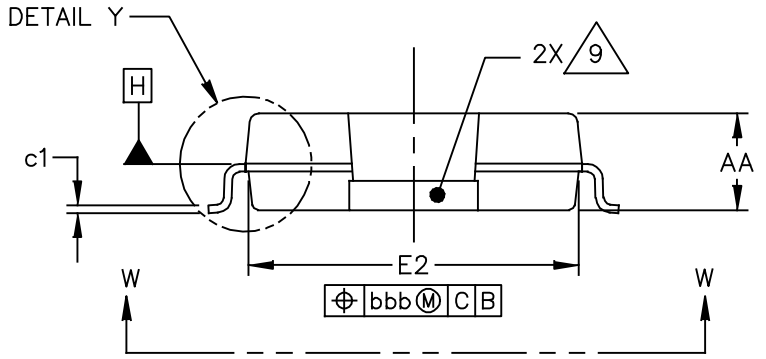

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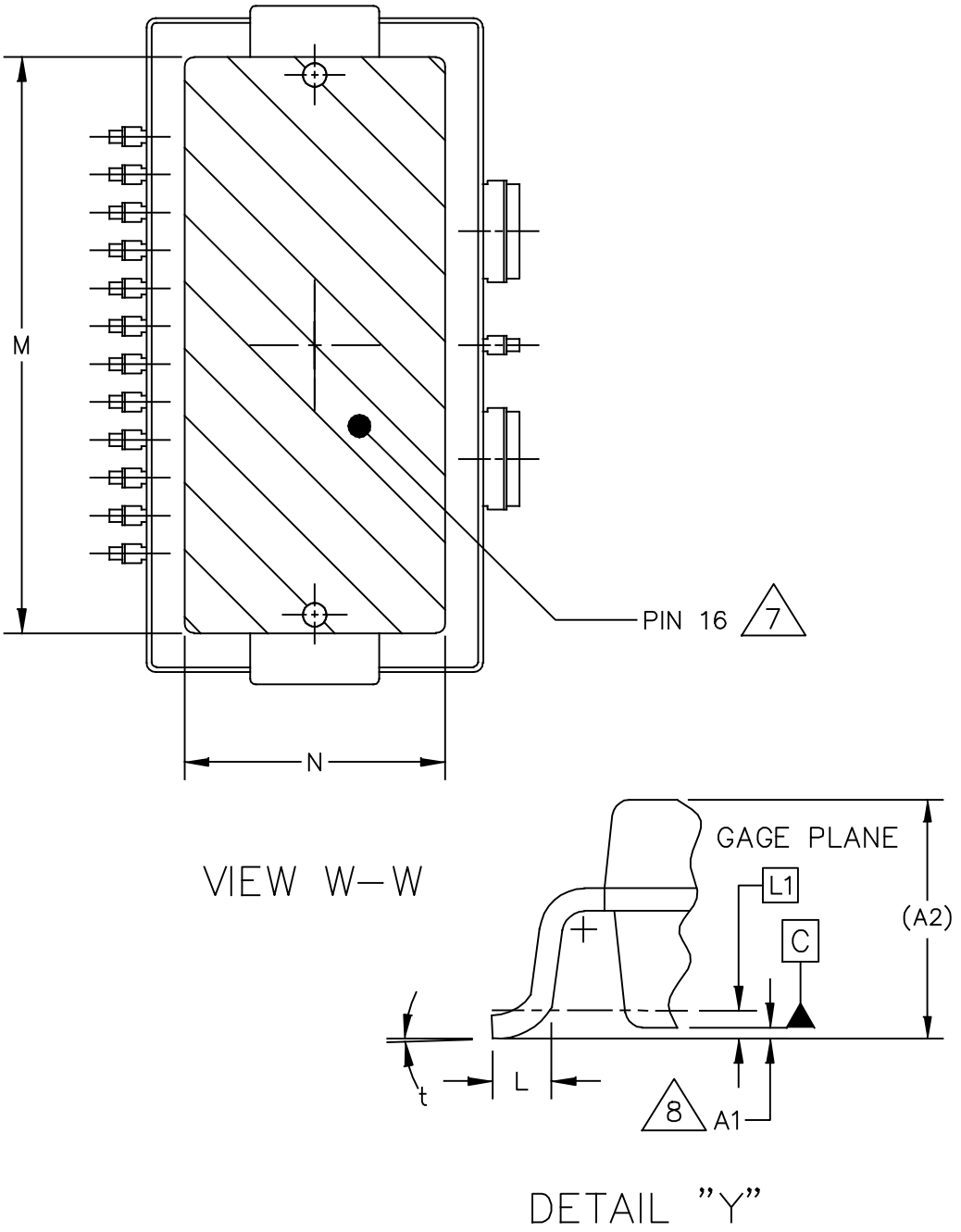

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NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUM PLANE H IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 INCH (0.15 MM) PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

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6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

7. HATCHING REPRESENTS THE EXPOSED AND SOLDERABLE AREA OF THE HEAT SLUG. DIMENSIONS M AND N REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF THE HEAT SLUG.

8. DIMENSION A1 IS MEASURED WITH REFERENCE TO DATUM C. THE POSITIVE VALUE IMPLIES THAT THE BOTTOM OF THE PACKAGE IS HIGHER THAN THE BOTTOM OF THE LEAD.

9. THESE SURFACES OF THE HEAT SLUG ARE NOT PART OF THE SOLDERABLE SURFACES AND MAY REMAIN UNPLATED.

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
AA	.099	.105	2.51	2.67	M	.600	----	15.24	----
A1	.001	.004	0.03	0.10	N	.270	----	6.86	----
A2	(.105)		(2.67)		bb	.097	.103	2.46	2.62
D	.688	.692	17.48	17.58	b1	.010	.016	0.25	0.41
D1	.712	.720	18.08	18.29	c1	.007	.011	0.18	0.28
E	.429	.437	10.90	11.10	e	.020 BSC		0.51 BSC	
E1	.353	.357	8.97	9.07	e1	.040 BSC		1.02 BSC	
E2	.346	.350	8.79	8.89	e2	.253 INFO ONLY		6.43 INFO ONLY	
E3	.132	.140	3.35	3.56	e3	.120 BSC		3.05 BSC	
L	.018	.024	0.46	0.61	t	2°	8°	2°	8°
L1	.010 BSC		0.25 BSC		aaa	.004		0.10	
					bbb	.008		0.20	

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PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Over-Molded Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN1977: Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family
- AN1987: Quiescent Current Control for the RF Integrated Circuit Device Family

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

Development Tools

- Printed Circuit Boards

To Download Resources Specific to a Given Part Number:

1. Go to http://www.nxp.com/RF
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Sept. 2018	• Initial release of data sheet

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