PRELIMINARY

PSoC® Analog Coprocessor: CY8C4Axx Family Datasheet

Programmable System-on-Chip (PSoC®)

General Description

Cypress's PSoC® Analog Coprocessor is a scalable and reconfigurable platform architecture of programmable analog coprocessors that simplify designing embedded systems with multiple sensors. The PSoC Analog Coprocessor device combines PSoC's flexible Analog Front Ends, programmable analog filters, and high-resolution analog-to-digital converters along with an efficient yet powerful 32-bit ARM® Cortex®-M0+ based signal processing engine – enabling host processors to easily fetch aggregated, pre-processed, and formatted complex sensor data over serial communication interfaces.

Features

Programmable Analog Blocks

- A switched-capacitor Universal Analog Block (UAB) programmable via PSoC Creator as a second-order analog filter, a 14-bit Incremental Delta-Sigma ADC, or a 13-bit Voltage DAC
- Two dedicated analog-to-digital converters (ADC) including a 12-bit SAR ADC and a 10-bit single-slope ADC
- Four opamps, two low-power comparators, and a flexible 38-channel analog mux to create custom Analog Front Ends (AFE)
- Two 7-bit Current DACs (IDACs) for general-purpose or capacitive sensing applications on any pin

CapSense® Capacitive Sensing

- Cypress's fourth-generation CapSense Sigma-Delta (CSD) providing best-in-class signal-to-noise ratio (SNR) and water tolerance
- Cypress-supplied software component makes capacitive sensing design easy
- Automatic hardware tuning (SmartSense™)

Segment LCD Drive

- LCD drive supported on all pins (common or segment)
- Operates in Deep-Sleep mode with four bits per pin memory

Programmable Digital Peripherals

- Three independent serial communication blocks (SCBs) that are run-time configurable as I2C, SPI or UART
- Eight 16-bit timer/counter/pulse-width modulator (TCPWM) blocks with center-aligned, edge, and pseudo-random modes

32-bit Signal Processing Engine

- ARM Cortex-M0+ CPU up to 48 MHz
- Up to 32 KB of flash with read accelerator
- Up to 4 KB of SRAM
- Eight-channel descriptor-based DMA controller

Low-Power Operation

- 1.71-V to 5.5-V operation
- Deep-Sleep mode with operational analog and 2.5-µA digital system current
- Watch Crystal Oscillator (WCO)

Programmable GPIO Pins

- Up to 38 GPIOs that can be used for analog, digital, CapSense, or LCD functions with programmable drive modes, strength and slew rates
- Includes eight Smart I/Os to implement pin-level Boolean operations on input and output signals
- 48-pin QFN, 48-pin TQFP, 28-pin SSOP, and 45-ball WLCSP packages

PSoC Creator Design Environment

- Integrated Design Environment (IDE) provides schematic-capture design entry and build (with automatic routing of analog and digital signals) and concurrent firmware development with an ARM-SWD debugger
- GUI-based configurable PSoC Components with fully engineered embedded initialization, calibration and correction algorithms
- Application Programming Interfaces (API) for all fixed-function and programmable peripherals

Industry-Standard Tool Compatibility

- After schematic-capture, firmware development can be done with ARM-based industry-standard development tools

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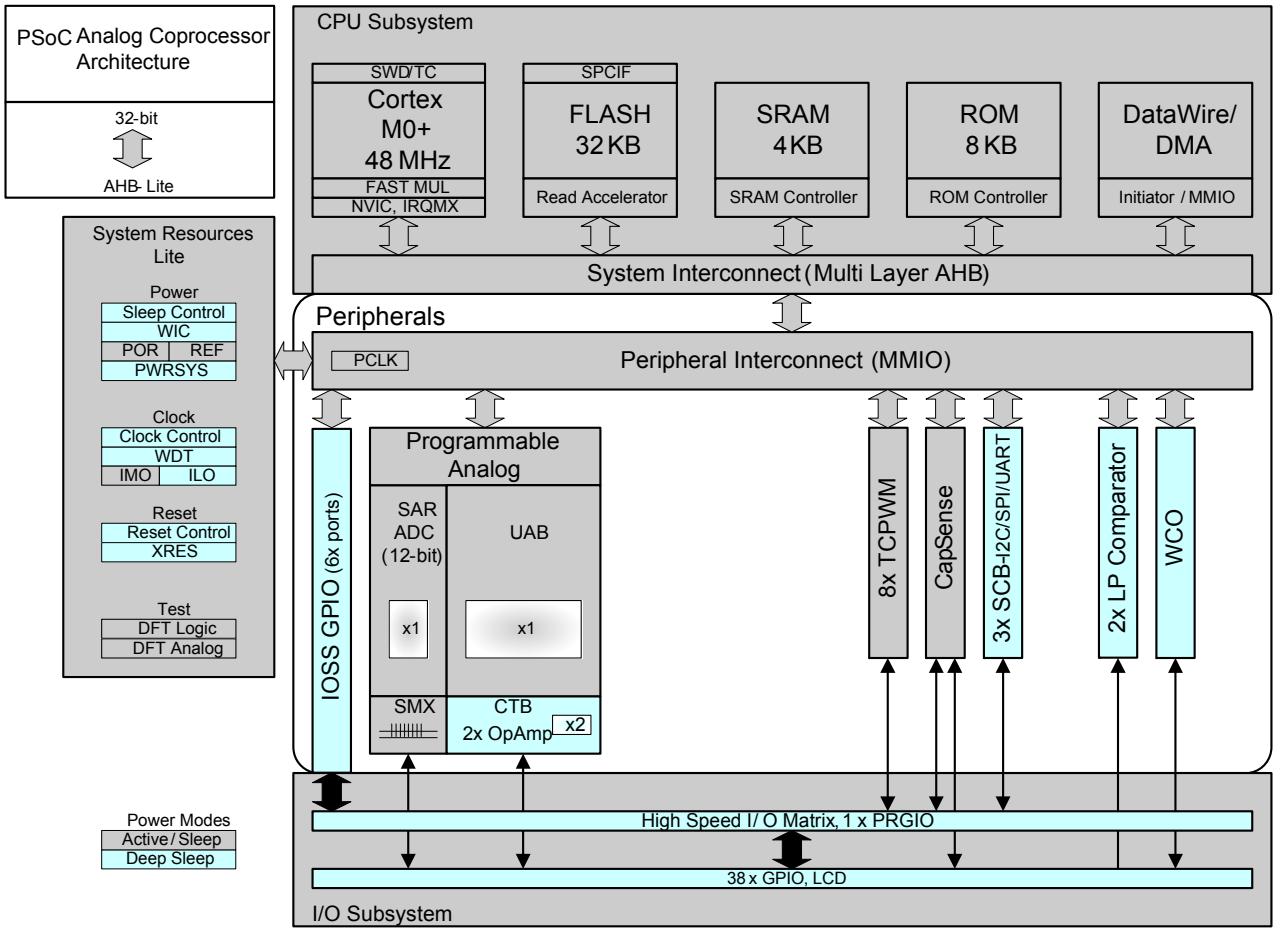
Figure 1. Block Diagram



PSoC Analog Coprocessor devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The ARM Serial-Wire Debug (SWD) interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full-device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC Creator IDE provides fully integrated programming and debug support for the PSoC Analog Coprocessor devices. The SWD interface is fully compatible with industry-standard third-party tools. The PSoC Analog Coprocessor family provides a level of security not possible with multi-chip application solutions or with microcontrollers. It has the following advantages:

- Allows disabling of debug features
- Robust flash protection
- Allows customer-proprietary functionality to be implemented in on-chip programmable blocks

The debug circuits are enabled by default and can be disabled in firmware. If they are not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging. Thus firmware control of debugging cannot be over-ridden without erasing the firmware thus providing security.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. All programming, debug, and test interfaces are disabled when maximum device security is enabled. Therefore, PSoC Analog Coprocessor, with device security enabled, may not be returned for failure analysis. This is a trade-off the PSoC Analog Coprocessor allows the customer to make.

Functional Definition

CPU and Memory Subsystem

CPU

The Cortex-M0+ CPU in the PSoC Analog Coprocessor is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. Most instructions are 16 bits in length and the CPU executes a subset of the Thumb-2 instruction set. It includes a nested vectored interrupt controller (NVIC) block with eight interrupt inputs and also includes a Wakeup Interrupt Controller (WIC). The WIC can wake the processor from Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in Deep Sleep mode.

The CPU also includes a debug interface, the serial wire debug (SWD) interface, which is a two-wire form of JTAG. The debug configuration used for PSoC Analog Coprocessor has four breakpoint (address) comparators and two watchpoint (data) comparators.

DMA/DataWire

The DMA engine will be capable of doing independent data transfers anywhere within the memory map via a user-programmable descriptor chain. The DataWire capability is used to effect single-element transfers from one location in memory to another. There are eight DMA channels with a range of selectable trigger sources.

Flash

The PSoC Analog Coprocessor device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The low-power flash block is designed to deliver two wait-state (WS) access time at 48 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average.

SRAM

Four KB of SRAM are provided with zero wait-state access at 48 MHz.

SROM

Eight KB of SROM are provided that contain boot and configuration routines.

System Resources

Power System

The power system is described in detail in the section Power on page 12. It provides an assurance that voltage levels are as required for each respective mode and either delays mode entry (for example, on power-on reset (POR) until voltage levels are as required for proper functionality, or generates resets (for example, on brown-out detection). The PSoC Analog Coprocessor operates with a single external supply over the range of either 1.8 V ±5% (externally regulated) or 1.8 to 5.5 V (internally regulated) and has three different power modes, transitions between which are managed by the power system. The PSoC Analog Coprocessor provides Active, Sleep, and Deep Sleep low-power modes.

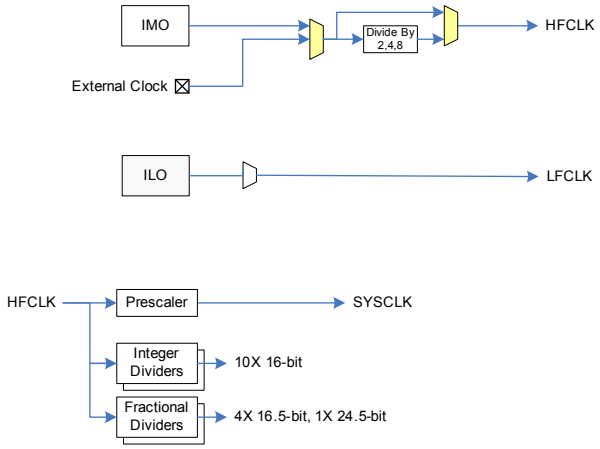
All subsystems are operational in Active mode. The CPU subsystem (CPU, flash, and SRAM) is clock-gated off in Sleep mode, while all peripherals and interrupts are active with instantaneous wake-up on a wake-up event. In Deep Sleep mode, the high-speed clock and associated circuitry is switched off; wake-up from this mode takes 35 µs. The opamps can remain operational in Deep Sleep mode.

Clock System

The PSoC Analog Coprocessor clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that there are no metastable conditions.

The clock system for the PSoC Analog Coprocessor consists of the internal main oscillator (IMO), internal low-frequency oscillator (ILO), a 32 kHz Watch Crystal Oscillator (WCO) and provision for an external clock. Clock dividers are provided to generate clocks for peripherals on a fine-grained basis. Fractional dividers are also provided to enable clocking of higher data rates for UARTs.

Figure 2. PSoC Analog Coprocessor MCU Clocking Architecture



The HFCLK signal can be divided down to generate synchronous clocks for the analog and digital peripherals. There are 15 clock dividers for the PSoC Analog Coprocessor. The 16-bit capability allows flexible generation of fine-grained frequency values (there is one 24-bit divider for large divide ratios), and is fully supported in PSoC Creator.

IMO Clock Source

The IMO is the primary source of internal clocking in the PSoC Analog Coprocessor. It is trimmed during testing to achieve the specified accuracy.The IMO default frequency is 24 MHz and it can be adjusted from 24 to 48 MHz in steps of 4 MHz. The IMO tolerance with Cypress-provided calibration settings is ±2%.

ILO Clock Source

The ILO is a very low power, nominally 40-kHz oscillator, which is primarily used to generate clocks for the watchdog timer (WDT) and peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Cypress provides a software component, which does the calibration.

Watch Crystal Oscillator (WCO)

The PSoC Analog Coprocessor clock subsystem also implements a low-frequency (32-kHz watch crystal) oscillator that can be used for precision timing applications.

Watchdog Timer

A watchdog timer is implemented in the clock block running from the ILO; this allows watchdog operation during Deep Sleep and generates a watchdog reset if not serviced before the set timeout occurs. The watchdog reset is recorded in a Reset Cause register, which is firmware readable.

Reset

The PSoC Analog Coprocessor can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the reset. An XRES pin is reserved for external reset by asserting it active low. The XRES pin has an internal pull-up resistor that is always enabled.

Voltage Reference

The PSoC Analog Coprocessor reference system generates all internally required references. A 1.2-V voltage reference is provided for the comparator. The IDACs are based on a ±5% reference.

Analog Blocks

12-bit SAR ADC

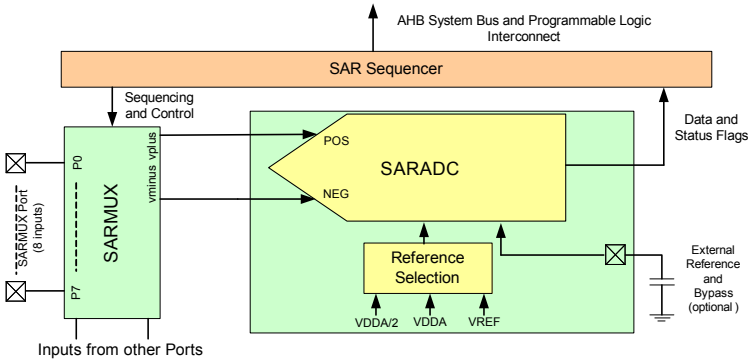
The 12-bit, 1-Msps SAR ADC can operate at a maximum clock rate of 18 MHz and requires a minimum of 18 clocks at that frequency to do a 12-bit conversion.

The Sample-and-Hold (S/H) aperture is programmable allowing the gain bandwidth requirements of the amplifier driving the SAR inputs, which determine its settling time, to be relaxed if required. It is possible to provide an external bypass (through a fixed pin location) for the internal reference amplifier.

The SAR is connected to a fixed set of pins through an 8-input sequencer. The sequencer cycles through selected channels autonomously (sequencer scan) with zero switching overhead (that is, aggregate sampling bandwidth is equal to 1 Msps whether it is for a single channel or distributed over several channels). The sequencer switching is effected through a state machine or through firmware driven switching. A feature provided by the sequencer is buffering of each channel to reduce CPU interrupt service requirements. To accommodate signals with varying source impedance and frequency, it is possible to have different sample times programmable for each channel. Also, signal range specification through a pair of range registers (low and high range values) is implemented with a corresponding out-of-range interrupt if the digitized value exceeds the programmed range; this allows fast detection of out-of-range values without the necessity of having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software.

The SAR is not available in Deep Sleep mode as it requires a high-speed clock (up to 18 MHz). The SAR operating range is 1.71 V to 5.5 V.

Figure 3. SAR ADC



Four Opamps (Continuous-Time Block; CTB)

The PSoC Analog Coprocessor has four opamps with Comparator modes which allow most common analog functions to be performed on-chip eliminating external components; PGAs, Voltage Buffers, Filters, Trans-Impedance Amplifiers, and other functions can be realized, in some cases with external passives, saving power, cost, and space. The on-chip opamps are designed with enough bandwidth to drive the Sample-and-Hold circuit of the ADC without requiring external buffering.

Universal Analog Block (UAB) Discrete-Time Block

The UAB Block consists of switched-capacitor feedback and input networks connected to two opamp structures; the two halves of the structure can be used independently, thus a bi-quad filter structure can be made using the two halves independently in single-ended mode. General analog functions can be implemented with the switched-capacitor network and the opamps examples of functions implementable with the UAB are: DAC, multi-pole SC filters (cascadable blocks), delta-sigma modulator, mixers, integrators, PGAs, and other useful functions using Cypress PSoC Creator with Cypress-supplied software components.

Low-power Comparators (LPC)

The PSoC Analog Coprocessor has a pair of low-power comparators, which can also operate in Deep Sleep modes. This allows the analog system blocks to be disabled while retaining the ability to monitor external voltage levels during low-power modes. The comparator outputs are normally synchronized to avoid metastability unless operating in an asynchronous power mode where the system wake-up circuit is activated by a comparator switch event. The LPC outputs can be routed to pins.

Current DACs

The PSoC Analog Coprocessor has two IDACs, which can drive any of the pins on the chip. These IDACs have programmable current ranges.

Analog Multiplexed Buses

The PSoC Analog Coprocessor has two concentric independent buses that go around the periphery of the chip. These buses (called amux buses) are connected to firmware-programmable analog switches that allow the chip's internal resources (IDACs, comparator) to connect to any pin on the I/O Ports.

Temperature Sensor

There is an on-chip temperature sensor which is calibrated during production to achieve ±1% typical (±5% maximum) deviation from accuracy. The SAR ADC is used to measure the temperature.

Fixed Function Digital

Timer/Counter/PWM (TCPWM) Block

The TCPWM block consists of a 16-bit counter with user-programmable period length. There is a capture register to record the count value at the time of an event (which may be an I/O event), a period register that is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals that are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow use as dead-band programmable complementary PWM outputs. It also has a Kill input to force outputs to a predetermined state; for example, this is used in motor drive systems when an over-current state is indicated and the PWM driving the FETs needs to be shut off immediately with no time for software intervention. There are eight TCPWM blocks in the PSoC Analog Coprocessor.

Serial Communication Block (SCB)

The PSoC Analog Coprocessor has three serial communication blocks, which can be programmed to have SPI, I^2C, or UART functionality.

I^2C Mode: The hardware I^2C block implements a full multi-master and slave interface (it is capable of multi-master arbitration). This block is capable of operating at speeds of up to 1 Mbps (Fast Mode Plus) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. It also supports EZI2C that creates a mailbox address range in the memory of the PSoC Analog Coprocessor and effectively reduces I^2C communication to reading from and writing to an array in memory. In addition, the block supports an 8-deep FIFO for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time.

The I^2C peripheral is compatible with the I^2C Standard-mode and Fast-mode devices as defined in the NXP I^2C-bus specification and user manual (UM10204). The I^2C bus I/O is implemented with GPIO in open-drain modes.

The PSoC Analog Coprocessor is not completely compliant with the I^2C spec in the following respect:

- GPIO cells are not overvoltage tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I^2C system.

UART Mode: This is a full-feature UART operating at up to 1 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. An 8-deep FIFO allows much greater CPU service latencies to be tolerated.

SPI Mode: The SPI mode supports full Motorola SPI, TI SSP (adds a start pulse used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI). The SPI block can use the FIFO.

GPIO

The PSoC Analog Coprocessor has up to 38 GPIOs. The GPIO block implements the following:

- Eight drive modes:
  - Analog input mode (input and output buffers disabled)
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL).
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes
- Selectable slew rates for dV/dt related noise control to improve EMI

The pins are organized in logical entities called ports, which are 8-bit in width (less for Ports 2 and 3). During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it (4 for PSoC Analog Coprocessor). The Smart I/O block is a fabric of switches and LUTs that allows Boolean functions to be performed on signals being routed to the pins of a GPIO port. The Smart I/O block can perform logical operations on input pins to the chip and on signals going out as outputs.

Special Function Peripherals

CapSense

CapSense is supported in the PSoC Analog Coprocessor through a CSD block that can be connected to any pins through an analog mux bus via an analog switch. CapSense function can thus be provided on any available pin or group of pins in a system under software control. A PSoC Creator component is provided for the CapSense block to make it easy for the user.

Shield voltage can be driven on another mux bus to provide water-tolerance capability. Water tolerance is provided by driving the shield electrode in phase with the sense electrode to keep the shield capacitance from attenuating the sensed input. Proximity sensing can also be implemented.

The CapSense block has two IDACs, which can be used for general purposes if CapSense is not being used (both IDACs are available in that case) or if CapSense is used without water tolerance (one IDAC is available). The CapSense block also provides a 10-bit Slope ADC function, which can be used in conjunction with the CapSense function.

The CapSense block is an advanced, low-noise, programmable block with programmable voltage references and current source ranges for improved sensitivity and flexibility. It can also use an external reference voltage. It has a full-wave CSD mode that alternates sensing to VDDA and ground to null out power-supply related noise

WLCSP Package Bootloader

The WLCSP package is supplied with an I^2C bootloader installed in flash. The bootloader is compatible with PSoC Creator bootloader project files.

Pinouts

The following table provides the pin list for PSoC Analog Coprocessor for the 48 QFN, 48 TQFP, 45 WLCSP, and 28 SSOP packages. All port pins support GPIO.

Packages							
48-QFN		48-TQFP		28-SSOP		45-CSP	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
28	P0.0	28	P0.0	21	P0.0	D3	P0.0
29	P0.1	29	P0.1	22	P0.1	E2	P0.1
30	P0.2	30	P0.2	23	P0.2	D2	P0.2
31	P0.3	31	P0.3			C3	P0.3
32	P0.4	32	P0.4			D1	P0.4
33	P0.5	33	P0.5			E1	P0.5
34	P0.6	34	P0.6			C2	P0.6
35	P0.7	35	P0.7			B2	P0.7
36	XRES	36	XRES	24	XRES	B3	XRES
37	P4.0	37	P4.0			A1	P4.0
38	P4.1	38	P4.1			B1	P4.1
39	P5.0	39	P5.0	25	P5.0	B4	P5.0
40	P5.1	40	P5.1			C1	P5.1
41	P5.2	41	P5.2	26	P5.2	A2	P5.2
42	P5.3	42	P5.3	27	P5.3	A3	P5.3
43	VDDA	43	VDDA	28	VDDA	J2	VDDA
44	VSSA	44	VSSA	29	VSSA	J3	VSSA
45	VCCD	45	VCCD	1	VCCD	A4	VCCD
						B5	VDDD
46	VSSD	46	VSSD	2	VSSD	A5	VSSD
47	VDDD	47	VDDD	3	VDDD		
48	P1.0	48	P1.0	4	P1.0	C5	P1.0
1	P1.1	1	P1.1	5	P1.1	C4	P1.1
2	P1.2	2	P1.2	6	P1.2	D5	P1.2
3	P1.3	3	P1.3	7	P1.3	D4	P1.3
4	P1.4	4	P1.4			E3	P1.4
5	P1.5	5	P1.5			E4	P1.5
6	P1.6	6	P1.6				
7	P1.7	7	P1.7			G3	P1.7
8	VDDA	8	VDDA	8	VDDA	E5	VDDA
9	VSSA	9	VSSA	9	VSSA	F5	VSSA
10	P2.0	10	P2.0	10	P2.0	F4	P2.0
11	P2.1	11	P2.1	11	P2.1	F3	P2.1
12	P2.2	12	P2.2	12	P2.2	G4	P2.2
13	P2.3	13	P2.3	13	P2.3	G5	P2.3
14	P2.4	14	P2.4			H5	P2.4
15	P2.5	15	P2.5			J4	P2.5

Packages							
48-QFN		48-TQFP		28-SSOP		45-CSP	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
16	P2.6	16	P2.6			H4	P2.6
17	P2.7/VREF	17	P2.7/VREF	14	P2.7/VREF	J5	P2.7/VREF
18	VSSA	18	VSSA	30	VSSA	J3	VSSA
19	VDDA	19	VDDA	15	VDDA	J2	VDDA
20	P3.0	20	P3.0			H2	P3.0
21	P3.1	21	P3.1	16	P3.1	F2	P3.1
22	P3.2	22	P3.2	17	P3.2	J1	P3.2
23	P3.3	23	P3.3	18	P3.3	H3	P3.3
24	P3.4	24	P3.4			F1	P3.4
25	P3.5	25	P3.5			G2	P3.5
26	P3.6	26	P3.6	19	P3.6	G1	P3.6
27	P3.7	27	P3.7	20	P3.7	H1	P3.7

Descriptions of the Power pins are as follows:

VDDD: Power supply for the digital section.

VDDA: Power supply for the analog section.

VSS: Ground pin.

VCCD: Regulated digital supply (1.8 V ±5%)

The 48-pin packages have 38 I/O pins. The 45 CSP and the 28 SSOP have 37 and 20 I/O pins respectively

Alternate Pin Functions

Each Port pin has can be assigned to one of multiple functions; it can, for example, be an Analog I/O, a Digital Peripheral function, or a CapSense or LCD pin. The pin assignments are shown in the following table.

Port/Pin	Analog	SmartIO	Active				DeepSleep	
			ACT #0	ACT #1	ACT #2	ACT #3	DS #0	DS #1
P0.0	lpcomp.in_p[0]	SmartIO[0].io[0]	tcpwm.line[4]:1		pass.dsi_sar_data[0]:0	tcpwm.tr_in[0]	cpuss.swd_data:0	scb[0].spi_select1:0
P0.1	lpcomp.in_n[0]	SmartIO[0].io[1]	tcpwm.line_compl[4]:1		pass.dsi_sar_data[1]:0	tcpwm.tr_in[1]	cpuss.swd_clk:0	scb[0].spi_select2:0
P0.2		SmartIO[0].io[2]	tcpwm.line[5]:1		srss.ext_clk	pass.tr_gen_trig_in[0]	pass.dsi_ctb_cmp0[0]	scb[0].spi_select3:0
P0.3		SmartIO[0].io[3]	tcpwm.line_compl[5]:1		pass.dsi_sar_data[2]:1	pass.tr_gen_trig_in[1]	pass.dsi_ctb_cmp1[0]	
P0.4		SmartIO[0].io[4]	tcpwm.line[6]:1	scb[1].uart_rx:0	pass.dsi_sar_data[3]:1	pass.tr_uab_trig0_out:0	scb[1].i2c_scl:0	scb[1].spi_mosi:0
P0.5		SmartIO[0].io[5]	tcpwm.line_compl[6]:1	scb[1].uart_tx:0	pass.dsi_sar_data[4]:1	pass.tr_uab_trig1_out:0	scb[1].i2c_sda:0	scb[1].spi_miso:0
P0.6		SmartIO[0].io[6]		scb[1].uart_cts:0	pass.dsi_sar_data[5]:1	pass.dsi_uab_cmp0	lpcomp.comp[0]:0	scb[1].spi_clk:0
P0.7		SmartIO[0].io[7]		scb[1].uart_rts:0	pass.dsi_sar_data[6]:1	pass.dsi_uab_cmp1	lpcomp.comp[1]:0	scb[1].spi_select0:0
P4.0	wco.wco_in		tcpwm.line[0]:2	scb[2].uart_rx:1	pass.dsi_sar_data[7]:1	tcpwm.tr_in[5]	scb[2].i2c_scl:1	scb[2].spi_mosi:1
P4.1	wco.wco_out		tcpwm.line_compl[0]:2	scb[2].uart_tx:1	pass.dsi_sar_data[8]:1	tcpwm.tr_in[6]	scb[2].i2c_sda:1	scb[2].spi_miso:1
P5.0	csd.cshieldpads		tcpwm.line[7]:1	scb[0].uart_rx:1	pass.dsi_sar_data_valid		scb[0].i2c_scl:1	scb[0].spi_mosi:1
P5.1	csd.vref_ext		tcpwm.line_compl[7]:1	scb[0].uart_tx:1	pass.dsi_sar_sample_done		scb[0].i2c_sda:1	scb[0].spi_miso:1
P5.2	csd.dsi_cmod		tcpwm.line[6]:2	scb[0].uart_cts:1	pass.tr_sar_out		pass.dsi_ctb_cmp0[1]	scb[0].spi_clk:1
P5.3	csd.dsi_csh_tank		tcpwm.line_compl[6]:2	scb[0].uart_rts:1	pass.dsi_sar_data[9]:0		pass.dsi_ctb_cmp1[1]	scb[0].spi_select0:1
P1.0	ctb_pads[8] lpcomp.in_p[1]		tcpwm.line[0]:1	scb[1].uart_rx:1	pass.dsi_sar_data[10]:0	pass.tr_decm_intr0	scb[1].i2c_scl:1	scb[1].spi_mosi:1
P1.1	ctb_pads[9] lpcomp.in_n[1]		tcpwm.line_compl[0]:1	scb[1].uart_tx:1	pass.dsi_sar_data[11]:0	pass.tr_decm_intr1	scb[1].i2c_sda:1	scb[1].spi_miso:1
P1.2	ctb_pads[10] ctb_oa0_out_10x[1]		tcpwm.line[1]:1	scb[1].uart_cts:1	pass.dsi_sar_data[2]:0			scb[1].spi_clk:1
P1.3	ctb_pads[11] ctb_oa1_out_10x[1]		tcpwm.line_compl[1]:1	scb[1].uart_rts:1	pass.dsi_sar_data[3]:0			scb[1].spi_select0:1
P1.4	ctb_pads[12]		tcpwm.line[2]:1					scb[1].spi_select1:0
P1.5	ctb_pads[13]		tcpwm.line_compl[2]:1					scb[1].spi_select2:0
P1.6	ctb_pads[14]		tcpwm.line[3]:1					scb[1].spi_select3:0
P1.7	ctb_pads[15]		tcpwm.line_compl[3]:1					
P2.0	ctb_pads[0]		tcpwm.line[4]:0	scb[2].uart_rx:0	pass.dsi_sar_data[4]:0		scb[2].i2c_scl:0	scb[2].spi_mosi:0

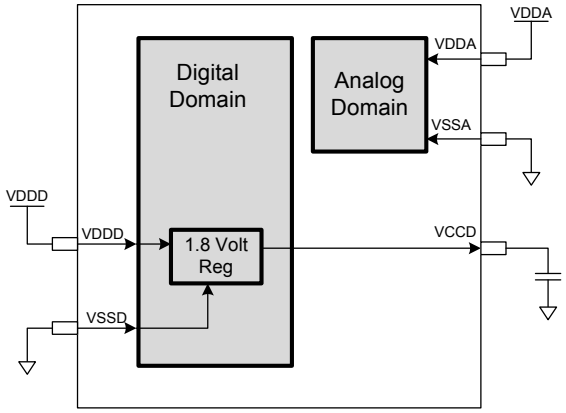
Port/Pin	Analog	SmartIO	Active				DeepSleep	
			ACT #0	ACT #1	ACT #2	ACT #3	DS #0	DS #1
P2.1	ctb_pads[1]		tcpwm.line_compl[4]:0	scb[2].uart_tx:0	pass.dsi_sar_data[5]:0		scb[2].i2c_sda:0	scb[2].spi_miso:0
P2.2	ctb_pads[2] ctb_oa0_out_10x[0]		tcpwm.line[5]:0	scb[2].uart_cts:0	pass.dsi_sar_data[6]:0			scb[2].spi_clk:0
P2.3	ctb_pads[3] ctb_oa1_out_10x[0]		tcpwm.line_compl[5]:0	scb[2].uart_rts:0	pass.dsi_sar_data[7]:0			scb[2].spi_select0:0
P2.4	ctb_pads[4] pass.lnfe_base_hv		tcpwm.line[0]:0					scb[2].spi_select1:0
P2.5	ctb_pads[5] pass.lnfe_emitter_hv		tcpwm.line_compl[0]:0					scb[2].spi_select2:0
P2.6	ctb_pads[6]		tcpwm.line[1]:0					scb[2].spi_select3:0
P2.7	ctb_pads[7]		tcpwm.line_compl[1]:0					
	sar_ext_vref0 sar_ext_vref1							
P3.0	sarmux_pads[0]		tcpwm.line[2]:0	scb[0].uart_rx:0			scb[0].i2c_scl:0	scb[0].spi_mosi:0
P3.1	sarmux_pads[1]		tcpwm.line_compl[2]:0	scb[0].uart_tx:0	pass.dsi_sar_data[8]:0		scb[0].i2c_sda:0	scb[0].spi_miso:0
P3.2	sarmux_pads[2]		tcpwm.line[3]:0	scb[0].uart_cts:0			cpuss.swd_data:1	scb[0].spi_clk:0
P3.3	sarmux_pads[3]		tcpwm.line_compl[3]:0	scb[0].uart_rts:0			cpuss.swd_clk:1	scb[0].spi_select0:0
P3.4	sarmux_pads[4]		tcpwm.line[6]:0		pass.dsi_sar_data[10]:1	tcpwm.tr_in[2]		scb[0].spi_select1:1
P3.5	sarmux_pads[5]		tcpwm.line_compl[6]:0		pass.dsi_sar_data[11]:1	tcpwm.tr_in[3]	csd.comp	scb[0].spi_select2:1
P3.6	sarmux_pads[6]		tcpwm.line[7]:0	scb[2].uart_rx:2		tcpwm.tr_in[4]	scb[2].i2c_scl:2	scb[2].spi_mosi:2
P3.7	sarmux_pads[7]		tcpwm.line_compl[7]:0	scb[2].uart_tx:2			scb[2].i2c_sda:2	scb[2].spi_miso:2

Power

The following power system diagram shows the set of power supply pins as implemented for the PSoC Analog Coprocessor. The system has one regulator in Active mode for the digital circuitry. There is no analog regulator; the analog circuits run directly from the V_{DDA} input.

Note that VDDD and VDDA must be shorted together on the PCB.

Figure 4. Power Supply Connections



There are two distinct modes of operation. In Mode 1, the supply voltage range is 1.8 V to 5.5 V (unregulated externally; internal regulator operational). In Mode 2, the supply range is1.8 V ±5% (externally regulated; 1.71 to 1.89, internal regulator bypassed).

Mode 1: 1.8 V to 5.5 V External Supply

In this mode, the PSoC Analog Coprocessor is powered by an external power supply that can be anywhere in the range of 1.8 to 5.5 V. This range is also designed for battery-powered operation. For example, the chip can be powered from a battery system that starts at 3.5 V and works down to 1.8 V. In this mode, the internal regulator of the PSoC Analog Coprocessor supplies the internal logic and its output is connected to the V_{CCD} pin. The V_{CCD} pin must be bypassed to ground via an external capacitor (0.1 µF; X5R ceramic or better) and must not be connected to anything else.

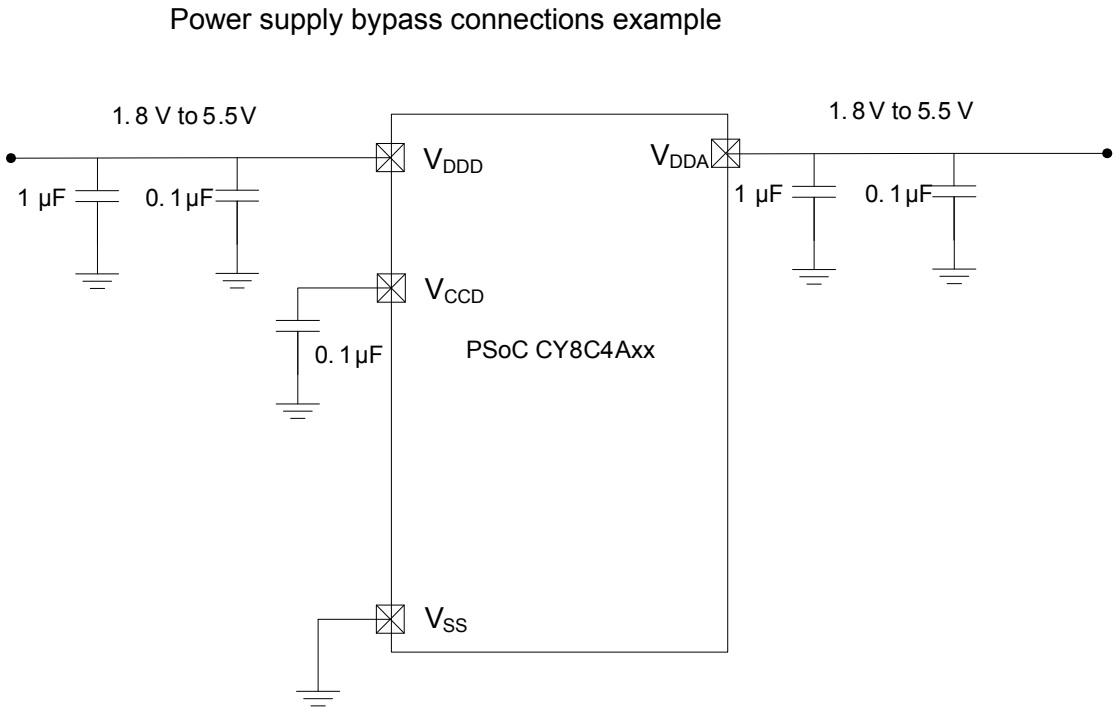
Mode 2: 1.8 V ±5% External Supply

In this mode, the PSoC Analog Coprocessor is powered by an external power supply that must be within the range of 1.71 to 1.89 V; note that this range needs to include the power supply ripple too. In this mode, the V_{DDD} and V_{CCD} pins are shorted together and bypassed. The internal regulator can be disabled in the firmware.

Bypass capacitors must be used from V_{DDD} and V_{DDA} to ground. The typical practice for systems in this frequency range is to use a capacitor in the 1-µF range, in parallel with a smaller capacitor (0.1 µF, for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

An example of a bypass scheme is shown in the following diagram.

Figure 5. External Supply Range from 1.8 V to 5.5 V with Internal Regulator Active



Development Support

The PSoC Analog Coprocessor family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit www.cypress.com/go/psoc4 to find out more.

Documentation

A suite of documentation supports the PSoC Analog Coprocessor family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

Software User Guide: A step-by-step guide for using PSoC Creator. The software user guide shows you how the PSoC Creator build process works in detail, how to use source control with PSoC Creator, and much more.

Component Datasheets: The flexibility of PSoC allows the creation of new peripherals (components) long after the device has gone into production. Component data sheets provide all of the information needed to select and use a particular component, including a functional description, API documentation, example code, and AC/DC specifications.

Application Notes: PSoC application notes discuss a particular application of PSoC in depth; examples include brushless DC motor control and on-chip filtering. Application notes often include example projects in addition to the application note document.

Technical Reference Manual: The Technical Reference Manual (TRM) contains all the technical detail you need to use a PSoC device, including a complete description of all PSoC registers. The TRM is available in the Documentation section at www.cypress.com/psoc4.

Online

In addition to print documentation, the Cypress PSoC forums connect you with fellow PSoC users and experts in PSoC from around the world, 24 hours a day, 7 days a week.

Tools

With industry standard cores, programming, and debugging interfaces, the PSoC Analog Coprocessor family is part of a development tool ecosystem. Visit us at www.cypress.com/go/psoccreator for the latest information on the revolutionary, easy to use PSoC Creator IDE, supported third party compilers, programmers, debuggers, and development kits.

Electrical Specifications

Absolute Maximum Ratings

Table 1. Absolute Maximum Ratings[1]

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID1	V_{DD_ABS}	Digital or Analog supply relative to V_{SS}	–0.5	–	6	V	V_{DDD}, V_{DDA}, Absolute Max
SID2	V_{CCD_ABS}	Direct digital core voltage input relative to V_{SS}	–0.5	–	1.95		–
SID3	V_{GPIO_ABS}	GPIO voltage	–0.5	–	V_{DD}+0.5		–
SID4	I_{GPIO_ABS}	Maximum current per GPIO	–25	–	25	mA	–
SID5	$I_{GPIO_injection}$	GPIO injection current, Max for V_{IH} > V_{DDD}, and Min for V_{IL} < V_{SS}	–0.5	–	0.5		Current injected per pin
BID44	ESD_HBM	Electrostatic discharge human body model	2200	–	–	V	–
BID45	ESD_CDM	Electrostatic discharge charged device model	500	–	–		–
BID46	LU	Pin current for latch-up	–140	–	140	mA	–

Device Level Specifications

All specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

Table 2. DC Specifications

Typical values measured at V_{DD} = 3.3 V and 25 °C.

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID53	V_{DD}	Power supply input voltage	1.8	–	5.5	V	With regulator enabled
SID255	V_{DD}	Power supply input voltage (V_{CCD} = V_{DD})	1.71	–	1.89		Internally unregulated supply
SID54	V_{DDIO}	V_{DDIO} domain supply	1.71	–	V_{DD}		–
SID55	C_{EFC}	External regulator voltage bypass	–	0.1	–	µF	X5R ceramic or better
SID56	C_{EXC}	Power supply bypass capacitor	–	1	–		X5R ceramic or better
Active Mode, V_{DD} = 1.8 V to 5.5 V. Typical values measured at VDD = 3.3 V and 25 °C.							
SID9	I_{DD5}	Execute from flash; CPU at 6 MHz	–	2	–	mA	–
SID12	I_{DD8}	Execute from flash; CPU at 24 MHz	–	5.6	–		–
SID16	I_{DD11}	Execute from flash; CPU at 48 MHz	–	10.4	–		–
Sleep Mode, VDDD = 1.8 V to 5.5 V (Regulator on)							
SID22	IDD17	I^2C wakeup WDT, and Comparators on	–	1.1	–	mA	6 MHz
SID25	IDD20	I^2C wakeup, WDT, and Comparators on.	–	3.1	–		12 MHz

Note
1. Usage above the absolute maximum conditions listed in Table 1 may cause permanent damage to the device. Exposure to Absolute Maximum conditions for extended periods of time may affect device reliability. The Maximum Storage Temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below Absolute Maximum conditions but above normal operating conditions, the device may not operate to specification.

Table 2. DC Specifications *(continued)*

Typical values measured at V_{DD} = 3.3 V and 25 °C.

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
Sleep Mode, V_{DDD} = 1.71 V to 1.89 V (Regulator bypassed)							
SID28	IDD23	I^2C wakeup, WDT, and Comparators on	–	1.1	–	mA	6 MHz
SID28A	IDD23A	I^2C wakeup, WDT, and Comparators on	–	3.1	–	mA	12 MHz
Deep Sleep Mode, V_{DD} = 1.8 V to 3.6 V (Regulator on)							
SID31	I_{DD26}	I^2C wakeup and WDT on	–	2.5	–	µA	–
Deep Sleep Mode, V_{DD} = 3.6 V to 5.5 V (Regulator on)							
SID34	I_{DD29}	I^2C wakeup and WDT on	–	2.5	–	µA	–
Deep Sleep Mode, V_{DD} = V_{CCD} = 1.71 V to 1.89 V (Regulator bypassed)							
SID37	I_{DD32}	I^2C wakeup and WDT on	–	2.5	–	µA	–
XRES Current							
SID307	I_{DD_XR}	Supply current while XRES asserted	–	2	5	mA	–

Table 3. AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID48	F_{CPU}	CPU frequency	DC	–	48	MHz	$1.71 \le V_{DD} \le 5.5$
SID49[2]	T_{SLEEP}	Wakeup from Sleep mode	–	0	–	µs	
SID50[2]	$T_{DEEPSLEEP}$	Wakeup from Deep Sleep mode	–	35	–		

Note
2. Guaranteed by characterization.

GPIO

Table 4. GPIO DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID57	V_{IH}[3]	Input voltage high threshold	0.7 × V_{DDD}	–	–	V	CMOS Input
SID58	V_{IL}	Input voltage low threshold	–	–	0.3 × V_{DDD}		CMOS Input
SID241	V_{IH}[3]	LVTTL input, V_{DDD} < 2.7 V	0.7 × V_{DDD}	–	–		–
SID242	V_{IL}	LVTTL input, V_{DDD} < 2.7 V	–	–	0.3 × V_{DDD}		–
SID243	V_{IH}[3]	LVTTL input, V_{DDD} ≥ 2.7 V	2.0	–	–		–
SID244	V_{IL}	LVTTL input, V_{DDD} ≥ 2.7 V	–	–	0.8		–
SID59	V_{OH}	Output voltage high level	V_{DDD} –0.6	–	–		I_{OH} = 4 mA at 3 V V_{DDD}
SID60	V_{OH}	Output voltage high level	V_{DDD} –0.5	–	–		I_{OH} = 1 mA at 1.8 V V_{DDD}
SID61	V_{OL}	Output voltage low level	–	–	0.6		I_{OL} = 4 mA at 1.8 V V_{DDD}
SID62	V_{OL}	Output voltage low level	–	–	0.6		I_{OL} = 10 mA at 3 V V_{DDD}
SID62A	V_{OL}	Output voltage low level	–	–	0.4		I_{OL} = 3 mA at 3 V V_{DDD}
SID63	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	–
SID64	$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5		–
SID65	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	25 °C, V_{DDD} = 3.0 V
SID66	C_{IN}	Input capacitance	–	3	7	pF	–
SID67[4]	V_{HYSTTL}	Input hysteresis LVTTL	15	40	–	mV	V_{DDD} ≥ 2.7 V
SID68[4]	$V_{HYSCMOS}$	Input hysteresis CMOS	0.05 × V_{DDD}	–	–		V_{DD} < 4.5 V
SID68A[4]	$V_{HYSCMOS5V5}$	Input hysteresis CMOS	200	–	–		V_{DD} > 4.5 V
SID69[4]	I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	µA	–
SID69A[4]	I_{TOT_GPIO}	Maximum total source or sink chip current	–	–	85	mA	–

Table 5. GPIO AC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID70	T_{RISEF}	Rise time in fast strong mode	2	–	12	ns	3.3 V V_{DDD}, Cload = 25 pF
SID71	T_{FALLF}	Fall time in fast strong mode	2	–	12		3.3 V V_{DDD}, Cload = 25 pF
SID72	T_{RISES}	Rise time in slow strong mode	10	–	60	ns	3.3 V V_{DDD}, Cload = 25 pF

Notes
3. V_{IH} must not exceed V_{DDD} + 0.2 V.
4. Guaranteed by characterization.

Table 5. GPIO AC Specifications

(Guaranteed by Characterization) *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID73	T_{FALLS}	Fall time in slow strong mode	10	–	60	ns	3.3 V V_{DDD}, Cload = 25 pF
SID74	$F_{GPIOUT1}$	GPIO F_{OUT}; 3.3 V ≤ V_{DDD} ≤ 5.5 V Fast strong mode	–	–	16	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID75	$F_{GPIOUT2}$	GPIO F_{OUT}; 1.71 V≤ V_{DDD}≤ 3.3 V Fast strong mode	–	–	16		90/10%, 25 pF load, 60/40 duty cycle
SID76	$F_{GPIOUT3}$	GPIO F_{OUT}; 3.3 V ≤ V_{DDD} ≤ 5.5 V Slow strong mode	–	–	7		90/10%, 25 pF load, 60/40 duty cycle
SID245	$F_{GPIOUT4}$	GPIO F_{OUT}; 1.71 V ≤ V_{DDD} ≤ 3.3 V Slow strong mode.	–	–	3.5		90/10%, 25 pF load, 60/40 duty cycle
SID246	F_{GPIOIN}	GPIO input operating frequency; 1.71 V ≤ V_{DDD} ≤ 5.5 V	–	–	16		90/10% V_{IO}

XRES

Table 6. XRES DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID77	V_{IH}	Input voltage high threshold	0.7 × V_{DDD}	–	–	V	CMOS Input
SID78	V_{IL}	Input voltage low threshold	–	–	0.3 × V_{DDD}		
SID79	R_{PULLUP}	Pull-up resistor	3.5	5.6	10	kΩ	–
SID80	C_{IN}	Input capacitance	–	3	7	pF	–
SID81[5]	$V_{HYSXRES}$	Input voltage hysteresis	–	05*V_{DD}	–	mV	Typical hysteresis is 200 mV for V_{DD} > 4.5 V

Table 7. XRES AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID83[5]	$T_{RESETWIDTH}$	Reset pulse width	1	–	–	µs	–
BID194[5]	$T_{RESETWAKE}$	Wake-up time from reset release	–	–	2.2	ms	–

Note
5. Guaranteed by characterization.

Analog Peripherals

Table 8. CTB Opamp Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
	I_{DD}	Opamp block current, No load					
SID269	I_{DD_HI}	power=hi	–	1100	1850	µA	–
SID270	I_{DD_MED}	power=med	–	550	950		–
SID271	I_{DD_LOW}	power=lo	–	150	350		–
	G_{BW}	Load = 20 pF, 0.1 mA V_{DDA} = 2.7 V					
SID272	G_{BW_HI}	power=hi	6	–	–	MHz	Input and output are 0.2 V to V_{DDA}-0.2 V
SID273	G_{BW_MED}	power=med	3	–	–		Input and output are 0.2 V to V_{DDA}-0.2 V
SID274	G_{BW_LO}	power=lo	–	1	–		Input and output are 0.2 V to V_{DDA}-0.2 V
	I_{OUT_MAX}	V_{DDA} = 2.7 V, 500 mV from rail					
SID275	$I_{OUT_MAX_HI}$	power=hi	10	–	–	mA	Output is 0.5 V V_{DDA}-0.5 V
SID276	$I_{OUT_MAX_MID}$	power=mid	10	–	–		Output is 0.5 V V_{DDA}-0.5 V
SID277	$I_{OUT_MAX_LO}$	power=lo	–	5	–		Output is 0.5 V V_{DDA}-0.5 V
	I_{OUT}	V_{DDA} = 1.71 V, 500 mV from rail					
SID278	$I_{OUT_MAX_HI}$	power=hi	4	–	–	mA	Output is 0.5 V V_{DDA}-0.5 V
SID279	$I_{OUT_MAX_MID}$	power=mid	4	–	–		Output is 0.5 V V_{DDA}-0.5 V
SID280	$I_{OUT_MAX_LO}$	power=lo	–	2	–		Output is 0.5 V V_{DDA}-0.5 V
	I_{DD_Int}	Opamp block current Internal Load					
SID269_I	$I_{DD_HI_Int}$	power=hi	–	1500	1700	µA	–
SID270_I	$I_{DD_MED_Int}$	power=med	–	700	900		–
	G_{BW}	V_{DDA} = 2.7 V					
SID272_I	$G_{BW_HI_Int}$	power=hi	8	–	–	MHz	Output is 0.25 V to V_{DDA}-0.25 V
		General opamp specs for both internal and external modes					
SID281	V_{IN}	Charge-pump on, V_{DDA} = 2.7 V	–0.05	–	V_{DDA}-0.2	V	–
SID282	V_{CM}	Charge-pump on, V_{DDA} = 2.7 V	-0.05	–	V_{DDA}-0.2		

Table 8. CTB Opamp Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID283	V_{OUT_1}	power=hi, Iload=10 mA	0.5	–	V_{DDA} -0.5	V	V_{DD} = 2.7 V
SID284	V_{OUT_2}	power=hi, Iload=1 mA	0.2	–	V_{DDA} -0.2		V_{DDA} = 2.7 V
SID285	V_{OUT_3}	power=med, Iload=1 mA	0.2	–	V_{DDA} -0.2		V_{DDA} = 2.7 V
SID286	V_{OUT_4}	power=lo, Iload=0.1 mA	0.2	–	V_{DDA} -0.2		V_{DDA} = 2.7 V
SID288	V_{OS_TR}	Offset voltage, trimmed	–1.0	±0.5	1.0	mV	High mode, input 0 V to V_{DDA}-0.2 V
SID288A	V_{OS_TR}	Offset voltage, trimmed	–	±1	–		Medium mode, input 0 V to V_{DDA}-0.2 V
SID288B	V_{OS_TR}	Offset voltage, trimmed	–	±2	–		Low mode, input 0 V to V_{DDA}-0.2 V
SID290	$V_{OS_DR_TR}$	Offset voltage drift, trimmed	-10	±3	10	µV/C	High mode
SID290A	$V_{OS_DR_TR}$	Offset voltage drift, trimmed	–	±10	–	µV/C	Medium mode
SID290B	$V_{OS_DR_TR}$	Offset voltage drift, trimmed	–	±10	–		Low mode
SID291	CMRR	DC	70	80	–	dB	Input is 0 V to V_{DDA}-0.2 V, Output is 0.2 V to V_{DDA}-0.2 V
SID292	PSRR	At 1 kHz, 10-mV ripple	70	85	–		V_{DDD} = 3.6 V, high-power mode, input is 0.2 V to V_{DDA}-0.2 V
	Noise						
SID294	VN2	input-referred, 1 kHz, power=Hi	–	72	–	nV/rtHz	Input and output are at 0.2 V to V_{DDA}-0.2 V
SID295	VN3	input-referred, 10 kHz, power=Hi	–	28	–		Input and output are at 0.2 V to V_{DDA}-0.2 V
SID296	VN4	input-referred, 100 kHz, power=Hi	–	15	–		Input and output are at 0.2 V to V_{DDA}-0.2 V
SID297	C_{LOAD}	Stable up to max. load. Performance specs at 50 pF.	–	–	125	pF	–
SID298	SLEW_RATE	Cload = 50 pF, Power = High, V_{DDA} = 2.7 V	6	–	–	V/µs	–
SID299	T_OP_WAKE	From disable to enable, no external RC dominating	–	–	25	µs	–
SID299A	OL_GAIN	Open Loop Gain	–	90	–	dB	

Table 8. CTB Opamp Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
	COMP_MODE	Comparator mode; 50-mV drive, T_{rise}=T_{fall} (approx)					
SID300	TPD1	Response time; power=hi	–	150	–	ns	Input is 0.2 V to V_{DDA}-0.2 V
SID301	TPD2	Response time; power=med	–	500	–		Input is 0.2 V to V_{DDA}-0.2 V
SID302	TPD3	Response time; power=lo	–	2500	–		Input is 0.2 V to V_{DDA}-0.2 V
SID303	VHYST_OP	Hysteresis	–	10	–	mV	–
SID304	WUP_CTB	Wake-up time from Enabled to Usable	–	–	25	µs	–
	Opamp Deep Sleep Mode	Mode 2 is lowest current range. Mode 1 has higher GBW.					
SID_DS_1	$I_{DD_HI_M1}$	Mode 1, High current	–	1400	–	µA	
SID_DS_2	$I_{DD_MED_M1}$	Mode 1, Medium current	–	700	–		
SID_DS_3	$I_{DD_LOW_M1}$	Mode 1, Low current	–	200	–		
SID_DS_4	$I_{DD_HI_M2}$	Mode 2, High current	–	120	–	µA	
SID_DS_5	$I_{DD_MED_M2}$	Mode 2, Medium current	–	60	–		
SID_DS_6	$I_{DD_LOW_M2}$	Mode 2, Low current	–	15	–		
SID_DS_7	$G_{BW_HI_M1}$	Mode 1, High current	–	4	–	MHz	20-pF load, no DC load 0.2 V to VDDA-0.2 V
SID_DS_8	$G_{BW_MED_M1}$	Mode 1, Medium current	–	2	–		20-pF load, no DC load 0.2 V to V_{DDA}-0.2 V
SID_DS_9	$G_{BW_LOW_M!}$	Mode 1, Low current	–	0.5	–		20-pF load, no DC load 0.2 V to V_{DDA}-0.2 V
SID_DS_10	$G_{BW_HI_M2}$	Mode 2, High current	–	0.5	–		20-pF load, no DC load 0.2 V to V_{DDA}-0.2 V
SID_DS_11	$G_{BW_MED_M2}$	Mode 2, Medium current	–	0.2	–		20-pF load, no DC load 0.2 V to V_{DDA}A-0.2 V
SID_DS_12	$G_{BW_Low_M2}$	Mode 2, Low current	–	0.1	–		20-pF load, no DC load 0.2 V to V_{DDA}-0.2 V
SID_DS_13	$V_{OS_HI_M1}$	Mode 1, High current	–	5	–	mV	With trim 25 °C, 0.2 V to V_{DDA}-0.2 V
SID_DS_14	$V_{OS_MED_M1}$	Mode 1, Medium current	–	5	–		With trim 25 °C, 0.2 V to V_{DDA}-0.2 V
SID_DS_15	$V_{OS_LOW_M2}$	Mode 1, Low current	–	5	–		With trim 25 °C, 0.2 V to V_{DDA}-0.2 V
SID_DS_16	$V_{OS_HI_M2}$	Mode 2, High current	–	5	–		With trim 25 °C, 0.2V to V_{DDA}-0.2 V
SID_DS_17	$V_{OS_MED_M2}$	Mode 2, Medium current	–	5	–		With trim 25 °C, 0.2 V to V_{DDA}-0.2 V
SID_DS_18	$V_{OS_LOW_M2}$	Mode 2, Low current	–	5	–		With trim 25 °C, 0.2 V to V_{DDA}-0.2 V

Table 8. CTB Opamp Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID_DS_19	$I_{OUT_HI_M!}$	Mode 1, High current	–	10	–	mA	Output is 0.5 V to V_{DDA}-0.5 V
SID_DS_20	$I_{OUT_MED_M1}$	Mode 1, Medium current	–	10	–		Output is 0.5 V to V_{DDA}-0.5 V
SID_DS_21	$I_{OUT_LOW_M1}$	Mode 1, Low current	–	4	–		Output is 0.5 V to V_{DDA}-0.5 V
SID_DS_22	$I_{OUT_HI_M2}$	Mode 2, High current	–	1	–		–
SID_DS_23	$I_{OU_MED_M2}$	Mode 2, Medium current	–	1	–		–
SID_DS_24	$I_{OU_LOW_M2}$	Mode 2, Low current	–	0.5	–		–

Table 9. PGA Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units
PGA Gain Values	–	Gain Values are 2,4,16, and 32.	2	–	32	–
SID_PGA_1	PGA_ERR_1	Gain Error for Low range; Gain = 2	–	1	–	%
		Gain Error for Medium range; Gain = 2	–	–	1.5	%
		Gain Error for High range; Gain = 2	–	–	1.5	%
SID_PGA_2	PGA_ERR_2	Gain Error for Low range; Gain = 4	–	1	–	%
		Gain Error for Medium range; Gain = 4	–	–	1.5	%
		Gain Error for High range; Gain = 4	–	–	1.5	%
SID_PGA_3	PGA_ERR_3	Gain Error for Low range; Gain = 16	–	3	–	%
		Gain Error for Medium range; Gain = 16	–	3	–	%
		Gain Error for High range; Gain = 16	–	3	–	%
SID_PGA_4	PGA_ERR_4	Gain Error for Low range; Gain = 32	–	5	–	%
		Gain Error for Medium range; Gain = 32	–	5	–	%
		Gain Error for High range; Gain = 32	–	5	–	%

Note
6. Guaranteed by characterization.

Table 10. Universal Analog Block (UAB) Specifications. All UAB Blocks are configured via PSoC Creator components.

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
–	–	Major functional block specifications for ADC, DAC, and filter	–	–	–	–	Specs apply for V_{DDA} ≥ 2.7 V
12-bit delta-sigma ADC	–	Realized with second-order delta-sigma modulator (single-ended)	–	–	–	–	Excludes reference drift in Auto-zero mode
SID_PADC_1	GE_DS2	Gain error	–	0.1	–	%	ADC error
SID_PADC_2	GED_DS2	Gain error drift	–	–	100	ppm / °C	–
SID_PADC_3	VOS_DS2	Offset voltage	–	–	2	mV	–
SID_PADC_4	VSO_DS2	Offset drift	–	–	100	ppm / °C	–
SID_PADC_5	INL_DS2	Integral non linearity (INL)	–3	1	3	LSB	–
SID_PADC_6	DNL_DS2	Differential non linearity (DNL)	–1	–	1	LSB	–
SID_PADC_7	SINAD_DS2	Signal-to-noise and distortion. ENOB = (SINAD-1.76)/6.02.	68	77	–	dB	–
SID_PADC_8	PSRR_DS2	Power supply rejection ratio	68	74	–	dB	–
SID_PADC_10	FS_DS2	Sample rate (ksps)	–	7.8	–	ksps	–
SID_PADC_11	FC_DS2	3-dB bandwidth as a fraction of sample frequency	0.26	0.26	0.26		–
SID_PADC_12	VIN_DS2	Input voltage range	–	75	–	$\%V_{REF}$	Based on Cypress Component usage
SID_PADC_13	IDD_DS2	Block current	–	900	–	µA	Medium power mode
SID_PADC_14	WUP_DS2	Wake-up time from Enabled to Usable	–	–	25	µS	For clock ≥ 1 MHz
14-bit Incremental Delta-Sigma ADC. V_{REF} = VDDA/2							
SID_IADC_1	INL_IADC	Integral non-linearity (INL)	–4	–	4	LSB	
SID_IADC_2	DNL_IADC	Differential non-linearity (DNL)	–1	–	1	LSB	
SID_IADC_3	SINAD_IADC	Signal-to-noise and distortion. ENOB = (SINAD-1.76)/6.02.	–	77	–	–	
SID_IADC_4	FS_IADC	Sample Rate (samples per second)	–	–	100	sps	
13-bit DAC		Differential output					
SID_DAC_1	INL_MDAC1	Integral non linearity (INL)	–	+5,–6	–	LSB	
SID_DAC_2	DNL_MDAC1	Differential non linearity (DNL)	–	+3.5, –0.75	–		
SID_DAC_3	VOUT_MDAC1	Output voltage range	0.01	–	V_{DDA}-0.01	V	Valid output range is 100 LSBs from rails. Full settling bandwidth to within 100 mV of rail.
SID_DAC_4	VOS_MDAC1	Zero scale error (output with all zeroes input)	–	5	–	mV	Zero scale is at analog ground

Table 10. Universal Analog Block (UAB) Specifications. All UAB Blocks are configured via PSoC Creator components.

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID_DAC_5	GE_MDAC1	Full scale error less offset	–	–	0.4	%	–
SID_DAC_6	IDD_MMDAC1	Block current	–	1.2	–	mA	–
SID_DAC_7	PSRR_MDAC1	Power supply rejection ratio	70		–	dB	–
SID_DAC_8	WUP_MDAC1	Wake-up time from Enabled to Usable	–	–	25	µs	For clock ≥ 1 MHz
SID_DAC_9	TS_MDAC1	Settling time for DAC	–	–	2	µs	–
SID_DAC_10	BW-MDAC1	3-dB bandwidth frequency	–	–	500	kHz	–
Two_Pole Bi-Quad Switched-Capacitor Filter. Low/Band/High/Notch Pass Filter							Configured via Cypress Component
SID_SC_1	SNR_SCF1	Signal-to-noise ratio	–	64	–	dB	Vin 2Vp-p, low-pass, OSR=100
SID_SC_2	THD_SCF1	Total harmonic distortion	–	70	–	dB	Vin 2Vp-p, low-pass, OSR = 100
SID_SC_3	F0_SCF1	Center frequency range	0.1		20	kHz	–
SID_SC_4	VOS_SFC1	Offset error	–	15	–	mV	–
SID_SC_6	QACC_SFC1	Q accuracy	–2	0.2	2	%	–
SID_SC_7	QRNG_SFC1	Q range	0.25	–	25	–	
SID_SC_9	FC_SCF1	Maximum sampling frequency	–	–	2	MHz	–
SID_SC_10	FR_SCF1	Ratio of sampling frequency to corner frequency	8	–	128	–	–
SID_SC_11	IDD_SCf1	Block current	–	900	–	µA	–
SID_SC_12	WUP_SCF1	Wake-up time from Enabled to Usable	–	–	25	µs	For clock ≥ 1 MHz

Table 11. Comparator DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID84	$V_{OFFSET1}$	Input offset voltage, Factory trim	–	–	±10	mV	–
SID85	$V_{OFFSET2}$	Input offset voltage, Custom trim	–	–	±4		–
SID86	V_{HYST}	Hysteresis when enabled	–	10	35		–
SID87	V_{ICM1}	Input common mode voltage in normal mode	0	–	V_{DDD}-0.1	V	Modes 1 and 2
SID247	V_{ICM2}	Input common mode voltage in low power mode	0	–	V_{DDD}		–
SID247A	V_{ICM3}	Input common mode voltage in ultra low power mode	0	–	V_{DDD}-1.15		V_{DDD} ≥ 2.2 V for Temp < 0 °C, V_{DDD} ≥ 1.8 V for Temp > 0 °C
SID88	C_{MRR}	Common mode rejection ratio	50	–	–	dB	V_{DDD} ≥ 2.7V
SID88A	C_{MRR}	Common mode rejection ratio	42	–	–		V_{DDD} ≤ 2.7V

Table 11. Comparator DC Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID89	I_{CMP1}	Block current, normal mode	–	–	400	µA	–
SID248	I_{CMP2}	Block current, low power mode	–	–	100		–
SID259	I_{CMP3}	Block current in ultra low-power mode	–	–	28		V_{DDD} ≥ 2.2 V for Temp < 0 °C, V_{DDD} ≥ 1.8 V for Temp > 0 °C
SID90	Z_{CMP}	DC Input impedance of comparator	35	–	–	MΩ	–

Table 12. Comparator AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID91	TRESP1	Response time, normal mode, 50 mV overdrive	–	38	110	ns	All V_{DD}
SID258	TRESP2	Response time, low power mode, 50 mV overdrive	–	70	200		–
SID92	TRESP3	Response time, ultra-low power mode, 200 mV overdrive	–	2.3	15	µs	V_{DDD} ≥ 2.2 V for Temp < 0 °C, V_{DDD} ≥ 1.8 V for Temp > 0 °C

Table 13. Temperature Sensor Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID93	TSENSACC	Temperature sensor accuracy	–5	±1	5	°C	–40 to +85 °C

Table 14. SAR Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SAR ADC DC Specifications							
SID94	A_RES	Resolution	–	–	12	bits	
SID95	A_CHNLS_S	Number of channels - single ended	–	–	8		8 full speed.
SID96	A-CHNKS_D	Number of channels - differential	–	–	4		
SID97	A-MONO	Monotonicity	–	–	–		Yes.
SID98	A_GAINERR	Gain error	–	–	±0.1	%	With external reference.
SID99	A_OFFSET	Input offset voltage	–	–	2	mV	Measured with 1-V reference
SID100	A_ISAR	Current consumption	–	–	1	mA	
SID101	A_VINS	Input voltage range - single ended	V_{SS}	–	V_{DDA}	V	
SID102	A_VIND	Input voltage range - differential[	V_{SS}	–	V_{DDA}	V	
SID103	A_INRES	Input resistance	–	–	2.2	KΩ	
SID104	A_INCAP	Input capacitance	–	–	10	pF	
SID260	VREFSAR	Trimmed internal reference to SAR	–	–	TBD	V	

Table 14. SAR Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SAR ADC AC Specifications							
SID106	A_PSRR	Power supply rejection ratio	70	–	–	dB	
SID107	A_CMRR	Common mode rejection ratio	66	–	–	dB	Measured at 1 V
SID108	A_SAMP	Sample rate	–	–	1	Msps	
SID109	A_SNR	Signal-to-noise and distortion ratio (SINAD)	65	–	–	dB	F_{IN} = 10 kHz
SID110	A_BW	Input bandwidth without aliasing	–	–	A_samp/2	kHz	
SID111	A_INL	Integral non linearity. V_{DD} = 1.71 to 5.5, 1 Msps	–1.7	–	2	LSB	V_{REF} = 1 to V_{DD}
SID111A	A_INL	Integral non linearity. V_{DDD} = 1.71 to 3.6, 1 Msps	–1.5	–	1.7	LSB	V_{REF} = 1.71 to V_{DD}
SID111B	A_INL	Integral non linearity. V_{DD} = 1.71 to 5.5, 500 ksps	–1.5	–	1.7	LSB	V_{REF} = 1 to V_{DD}
SID112	A_DNL	Differential non linearity. V_{DD} = 1.71 to 5.5, 1 Msps	–1	_	2.2	LSB	V_{REF} = 1 to V_{DD}
SID112A	A_DNL	Differential non linearity. V_{DD} = 1.71 to 3.6, 1 Msps	–1	_	2	LSB	V_{REF} = 1.71 to V_{DD}
SID112B	A_DNL	Differential non linearity. V_{DD} = 1.71 to 5.5, 500 ksps	–1	_	2.2	LSB	V_{REF} = 1 to V_{DD}
SID113	A_THD	Total harmonic distortion	–	–	–65	dB	Fin = 10 kHz
SID261	FSARINTREF	SAR operating speed without external ref. bypass	_	_	100	ksps	12-bit resolution

Table 15. CapSense and IDAC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SYS.PER#3	VDD_RIPPLE	Max allowed ripple on power supply, DC to 10 MHz	–	–	±50	mV	V_{DD} > 2 V (with ripple), 25 °C T_A, Sensitivity = 0.1pF
SYS.PER#16	VDD_RIPPLE_1.8	Max allowed ripple on power supply, DC to 10 MHz	–	–	±25	mV	VDD > 1.75 V (with ripple), 25 °C T_A, Parasitic Capacitance (CP) < 20 pF, Sensitivity ≥ 0.4 pF
SID.CSD.BLK	ICSD	Maximum block current			1700	µA	Block current per IDAC with comparators and reference
SID.CSD#15	VREF	Voltage reference for CSD and Comparator	0.6	1.2	V_{DDA} - 0.6	V	V_{DDA} - 0.6 or 4.4, whichever is lower
SID.CSD#15A	VREF_EXT	External Voltage reference for CSD and Comparator	0.6		V_{DDA} - 0.6	V	V_{DDA} - 0.6 or 4.4, whichever is lower
SID.CSD#16	IDAC1IDD	IDAC1 (7 bits) block current	–	–	1500	µA	
SID.CSD#17	IDAC2IDD	IDAC2 (7 bits) block current	–	–	1500	µA	
SID308	VCSD	Voltage range of operation	1.71	–	5.5	V	1.8 V ±5% or 1.8 V to 5.5 V
SID308A	VCOMPIDAC	Voltage compliance range of IDAC	0.6	–	V_{DDA} –0.6	V	V_{DDA} –0.6 or 4.4, whichever is lower
SID309	IDAC1DNL	DNL	–1	–	1	LSB	

Table 15. CapSense and IDAC Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID310	IDAC1INL	INL	–3	–	3	LSB	
SID311	IDAC2DNL	DNL	–1	–	1.0	LSB	
SID312	IDAC2INL	INL	–3	–	3	LSB	
SID313	SNR	Ratio of counts of finger to noise. Guaranteed by characterization	5.0	–	–	Ratio	Capacitance range of 5 to 200 pF, 0.1 pF sensitivity. All use cases. V_{DDA} > 2 V.
SID314	IDAC7_SRC1	Maximum Source current of 7-bit IDAC in low range	4.2		5.2	µA	LSB = 37.5 nA typ.
SID314A	IDAC7_SRC2	Maximum Source current of 7-bit IDAC in medium range	34		41	µA	LSB = 300 nA typ.
SID314B	IDAC7_SRC3	Maximum Source current of 7-bit IDAC in high range	275		330	µA	LSB = 2.4 µA typ.
SID314C	IDAC7_SRC4	Maximum Source current of 7-bit IDAC in low range, 2X mode	8		10.5	µA	LSB = 37.5 nA typ. 2X output stage
SID314D	IDAC7_SRC5	Maximum Source current of 7-bit IDAC in medium range, 2X mode	69		82	µA	LSB = 300 nA typ. 2X output stage
SID314E	IDAC7_SRC6	Maximum Source current of 7-bit IDAC in high range, 2X mode	540		660	µA	LSB = 2.4 µA typ.2X output stage
SID315	IDAC7_SINK_1	Maximum Sink current of 7-bit IDAC in low range	4.2		5.7	µA	LSB = 37.5 nA typ.
SID315A	IDAC7_SINK_2	Maximum Sink current of 7-bit IDAC in medium range	34		44	µA	LSB = 300 nA typ.
SID315B	IDAC7_SINK_3	Maximum Sink current of 7-bit IDAC in high range	270		335	µA	LSB = 2.4 µA typ.
SID315C	IDAC7_SINK_4	Maximum Sink current of 7-bit IDAC in low range, 2X mode	8		11.5	µA	LSB = 37.5 nA typ. 2X output stage
SID315D	IDAC7_SINK_5	Maximum Sink current of 7-bit IDAC in medium range, 2X mode	68		86	µA	LSB = 300 nA typ. 2X output stage
SID315E	IDAC7_SINK_6	Maximum Sink current of 7-bit IDAC in high range, 2X mode	540		700	µA	LSB = 2.4 µA typ.2X output stage
SID315F	IDAC8_SRC_1	Maximum Source current of 8-bit IDAC in low range	8.4		10.4	µA	LSB = 37.5 nA typ.
SID315G	IDAC8_SRC_2	Maximum Source current of 8-bit IDAC in medium range	68		82	µA	LSB = 300 nA typ.
SID315H	IDAC8_SRC_3	Maximum Source current of 8-bit IDAC in high range	550		660	µA	LSB = 2.4 µA typ.
SID315J	IDAC8_SINK_1	Maximum Sink current of 8-bit IDAC in low range	8.4		11.4	µA	LSB = 37.5 nA typ.
SID315K	IDAC8_SINK_2	Maximum Sink current of 8-bit IDAC in medium range	68		88	µA	LSB = 300 nA typ.
SID315L	IDAC8_SINK_3	Maximum Sink current of 8-bit IDAC in high range	540		670	µA	LSB = 2.4 µA typ.
SID320	IDACOFFSET1	All zeroes input; Medium and High range	–	–	1	LSB	Polarity set by Source or Sink
SID320A	IDACOFFSET2	All zeroes input; Low range	–	–	2	LSB	Polarity set by Source or Sink
SID321	IDACGAIN	Full-scale error less offset	–	–	±20	%	

Table 15. CapSense and IDAC Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID322	IDACMISMATCH1	Mismatch between IDAC1 and IDAC2 in Low mode	–	–	9.2	LSB	LSB = 37.5 nA typ.
SID322A	IDACMISMATCH2	Mismatch between IDAC1 and IDAC2 in Medium mode	–	–	6	LSB	LSB = 300 nA typ.
SID322B	IDACMISMATCH3	Mismatch between IDAC1 and IDAC2 in High mode	–	–	5.8	LSB	LSB = 2.4 µA typ.
SID323	IDACSET8	Settling time to 0.5 LSB for 8-bit IDAC	–	–	10	µs	Full-scale transition. No external load.
SID324	IDACSET7	Settling time to 0.5 LSB for 7-bit IDAC	–	–	10	µs	Full-scale transition. No external load.
SID325	CMOD	External modulator capacitor.	–	2.2	–	nF	5-V rating, X7R or NP0 cap.

Table 16. 10-bit CapSense ADC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SIDA94	A_RES	Resolution	–	–	10	bits	8 full speed.
SID95	A_CHNLS_S	Number of channels - single-ended	–	–	16		Diff inputs use neighboring I/O
SIDA97	A-MONO	Monotonicity	–	–	–	Yes	Yes
SIDA98	A_GAINERR	Gain error	–	–	TBD	%	With external reference.
SIDA99	A_OFFSET	Input offset voltage	–	–	TBD	mV	Measured with 1-V reference
SIDA100	A_ISAR	Current consumption	–	–	TBD	mA	
SIDA101	A_VINS	Input voltage range - single-ended	V_{SSA}	–	V_{DDA}	V	
SIDA103	A_INRES	Input resistance	–	2.2	–	KΩ	
SIDA104	A_INCAP	Input capacitance	–	20	–	pF	
SIDA106	A_PSRR	Power supply rejection ratio	TBD	–	–	dB	
SIDA107	A_TACQ	Sample acquisition time	–	1	–	µs	
SIDA108	A_CONV8	Conversion time for 8-bit resolution at conversion rate = Fhclk/(2^(N+2)). Clock frequency = 48 MHz.	–	–	21.3	µs	Does not include acquisition time. Equivalent to 44.8 ksps including acquisition time
SIDA108A	A_CONV10	Conversion time for 10-bit resolution at conversion rate = Fhclk/(2^(N+2)). Clock frequency = 48 MHz.	–	–	85.3	µs	Does not include acquisition time. Equivalent to 11.6 ksps including acquisition time.
SIDA109	A_SND	Signal-to-noise and distortion ratio (SINAD)	TBD	–	–	dB	
SIDA110	A_BW	Input bandwidth without aliasing	–	–	22.4	kHz	8-bit resolution
SIDA111	A_INL	Integral non linearity. V_{DD} = 1.71 to 5.5, 1 ksps	–	–	2	LSB	V_{REF} = 2.4 V or greater
SIDA112	A_DNL	Differential non linearity. V_{DD} = 1.71 to 5.5, 1 ksps	–	–	1	LSB	

Digital Peripherals

Timer Counter Pulse-Width Modulator (TCPWM)

Table 17. TCPWM Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.TCPWM.1	ITCPWM1	Block current consumption at 3 MHz	–	–	45	µA	All modes (TCPWM)
SID.TCPWM.2	ITCPWM2	Block current consumption at 12 MHz	–	–	155		All modes (TCPWM)
SID.TCPWM.2A	ITCPWM3	Block current consumption at 48 MHz	–	–	650		All modes (TCPWM)
SID.TCPWM.3	$TCPWM_{FREQ}$	Operating frequency	–	–	Fc	MHz	Fc max = CLK_SYS Maximum = 48 MHz
SID.TCPWM.4	$TPWM_{ENEXT}$	Input trigger pulse width	2/Fc	–	–	ns	For all trigger events[7]
SID.TCPWM.5	$TPWM_{EXT}$	Output trigger pulse widths	2/Fc	–	–		Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) outputs
SID.TCPWM.5A	TC_{RES}	Resolution of counter	1/Fc	–	–		Minimum time between successive counts
SID.TCPWM.5B	PWM_{RES}	PWM resolution	1/Fc	–	–		Minimum pulse width of PWM Output
SID.TCPWM.5C	Q_{RES}	Quadrature inputs resolution	1/Fc	–	–		Minimum pulse width between Quadrature phase inputs

I^2C

Table 18. Fixed I^2C DC Specifications[8]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID149	I_{I2C1}	Block current consumption at 100 kHz	–	–	50	µA	–
SID150	I_{I2C2}	Block current consumption at 400 kHz	–	–	135		–
SID151	I_{I2C3}	Block current consumption at 1 Mbps	–	–	310		–
SID152	I_{I2C4}	I^2C enabled in Deep Sleep mode	–	–	1.4		

Table 19. Fixed I^2C AC Specifications[8]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID153	F_{I2C1}	Bit rate	–	–	1	Msps	–

Table 20. SPI DC Specifications[9]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID163	ISPI1	Block current consumption at 1 Mbits/sec	–	–	360	µA	–
SID164	ISPI2	Block current consumption at 4 Mbits/sec	–	–	560		–
SID165	ISPI3	Block current consumption at 8 Mbits/sec	–	–	600		–

Note
7. Trigger events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected.
8. Guaranteed by characterization.

Table 21. SPI AC Specifications[9]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID166	FSPI	SPI Operating frequency (Master; 6X Oversampling)	–	–	8	MHz	SID166
Fixed SPI Master Mode AC Specifications							
SID167	TDMO	MOSI Valid after SClock driving edge	–	–	15	ns	–
SID168	TDSI	MISO Valid before SClock capturing edge	20	–	–		Full clock, late MISO sampling
SID169	THMO	Previous MOSI data hold time	0	–	–		Referred to Slave capturing edge
Fixed SPI Slave Mode AC Specifications							
SID170	TDMI	MOSI Valid before Sclock Capturing edge	40	–	–	ns	–
SID171	TDSO	MISO Valid after Sclock driving edge	–	–	42 + 3*Tcpu		Tcpu = $1/F_{CPU}$
SID171A	TDSO_EXT	MISO Valid after Sclock driving edge in Ext. Clk mode	–	–	48		–
SID172	THSO	Previous MISO data hold time	0	–	–		–

Table 22. UART DC Specifications[9]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID160	I_{UART1}	Block current consumption at 100 Kbits/sec	–	–	55	µA	–
SID161	I_{UART2}	Block current consumption at 1000 Kbits/sec	–	–	312	µA	–

Table 23. UART AC Specifications[9]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID162	F_{UART}	Bit rate	–	–	1	Mbps	–

Table 24. LCD Direct Drive DC Specifications[9]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID154	I_{LCDLOW}	Operating current in low power mode	_	5	–	µA	16 × 4 small segment disp. at Hz
SID155	C_{LCDCAP}	LCD capacitance per segment/common driver	_	500	5000	pF	–
SID156	LCD_{OFFSET}	Long-term segment offset	–	20	–	mV	–
SID157	I_{LCDOP1}	LCD system operating current Vbias = 5 V	_	2	–	mA	32 × 4 segments. 50 Hz. 25 °C
SID158	I_{LCDOP2}	LCD system operating current Vbias = 3.3 V	_	2	–		32 × 4 segments. 50 Hz. 25 °C 4 segments. 50 Hz. 25 °C

Table 25. LCD Direct Drive AC Specifications[9]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID159	F_{LCD}	LCD frame rate	10	50	150	Hz	–

Note
9. Guaranteed by characterization.

Memory

Table 26. Flash DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID173	V_{PE}	Erase and program voltage	1.71	–	5.5	V	–

Table 27. Flash AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID174	$T_{ROWWRITE}$[10]	Row (block) write time (erase and program)	–	–	20	ms	Row (block) = 64 bytes
SID175	$T_{ROWERASE}$[10]	Row erase time	–	–	13		–
SID176	$T_{ROWPROGRAM}$[10]	Row program time after erase	–	–	7		–
SID178	$T_{BULKERASE}$[10]	Bulk erase time (16 KB)	–	–	15		–
SID180[11]	$T_{DEVPROG}$[10]	Total device program time	–	–	7.5	Seconds	–
SID181[11]	F_{END}	Flash endurance	100 K	–	–	Cycles	–
SID182[11]	F_{RET}	Flash retention. $T_A \le 55$ °C, 100 K P/E cycles	20	–	–	Years	–
SID182A[11]	–	Flash retention. $T_A \le 85$ °C, 10 K P/E cycles	10	–	–		–
SID256	TWS48	Number of Wait states at 48 MHz	2	–	–		CPU execution from Flash
SID257	TWS24	Number of Wait states at 24 MHz	1	–	–		CPU execution from Flash

System Resources

Power-on Reset (POR)

Table 28. Power On Reset (PRES)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.CLK#6	SR_POWER_UP	Power supply slew rate	1	–	67	V/ms	At power-up
SID185[11]	$V_{RISEIPOR}$	Rising trip voltage	0.80	–	1.5	V	–
SID186[11]	$V_{FALLIPOR}$	Falling trip voltage	0.70	–	1.4		–

Table 29. Brown-out Detect (BOD) for V_{CCD}

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID190[11]	$V_{FALLPPOR}$	BOD trip voltage in active and sleep modes	1.48	–	1.62	V	–
SID192[11]	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep	1.1	–	1.5		–

Notes

10. It can take as much as 20 milliseconds to write to Flash. During this time the device should not be Reset, or Flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.
11. Guaranteed by characterization.

SWD Interface

Table 30. SWD Interface Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID213	F_SWDCLK1	3.3 V ≤ V_{DD} ≤ 5.5 V	–	–	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID214	F_SWDCLK2	1.71 V ≤ V_{DD} ≤ 3.3 V	–	–	7		SWDCLK ≤ 1/3 CPU clock frequency
SID215[12]	T_SWDI_SETUP	T = 1/f SWDCLK	0.25*T	–	–	ns	–
SID216[12]	T_SWDI_HOLD	T = 1/f SWDCLK	0.25*T	–	–		–
SID217[12]	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.5*T		–
SID217A[12]	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–		–

Internal Main Oscillator

Table 31. IMO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID218	I_{IMO1}	IMO operating current at 48 MHz	–	–	250	µA	–
SID219	I_{IMO2}	IMO operating current at 24 MHz	–	–	180	µA	–

Table 32. IMO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID223	$F_{IMOTOL1}$	Frequency range from 24 to 48 MHz (4-MHz increments)	–2	–	+2	%	2 V ≤ V_{DD} ≤ 5.5 V, and –25 °C ≤ T_A ≤ 85 °C
SID226	$T_{STARTIMO}$	IMO startup time	–	–	7	µs	–
SID228	$T_{JITRMSIMO2}$	RMS jitter at 24 MHz	–	145	–	ps	–
SID330	IMO_{WCO1}	Frequency range from 24 to 48 MHz (4-MHz increments)	–0.25	–	0.25	%	Watch Crystal DPLL Frequency Locked mode

Internal Low-Speed Oscillator

Table 33. ILO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID231[12]	I_{ILO1}	ILO operating current	–	0.3	1.05	µA	–

Table 34. ILO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID234[12]	$T_{STARTILO1}$	ILO startup time	–	–	2	ms	–
SID236[12]	$T_{ILODUTY}$	ILO duty cycle	40	50	60	%	–
SID237	$F_{ILOTRIM1}$	ILO frequency range	20	40	80	kHz	–

Note
12. Guaranteed by characterization.

Table 35. Watch Crystal Oscillator (WCO) Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID398	FWCO	Crystal Frequency	–	32.768	–	kHz	
SID399	FTOL	Frequency tolerance	–	50	250	ppm	With 20-ppm crystal
SID400	ESR	Equivalent series resistance	–	50	–	kΩ	
SID401	PD	Drive Level	–	–	1	µW	
SID402	TSTART	Startup time	–	–	500	ms	
SID403	CL	Crystal Load Capacitance	6	–	12.5	pF	
SID404	C0	Crystal Shunt Capacitance	–	1.35	–	pF	
SID405	IWCO1	Operating Current (high power mode)	–	–	8	µA	
SID406	IWCO2	Operating Current (low power mode)	–	–	1	µA	

Table 36. External Clock Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID305[13]	ExtClkFreq	External clock input frequency	0	–	16	MHz	–
SID306[13]	ExtClkDuty	Duty cycle; measured at $V_{DD/2}$	45	–	55	%	–

Table 37. Block Specs

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID262[13]	$T_{CLKSWITCH}$	System clock source switching time	3	–	4	Periods	–

Table 38. PRGIO Pass-through Time (Delay in Bypass Mode)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID252	PRG_BYPASS	Max. delay added by PRGIO in bypass mode	–	–	1.6	ns	

Note
13. Guaranteed by characterization.

Ordering Information

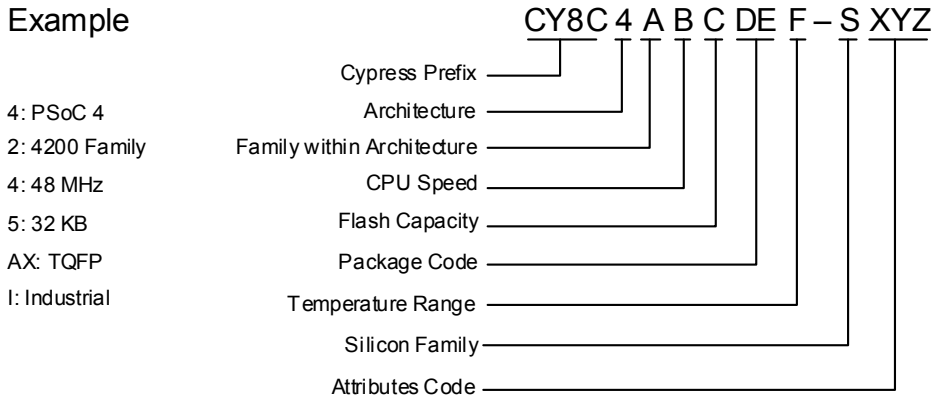
Category	MPN	Features															Package			
		Max CPU Speed (MHz)	DMA	Flash (KB)	SRAM (KB)	UAB	Opamp (CTB)	CSD	Direct LCD Drive	RTC	12-bit SAR ADC	LP Comparators	TCPWM Blocks	SCB Blocks	Smart I/Os	GPIO	28-SSOP	45-WLCSP	48-QFN	48-LQFP
4A24	CY8C4A24PVI-431	24	–	16	4	1	2	–	–	✔	1000 ksps	2	4	2	8	19	✔	–	–	–
	CY8C4A24AZI-433	24	–	16	4	1	2	–	–	✔	1000 ksps	2	4	2	8	38	–	–	–	✔
	CY8C4A24PVI-441	24	–	16	4	1	2	✔	✔	✔	1000 ksps	2	4	2	8	19	✔	–	–	–
	CY8C4A24FNI-443	24	–	16	4	1	2	✔	✔	✔	1000 ksps	2	4	2	8	38	–	✔	–	–
	CY8C4A24LQI-443	24	–	16	4	1	2	✔	✔	✔	1000 ksps	2	4	2	8	38	–	–	✔	–
	CY8C4A24AZI-443	24	–	16	4	1	2	✔	✔	✔	1000 ksps	2	4	2	8	38	–	–	–	✔
4A44	CY8C4A25PVI-471	24	–	32	4	1	4	–	–	✔	1000 ksps	2	8	3	8	19	✔	–	–	–
	CY8C4A25FNI-473	24	–	32	4	1	4	–	–	✔	1000 ksps	2	8	3	8	38	–	✔	–	–
	CY8C4A25LQI-473	24	–	32	4	1	4	–	–	✔	1000 ksps	2	8	3	8	38	–	–	✔	–
	CY8C4A25AZI-473	24	–	32	4	1	4	–	–	✔	1000 ksps	2	8	3	8	38	–	–	–	✔
	CY8C4A25PVI-481	24	–	32	4	1	4	✔	✔	✔	1000 ksps	2	8	3	8	19	✔	–	–	–
	CY8C4A25FNI-483	24	–	32	4	1	4	✔	✔	✔	1000 ksps	2	8	3	8	38	–	✔	–	–
	CY8C4A25LQI-483	24	–	32	4	1	4	✔	✔	✔	1000 ksps	2	8	3	8	38	–	–	✔	–
	CY8C4A25AZI-483	24	–	32	4	1	4	✔	✔	✔	1000 ksps	2	8	3	8	38	–	–	–	✔
4A45	CY8C4A45PVI-471	48	✔	32	4	1	4	–	–	✔	1000 ksps	2	8	3	8	19	✔	–	–	–
	CY8C4A45FNI-473	48	✔	32	4	1	4	–	–	✔	1000 ksps	2	8	3	8	38	–	✔	–	–
	CY8C4A45LQI-473	48	✔	32	4	1	4	–	–	✔	1000 ksps	2	8	3	8	38	–	–	✔	–
	CY8C4A45AZI-473	48	✔	32	4	1	4	–	–	✔	1000 ksps	2	8	3	8	38	–	–	–	✔
	CY8C4A45PVI-481	48	✔	32	4	1	4	✔	✔	✔	1000 ksps	2	8	3	8	19	✔	–	–	–
	CY8C4A45FNI-483	48	✔	32	4	1	4	✔	✔	✔	1000 ksps	2	8	3	8	38	–	✔	–	–
	CY8C4A45LQI-483	48	✔	32	4	1	4	✔	✔	✔	1000 ksps	2	8	3	8	38	–	–	✔	–
	CY8C4A45AZI-483	48	✔	32	4	1	4	✔	✔	✔	1000 ksps	2	8	3	8	38	–	–	–	✔

The nomenclature used in the preceding table is based on the following part numbering convention:

Field	Description	Values	Meaning
CY8C	Cypress Prefix		
4	Signal Processing Engine	4	4 = ARM Cortex-M0+ CPU
A	Family	A	A = Analog Coprocessor
B	Signal Processing Engine Speed	2	24 MHz
		4	48 MHz
C	Flash Memory Capacity	4	16 KB
		5	32 KB
		6	64 KB
		7	128 KB
DE	Package Code	AX	TQFP (0.8mm pitch)
		AZ	TQFP (0.5mm pitch)
		LQ	QFN
		PV	SSOP
		FN	CSP
F	Temperature Range	I	Industrial
S	Silicon Family	N/A	Base Series: PSoC 4B-S0
		M	Reserved for future products
		L	Reserved for future products
		BL	Reserved for future products
XYZ	Attributes Code	000-999	Code of feature set in the specific family

The following is an example of a part number:

Example



Packaging

SPEC ID#	Package	Description	Package DWG #
BID20	48-pin TQFP	7 × 7 × 1.4 mm height with 0.5-mm pitch	51-85135
BID27	48-pin QFN	6 × 6 × 0.6 mm height with 0.4-mm pitch	001-57280
BID34	45-ball WLCSP	3.7 × 2 × 0.5 mm height with 0.38-mm pitch	002-10531
BID34A	28-pin SSOP	5.3 × 10.2 × 0.65-mm pitch	51-85079

Table 39. Package Thermal Characteristics

Parameter	Description	Package	Min	Typ	Max	Units
T_A	Operating Ambient temperature		–40	25	85	°C
T_J	Operating junction temperature		–40	–	100	°C
T_{JA}	Package θ_{JA}	48-pin TQFP	–	71	–	°C/Watt
T_{JC}	Package θ_{JC}	48-pin TQFP	–	34.3	–	°C/Watt
T_{JA}	Package θ_{JA}	48-pin QFN	–	18	–	°C/Watt
T_{JC}	Package θ_{JC}	48-pin QFN	–	4.5	–	°C/Watt
T_{JA}	Package θ_{JA}	45-Ball WLCSP	–	37.2	–	°C/Watt
T_{JC}	Package θ_{JC}	45-Ball WLCSP	–	0.31	–	°C/Watt
T_{JA}	Package θ_{JA}	28-pin SSOP	–	60	–	°C/Watt
T_{JC}	Package θ_{JC}	28-pin SSOP	–	25	–	°C/Watt

Table 40. Solder Reflow Peak Temperature

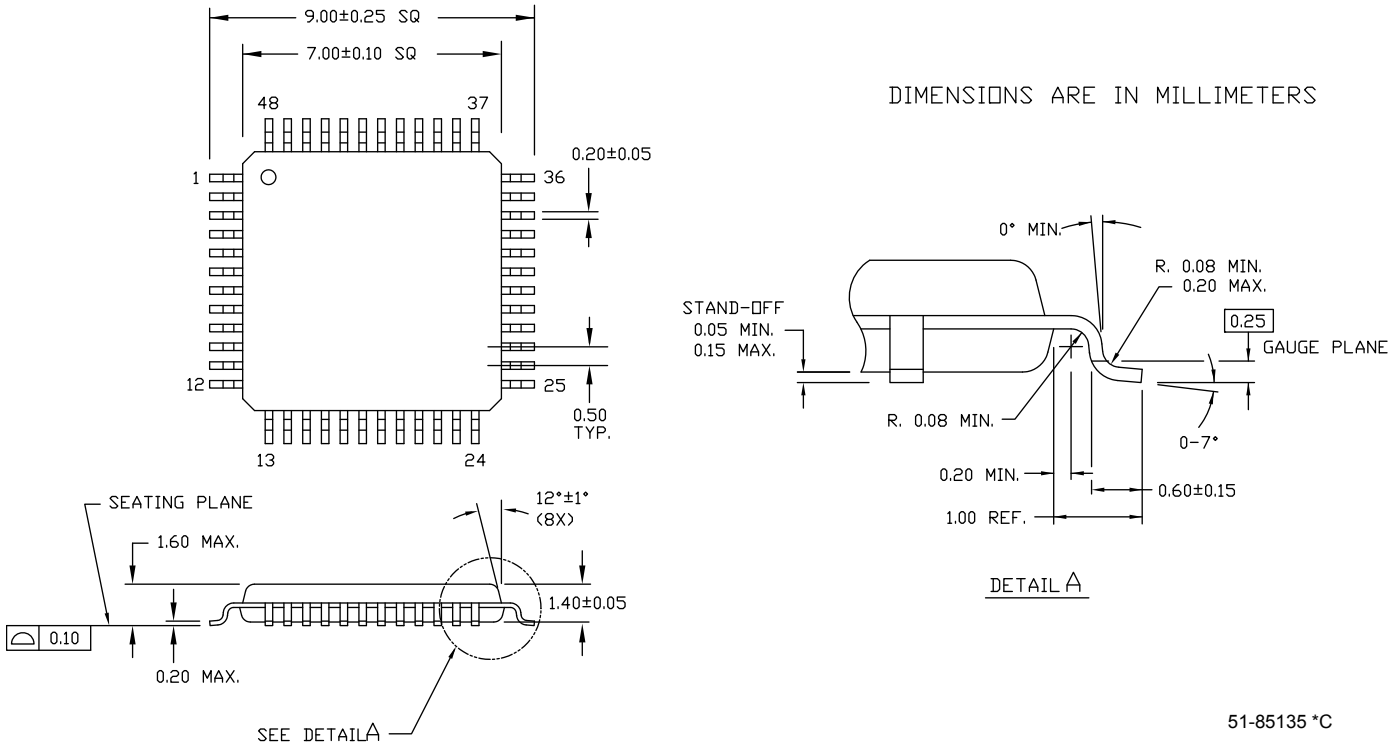
Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
All	260 °C	30 seconds

Table 41. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-020

Package	MSL
All	MSL 3

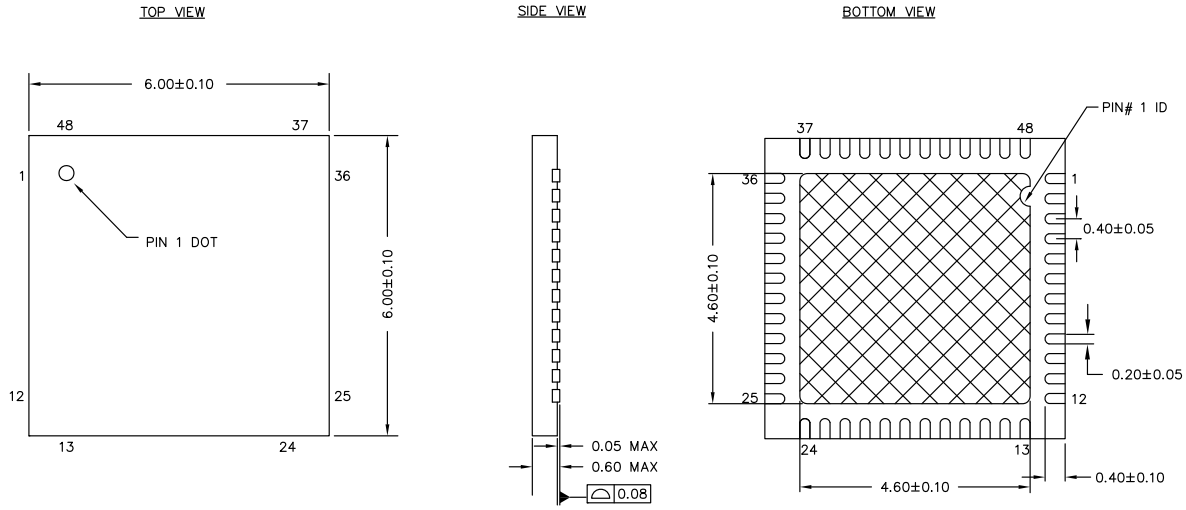
Package Diagrams

Figure 6. 48-pin TQFP Package Outline



51-85135 *C

Figure 7. 48-Pin QFN Package Outline

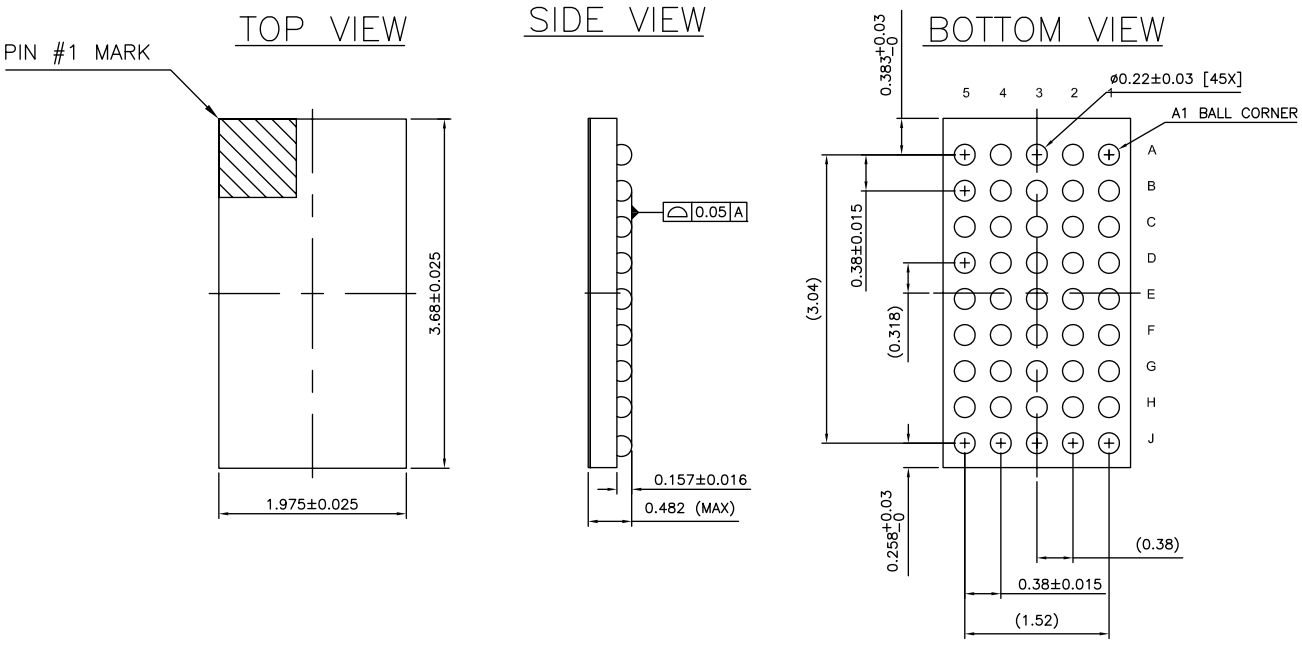


NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. REFERENCE JEDEC # MO-248
3. PACKAGE WEIGHT: 68 ±7 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-57280 *E

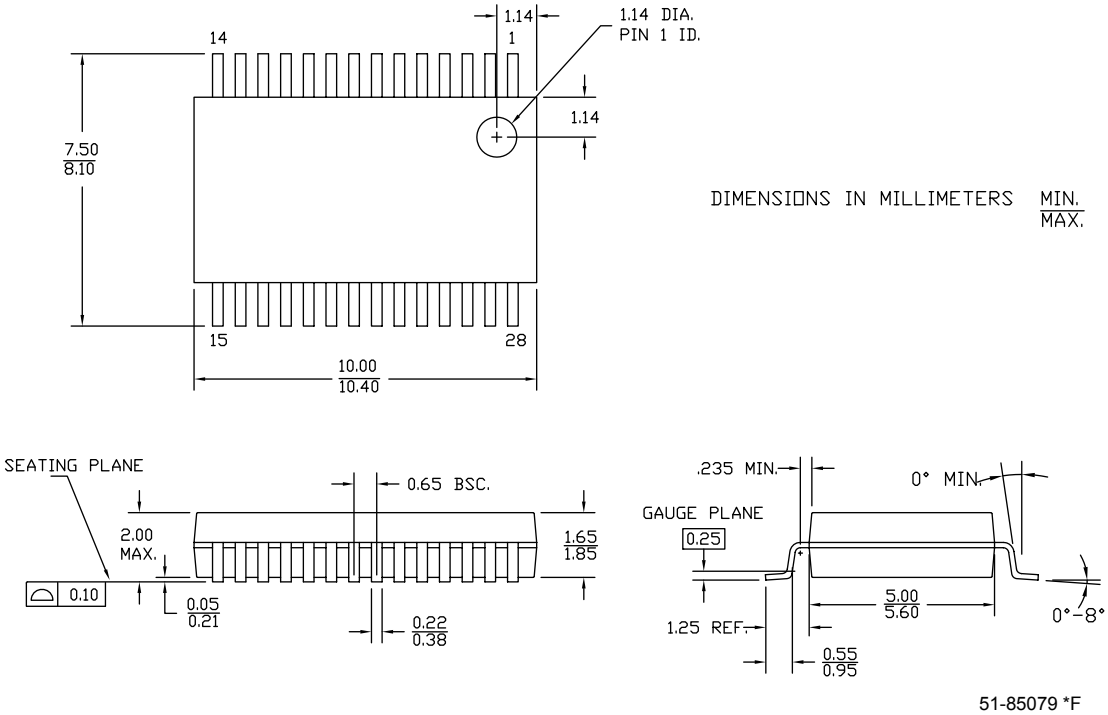
Figure 8. 45-Ball WLCSP Dimensions



ALL DIMENSIONS ARE IN MM
JEDEC Publication 95; Design Guide 4.18

002-10531 **

Figure 9. 28-Pin SSOP Package Outline



51-85079 *F

Acronyms

Table 42. Acronyms Used in this Document

Acronym	Description
abus	analog local bus
ADC	analog-to-digital converter
AG	analog global
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an ARM data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
ARM®	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
DAC	digital-to-analog converter, see also IDAC, VDAC
DFB	digital filter block
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMIPS	Dhrystone million instructions per second
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DNU	do not use
DR	port write data registers
DSI	digital system interconnect
DWT	data watchpoint and trace
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame
EPSR	execution program status register
ESD	electrostatic discharge

Table 42. Acronyms Used in this Document *(continued)*

Acronym	Description
ETM	embedded trace macrocell
FIR	finite impulse response, see also IIR
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC pin
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
opamp	operational amplifier
PAL	programmable array logic, see also PLD

Table 42. Acronyms Used in this Document *(continued)*

Acronym	Description
PC	program counter
PCB	printed circuit board
PGA	programmable gain amplifier
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset
PRES	precise power-on reset
PRS	pseudo random sequence
PS	port read data register
PSoC®	Programmable System-on-Chip™
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I^2C serial clock
SDA	I^2C serial data
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SOC	start of conversion
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
SWD	serial wire debug, a test protocol

Table 42. Acronyms Used in this Document *(continued)*

Acronym	Description
SWV	single-wire viewer
TD	transaction descriptor, see also DMA
THD	total harmonic distortion
TIA	transimpedance amplifier
TRM	technical reference manual
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSoC pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal

Document Conventions

Units of Measure

Table 43. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibel
fF	femto farad
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohour
kHz	kilohertz
kΩ	kilo ohm
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µH	microhenry
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
sqrtHz	square root of hertz
V	volt

Errata

This section describes the errata for the PSoC Analog Coprocessor, CY8C4AXX product family. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability. Contact your local Cypress Sales Representative if you have questions. For a list of sales offices, go to http://www.cypress.com/sales.

Part Numbers Affected

Part Number	Device Characteristics
CY8C4AXX	PSoC Analog Coprocessor Product Family

PSoC Analog Coprocessor Qualification Status

Product Status: Engineering Samples

PSoC Analog Coprocessor Errata Summary

The following table defines the errata applicability to available PSoC Analog Coprocessor family devices.

Items	CY8C4AXX	Silicon Revision	Fix Status
1. Sensitivity in capacitance measurement	All	First silicon	Silicon and/or firmware fix is planned in Q3 2016
2. SNR value in Switched Cap Filter	All	First silicon	Silicon and/or firmware fix is planned in Q3 2016

1. Sensitivity in capacitance measurement

■ **Problem Definition**

Sensitivity in Capacitance measurement is 0.2 pF instead of 0.1 pF as specified.

■ **Parameters Affected**

Datasheet parameter SID313 (SNR) is measured as 0.2 pF instead of 0.1 pF as specified.

■ **Trigger Condition(s)**

No specific trigger condition.

■ **Scope Of Impact**

Reduced sensitivity implies some corner cases will exhibit increased susceptibility to noise and may not work.

■ **Workaround**

None

■ **Fix Status**

Silicon and/or firmware fix is planned in Q3 2016 when this erratum will be removed from the datasheet.

2. SNR value in Switched Cap Filter

■ **Problem Definition**

SNR is measured as 58 dB instead of 64 dB as specified.

■ **Parameters Affected**

Datasheet parameter SID_SC_1 (Signal-to-Noise Ratio).

■ **Trigger Condition(s)**

No specific trigger condition.

■ **Scope Of Impact**

Reduced sensitivity to noise.

■ **Workaround**

None

■ **Fix Status**

Silicon and/or firmware fix is planned in Q3 2016 when this erratum will be removed from the datasheet.

Revision History

Description Title: PSoC® Analog Coprocessor: CY8C4Axx Family Datasheet Programmable System-on-Chip (PSoC®) Document Number: 001-96467				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*E	5312324	GUL/WKA	06/30/2016	Release to web
*F	5518120	WKA	11/11/2016	Formatted page layout for Alternate Pin Functions.

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