ISL97692, ISL97693, ISL97694A

Single or Multiple Cell Li-ion Battery Powered 4-Channel and 6-Channel LED Drivers

FN7839
Rev.6.00
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The ISL97692, ISL97693, ISL97694A are Intersil's highly integrated 4- and 6-channel LED drivers for display backlighting. These parts maximize battery life by featuring only 1mA quiescent current, and by operating down to 2.4V input voltage, with no need for higher voltage supplies.

The ISL97692 has four channels and provides 8-bit PWM dimming with adjustable dimming frequency up to 30kHz. The ISL97693 has six channels with Direct PWM dimming control. The ISL97694A has 6 channels and provides 8-, 10-, or 12-bit PWM dimming with adjustable dimming frequency up to 30kHz, 7.5kHz, or 1.875kHz, respectively, controlled with I^2C or PWM input.

The ISL97692 and ISL97694A feature phase shifting that may be enabled optionally, providing an optimized phase delay between channels. In the ISL97692 and ISL97694A, phase shifting can multiply the effective dimming frequency by four and six allowing above audio-band PWM dimming with 10-bit dimming resolution.

The ISL97692, ISL97693, ISL97694A employ adaptive boost architecture, which keeps the headroom voltage as low as possible to maximize battery life while allowing ultra low dimming duty cycle as low as 0.005% at 100Hz dimming frequency in Direct PWM mode.

The ISL97692, ISL97693, ISL97694A incorporate extensive protection functions including string open and short circuit detections, OVP, and OTP.

The ISL97692 and ISL97693 are offered in the 16 Ld 3x3mm TQFN package, and a 16 bump 1.7x1.7mm WLCSP for the ISL97692. The ISL97694A is offered in the 20 Ld 3x4mm TQFN package. All parts operate in the ambient temperature range of -40°C to +85°C.

Features

- 2.4V minimum input voltage, supports single cell applications
- 4 channels, up to 40mA each (ISL97692) or 6 channels, up to 30mA each (ISL97693, ISL97694A)
- 90% efficient at 6P5S, 3.7V and 20mA (ISL97693, ISL97694A)
- Low 0.8mA quiescent current
- PWM dimming control with internally generated clock
  - 8-bit resolution with adjustable dimming frequency up to 30kHz (ISL97692, ISL97694A)
  - 12-bit resolution with adjustable dimming frequency up to 1.875kHz (ISL97694A)
  - Optional automatic channel phase shift (ISL97692, ISL97694A)
  - Linear dimming from 0.025%~100% up to 5kHz or 0.4%~100% up to 30kHz (ISL97692, ISL97694A)
- Direct PWM dimming with 0.005% minimum duty cycle at 100Hz
- ±2.5% output current matching
- Adjustable switching frequency from 400kHz to 1.5MHz

Applications

- Tablet, Notebook PC and Smart Phone Displays LED Backlighting

Related Literature

- For a full list of related documents, visit our website
  - ISL97692, ISL97693, ISL97694A product pages

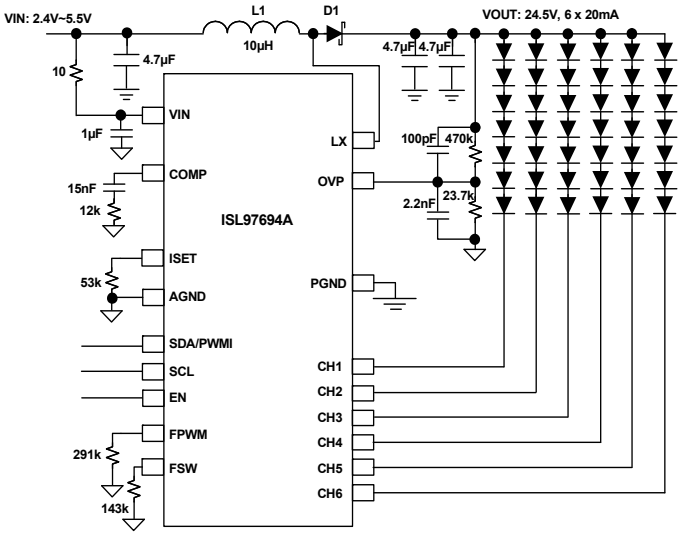

FIGURE 1. ISL97694A TYPICAL APPLICATION DIAGRAM

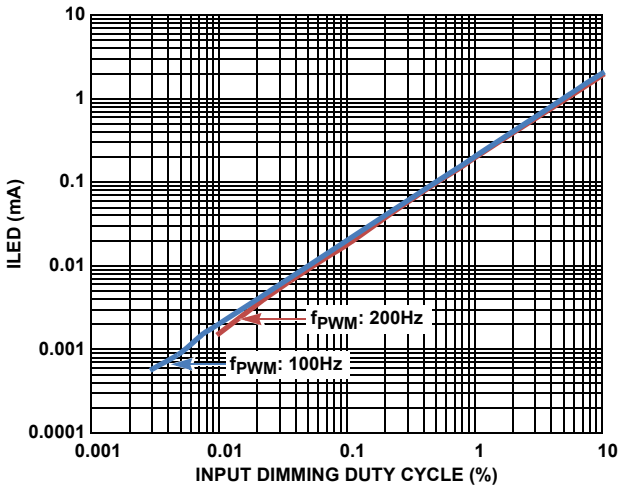

FIGURE 2. ULTRA LOW PWM DIMMING LINEARITY

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Typical Application Circuits

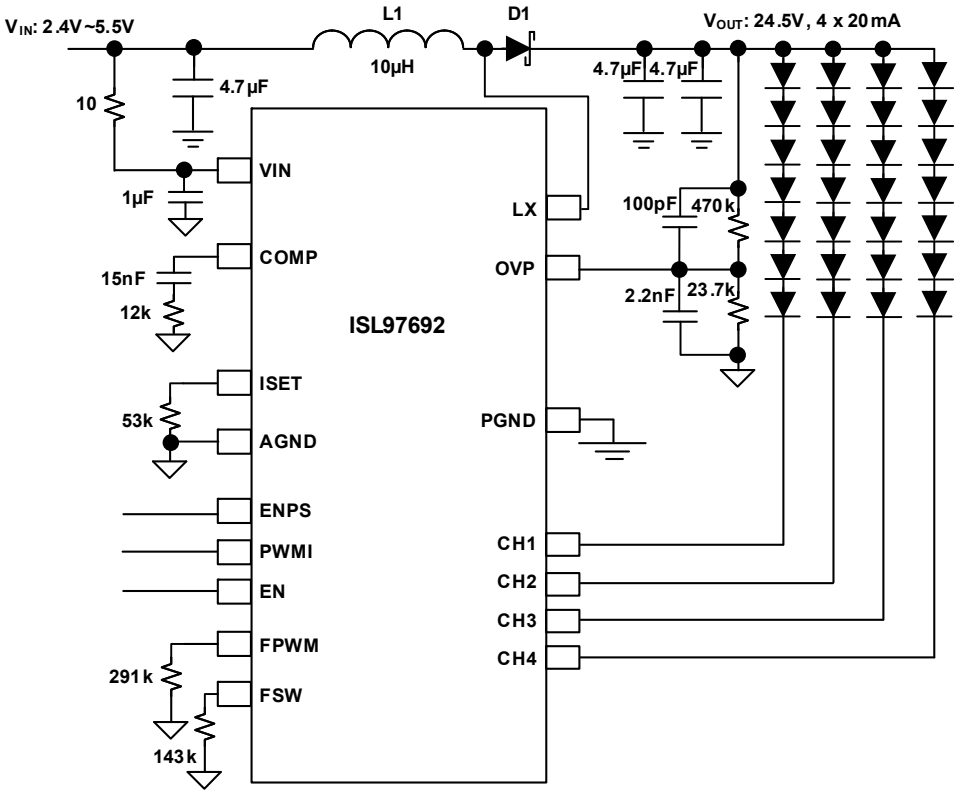


FIGURE 3. ISL97692 TYPICAL APPLICATION DIAGRAM - 4P7S

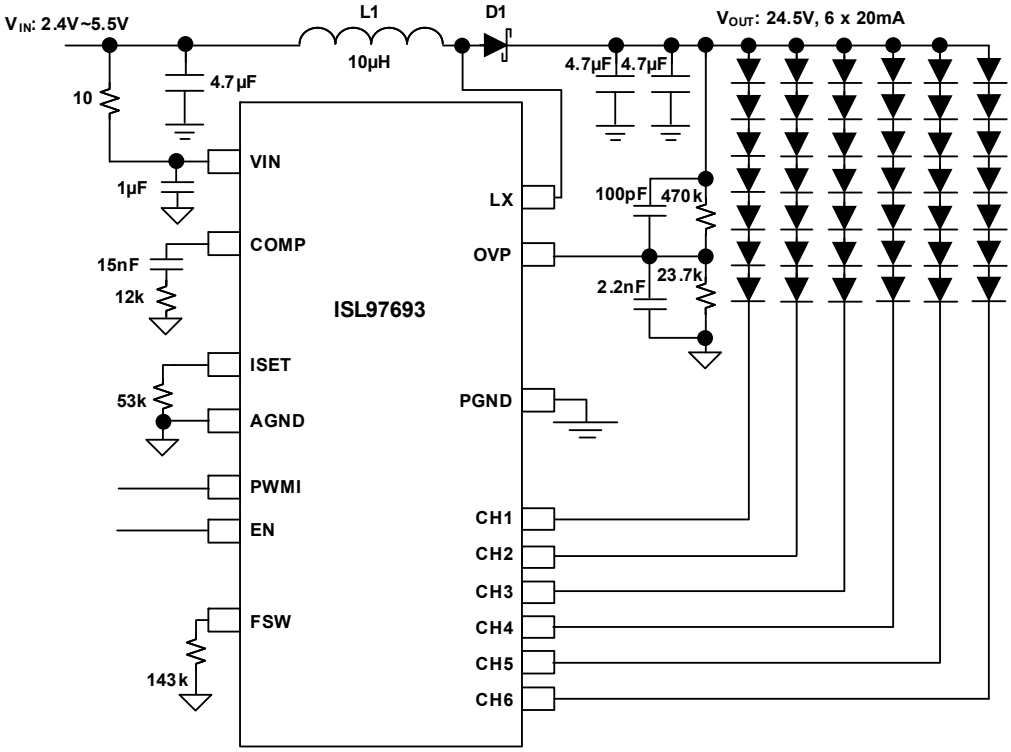


FIGURE 4. ISL97693 TYPICAL APPLICATION DIAGRAM - 6P7S

Typical Application Circuits (Continued)

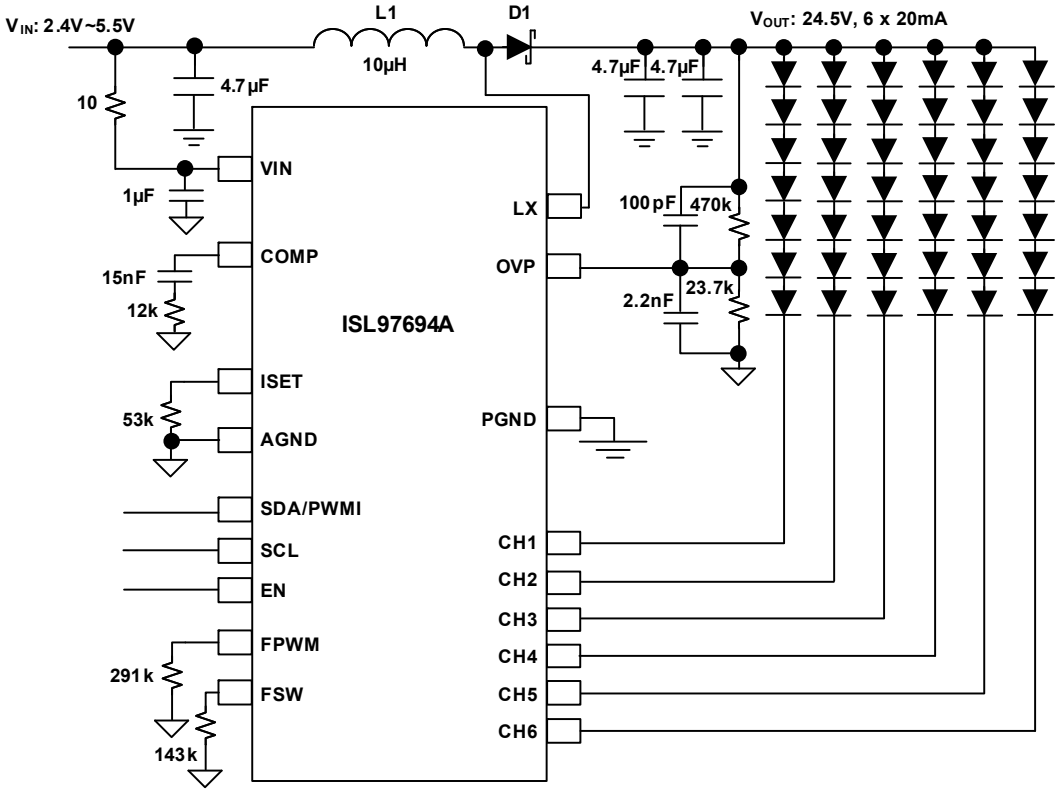


FIGURE 5. ISL97694A TYPICAL APPLICATION DIAGRAM- 6P7S

Block Diagrams

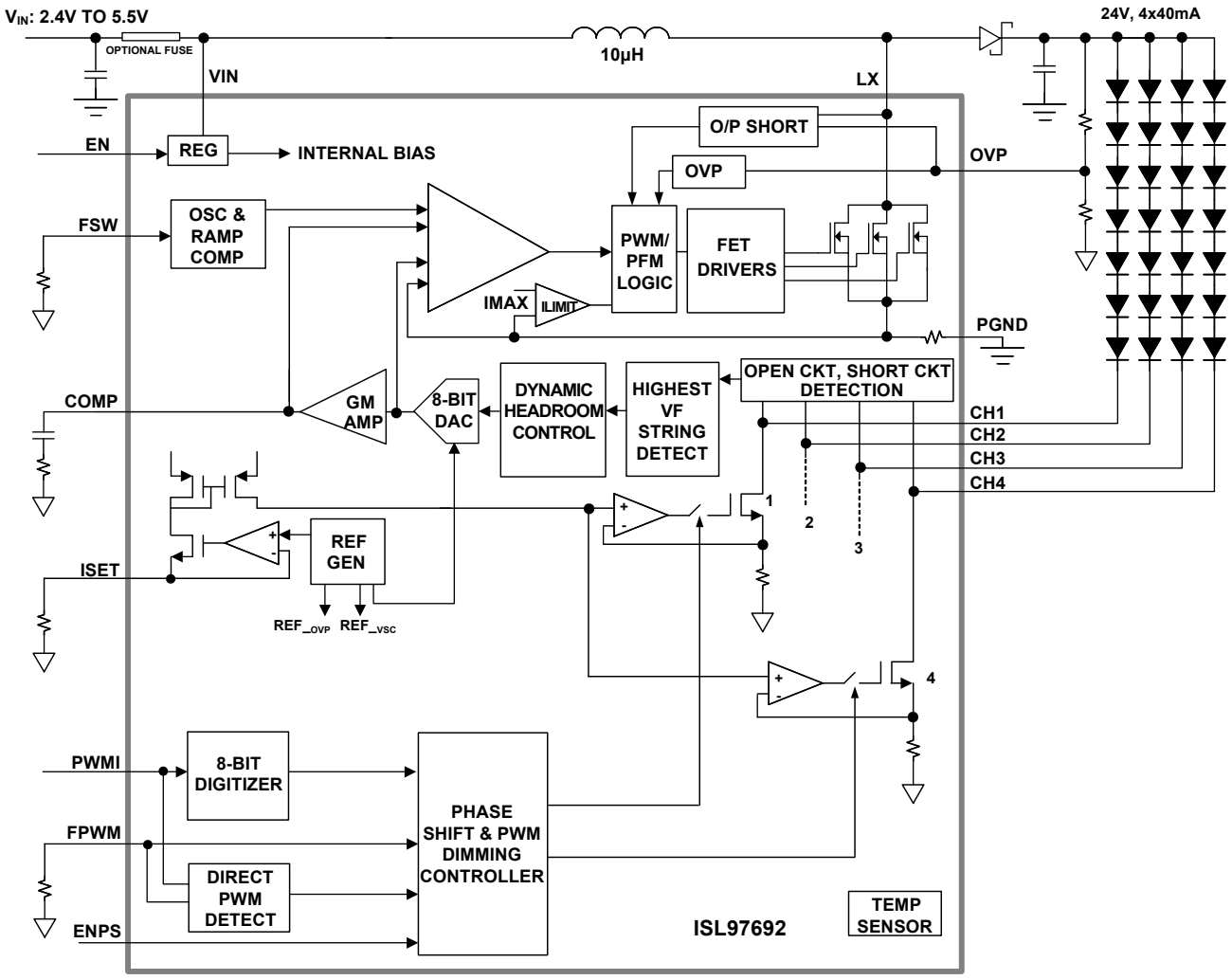


FIGURE 6. ISL97692 BLOCK DIAGRAM

Block Diagrams (Continued)

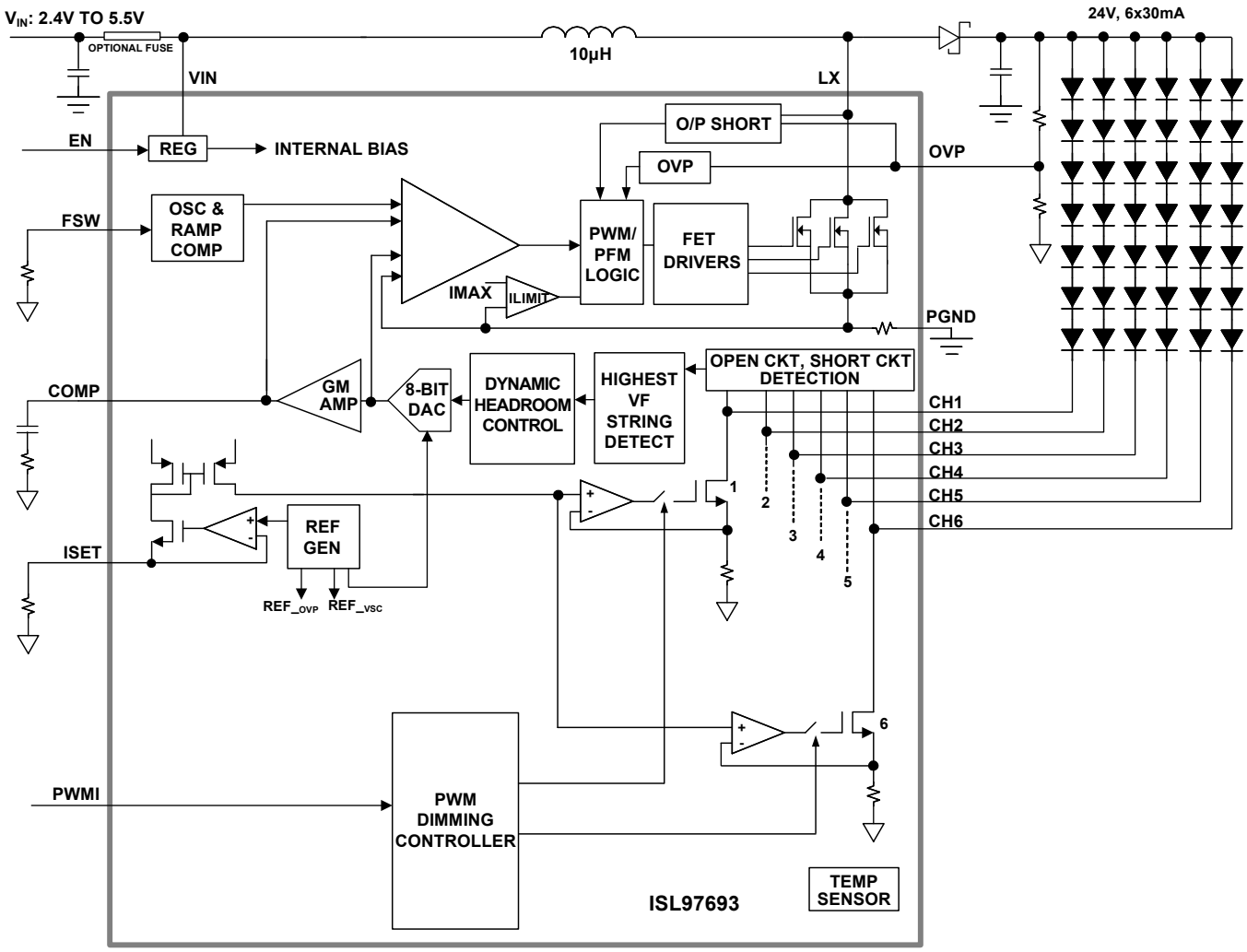


FIGURE 7. ISL97693 BLOCK DIAGRAM

Block Diagrams (Continued)

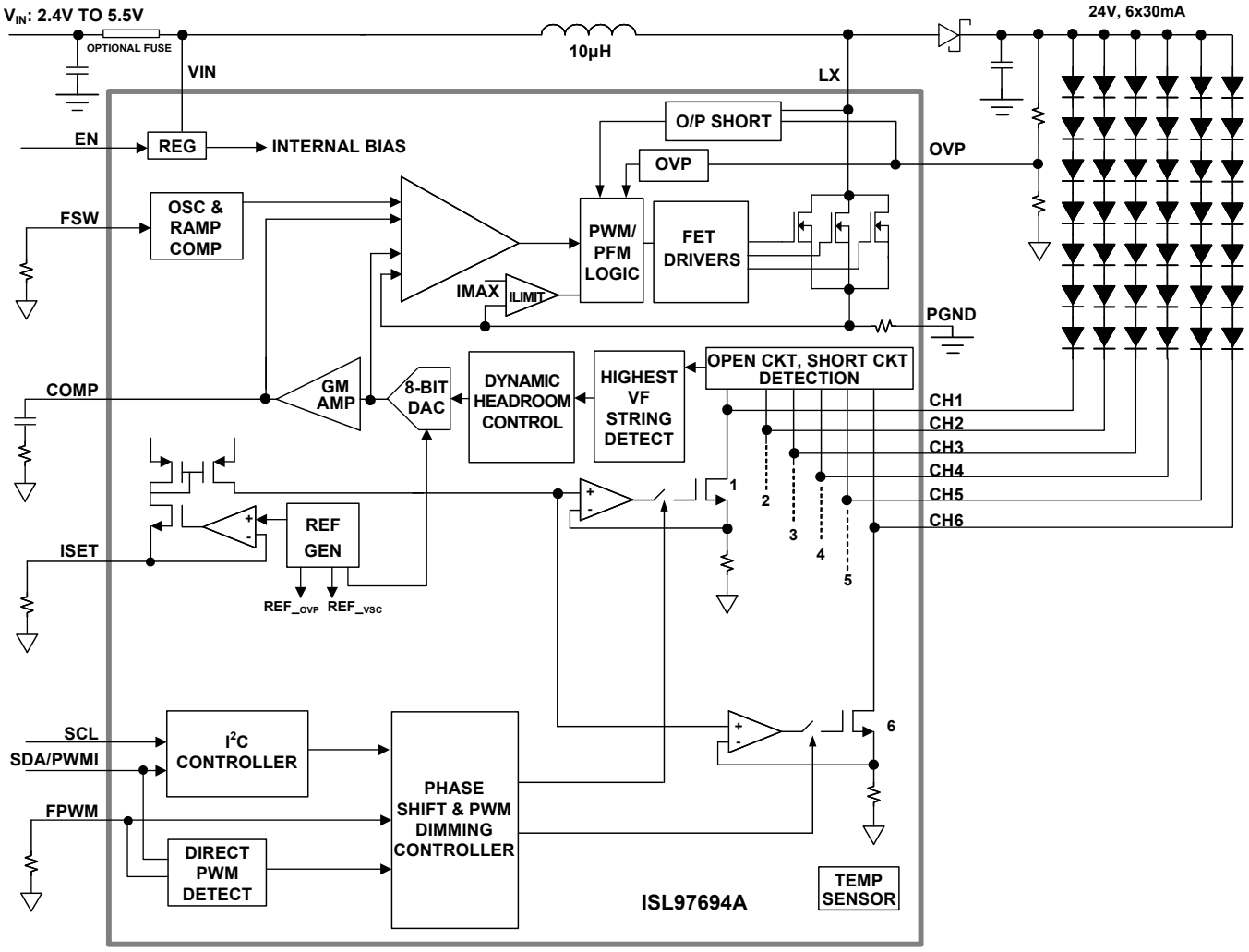
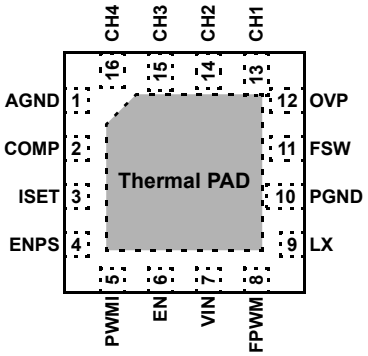


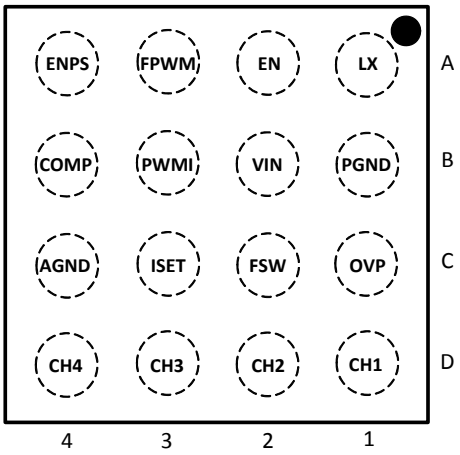
FIGURE 8. ISL97694A BLOCK DIAGRAM

Pin Configurations

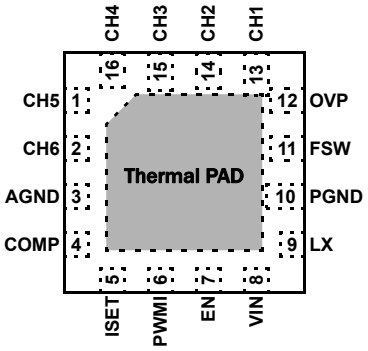
ISL97692
(16 LD TQFN)
TOP VIEW



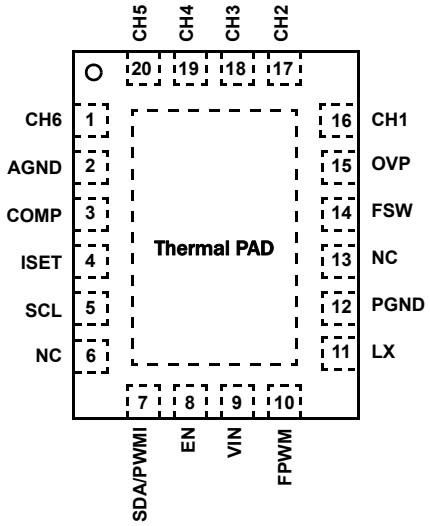
ISL97692
(1.7x1.7x0.53mm, 16 BALL, 0.4mm PITCH WLCSP)
TOP VIEW



ISL97693
(16 LD TQFN)
TOP VIEW



ISL97694A
(20 LD TQFN)
TOP VIEW



Pin Descriptions

PIN NAME	ISL97692		ISL97693	ISL97694A	DESCRIPTION
	TQFN	WLCSP			
AGND	1	C4	3	2	Analog Ground for precision circuits.
CH5	-	-	1	20	Channel 5 current sink and channel monitoring. Tie pin to GND if channel unused.
CH6	-	-	2	1	Channel 6 current sink and channel monitoring. Tie pin to GND if channel unused.
COMP	2	B4	4	3	External compensation. Fit a series RC comprising 12kΩ and 15nF from COMP to GND.
ISET	3	C3	5	4	Channel current setting. The LED channel current is adjusted from 2mA to 40mA (ISL97692) or to 30mA with (ISL97693, ISL97694A) resistor R_{SET} from ISET pin to GND.
ENPS	4	A4	-	-	Enable Phase Shift PWM Dimming Control. High = Enable. Low = Disable.
PWMI	5	B3	6	-	PWM Input Signal for ISL97692/3 for brightness control.
SCL (ISL97694A)	-	-	-	5	I^2C serial clock input. Mode selection to PWMI input when tied to GND for ISL97694A.
SDA/PWMI (ISL97694A)	-	-	-	7	I^2C serial data input and output. PWMI input when SCL tied to GND for ISL97694A.
EN	6	A2	7	8	Enable Input. High = Normal operation. Low = Shutdown.
VIN	7	B2	8	9	Input Supply Voltage.
FPWM	8	A3	-	10	Tie FPWM to VIN to select Direct PWM mode. In Direct PWM mode, the channel outputs follow the PWMI pin's frequency and pulse width. Connect resistor R_{FPWM} from FPWM to GND to select PWM dimming frequency adjustment. In this mode, the channel outputs follow the PWMI pin's PWM duty, and the LED PWM dimming frequency is set by the value of resistor R_{FPWM}.
LX	9	A1	9	11	Input to boost switch.
PGND	10	B1	10	12	Power ground (LX, C_{IN}, and C_{OUT} Power return).
FSW	11	C2	11	14	Switching Frequency Adjustment. The boost switching frequency is adjusted from 400kHz to 1.5MHz with resistor R_{FSW} from FSW pin to GND.
OVP	12	C1	12	15	Overvoltage protection input.
CH1	13	D1	13	16	Channel 1 current sink and channel monitoring. Tie pin to GND if channel unused.
CH2	14	D2	14	17	Channel 2 current sink and channel monitoring. Tie pin to GND if channel unused.
CH3	15	D3	15	18	Channel 3 current sink and channel monitoring. Tie pin to GND if channel unused.
CH4	16	D4	16	19	Channel 4 current sink and channel monitoring. Tie pin to GND if channel unused.
NC	-	-	-	6, 13	Not connected internally.
PAD		-			Connect to PGND and refer to Figure 32 in the General Power PAD Design Considerations.

Ordering Information

PART NUMBER (Note 5)	PART MARKING	TEMP RANGE (°C)	PACKAGE (RoHS Compliant	PKG. DWG. #
ISL97692IRTZ (Notes 1, 3)	7692	-40 to +85	16 Ld 3x3x0.75mm TQFN	L16.3x3D
ISL97692IIZ-T (Notes 2, 4)	7692	-40 to +85	16 Bump 1.7x1.7mm, 0.4mm Pitch WLCSP	W4x4.16B
ISL97693IRTZ (Notes 1, 3)	7693	-40 to +85	16 Ld 3x3x0.75mm TQFN	L16.3x3D
ISL97694AIRTZ (Notes 1, 3)	694A	-40 to +85	20 Ld 3x4x0.8mm TQFN	L20.3x4A

NOTES:

1. Add “-T” suffix for for 6k unit or “-TK” suffix for 1k unit tape and reel options. Refer to TB347 for details on reel specifications.
2. Add “-T” suffix for for 3k unit tape and reel option. Refer to TB347 for details on reel specifications.
3. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. These Intersil Pb-free WLCSP packaged products employ special Pb-free material sets; molding compounds/die attach materials and SnAgCu - e1 solder ball terminals, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free WLCSP packaged products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
5. For Moisture Sensitivity Level (MSL), see the product information page for ISL97692, ISL97693, ISL97694A. For more information on MSL, see TB363.

Absolute Maximum Ratings (Note 6)

VIN, ISET, COMP, OVP . . . . . -0.3V to 6V
PWMI, FPWM, FSW . . . . . -0.3V to 6V
EN, ENPS, SCL, SDA/PWMI . . . . . -0.3V to 6V
CH1 to CH6, LX . . . . . -0.3V to 28V
PGND, AGND . . . . . -0.3V to +0.3V
Maximum Average Current Into LX Pin for TQFN 2.6A
Maximum Average Current Into LX Pin for CSP 1A
ESD Ratings
Human Body Model (Tested per JESD22-A114F)
(ISL97692, ISL97693) 2kV
Human Body Model (Tested per JESD22-A114F) (ISL97694A) . . . 2.5kV
Machine Model (Tested per JESD22-A115C) 200V
Charged Device Model (JESD22-C101E) 2kV
Latch-Up (Tested per JESD-78B; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
16 Ld TQFN (Notes 7, 8)	51	4.6
20 Ld TQFN (Notes 7, 8)	45	3.0
16 Bump WLCSP (Note 7)	82	N/A
Thermal Characterization (Typical) (Note 9)		PSI_{JT} (°C/W)
16 Ld TQFN		0.11
20 Ld TQFN		0.1
Thermal Characterization (Typical)		PSI_{JB} (°C/W)
16 Bump WLCSP (Note 10)		22

Maximum Continuous Junction Temperature . . . . . +125°C
Storage Temperature . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

Input Voltage (V_{IN}) . . . . . 2.4V to 5.5V
Output Voltage (V_{OUT}) . . . . . Up to 26V
Ambient Temperature Range . . . . . -40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

6. Voltage Ratings are all with respect to the AGND pin.
7. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with "direct attach" features. See TB379.
8. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
9. PSI_{JT} is the PSI junction-to-top thermal characterization parameter. If the package top temperature can be measured with this rating then the die junction temperature can be estimated more accurately than the θ_{JC} and θ_{JC} thermal resistance ratings.
10. PSI_{JB} is the PSI junction-to-board thermal characterization parameter.

Electrical Specifications

V_{IN} = EN = 3.3V, T_A = +25°C unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 11)	TYP	MAX (Note 11)	UNIT
GENERAL						
V_{IN}	Backlight Supply Voltage, (Notes 12, 13)	T_A = +25°C	2.4		5.5	V
$I_{VIN\_Standby}$	Standby current	EN = Low, LDO disabled		1		µA
I_{VIN}	V_{IN} Active Current, I_{LED} = 40mA (ISL97692) 30mA (ISL97693/(ISL97694A)	All channels 100% duty		2.5		mA
		All channels 0% duty		0.8		mA
V_{OUT}	Output Voltage	V_{IN} ≥ 2.7V, I_{LED} = 40mA (ISL97692) 30mA (ISL97693/4A)			**26**	V
V_{UVLO}	Undervoltage Lockout Threshold		**2**	2.15	**2.35**	V
V_{UVLO_HYS}	Undervoltage Lockout Hysteresis			150		mV
ENLow	EN Input Low Voltage				**0.5**	V
ENHi	EN Input High Voltage		**1.5**			V
BOOST SWITCHING REGULATOR						
SS	Soft-start	100% LED Duty Cycle		7		ms
SWILimit	Boost FET Current Limit for QFN	2.7V < V_{IN} < 5.5V, f_{SW} = 600kHz, L = 10µH, T_A ≤ +55°C	**2.45**	2.8	**3.2**	A
	Boost FET Current Limit for CSP		**1.2A**	1.6A		A
$r_{DS(ON)}$	Internal Boost Switch ON-Resistance	T_A = +25°C		212		mΩ

Electrical Specifications V_{IN} = EN = 3.3V, T_A = +25°C unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 11)	TYP	MAX (Note 11)	UNIT
Eff_peak	Peak Efficiency	V_{IN} = 5.5V, V_{OUT} = 21V, T_A = +25°C, R_{FSW} = 144kΩ, $I_{CH1-CH6}$ = 20mA, L = 10µH with DCR ≤ 150mΩ		90		%
		V_{IN} = 2.7V, V_{OUT} = 21V, T_A = +25°C, R_{FSW} = 144kΩ, $I_{CH1-CH6}$ = 20mA, L = 10µH with DCR ≤ 150mΩ		76		%
D_{MAX}	Boost Maximum Duty Cycle	F_{SW} = 400kHz	**93.5**			%
		F_{SW} = 1.5MHz	**93**			%
D_{MIN}	Boost Minimum Duty Cycle	F_{SW} = 400kHz			**11**	%
		F_{SW} = 1.5MHz			**15**	%
f_{SW}	Boost Switching Frequency	R_{FSW} = 216kΩ	**360**	400	**440**	kHz
		R_{FSW} = 72.1kΩ		1.2		MHz
		R_{FSW} = 57.7kΩ	**1.35**	1.5	**1.65**	MHz
ILX_leakage	LX Leakage Current	LX = 26V			**10**	µA
REFERENCE						
I_{MATCH}	Channel-to-Channel DC Current Matching	I_{LED} = 20mA	**-2.5**		**+2.5**	%
I_{ACC}	Current Accuracy	I_{LED} = 20mA	**-3**		**+3**	%
FAULT DETECTION						
V_{SC}	Channel Short Circuit Threshold		**6.75**	8	**9.25**	V
V_{temp}	Over-Temperature Threshold			150		°C
V_{OVPlo}	Overvoltage Limit on OVP Pin		**1.180**	1.22	**1.245**	V
OVP_{fault}	OVP Short Detection Fault Level			75		mV
CURRENT SOURCES						
$V_{headroom}$	Dominant Channel Current Source Headroom at CH Pin	I_{LED} = 20mA, T_A = +25°C		300 (Note 14)		mV
$V_{HEADROOM\_RANGE}$	Dominant Channel Current Sink Headroom Range at CHx Pin	I_{LED} = 20mA, T_A = +25°C		65		mV
$I_{LED(max)}$	Maximum LED Current per Channel	2.7V < V_{IN} < 5.5V, V_{OUT} = 21V (ISL97692 QFN)	40			mA
		2.7V < V_{IN} < 5.5V, V_{OUT} = 21V (ISL97692 WLCSP, ISL97693, and ISL97694A)	30			mA
PWM GENERATOR						
V_{IL}	Guaranteed Range for PWM Input Low Voltage				**0.5**	V
V_{IH}	Guaranteed Range for PWM Input High Voltage		**1.5**			V
F_{PWMI}	PWMI Input and Output Frequency Range	8-bit Dimming Resolution	**100**		**30,000**	Hz
		10-bit Dimming Resolution	**100**		**7.5**	kHz
		12-bit Dimming Resolution	**100**		**1.87**	kHz
$DPWM_{ACC}$	Direct PWM Dimming Output Resolution	(ISL97692, ISL97693 and ISL97694A)		80		ns
$t_{DPWM\_ON\_MIN}$	Direct PWM Dimming Minimum On-Time	(ISL97692, ISL97693 and ISL97694A)		350		ns
PWM_{ACC}	PWM Dimming with Adjustable Dimming Frequency Output Resolution	(ISL97692, ISL97694A)		8		bit
		ISL97694A, En10Bit = 1		10		bit
		ISL97694A, En12Bit = 1		12		bit

Electrical Specifications V_{IN} = EN = 3.3V, T_A = +25°C unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 11)	TYP	MAX (Note 11)	UNIT
F_{PWM}	Generated PWM Dimming Frequency Range	(ISL97692, ISL97694A)	**100**		**30,000**	Hz
SMBus/I²C INTERFACE (ISL97694A only)						
VIL	Guaranteed Range for Data, Clock Input Low Voltage				**0.5**	V
VIH	Guaranteed Range for Data, Clock Input High Voltage		**1.5**		**VDD**	V
VOL	SMBus/I²C Output Data Line Logic Low Voltage	I_{PULLUP} = 4mA			**0.17**	V
I_{LEAK}	Input Leakage On SDA/SCL	Measured at 4.8V	**-10**		**10**	µA
SMBus/I²C TIMING SPECIFICATIONS (ISL97694A only)						
tEN-SMBus/I²C	Minimum Time between VIN>UVLO and SMBus/I²C Enabled		**2**			ms
F_{SCL}	SCL Clock Frequency				**400**	kHz
t_{BUF}	Bus Free Time Between Stop and Start Condition		**1.3**			µs
$t_{HD:STA}$	Hold Time After (Repeated) START Condition	After this Period, the First Clock is Generated	**0.6**			µs
$t_{SU:STA}$	Repeated Start Condition Setup Time		**0.6**			µs
$t_{SU:STO}$	Stop Condition Setup Time		**0.6**			µs
$t_{HD:DAT}$	Data Hold Time		**300**			ns
$t_{SU:DAT}$	Data Setup Time		**100**			ns
t_{HIGH}	Low Period of SCL Clock		**1.3**			µs
t_{LOW}	High Period of SCL Clock		**0.6**			µs
t_F	Clock/data Fall Time				300	ns
t_R	Clock/data Rise Time				300	ns

NOTES:

11. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
12. At maximum V_{IN} of 5.5V, minimum V_{OUT} is 6V. Minimum V_{OUT} can be lower at lower V_{IN}.
13. Limits established by characterization and are not production tested.
14. Varies within the range specified by $V_{HEADROOM\_RANGE}$.

Typical Performance Curves

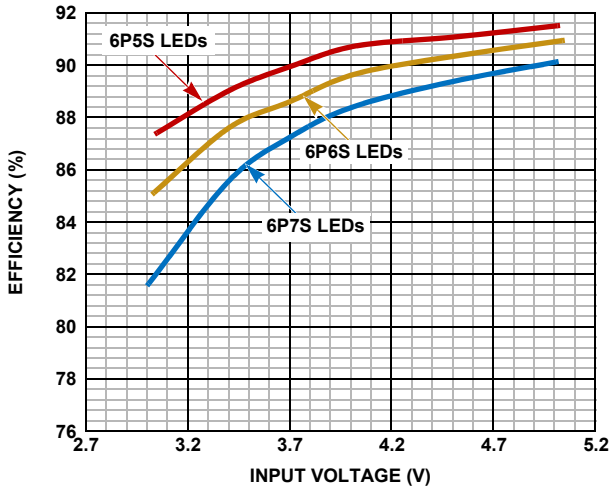


FIGURE 9. EFFICIENCY vs V_{IN} (I_{CH}: 20mA, f_{DIM}: 200Hz, FOR LEDs: 6P5S, 6P6S, 6P7S)

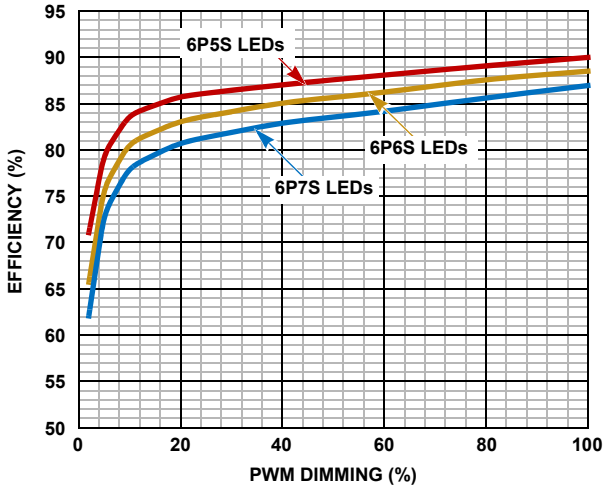


FIGURE 10. EFFICIENCY vs PWM DIMMING (V_{IN}: 3.7V, I_{CH}: 20mA, f_{DIM}: 200Hz, FOR LEDs: 6P5S, 6P6S, 6P7S)

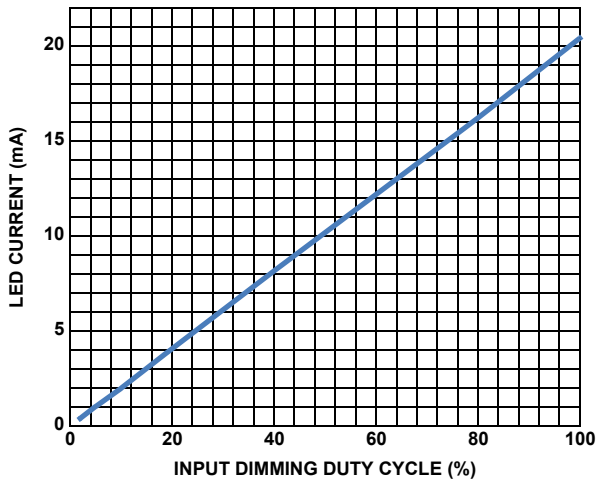


FIGURE 11. PWM DIMMING LINEARITY (V_{IN}: 3.7V, V_{OUT}: 21V FOR 6P7S, f_{DIM}: 200Hz)

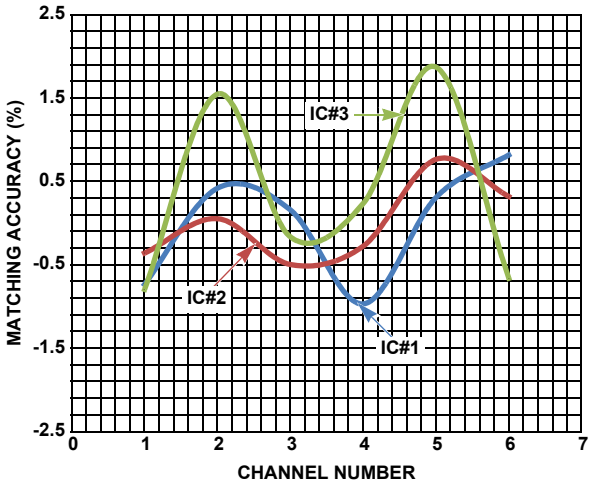


FIGURE 12. CHANNEL MATCHING ACCURACY (V_{IN}: 3.7V, V_{OUT}: 21V FOR 6P7S, I_{CH}: 20mA)

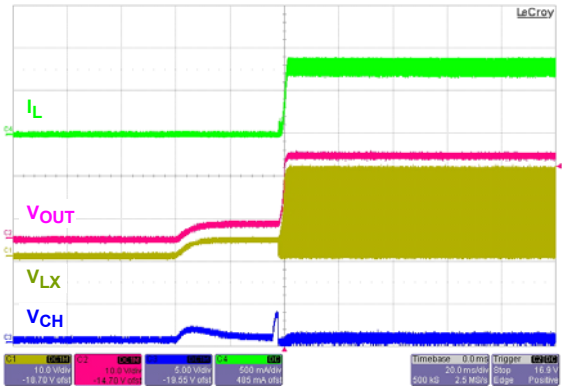


FIGURE 13. START-UP (100% DIRECT PWM DIMMING, V_{IN}: 3.7V, I_{CH}: 20mA, LEDs: 6P7S, f_{DIM}: 200Hz)

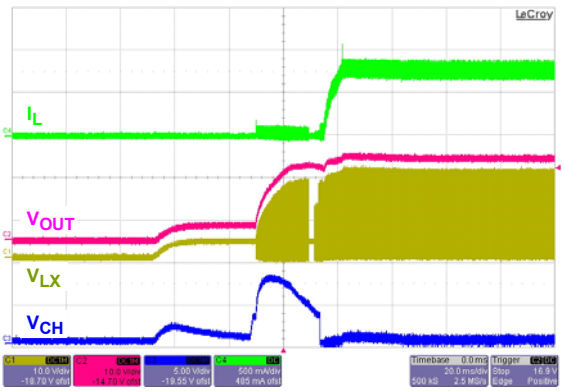


FIGURE 14. START-UP (100% DECODED PWM DIMMING, V_{IN}: 3.7V, I_{CH}: 20mA, LEDs: 6P7S, f_{DIM}: 200Hz)

Typical Performance Curves (Continued)

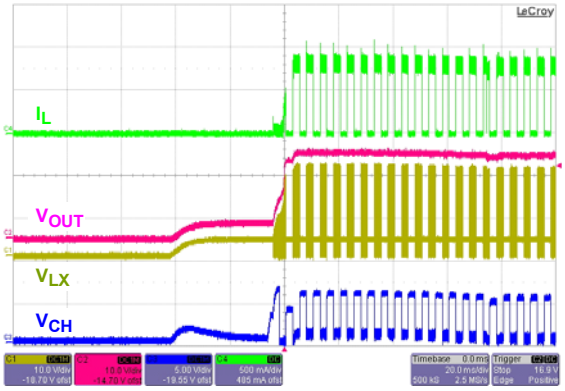


FIGURE 15. START-UP (50% DIRECT PWM DIMMING, V_{IN}: 3.7V, I_{CH}: 20mA, LEDs: 6P7S, f_{DIM}: 200Hz)

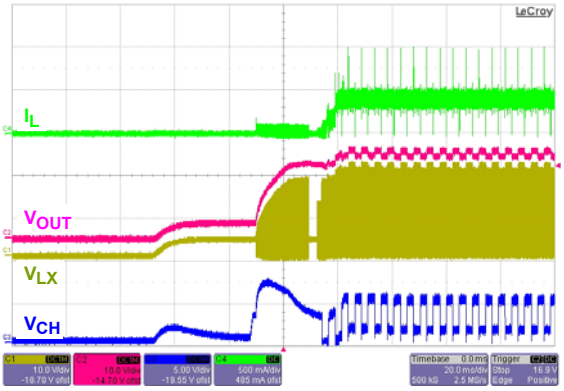


FIGURE 16. START-UP (50% DECODED PWM DIMMING, V_{IN}: 3.7V, I_{CH}: 20mA, LEDs: 6P7S, f_{DIM}: 200Hz)

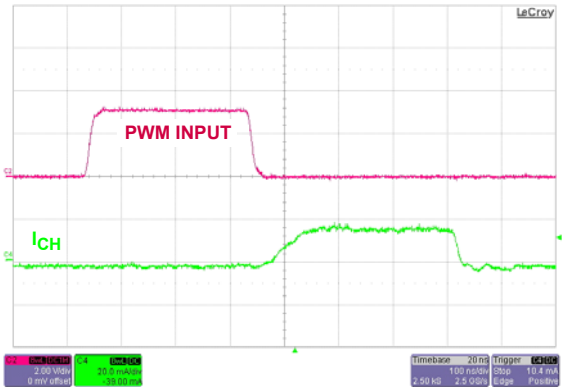


FIGURE 17. MINIMUM DIMMING DUTY CYCLE (0.003% DIRECT PWM DIMMING MODE, f_{DIM}: 100Hz)

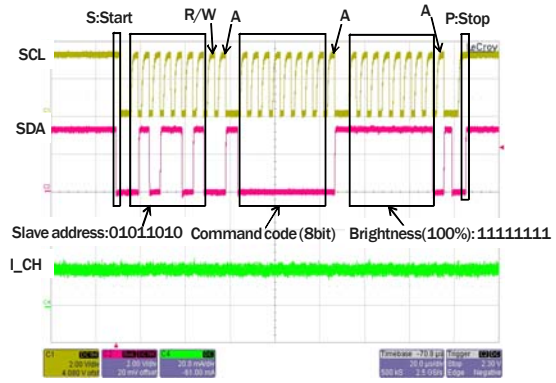


FIGURE 18. I^2C CONTROL TIMING AND CHANNEL CURRENT (100% DIMMING, ISL97694A)

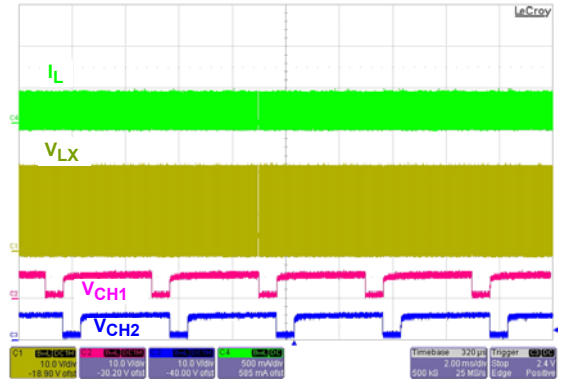


FIGURE 19. DECODED PWM DIMMING WITH PHASE SHIFT (V_{IN}: 3.7V, I_{CH}: 20mA, DIM: 17%, f_{DIM}: 250Hz, LEDs: 6P6S)

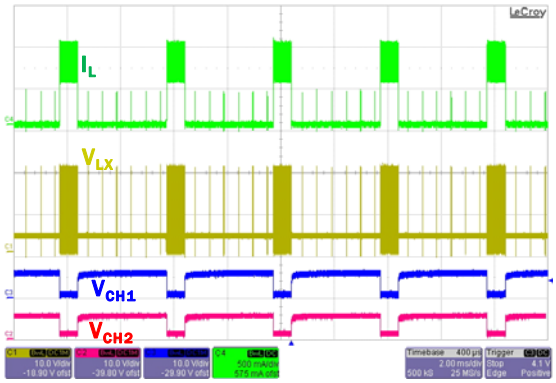


FIGURE 20. DIRECT PWM DIMMING WITHOUT PHASE SHIFT (V_{IN}: 3.7V, I_{CH}: 20mA, DIM: 17%, f_{DIM}: 250Hz, LEDs: 6P6S)

Theory of Operation

PWM Boost Converter

The current mode PWM boost converter produces the minimal voltage needed to enable the LED stack with the highest forward voltage drop to run at the programmed current. The ISL97692, ISL97693, ISL97694A employs current mode control boost architecture that has a fast current sense loop and a slow voltage feedback loop. This architecture achieves the fast transient response, which is essential for portable product backlight applications where the backlight must not flicker when the power source is changed from a drained battery to an AC/DC adapter.

The number of LEDs that can be driven by ISL97692, ISL97693, ISL97694A depends on the type of LED chosen in the application. The maximum output is 26V at 40mA from 2.7V input.

Enable

Take the EN input high to enable the ISL97692, ISL97693, ISL97694A for normal operation and low to enter low-power shutdown, which immediately turns off LED channels and the boost regulator.

Dimming Controls

The ISL97692, ISL97693, ISL97694A allows the LED current to be programmed in the range 2mA to 40mA (ISL97692) or 2mA to 30mA (ISL97693, ISL97694A) by R_{SET} per Equation 1:

$$I_{LEDmax} = \frac{1066}{R_{SET}} \quad \text{(EQ. 1)}$$

Where:

- 1066 is a constant determined by design
- R_{SET} is the resistor from ISET pin to GND (Ω)
- I_{LEDmax} is the peak current set by resistor R_{SET} (A)

For example, if the required LED current (I_{LEDmax}) is 40mA, then the R_{SET} value needed is:

$$R_{SET} = 1066/0.04 = 26.65k\Omega \quad \text{(EQ. 2)}$$

Choose the nearest standard resistor: 26.65kΩ, 0.1%

Direct PWM Dimming

The ISL97693 always operates in Direct PWM dimming mode. The ISL97692 and ISL97694A can be selected to operate in Direct PWM dimming mode by connecting the FPWM pin to VIN and the SCL pin of ISL97694A must be tied to GND.

With Direct PWM, the channel outputs follow the input PWM signal frequency and pulse width, as provided to the PWMI pin. When PWMI is high, all channels sink the current set by the R_{SET} resistor. When PWMI is low, all channels are high-Z.

The maximum allowed input PWM frequency at PWMI is 30kHz. The minimum duty is calculated by Equation 3 according to the input PWM frequency, and is set by the minimum channel on-time of 350ns.

$$\text{Min Duty Cycle} = 350ns \times \text{Input PWM Frequency} \quad \text{(EQ. 3)}$$

For example, for a 200Hz input PWM frequency, the minimum duty cycle is:

$$\text{Min Duty Cycle} = 350ns \times 200Hz = 0.007\% \quad \text{(EQ. 4)}$$

The resolution is calculated by Equation 5 according to the input PWM frequency, and the fixed 80ns resolution of ISL97692, ISL97693, ISL97694A.

$$\text{PWM Resolution} = \frac{1}{80ns \times \text{Input PWM Frequency}} \quad \text{(EQ. 5)}$$

Thus the effective resolution at 200Hz is 15.9 bits:

$$\text{PWM Resolution} = \frac{1}{80ns \times 200Hz} = 62500 = 15.9bits \quad \text{(EQ. 6)}$$

Phase Shift Control

The ISL97692, ISL97694A are capable of delaying the phase of each current source. Conventional LED drivers exhibit the worst load transients to the boost circuit by turning on all channels simultaneously, as shown in Figures 21 and 23. In contrast, the ISL97692, ISL97694A phase shift each channel by turning them on once during each PWM dimming period, as shown in Figures 22 and 24. At each dimming duty cycle (except at 100%) the sum of the phase shifted total current will be less than a conventional LED drivers' total current.

For the ISL97692, ISL97694A, the channels are separated by 360°/N, where N is number of channels enabled. For example, if three channels are enabled, they will be separated by 120°.

If the channels are combined for higher current application, the phase shift function must be disabled by connecting the ENPS pin to ground.

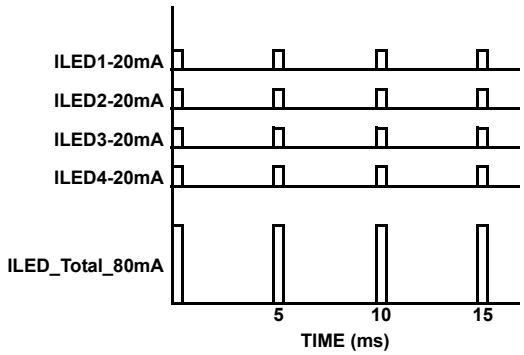


FIGURE 21. CONVENTIONAL 4-CH LED DRIVER WITH 10% PWM DIMMING CHANNEL CURRENT (UPPER) AND TOTAL CURRENT (LOWER)

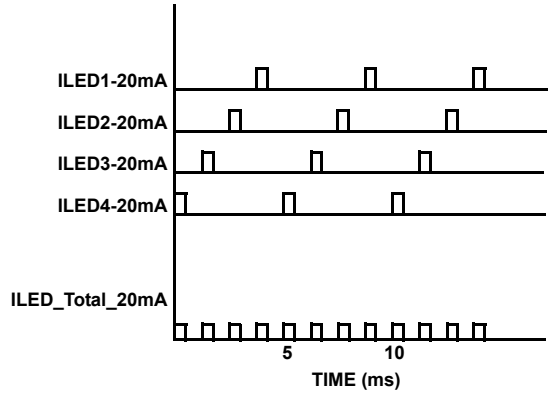


FIGURE 22. ISL97692 PHASE SHIFT 4-CHANNELS LED DRIVER WITH 10% PWM DIMMING CHANNEL CURRENT (UPPER) AND TOTAL CURRENT (LOWER)

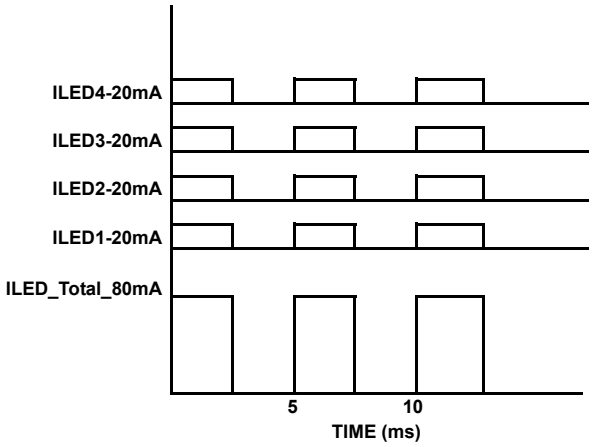


FIGURE 23. CONVENTIONAL LED DRIVER PWM DIMMING CHANNEL AND TOTAL CURRENT AT 50% DUTY CYCLE

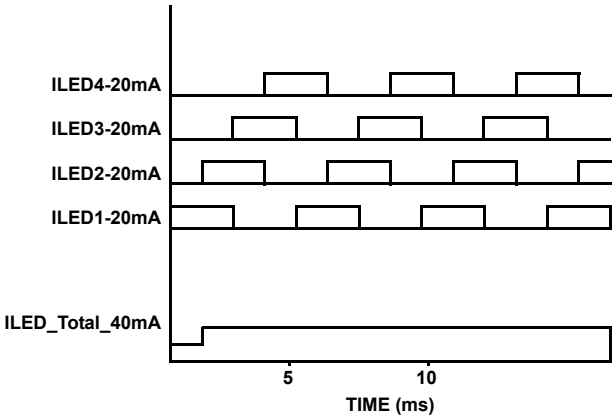


FIGURE 24. ISL97692 PHASE SHIFT LED DRIVER PWM DIMMING CHANNEL AT 50% DUTY CYCLE

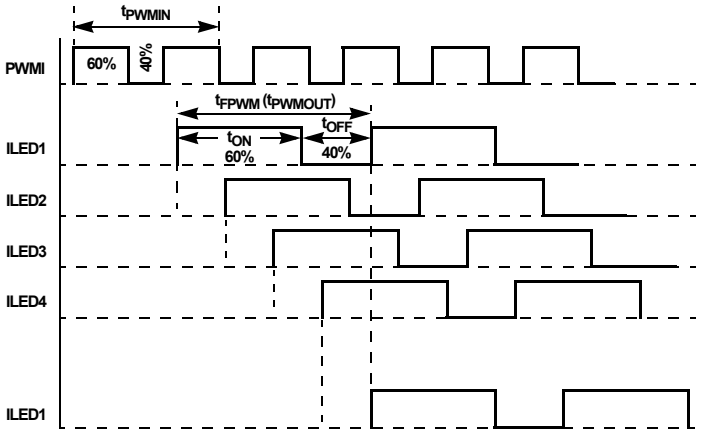


FIGURE 25. ISL97692 4 -CHANNELS PHASE SHIFT TIMING ILLUSTRATION

PWM Dimming Frequency Adjustment (ISL97692, ISL97694A)

The ISL97692 and ISL97694A can use an internal oscillator to generate the PWM dimming frequency. In this mode, the duty of the signal at PWMI pin is measured with 8-, 10- or 12-bit resolution, and applied to the internally generated PWM dimming frequency. The dimming frequency is set by an external resistor R_{FPWM} at the FPWM pin for ISL97692 and ISL97694A, per Equation 7:

$$R_{FPWM} = \frac{R0}{F_{PWM}} \quad \text{(EQ. 7)}$$

Where:

- R0 is determined by design
- R0 = 58.1 X 10^6 for 8-bit
- R0 = 14.5 X 10^6 for 10-bit
- R0 = 36.2 X 10^5 for 12-bit
- F_{PWM} is the required PWM dimming frequency (Hz)
- R_{FPWM} is the resistor from FPWM pin to GND (Ω)

For example, to set the PWM dimming frequency to 480Hz at 8-bit resolution:

$$R_{FPWM} = \frac{58.1 \times 10^6}{480} = 121\text{k}\Omega \quad \text{(EQ. 8)}$$

The maximum allowed input and output PWM dimming frequency varies according to the PWM resolution, per Table 1. This is configurable for the ISL97694A by the En12Bit and En10Bit bits in register 0x01.

TABLE 1. MAX PWM DIMMING FREQUENCY SET BY R_{FPWM}

PART	MAX FREQUENCY (kHz)	PWM RESOLUTION (BIT MODE)
ISL97692	30	8
ISL97694A	30	8
	7.5	10
	1.875	12

Current Matching and Current Accuracy

Each channel of the LED current is regulated by a current sink circuit.

The LED peak current is set by the external R_{SET} resistor according to Equation 1. The current sink MOSFETs in each LED driver channel output are designed to operate within a range at about 300mV to optimize power loss versus accuracy requirements. The sources of errors of the channel-to-channel current matching come from internal amplifier offsets, internal layout and reference accuracy. These parameters are optimized for current matching and absolute current accuracy. Absolute accuracy is also determined by the external resistor R_{SET}, and so a 0.1% tolerance resistor is recommended.

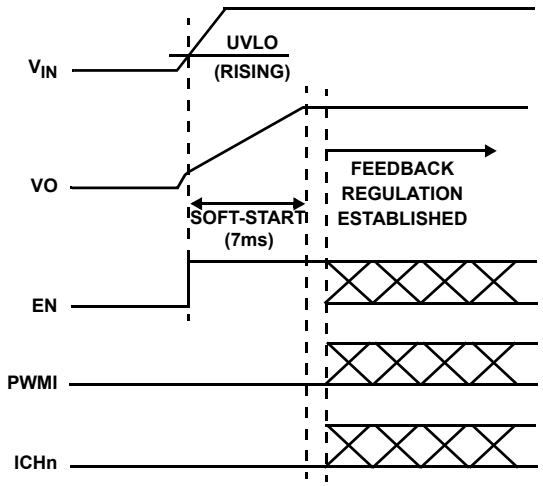
Dynamic Headroom Control

The ISL97692, ISL97693, ISL97694A features a proprietary Dynamic Headroom Control circuit that detects the highest forward voltage string or effectively the lowest voltage on any of the channel pins. When this lowest channel voltage is lower than the short circuit threshold, V_{SC}, such voltage will be used as the feedback signal for the boost regulator. The boost makes the output to the correct level, such that the lowest channel pin is at the target headroom voltage. Since all LED stacks are connected to the same output voltage, the other channel pins will have a higher voltage, but the regulated current source circuit on each channel will ensure that each channel has the same current. The output voltage will regulate cycle-by-cycle and it is always referenced to the highest forward voltage string in the architecture.

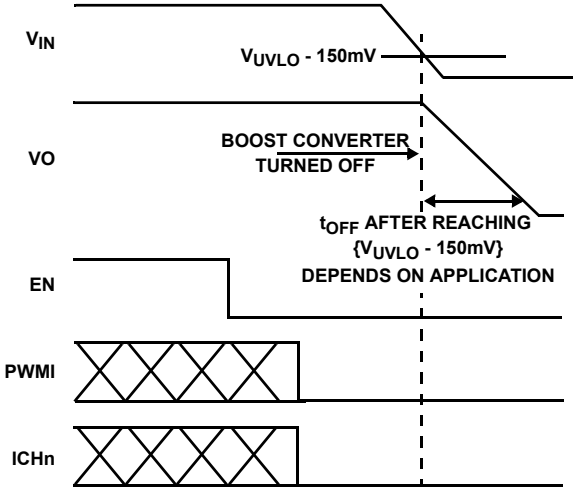
Soft-Start and Power ON

Once the ISL97692, ISL97693, ISL97694A are powered up and the EN pin is taken high, the boost regulator will begin to switch and the current in the inductor will ramp-up. The current in the boost power switch is monitored and the switching is terminated in any cycle where the current exceeds the current limit. The ISL97692, ISL97693, ISL97694A includes a soft-start feature where this current limit starts at a low value (350mA). This is stepped up to the final 2.8A current limit in seven further steps of 350mA. These steps will happen over typically 7ms, and will be extended at low LED PWM frequencies if the LED duty cycle is low. This allows the output capacitor to be charged to the required value at a low current limit and prevents high input current for systems that have only a low to medium output current requirement.

Note that there will be also an initial in-rush current to C_{OUT} when V_{IN} is applied. This is determined by the ramp rate of V_{IN} and the values of C_{OUT} and L



Power-OFF Sequence



Operation with Input Voltage Greater than 5.5V

The ISL97692, ISL97693, ISL97694A boost regulator can operate from an input voltage higher than 5.5V, and up to 23V, as long as an additional supply voltage between 2.4V and 5.5V is available for the VIN pin. Please refer to Figure 26 for a typical application schematic adopting this solution.

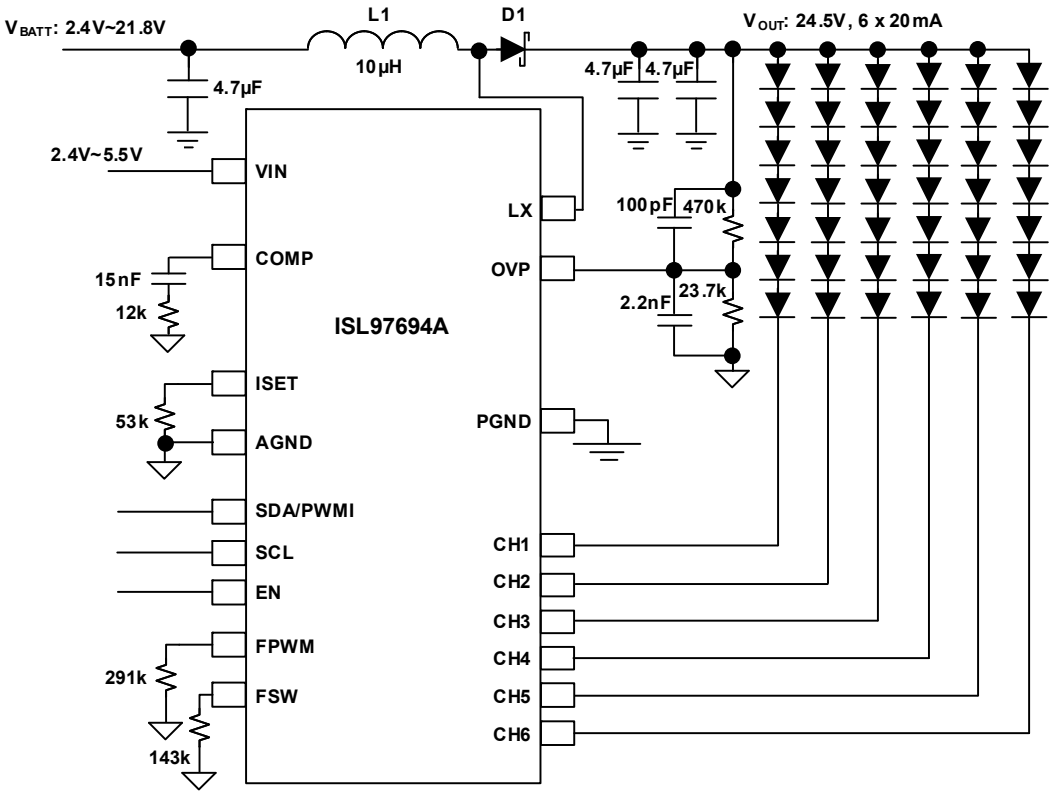


FIGURE 26. LED DRIVER OPERATION WITH INPUT VOLTAGE UP TO 26V

SMBus/I²C Communications

The ISL97694A is controlled by SMBus/I²C for PWM dimming, and powers up in the shutdown state. The ISL97694A is enabled when both the EN pin is high and the BL_CTL bit in register 0x01 is programmed to 1.

Write Byte

The Write Byte protocol is only three bytes long. The first byte starts with the slave address followed by the "command code," which translates to the "register index" being written. The third byte contains the data byte that must be written into the register selected by the "command code". A shaded label is used on cycles during which the slaved backlight controller "owns" or "drives" the Data line. All other cycles are driven by the "host master."

Read Byte

As shown in Figure 30, the four byte long Read Byte protocol starts out with the slave address followed by the "command code", which translates to the "register index." Subsequently, the bus direction turns around with the rebroadcast of the slave address with bit 0 indicating a read ("R") cycle. The fourth byte contains the data being returned by the backlight controller. That byte value in the data byte reflects the value of the register being queried at the "command code" index. Note the bus directions, which are highlighted by the shaded label that is used on cycles during which the slaved backlight controller "owns" or "drives" the Data line. All other cycles are driven by the "host master."

Slave Device Address

The slave address contains 7 MSB plus one LSB as R/W bit, but these 8 bits are usually called Slave Address bytes. As shown in Figure 27, the high nibble of the Slave Address byte is 0x5 or b'0101' to denote the "backlight controller class". Bit 0 is always the R/W bit, as specified by the SMBus/I²C protocol. If the device is in the write mode where bit 0 is 0, the slave address byte is 0x5A or b'01011010'. If the device is in the read mode where bit 0 is 1, the slave address byte is 0x5B or b'01011011'.

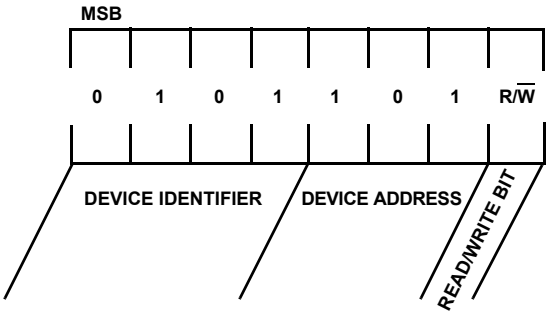
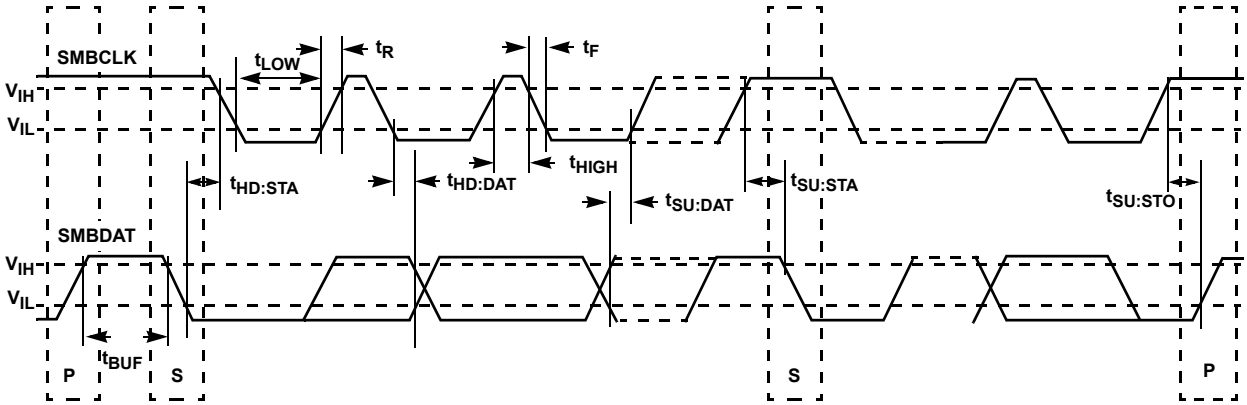


FIGURE 27. SLAVE ADDRESS BYTE DEFINITION

SMBus/I²C Register Definitions

The backlight controller registers are Byte wide and accessible via the SMBus/I²C Read/Write Byte protocols. Their bit assignments are provided in Figures 29 and 30 with reserved bits containing a default value of “0”.

When the ISL97694A is configured to 10-bit or 12-bit operation, write the PWM Brightness Control Register LSB (address 0x02) first. The subsequent write of PWM Brightness Control Register MSB (address 0x00) updates the contents of both registers to the PWM engine.



NOTES:

SMBus/I²C DESCRIPTION

S = START CONDITION

P = STOP CONDITION

A = ACKNOWLEDGE

A = NOT ACKNOWLEDGE

R/W = READ ENABLE AT HIGH; WRITE ENABLE AT LOW

FIGURE 28. SMBUS/I²C INTERFACE for ISL97694A

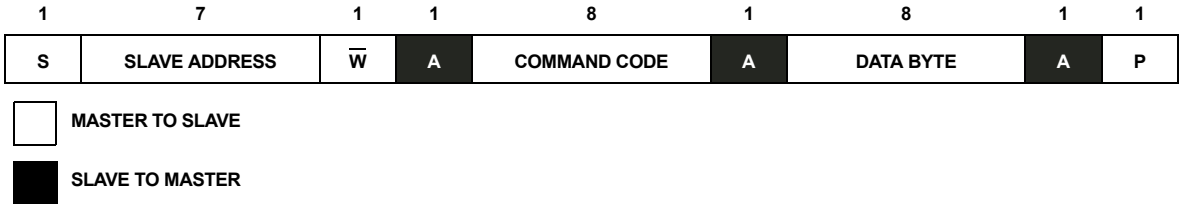


FIGURE 29. WRITE BYTE PROTOCOL for ISL97694A

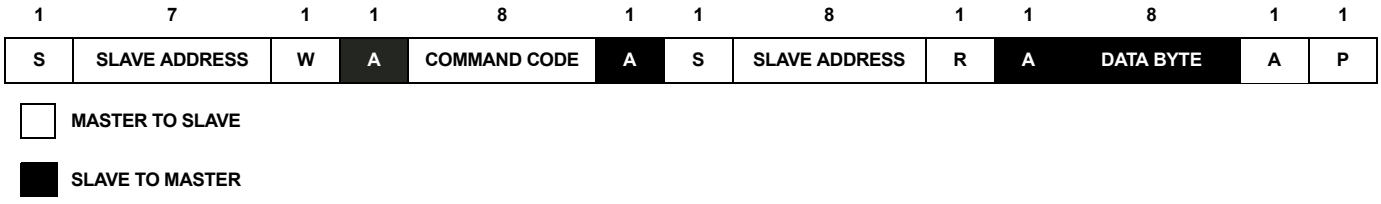


FIGURE 30. READ BYTE PROTOCOL for ISL97694A

TABLE 2. I^2C REGISTER ALL LOCATIONS FOR ISL97694A

ADDRESS	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	DEFAULT VALUE	SMBUS/I^2C PROTOCOL
0x00	PWM Brightness Control Register MSB	BRT11	BRT10	BRT9	BRT8	BRT7	BRT6	BRT5	BRT4	0xFF	Read and Write
0x01	Device Control Register	-	-	-	-	En12Bit	En10Bit	PS_EN	BL_CTL	0x00	Read and Write
0x02	PWM Brightness Control Register LSB	BRT3	BRT2	BRT1	BRT0	-	-	-	-	0xF0	Read and Write

TABLE 3. I^2C REGISTER FUNCTIONS FOR ISL97694A

ADDRESS	REGISTER	DATA BIT DESCRIPTIONS
0x00	PWM Brightness Control Register MSB	BRT[11..4] = DPWM duty cycle brightness control In 8 bit PWM data mode, PWM data is BRT[11..4] In 10 bit PWM data mode, PWM data is BRT[11..2] In 12 bit PWM data mode, PWM data is BRT[11..0]
0x01	Device Control Register	PS_EN = Phase shift On/Off (1: Phase shift enabled, 0: Phase shift disabled) BL_CTL = Backlight On/Off (1: driver enabled if EN pin is high, 0 = driver shutdown) {En12Bit, En10Bit} = {0,0} to select 8 bit PWM data mode {En12Bit, En10Bit} = {0,1} to select 10 bit PWM data mode {En12Bit, En10Bit} = {1,0} to select 12 bit PWM data mode
0x02	PWM Brightness Control Register LSB	BRT[3.0] = DPWM duty cycle brightness control (10 and 12 bit PWM data modes only). *Note: this data is saved, but the PWM engine is only updated with BRT[11..0] or BRT[11..2] when the PWM Brightness Control Register MSB 0x00 is written*

Component Selection

The design of the boost converter is simplified by an internal compensation scheme allowing easy design without complicated calculations. Please select your component values using the following recommendations.

Input Capacitor

It is recommended that a 4.7µF to 10µF X5R/X7R or equivalent ceramic input capacitor is used.

Overvoltage Protection (OVP)

The integrated OVP circuit monitors the boost output voltage, V_{OUT}, and keeps the voltage at a safe level. The OVP threshold is set as Equation 9:

$$V_{OVP}(min) = 1.22V \times \frac{R1 + R2}{R2} \quad \text{(EQ. 9)}$$

Where:

- 1.22V is the intended bandgap voltage by design
- V_{OVP} is the maximum boost output voltage, V_{OUT} (V)
- R1 is the resistor from OVP pin to the boost output (Ω)
- R2 is the resistor from OVP pin to GND (WΩ).

The total R1 plus R2 series resistance should be high to minimize power loss through the resistor network.

For example, choosing R1 = 470kΩ and R2 = 23.7kΩ per the Typical Application Circuits on page 3 and Block Diagrams on page 5. Set V_{OVP}(typ) to 25.41V (Equation 10).

$$V_{OVP}(typ) = 1.22V \times \frac{470 + 23.7}{23.7} = 25.41V \quad \text{(EQ. 10)}$$

The OVP threshold, R1, and R2 tolerances should also be taken into account (Equations 11 and 12).

$$V_{OVP}(min) = 1.18V \times \frac{R1min + R2max}{R2max} \quad \text{(EQ. 11)}$$

$$V_{OVP}(max) = 1.24V \times \frac{R1max + R2min}{R2min} \quad \text{(EQ. 12)}$$

Calculating V_{OVP} using the OVP threshold range (1.18V to 1.24V) and 0.1% resistor tolerances gives an actual V_{OVP} range of 24.53V to 25.88V for the 25.4V previous example (Equations 13 and 14).

$$V_{OVP}(min) = 1.18V \times \frac{(470 \times 0.999) + (23.7 \times 1.001)}{(23.7 \times 1.001)} = 24.53V \quad \text{(EQ. 13)}$$

$$V_{OVP}(max) = 1.24V \times \frac{(470 \times 1.001) + (23.7 \times 0.999)}{(23.7 \times 0.999)} = 25.88V \quad \text{(EQ. 14)}$$

It is recommended that parallel capacitors are placed across the OVP resistors such that R1/R2 = C2/C1. Using a C1 value of at least 30pF is recommended. These capacitors reduce the AC impedance of the OVP node, which reduces noise susceptibility when using high value resistors.

Boost Output Voltage Range

The working range of the boost output voltage, V_{OUT} is from 40% to 100% of the maximum output voltage, V_{OVP}, set by resistors R1 and R2, as described in the previous section.

The target applications should be considered carefully to ensure that V_{OVP} is not set unnecessarily high. For example, using R = 470kΩ and R2 = 23.7kΩ per the "Typical Application Circuits" on page 3 sets V_{OVP} to between 24.53V to 25.88V when tolerances are considered.

The minimum voltage, V_{OVP}(min) = 24.53V, sets the maximum number of LEDs per channel because this is the worst case minimum voltage that the boost converter is guaranteed to supply.

The maximum voltage, V_{OVP}(max) = 25.88V, sets the minimum number of LEDs per channel because it sets the lowest voltage that the boost converter is guaranteed to reach:
40% x 25.88V = 10.35V.

Using LEDs with a V_F tolerance of 3V to 4V, this V_{OVP} example is suitable for strings of 4 to 6 LEDs. If fewer than 4 LEDs per channel are specified, V_{OVP} must be reduced.

Switching Frequency

The boost switching frequency is adjusted by resistor R_{FSW} (Equation 15):

$$f_{SW} = \frac{(8.65 \times 10^{10})}{R_{FSW}} \quad \text{(EQ. 15)}$$

Where:

- $8.65x10^{10}$ is determined by design
- f_{SW} is the desirable boost switching frequency (Hz)
- R_{FSW} is resistor from FSW pin to GND (Ω)

Inductor

Choose the inductance according to Table 4:

TABLE 4. INDUCTOR SELECTION

BOOST FREQUENCY	INDUCTANCE (µH)
400kHz to 700kHz	10 to 15
700kHz to 1MHz	6.8 to 10
1MHz to 1.5MHz	4.7 to 8.2
1.5MHz	3.3 to 4.7

The inductor saturation current rating should be as provided by Equation 16:

$$I_L = \frac{1.35 \times V_{OUT} \times I_{LED}}{V_{IN}} \quad \text{(EQ. 16)}$$

Where:

- I_L is the minimum inductor saturation current rating (A)
- V_{OUT} is the maximum output voltage set by OVP (V)
- I_{LED} is the sum of the channel currents (A)
- V_{IN} is the minimum input voltage (V)

If the calculation produces a current rating higher than the 3.08A maximum boost switch current limit, then a 3A inductor current rating is adequate.

For example, for a system using 4 LED channels with 30mA per channel and a maximum output voltage (OVP) of 24.53V with an input supply of 2.7V minimum as shown by Equation 17:

$$I_L = \frac{1.35 \times 24.53 \times (4 \times 0.03)}{2.7} = 1.47A \quad \text{(EQ. 17)}$$

Output Capacitor

It is recommended that a two of 4.7µF X5R/X7R or equivalent ceramic output capacitor is used.

Schottky Diode

The Schottky diode should be rated for at least the same forward current as the inductor, and for a reverse voltage equal to at least the maximum output voltage, OVP.

Compensation

The ISL97692, ISL97693, ISL97694A are boost regulator uses a current mode control architecture with a standardized external compensation network connected to the COMP pin. The component values shown in the "Typical Application Circuits" on page 3, are ideal for most typical applications. The network comprises a series RC of 12kΩ and 15nF from COMP to GND.

Applications

Unused LED Channels

Connect unused LED channels to GND.

Dimming Mode Setting

TABLE 5. DIMMING MODE SETTING OF ISL97694A

DIMMING MODE	SCL	SDA /PWMI	FPWM
Direct PWM	GND	PWM	V_{IN}
Phase shift PWM	GND	PWM	Connect a resistor FPWM pin to GND
I^2C Control	SCL	SDA	Connect a resistor FPWM pin to GND

High Current Applications

Each channel of the ISL97692 supports 40mA continuous sink current. Each channel of the ISL97693, ISL97694A supports 30mA continuous sink current. For applications that need higher current, multiple channels can be ganged together (Tables 6 and 7).

TABLE 6. GANGED ISL97692 CHANNELS FOR HIGHER CURRENT

TOTAL CHANNELS	CHANNEL CURRENT	CHANNEL CONNECTIONS
4	40mA per channel	CH1, CH2, CH3, CH4
2	80mA per channel	{CH1 & CH2}, {CH3 & CH4}
1	160mA	{CH1 & CH2 & CH3 & CH4}

TABLE 7. GANGED ISL97693, ISL97694A CHANNELS FOR HIGHER CURRENT

TOTAL CHANNELS	CHANNEL CURRENT	CHANNEL CONNECTIONS
6	30mA per channel	CH1, CH2, CH3, CH4, CH5, CH6
3	60mA per channel	{CH1, CH2}, {CH3, CH4}, {CH5, CH6}
2	90mA per channel	{CH1, CH2, CH3}, {CH4, CH5, CH6}
1	180mA	{CH1, CH2, CH3, CH4, CH5, CH6}

Figure 31 shows CH1 and CH2 ganged for a high current application.

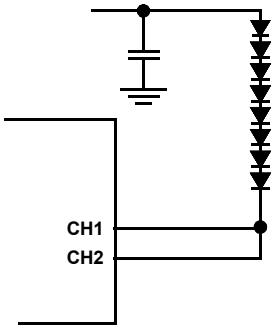


FIGURE 31.

PCB Layout Considerations

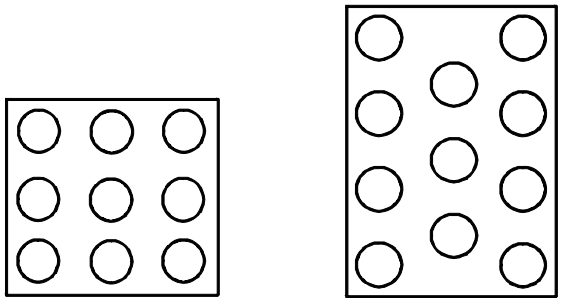
PCB Layout with TQFN and WLCSP Package

Figures 33 and 34 shows the example of the PCB layout of ISL97694A and ISL97692 WLCSP. This type of layout is particularly important for this type of product, resulting in high-current flow in the main loop's traces. Careful attention should be focused in the following layout details:

1. The typical application diagram (Figures 3, 4 and 5 on pages 3, and 4) the separation of PGND and AGND is essential, keeping the AGND referenced only local to the chip. This minimizes switching noise injection to the feedback sensing and analog areas, as well as eliminating DC errors form high-current flow in resistive PC board traces.
2. Boost input capacitors, output capacitors, inductor and Schottky diode should be placed together in a nice tight layout. Keeping the grounds of the input, and output connected with low impedance and wide metal is very important to keep these nodes closely coupled.
3. If possible, try to maintain central ground node on the board and use the input capacitors to avoid excessive input ripple for high output current supplies. The filtering capacitors should be placed close by the VIN pin.
4. Careful consideration should be taken with any traces carrying high di/dt pulsating signals. Traces carrying high di/dt pulsating signals should be kept as short and as tight as possible. The current loop generates a magnetic field which can couple to another conductor inducing unwanted voltage. Components should be placed such that current flows through them in a straight line as much as possible. This will help reduce size of loops and reduce the EMI from the PCB.
5. If trace lengths are long, the resistance of the trace increases and can cause some reduction in IC efficiency, and can also cause system instability. Traces carrying power should be made wide and short.
6. In discontinuous conduction mode, the direction of the current is interrupted every few cycles. This may result in large di/dt (transient load current). When injected in the ground plane the current may cause voltage drops, which can interfere with sensitive circuitry. The analog ground and power ground of the IC should be connected very close to the IC to mitigate this issue
7. For optimum load regulation and true V_{OUT} sensing, the OVP resistors should be connected independently to the top of the output capacitors and away from the higher dv/dt traces. The OVP connection then needs to be as short as possible to the pin. The AGND connection of the lower OVP components is critical for good regulation.
8. The COMP network and the rest of the analog components (on ISET, FPWM, FSW, etc.) should be reference to AGND.
9. The heat of the chip is mainly dissipated through the exposed thermal pad so maximizing the copper area around is a good idea. A solid ground is always helpful for the thermal and EMI performance.
10. The inductor and input and output capacitors should be mounted as tight as possible, to reduce the audible noise and inductive ringing.
11. For WLCSP, the solder pad on the PCB should not be larger than the solder mask opening for the ball pad on the package. The optimal solder joint strength, it is recommended a 1:1 ratio for the two pads. Generally, vias should not be used to route high-current paths.
12. The amount of copper that should be poured (thickness) depends upon the power requirement of the system. Insufficient copper will increase resistance of the PCB, which will increase heat dissipation.
13. While designing the layout of switched controllers, do not use the auto routing function of the PCB layout software. The auto routing connects the nets with same electrical name and does not account for ideal trace lengths and positioning.

General Power PAD Design Considerations

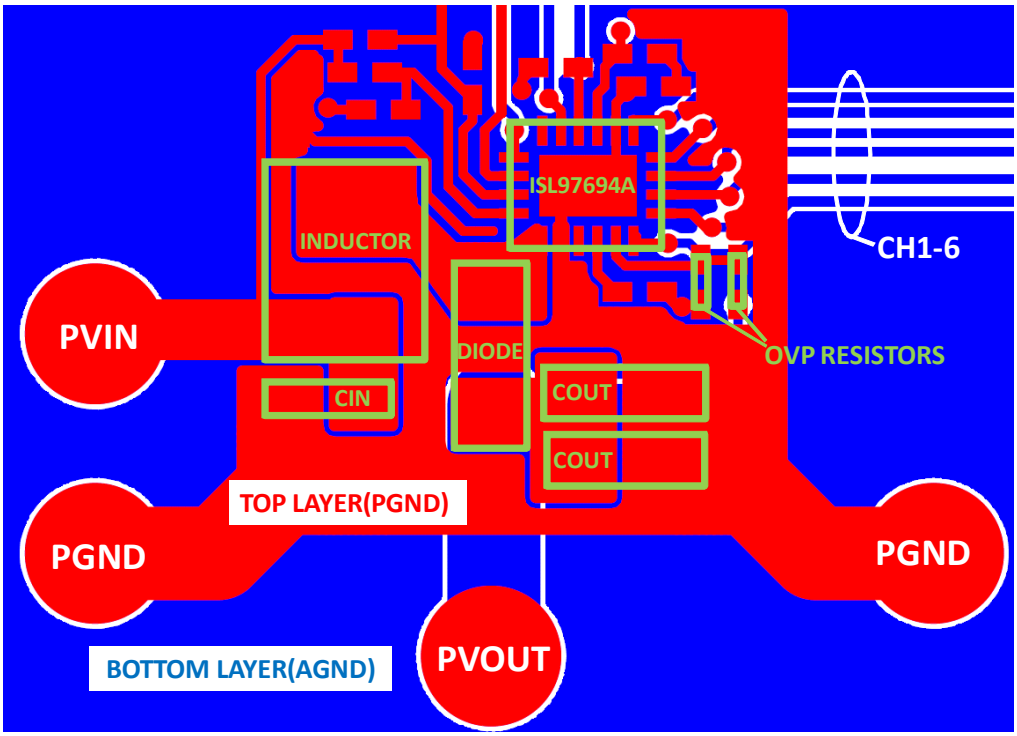
Figures 32 show an example of how to use vias to reduce the heat from the IC. For optimal thermal performance, use vias to distribute heat away from the IC and to a system power plane. Fill the thermal pad area with vias that are spaced 3x their radius (typically), center-to-center, from each other. The via diameters should be kept small, but they should be large enough to allow solder wicking during reflow. To optimize heat transfer efficiency, do not connect vias using "thermal relief" patterns. The vias should be directly connected to the plane with plated through-holes. Connect all vias to the correct voltage potential (power plane) indicated in the datasheet. For the ISL97692, ISL97693, ISL97694A, the thermal pad can be connected to ground (GND).



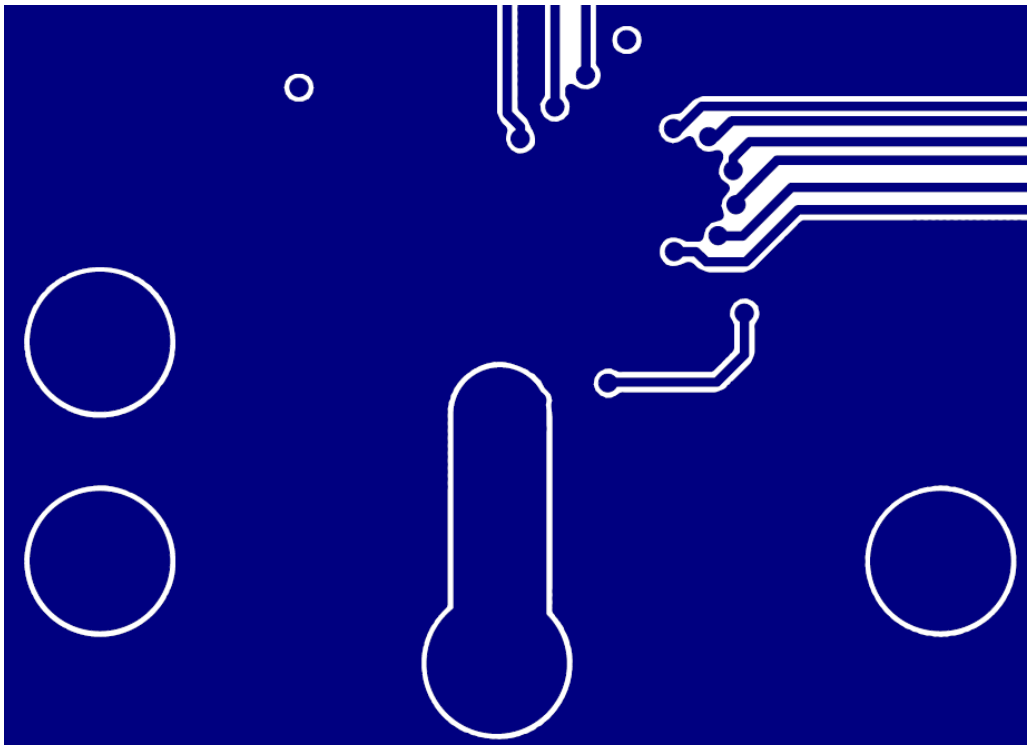
ISL97692, ISL97693 TQFN ISL97694A TQFN

FIGURE 32. VIA PATTERN

PCB Layout



TOP VIEW



BOTTOM VIEW

FIGURE 33. EXAMPLE OF PCB LAYOUT of ISL97694A

PCB Layout (Continued)

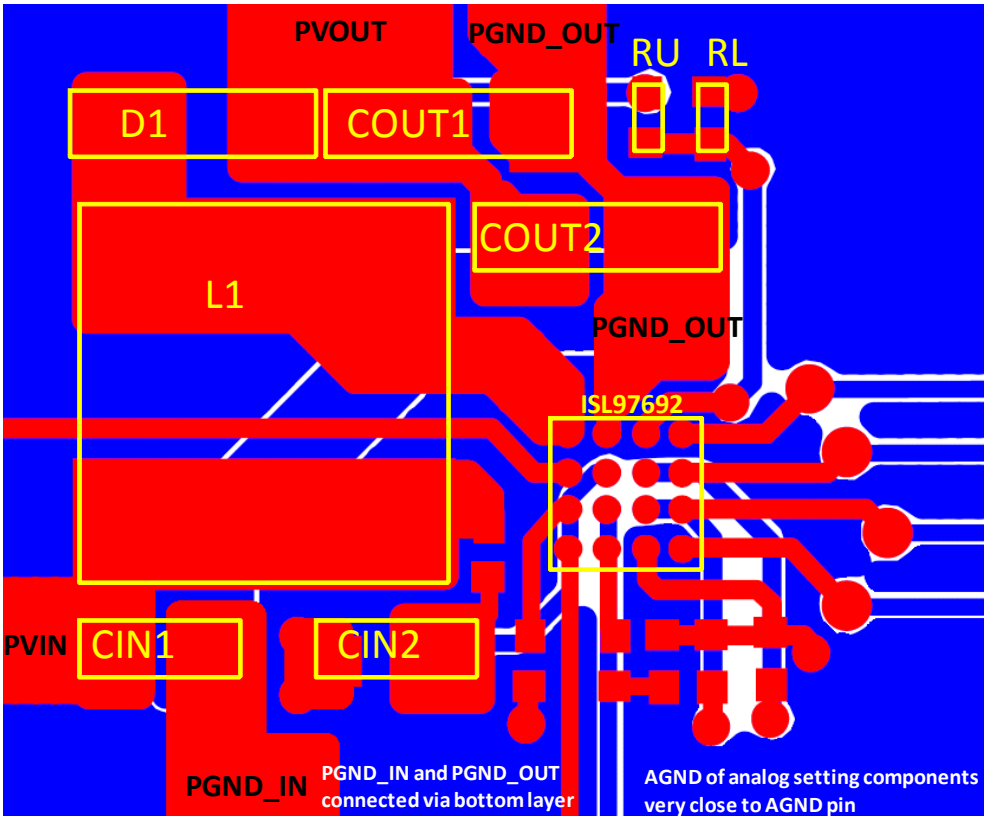


FIGURE 34. EXAMPLE OF PCB LAYOUT of ISL97692 WLCSP

Fault Protection and Monitoring

The ISL97692, ISL97693, ISL97694A features extensive protection functions to handle failure conditions automatically. Refer to Figure 35 and Table 8 for details of the fault protections.

The LED failure mode is either open or short circuit. An open circuit failure of an LED only results in the loss of one channel of LEDs without affecting other channels. Similarly, a short circuit condition on a channel that results in that channel being turned off does not affect other channels.

Due to the lag in boost response to any load change at its output, certain transient events (such as LED current steps or significant step changes in LED duty cycle) can transiently look like LED fault modes. The ISL97692, ISL97693, ISL97694A use feedback from the LEDs to determine when it is in a stable operating region and prevents apparent faults during these transient events from allowing any of the LED stacks to fault out. See Table 8 for more details.

Short Circuit Protection (SCP)

The short circuit detection circuit monitors the voltage on each channel and disables faulty channels, which are above the short circuit protection threshold, nominally 8V (the action taken is described in Table 8).

Open Circuit Protection (OCP)

When one of the LEDs becomes open circuit, it can behave as either an infinite resistance or a gradually increasing finite resistance. The ISL97692, ISL97693, ISL97694A monitors the current in each channel such that any string, which reaches the intended output current is considered “good”. Should the current subsequently fall below the target, the channel will be considered an “open circuit”. Furthermore, should the boost output of the ISL97692, ISL97693, ISL97694A reaches the V_{OVP} limit, all channels which are not “good” will immediately be considered as “open circuit”.

Detection of an “open circuit” channel will result in a time-out before disabling of the affected channel.

Overvoltage Protection (OVP)

The integrated OVP circuit monitors the boost output voltage, V_{OUT}, and keeps the voltage at a safe level. The OVP threshold is set as Equation 18:

$$OVP = 1.22V \times (R_{UPPER} + R_{LOWER}) / R_{LOWER} \quad \text{(EQ. 18)}$$

Where:

- 1.22V is the intended bandgap voltage by design
- V_{OVP} is the maximum boost output voltage, V_{OUT} (V)
- R_{UPPER} is resistor from OVP pin to the boost output (Ω)
- R_{LOWER} is resistor from OVP pin to GND (Ω)

Undervoltage Lockout

If the input voltage falls below the V_{UVLO} level of ~2V, the ISL97692, ISL97693, ISL97694A will stop switching and be reset. Operation will restart only if the V_{IN} is back in the normal operating range.

Over-Temperature Protection (OTP)

The ISL97692, ISL97693, ISL97694A have an over-temperature protection threshold set to +150°C. If this threshold is reached, the boost stops switching and the ISL97692, ISL97693, ISL97694A output current sinks are switched off. The ISL97692, ISL97693, ISL97694A can be restarted by toggling V_{IN} to below the V_{UVLO} level of ~2V, then back up to the normal input voltage level, or by power recycling V_{IN}.

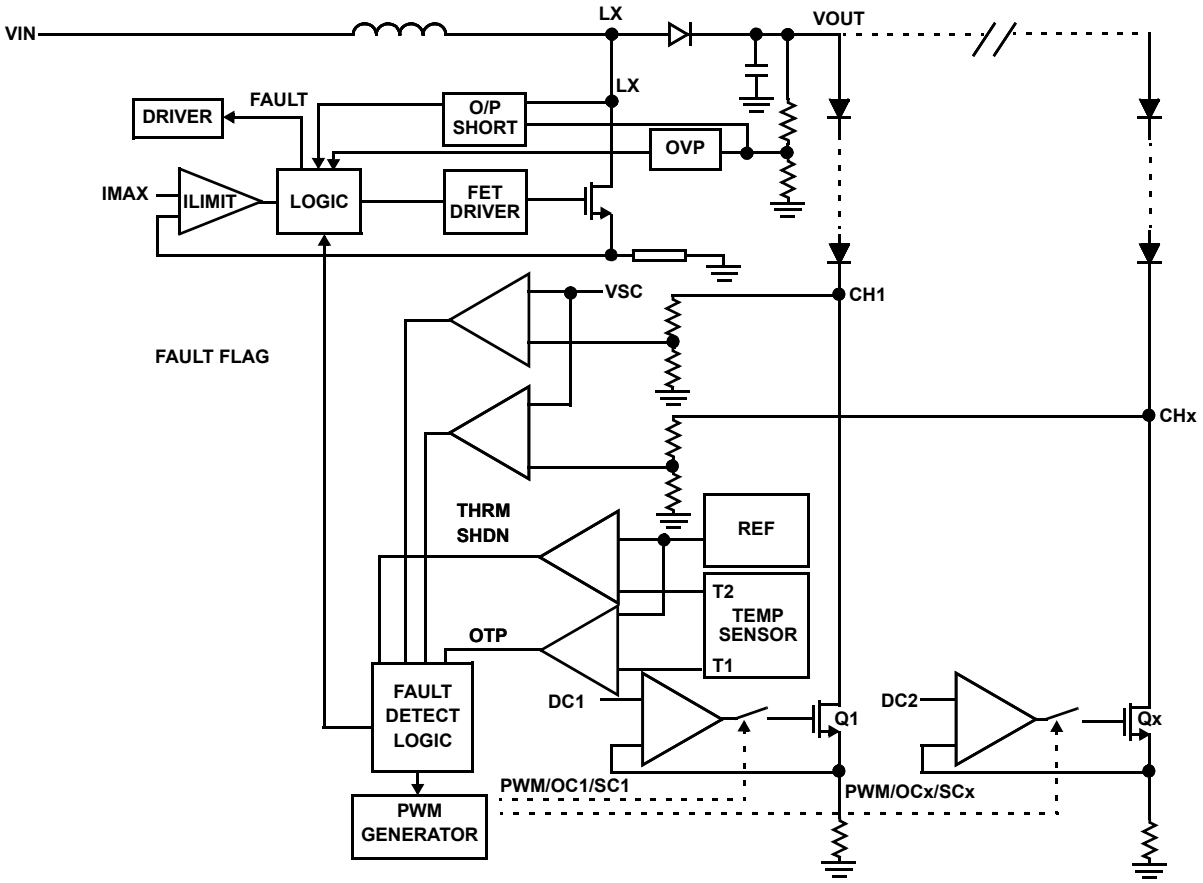


FIGURE 35. ISL97692, ISL97693, ISL97694A SIMPLIFIED FAULT PROTECTIONS

TABLE 8. ISL97692, ISL97693, ISL97694A PROTECTIONS TABLE

CASE	FAILURE MODE	DETECTION MODE	FAILED CHANNEL ACTION	OTHER CHANNELS ACTION	V_{OUT} REGULATED BY
1	CH1 Short Circuit	Upper Over-Temperature Protection limit (OTP) not triggered and CH1 < 8V	CH1 ON and burns power.	Normal Operation	Highest LED string V_F of other channels
2	CH1 Short Circuit	OTP triggered	Boost converter and channels are shut down until V_{IN} is cycled		-
3	CH1 Short Circuit	OTP not triggered, CH1 > 8V	CH1 disabled after 6 PWM cycle time-out	Normal Operation	Highest LED string V_F of other channels
4	CH1 Open Circuit with infinite resistance	OTP not triggered, CH1 < 8V	V_{OUT} will ramp to OVP. CH1 will time-out after 6 PWM cycles and switch off. V_{OUT} will then reduce to normal level	Normal Operation	Highest LED string V_F of other channels
5	Output LED stack voltage too high	$V_{OUT} = V_{OVP}$	Any channel that is below the target current will time-out after 6 PWM cycles while V_{OUT} is regulated at V_{OVP}, and V_{OUT} will then return to the normal regulation voltage required for other channels		Highest LED string V_F of channels above target current

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the website to make sure that you have the latest revision.

DATE	REVISION	CHANGE
September 8, 2017	FN7839.6	Applied new header/footer. Updated Related Literature on page 1. Updated Ordering Information table and notes. Added $V_{HEADROOM\_RANGE}$ spec to Electrical Specifications table. Added corresponding Note 14. In the Current Matching and Current Accuracy section - updated 2nd sentence in paragraph 2 for clarification. Updated About Intersil section.
May 1, 2014	FN7839.5	Electrical Spec table under“Boost FET Current Limit for CSP” on page 11: Changed the Min from 1.20 to 1.2A and Typ from 1.6 to 1.6A, removed the Max 2.0 value.
November 27, 2013		Electrical spec table on page 12 under F_{PWMI}: Added 8- bit, 10-bit and 12-bit dimming resolution. Electrical spec table on page 12 under PWM_{ACC} frequency output resolution: Added ISL97694A with frequency range 10-bit and 12-bit. Updated Equation 7 on page 17: From $58.1x10^6$ to R0 and added R0 for 10-bit and 12-bit of ISL97694A.
November 6, 2013		- Updated Equation 6 on page 16: From 350ns to 80ns and the effective resolution at 200Hz from 13.50 bits to 15.9 bits
October 28, 2013		Ordering information table on page 10: Changed part marking for Part number ISL97692IIZ-T from TBD to 7692. Electrical Spec Table on “BOOST SWITCHING REGULATOR” on page 11: Added “Boost FET Current Limit for CSP”.
September 19, 2013		- Added ISL97692 WLCSP to pin description, pin configuration, package diagram. - Replaced “Operating Conditions” to “Recommended Operating Conditions” on page 11. - Added part number ISL97692IIZ-T and ISL97693IRT-EVZ to Ordering information on page 10. - Added Maximum Average Current into LX pin for WLCSP in Absolute Maximum Ratings on page 11. - Added Boost FET current limit for WLCSP on page 11. - Added LED max current for WLCSP on page 12. - Updated Equation 6 on page 16. - Thermal Information table on page 11: Added 16 Bump WLSCP to thermal resistance and thermal characterization sections. - PCB layout considerations updated on page 23. - Example of WLCSP PCB layout added in Figure 35 on page 26. - Added POD W4x4.16B “16 Ball Wafer Level Chip Scale Package (WLCSP)” to data sheet.
November 30, 2012	FN7839.4	Changed HBM from 2kV to 2.5kV.
September 7, 2012	FN7839.3	Changed CDM from 1kV to 2kV.
June 28, 2012	FN7839.2	- Modified title on page 1 - IVIN typ lowered to 0.8mA - tENLow typ removed - Added “Operation with Input Voltage Greater than 5.5V” on page 18. - Updated Figure 20 - Added Figure 26, “LED DRIVER OPERATION WITH INPUT VOLTAGE UP TO 26V,” on page 19. -Removed “Coming Soon” from ISL97694A parts in “Ordering Information” on page 10.
May 25, 2012	FN7839.1	Corrected LX pin connection in Figures 1, 3, 4 and 5. Moved tie point in between L1 and D1. Changed Title in Figure 12 from “Accuracy vs WPM Dimming” to “Channel Matching Accuracy” Revised Figures 9 and 10.
April 16, 2012	FN7839.0	Initial release.

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing, and high-end consumer markets.

For the most updated datasheet, application notes, related documentation, and related parts, see the respective product information page found at www.intersil.com.

For a listing of definitions and abbreviations of common terms used in our documents, visit www.intersil.com/glossary.

You can report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support.

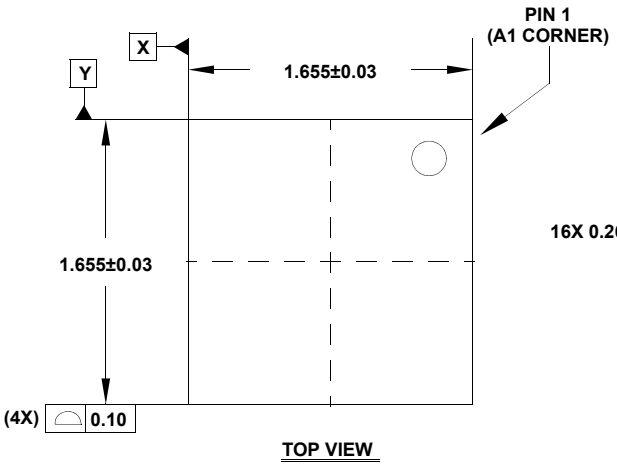
Package Outline Drawing

For the most recent package outline drawing, see W4x4.16B.

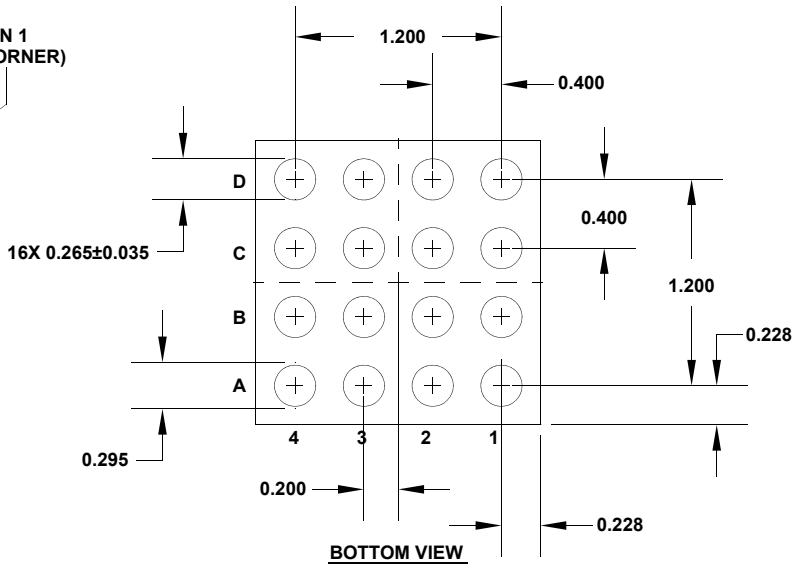
W4x4.16B

4x4 ARRAY 16 BALL WAFER LEVEL CHIP SCALE PACKAGE (WLCSP)

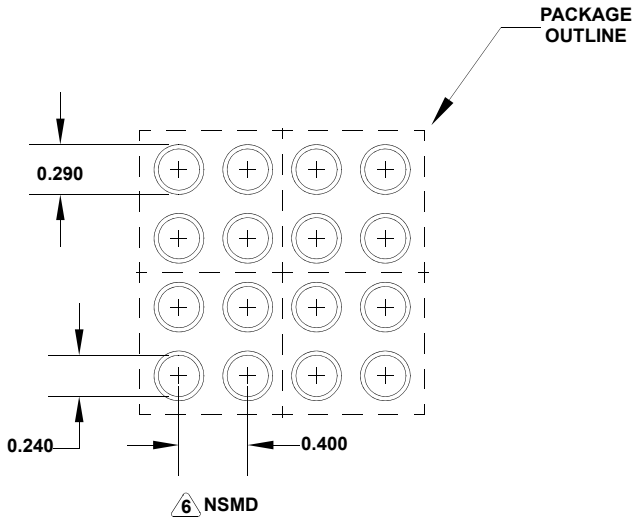
Rev 2, 8/13



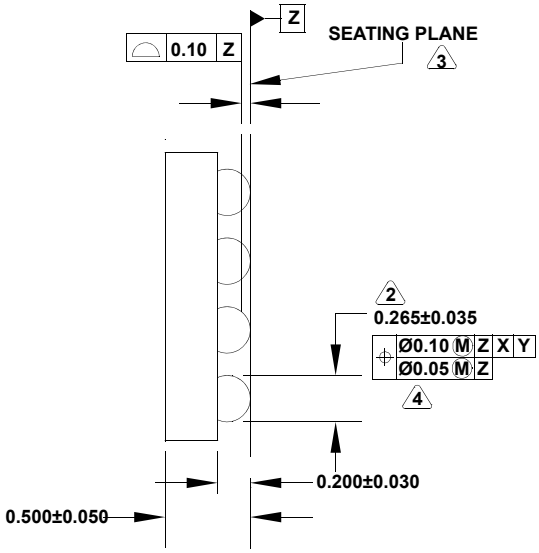
TOP VIEW



BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW

NOTES:

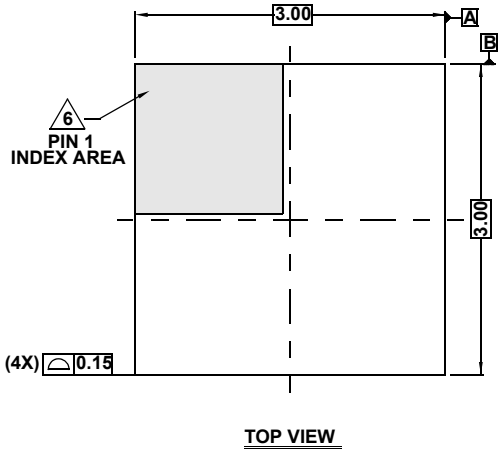
1. Dimensions and tolerance and tolerance per ASMEY 14.5 - 1994.
2. Dimension is measured at the maximum bump diameter parallel to primary datum Z.
3. Primary datum Z and seating plane are defined by the spherical crowns of the bump.
4. Bump position designation per JESD 95-1, SPP-010.
5. All dimensions are in millimeters.
6. NSMD refers to non-solder mask defined pad design per Intersil Techbrief www.intersil.com/data/tb/tb451.pdf

Package Outline Drawing

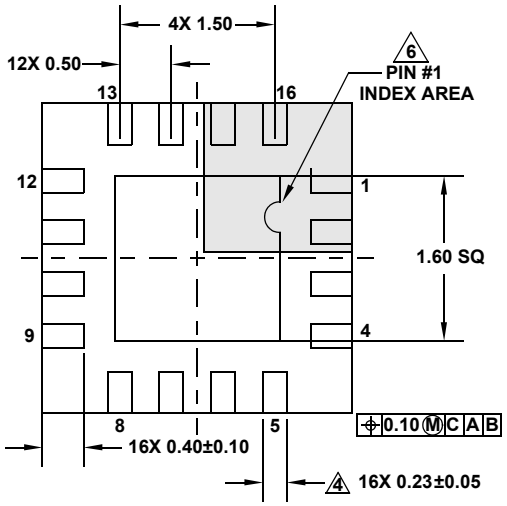
For the most recent package outline drawing, see L16.3x3D.

L16.3x3D

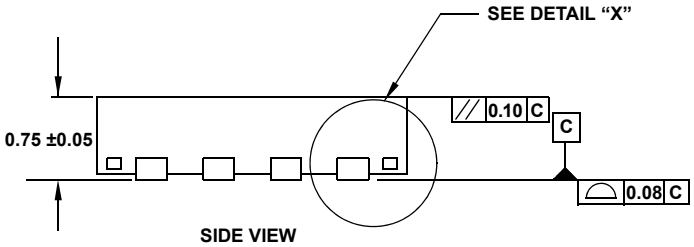
16 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 0, 3/10



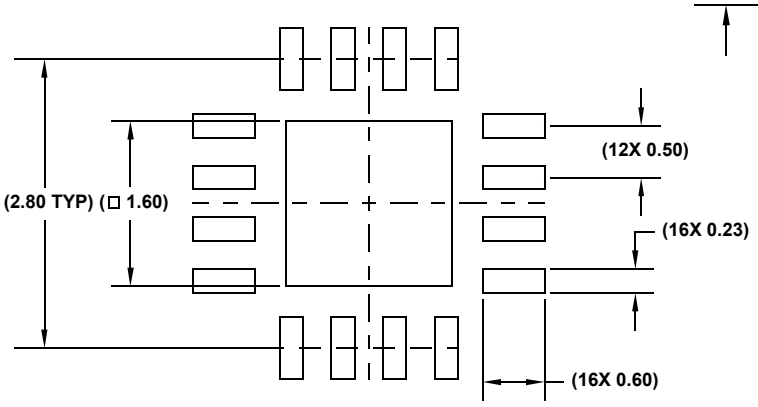
TOP VIEW



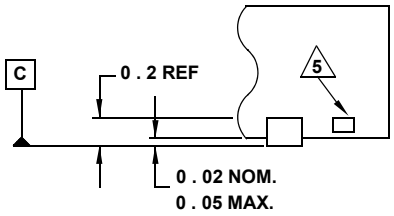
BOTTOM VIEW



SIDE VIEW



TYPICAL RECOMMENDED LAND PATTERN



DETAIL "X"

NOTES:

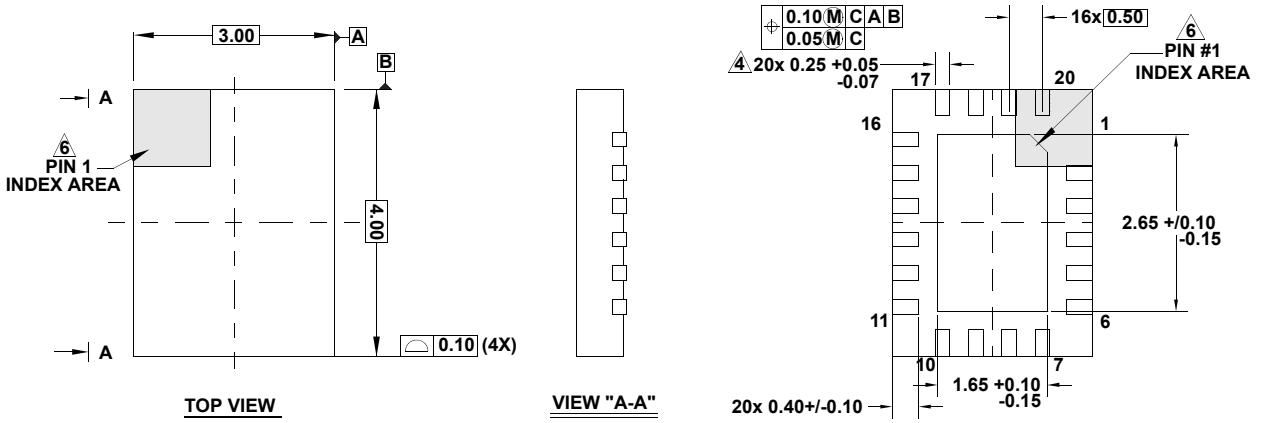
1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.25mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. JEDEC reference drawing: MO-220 WEED.

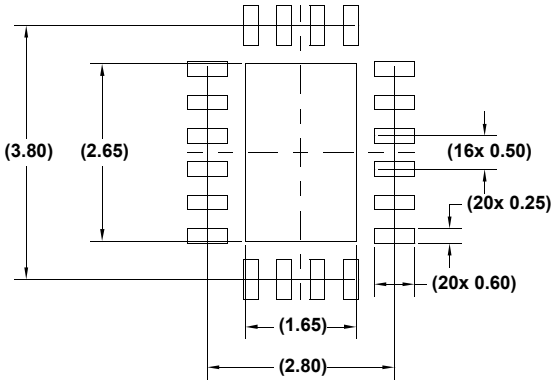
Package Outline Drawing

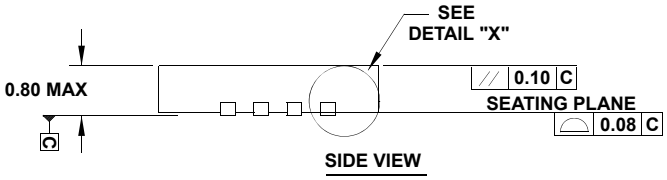
For the most recent package outline drawing, see L20.3x4A.

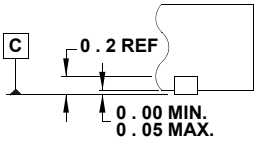
L20.3x4A

20 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 0, 6/10









NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. JEDEC reference drawing: MO-220VEGD-NJI.