0.6 GHz to 3.0 GHz, 0.5 dB LSB, 6-Bit, Silicon Digital Step Attenuator

Data Sheet **HMC8073**

FEATURES

- Attenuation range: 0.5 dB LSB steps to 31.5 dB
- Low insertion loss
  - 1.1 dB to 1.0 GHz
  - 1.5 dB to 2.0 GHz
- Tight attenuation accuracy
  - Less than ±0.25 dB (plus 3% of attenuation state)
- Low phase shift error: 4° phase shift to 1.0 GHz
- Bidirectional use: 30 dBm high power handling
- Internal dc block on the RFIN/RFOUT pins
- High linearity
  - P1dB: 31 dBm typical
  - Input IP3: 52 dBm typical
- Safe state transitions
- Serial interface with TTL/CMOS
  - Up to 8 devices on a single data bus
- Single-supply operation: 3.3 V to 5.0 V
- ESD sensitivity rating: Class 1C (1 kV human body model)
- 16-lead, 3 mm × 3 mm LFCSP package: 9 mm²

APPLICATIONS

- Cellular infrastructure
- Microwave radios
- Very small aperture terminals
- Test equipment and sensors

FUNCTIONAL BLOCK DIAGRAM

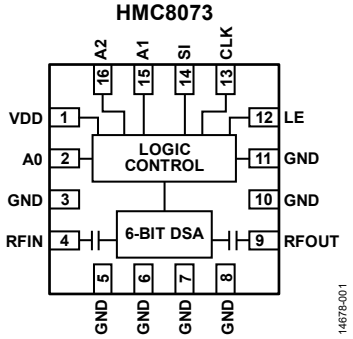

Figure 1.

GENERAL DESCRIPTION

The HMC8073 is a 6-bit digital step attenuator (DSA), operating from 0.6 GHz to 3.0 GHz, that features 31.5 dB of attenuation range with 0.5 dB steps.

The HMC8073 is implemented in a silicon process, offering a fast settling time, low power consumption, and high electrostatic discharge (ESD) robustness. The device features safe state transitions, allowing attenuation state changes without overshooting, and is optimized for excellent step accuracy and high power and high linearity over frequency and temperature range. The radio frequency (RF) input and output are internally matched to 50 Ω and do not require any external matching components. The design is bidirectional, and the RF input and output are interchangeable.

The external address feature of the HMC8073 allows users to control up to eight DSAs using a single bus. The DSA has an on-chip regulator that supports a wide supply operating range from 3.3 V to 5.0 V with no performance change in electrical characteristics. The HMC8073 incorporates a complementary metal-oxide semiconductor (CMOS)- and transistor transitory logic (TTL)- compatible interface that supports serial (3-wire) control of the attenuator.

The HMC8073 comes in an RoHS compliant, compact, 3 mm × 3 mm LFCSP package.

Rev. B

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REVISION HISTORY

4/2020—Rev. A to Rev. B

Changes to Figure 1 ... 1
Changes to Figure 3 and Table 5 ... 6
Change to Figure 25 ... 12

4/2018—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

V_{DD} = 5.0 V, T_A = 25°C, 50 Ω system, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE		0.6		3.0	GHz
INSERTION LOSS	0.6 GHz to 1.0 GHz		1.1		dB
	1.0 GHz to 2.0 GHz		1.5		dB
	2.0 GHz to 3.0 GHz		2.2		dB
ATTENUATION	0.6 GHz to 3.0 GHz				
Range	Delta between minimum and maximum attenuation states		31.5		dB
Step Size, LSB	Between any successive attenuation states		0.5		dB
Accuracy	Referenced to insertion loss; all attenuation states	−(0.25 + 3% of attenuation state)		+(0.25 + 3% of attenuation state)	dB
Step Error	All attenuation states		±0.4		dB
RETURN LOSS	All attenuation states				
RFIN, RFOUT	0.6 GHz to 1.0 GHz		14		dBm
	1.0 GHz to 2.0 GHz		12		dBm
	2.0 GHz to 3.0 GHz		9		dBm
RELATIVE PHASE	0.6 GHz to 1.0 GHz		4		Degrees
	1.0 GHz to 2.0 GHz		14		Degrees
	2.0 GHz to 3.0 GHz		38		Degrees
SWITCHING CHARACTERISTICS					
Rise and Fall Time (t_{RISE}, t_{FALL})	10% to 90% of RF output		65		ns
On and Off Time (t_{ON}, t_{OFF})	50% V_{CTL} to 90% of RF output		260		ns
INPUT LINEARITY	All attenuation states				
0.1 dB Compression (P0.1dB)			28		dBm
1 dB Compression (P1dB)			31		dBm
Input Third-Order Intercept (IP3)	Two-tone input power = 16 dBm/tone, Δf = 1 MHz		52		dBm
SUPPLY CURRENT (I_{DD})	V_{DD} = 3.3 V		0.3		mA
	V_{DD} = 5.0 V		0.3		mA
CONTROL VOLTAGE THRESHOLD, V_{CTL}	For CLK, LE, SI, A0, A1, A2; <1 µA typical				
Low, V_{IL}	V_{DD} = 3.3 V	0		0.8	V
	V_{DD} = 5.0 V	0		0.8	V
High, V_{IH}	V_{DD} = 3.3 V	2		3.3	V
	V_{DD} = 5.0 V	2		5.0	V
RECOMMENDED OPERATING CONDITIONS					
Supply Voltage Range (V_{DD})		3.3		5.0	V
Digital Control Voltage Range	For CLK, LE, SI, A0, A1, A2	0		V_{DD}	V
Maximum RF Input Power	Worst case at maximum attenuation			30	dBm
Case Temperature (T_{CASE})		−40		+85	°C

TIMING SPECIFICATIONS

Table 2.

Parameter	Description	Min	Typ	Max	Unit
t_1	CLK period	5			ns
t_2	CLK high	2.5			ns
t_3	CLK low	2.5			ns
t_4	SI to CLK setup time	1.5			ns
t_5	CLK to SI hold time	1.5			ns
t_6	LE to CLK setup time	1.5			ns
t_7	CLK to LE hold time	1.5			ns
t_8	LE pulse width	2.5			ns

Timing Diagram

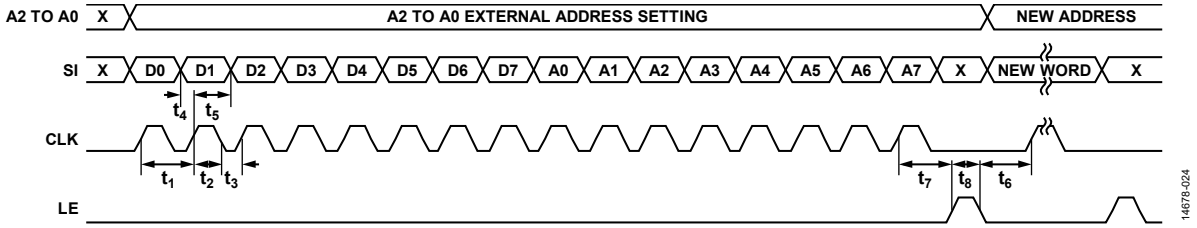

Figure 2. Serial Control Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
RF Input Power (T_{CASE} = 85°C)	30 dBm
Digital Control Inputs (CLK, LE, SI, A0, A1, A2)	−0.3 V to V_{DD} + 0.4 V
Supply Voltage (V_{DD})	5.4 V
Continuous Power Dissipation (P_{DISS})	0.999 W
Temperature	
Channel Temperature	140°C
Storage	−65°C to +150°C
Maximum Reflow Temperature	260°C (MSL3 Rating)
ESD Sensitivity	
Human Body Model (HBM)	1 kV (Class 1C)

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case bottom (channel to package bottom) thermal resistance.

Table 4. Thermal Resistance

Package Type	θ_{JC}	Unit
CP-16-38	55	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

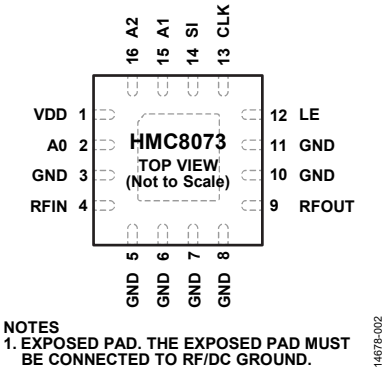

Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VDD	Supply Voltage Pin.
2, 15, 16	A0, A1, A2	Parallel Control Voltage Inputs. Apply V_{IH} or V_{IL} to attain the desired address for attenuator. See Figure 4 for the interface schematic.
3, 5 to 8, 10, 11	GND	Ground. The package bottom has an exposed metal pad that must connect to the PCB RF/dc ground. See Figure 5 for the GND interface schematic.
4	RFIN	Attenuator Input. This pin is ac-coupled and matched to 50 Ω. No external dc blocking capacitors are required on the RF lines. See Figure 6 for the interface schematic.
9	RFOUT	Attenuator Output. This pin is ac-coupled and matched to 50 Ω. No external dc blocking capacitors are required on the RF lines. See Figure 6 for the interface schematic.
12	LE	Serial Interface Latch Enable Input. See the Theory of Operation section for more information. See Figure 7 for the interface schematic.
13	CLK	Serial Interface Clock Input. See the Theory of Operation section for more information. See Figure 7 for the interface schematic.
14	SI	Serial Interface Data Input. See the Theory of Operation section for more information. See Figure 7 for the interface schematic.
	EPAD	Exposed Pad. The exposed pad must be connected to RF/dc ground.

INTERFACE SCHEMATICS

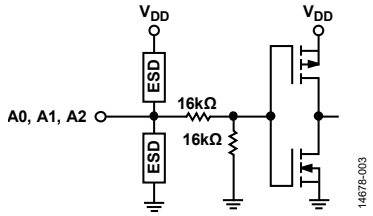

Figure 4. A0 to A2 Interface Schematic

Figure 5. GND Interface Schematic

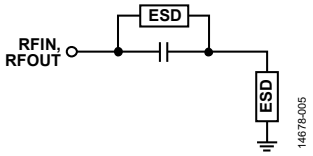

Figure 6. RFIN and RFOUT Interface Schematic

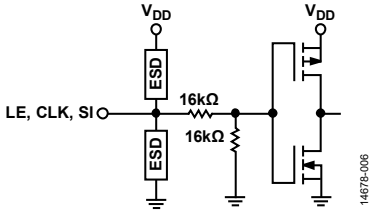

Figure 7. LE, CLK, and SI Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, STATE ERROR, NORMALIZED ATTENUATION, STEP ERROR, AND RELATIVE PHASE

V_{DD} = 5.0 V, T_A = 25°C, 50 Ω system, unless otherwise noted.

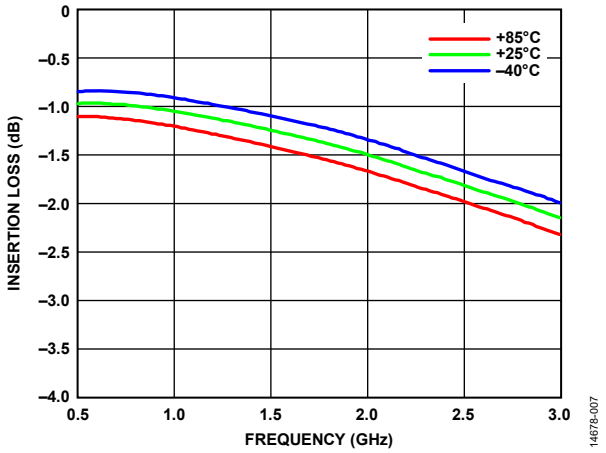

Figure 8. Insertion Loss vs. Frequency at Various Temperatures

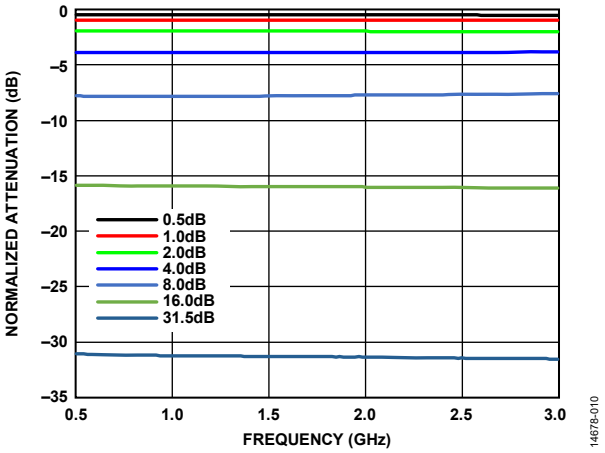

Figure 11. Normalized Attenuation vs. Frequency, Major States Only

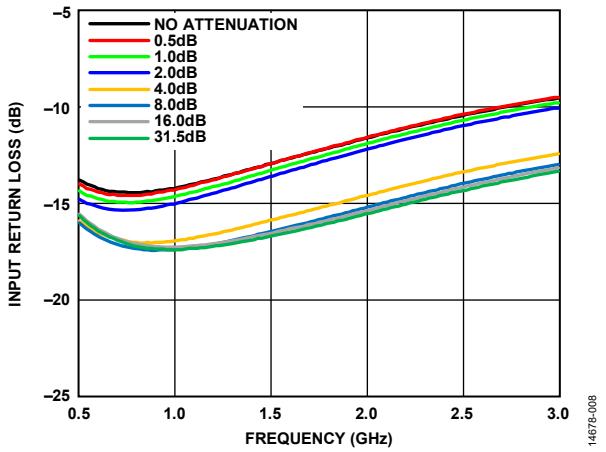

Figure 9. Input Return Loss vs. Frequency, Major States Only

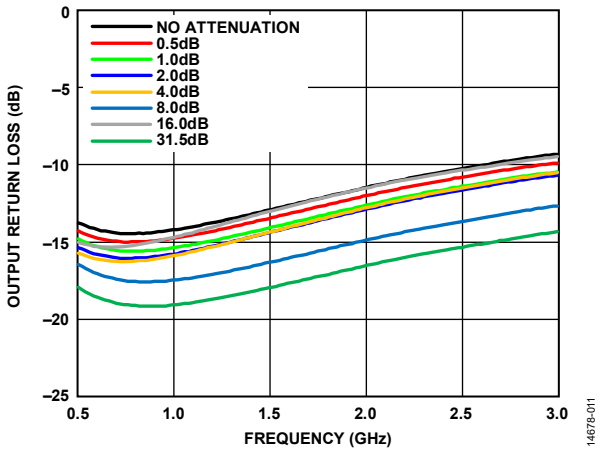

Figure 12. Output Return Loss vs. Frequency, Major States Only

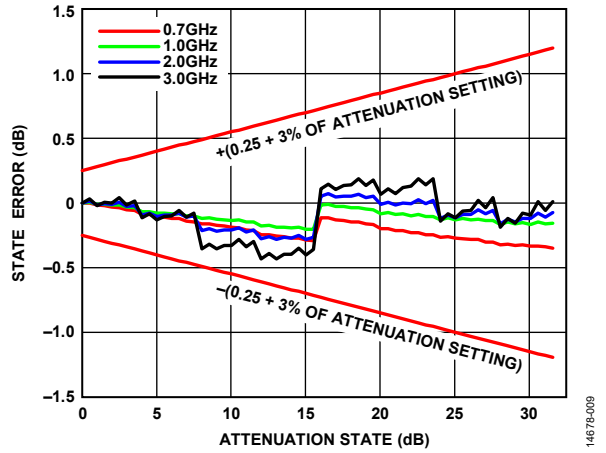

Figure 10. State Error vs. Attenuation State

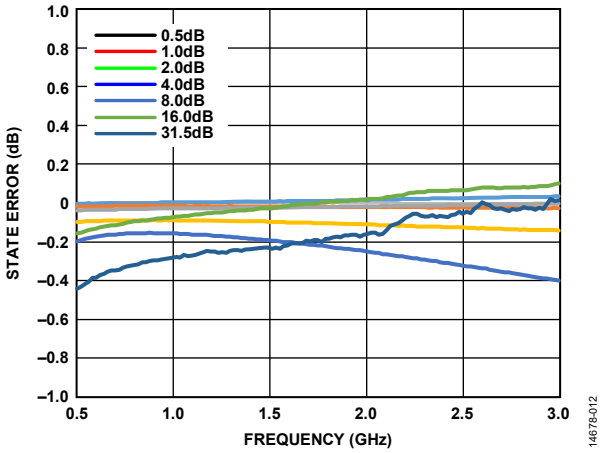

Figure 13. State Error vs. Frequency, Major States Only

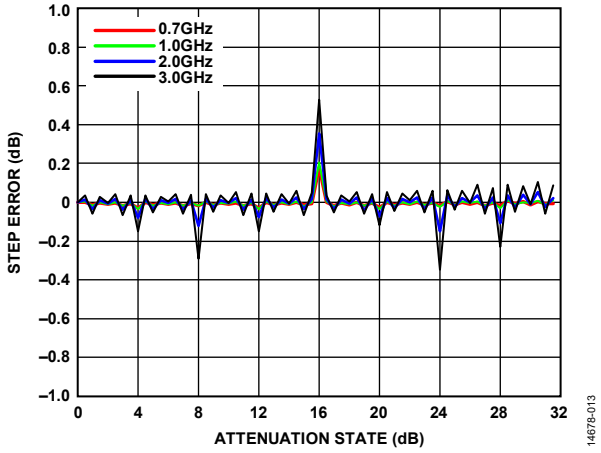

Figure 14. Step Error vs. Attenuation State

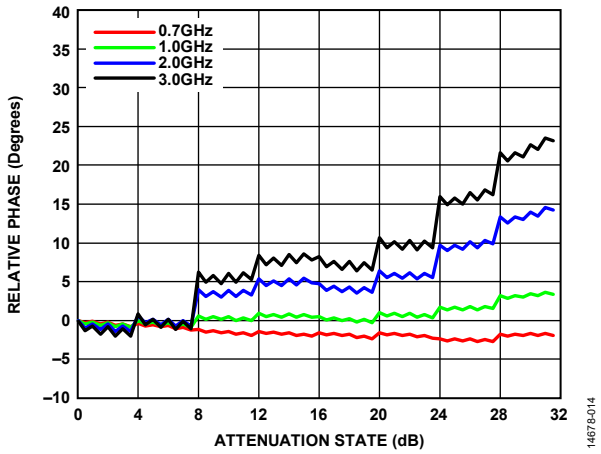

Figure 15. Relative Phase vs. Attenuation State

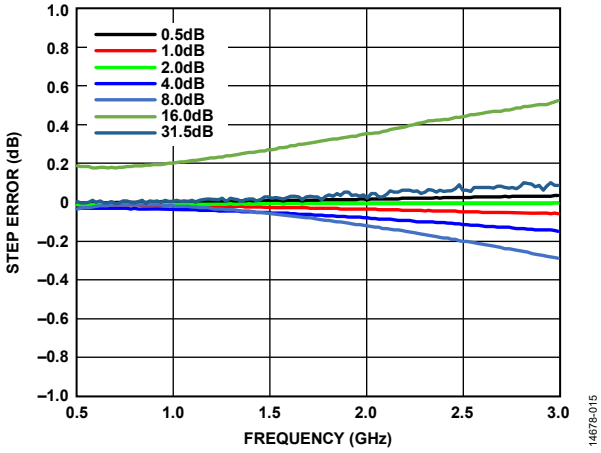

Figure 16. Step Error vs. Frequency, Major States Only

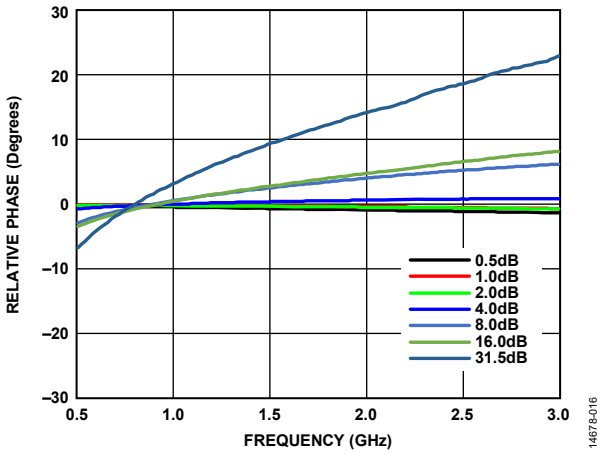

Figure 17. Relative Phase vs. Frequency, Major States Only

INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

V_{DD} = 5.0 V, T_A = 25°C, 50 Ω system, unless otherwise noted.

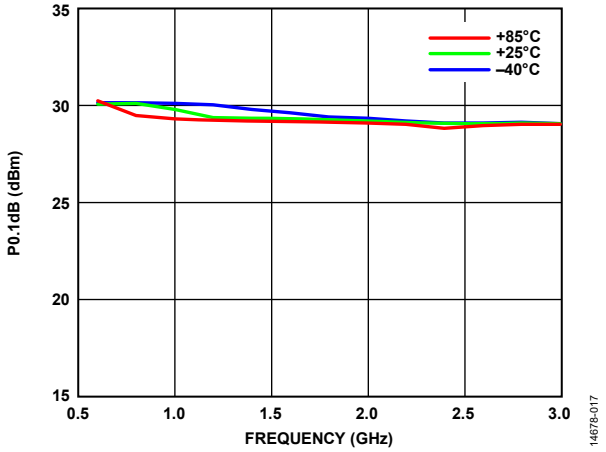

Figure 18. P0.1dB vs. Frequency at Various Temperatures, No Attenuation State

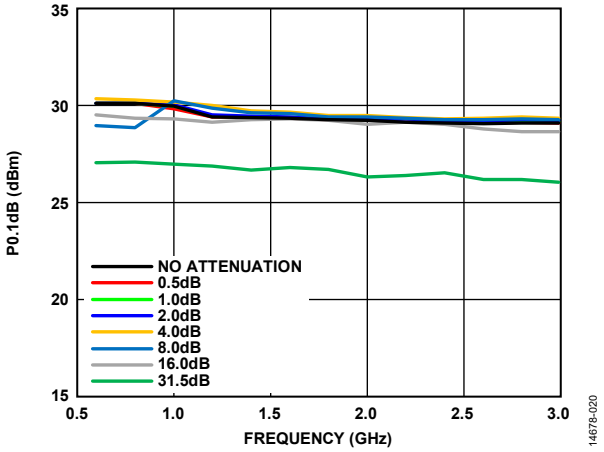

Figure 21. P0.1dB vs. Frequency, Major States Only

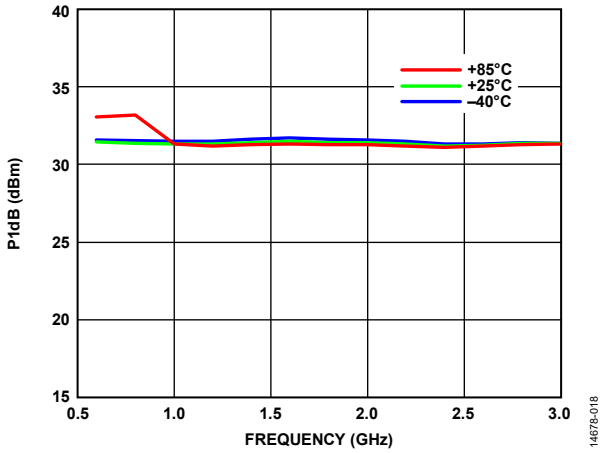

Figure 19. P1dB vs. Frequency at Various Temperatures, No Attenuation State

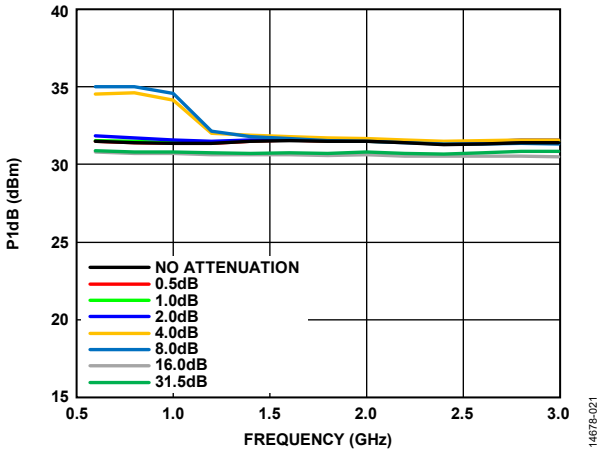

Figure 22. P1dB vs. Frequency, Major States Only

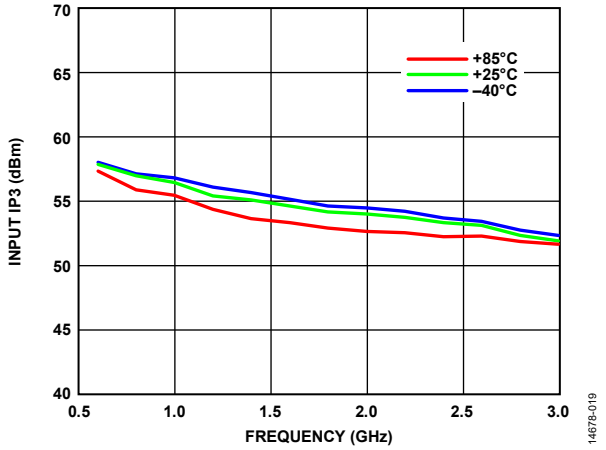

Figure 20. Input IP3 vs. Frequency at Various Temperatures, No Attenuation State

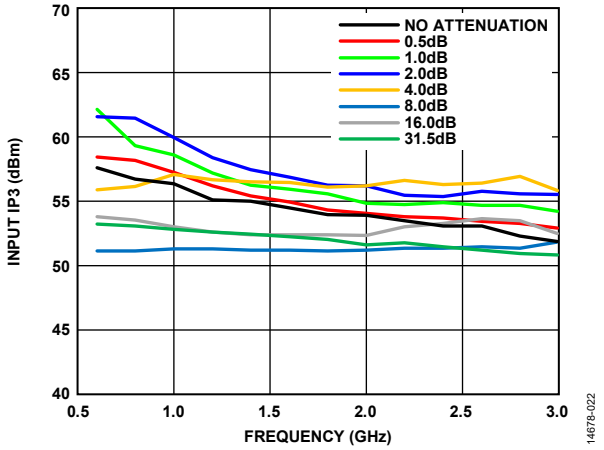

Figure 23. Input IP3 vs. Frequency, Major States Only

THEORY OF OPERATION

A simplified circuit diagram of the HMC8073 is shown in Figure 24. The HMC8073 incorporates a 6-bit fixed attenuator array that offers an attenuation range of 31.5 dB in 0.5 dB steps. An on-chip driver provides control of the attenuator from a 3-wire serial peripheral interface (SPI) and features 3-bit address pins (A0 to A2) to enable the control of up to eight devices on a single bus.

POWER-UP SEQUENCE

The HMC8073 requires a single dc voltage applied to the VDD pin. The ideal power-up sequence is as follows:

1. Connect the GND pin to a ground reference.
2. Apply a supply voltage to the VDD pin.
3. Power up the digital control inputs. The relative order of the digital control inputs is not important.
4. Apply an RF input signal to RFIN or RFOUT.

RF INPUT AND OUTPUT

The attenuator in the HMC8073 is bidirectional. The RFIN and RFOUT pins are interchangeable as the RF input and output ports. The attenuator is internally matched to 50 Ω at both the input and the output, and no external matching components are required. There are internal dc blocking capacitors on the RFIN and RFOUT pins, and no external dc blocking capacitors are required on the RF lines.

SERIAL CONTROL INTERFACE

The HMC8073 has a 3-wire SPI that consists of the serial data input (SI), the clock (CLK), and the latch enable (LE) pins. The serial control inputs are both TTL- and 5 V CMOS-compatible {fix space issue} and can easily interface to most industry-standard field programmable gate arrays (FPGAs) and microcontrollers.

As shown in Figure 24, the driver portion contains a 16-bit serial to parallel shift register, an 8-bit comparator, and an 8-bit latch.

The serial input data bits in LSB first format are clocked into the shift register on the rising edge of the clock signal. The latch enable signal must be kept low during data transmission. Otherwise, the clock signal is masked by a high latch enable with logical OR operation. When all 16 data bits are loaded, a high going latch enable pulse updates the attenuation state. Figure 2 and Table 2 provide the general signal requirements and the specific timing requirements, respectively, that must be met for the data transfer to be accomplished properly.

In a bit stream to serial data input, the first eight bits (D[7:0]) are designated as attenuation data, and the last eight bits (A[7:0]) are designated as address data. D[6:1] specifies the attenuation setting, whereas D0 and D7 are don't care bits and can be set low or high without affecting the attenuation state (see Table 7). Bits A[2:0] must be matched to the address setting by the A2 to A0 pins and A[7:3] must all be low so that D[6:1] can be latched into the attenuator bits when the latch enable signal is pulsed.

ATTENUATION STATE AT POWER-UP

The HMC8073 powers up at a maximum attenuation if the LE pin is kept low during the initial power-up. At initial power-up or immediately after the initial power-up, when the serial input data is not clocked to the device, and when the LE pin is set high while keeping the A2 to A0 pins low, the HMC8073 is latched into an insertion loss state due to the internal pull-down resistors at the shift register outputs. If the address set by the A2 to A0 pins is not equal to 000, the device stays at a maximum attenuation even with the high latch enabled.

Table 6. Attenuation State at Power-Up

Attenuation State	LE	Address Setting (A2, A1, A0 Pins)
31.5 dB (Maximum)	Low	Don't care
0 dB (Reference)	High	000
31.5 dB (Maximum)	High	≠ 000 (001, 010, 011, 100, 101, 110, 111)

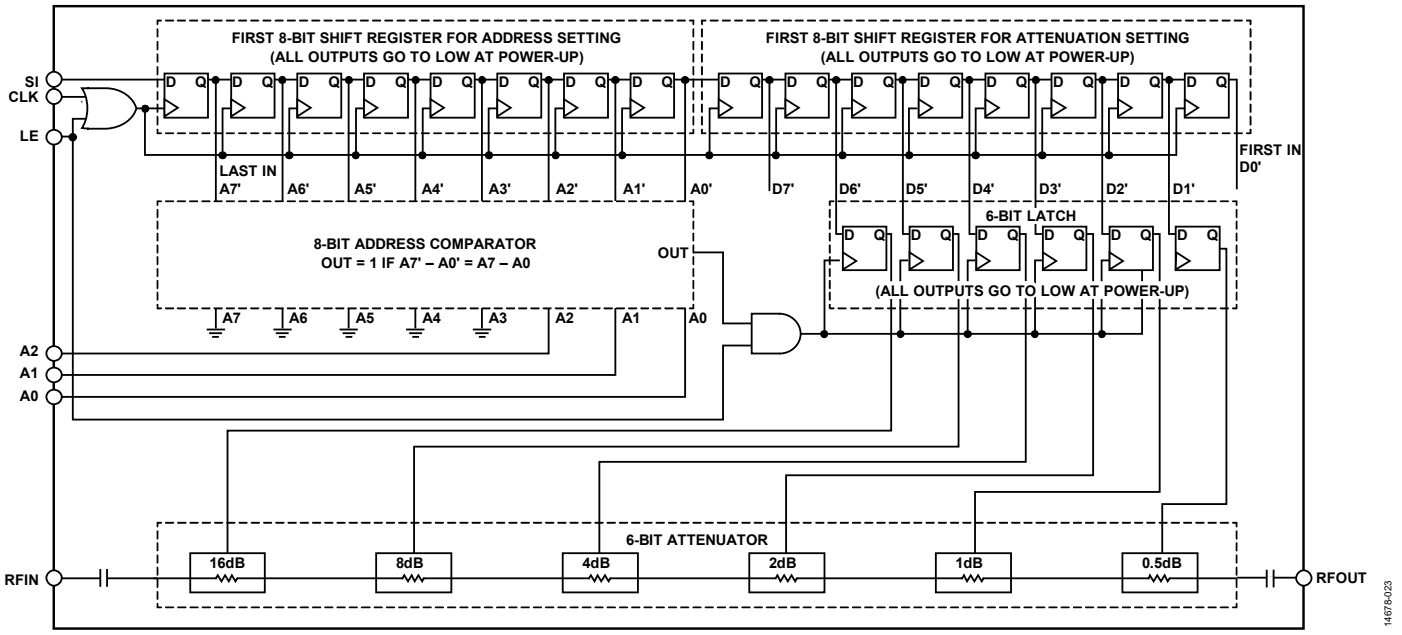

Figure 24. Simplified Circuit Diagram

Table 7. Attenuation Truth Table

Attenuation Control Input[1]								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Attenuation State (dB)**
Don't care	Low	Low	Low	Low	Low	Low	Don't care	0 (reference)
Don't care	Low	Low	Low	Low	Low	High	Don't care	0.5
Don't care	Low	Low	Low	Low	High	Low	Don't care	1.0
Don't care	Low	Low	Low	High	Low	Low	Don't care	2.0
Don't care	Low	Low	High	Low	Low	Low	Don't care	4.0
Don't care	Low	High	Low	Low	Low	Low	Don't care	8.0
Don't care	High	Low	Low	Low	Low	Low	Don't care	16.0
Don't care	High	High	High	High	High	High	Don't care	31.5

[1] Any combination of the control voltage input states shown in Figure 24 provides an attenuation equal to the sum of the bits selected.

Table 8. Address Truth Table

Address Control Input								
A7	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**	**Address Setting (A2, A1, A0 Pins)**
Low	Low	Low	Low	Low	Low	Low	Low	000
Low	Low	Low	Low	Low	Low	Low	High	001
Low	Low	Low	Low	Low	Low	High	Low	010
Low	Low	Low	Low	Low	Low	High	High	011
Low	Low	Low	Low	Low	High	Low	Low	100
Low	Low	Low	Low	Low	High	Low	High	101
Low	Low	Low	Low	Low	High	High	Low	110
Low	Low	Low	Low	Low	High	High	High	111

APPLICATIONS INFORMATION

EVALUATION PCB

The EV1HMC8073LP3D with component placement is shown in Figure 25. The EV1HMC8073LP3D is constructed of a 4-layer material with a copper thickness of 0.7 mil on each layer. Every copper layer is separated with a dielectric material. The top dielectric material is 10 mil RO4350. The middle and bottom dielectric material is FR-4, used for mechanical strength and overall board thickness of approximately 62 mil, which allows SMA connectors to be slipped in at the board edges.

All RF and dc traces are routed on the top copper layer. The RF transmission lines are designed using a coplanar waveguide (CPWG) model, with a width of 18 mil, spacing of 13 mil, and dielectric thickness of 10 mil, to have a characteristic impedance of 50 Ω. The inner and bottom layers are grounded planes that provide a solid ground for the RF transmission lines. For optimal electrical and thermal performance, as many vias as possible are arranged around the transmission lines and under the package exposed pad. The evaluation board layout shown in Figure 25 serves as a recommendation for optimal and stable performance as well as for improvement of thermal efficiency.

The EV1HMC8073LP3D is grounded from the dc test point, TP3. The dc supply must be connected to the dc test point, TP1, of the EV1HMC8073LP3D. The decoupling capacitors are populated on the supply trace to filter high frequency noise.

The RF input and output ports (RFIN and RFOUT) are connected through 50 Ω transmission lines to the SMA connectors, J1 and J2, respectively. All the digital control pins are connected through digital signal traces to the 2 × 6-pin header, J5. A thru calibration transmission line can estimate the loss of PCB over the environmental conditions being evaluated.

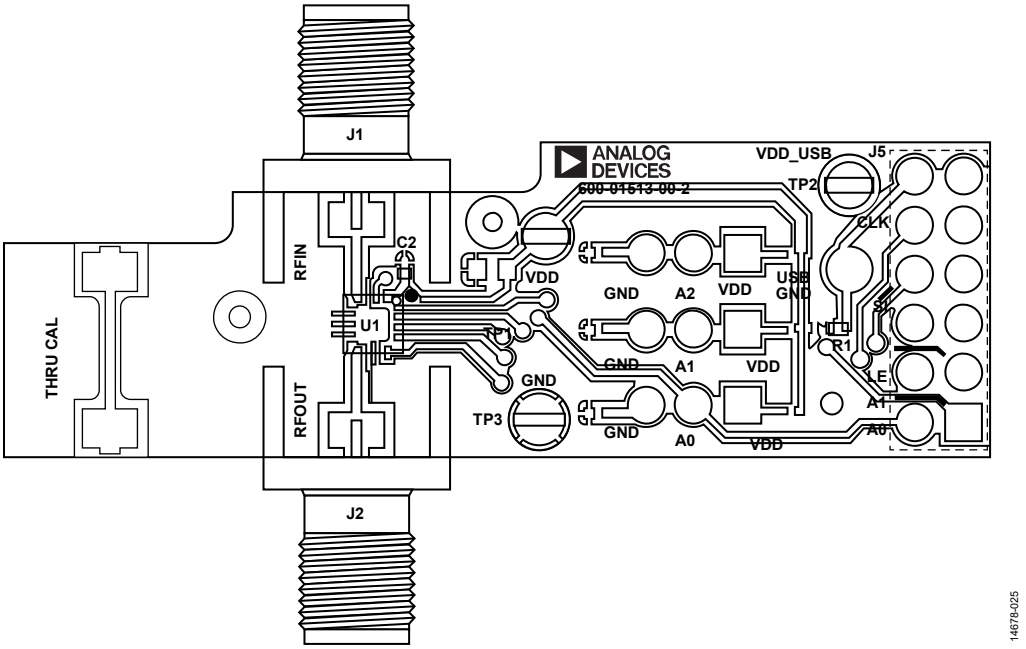

Figure 25. EV1HMC8073LP3D Evaluation PCB

Table 9. Bill of Materials for EV1HMC8073LP3D PCB

Item	Value[1]	Description	Manufacturer[2]
J1, J2		PCB mount SMA connectors	
J5		Socket strip, dual-row 2 × 6	
TP1 to TP3		Through hole mount test points	
C2	470 pF	Capacitor, 0402 package	
R1	0 Ω	Resistor, 0402 package	
U1		HMC8073 digital attenuator	Analog Devices, Inc.
PCB[3]		600-01513-00 evaluation PCB	EV1HMC8073LP3D[4] from Analog Devices

[1] Blank cells in the value column indicate that there is no specific value recommendation for the listed component.
[2] Blank cells in the manufacturer column indicate that there is no specific manufacturer recommendation for the listed component.
[3] Circuit board material is Arlon 25FR.
[4] Reference this number when ordering the full evaluation PCB. See the Ordering Guide section.

PACKAGING AND ORDERING INFORMATION

OUTLINE DIMENSIONS

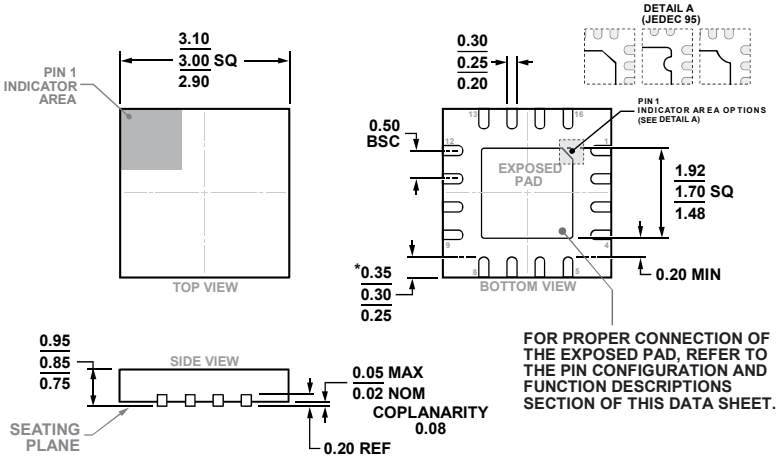

Figure 26. 16-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.85 mm Package Height
(CP-16-38)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	MSL Rating[2]	Package Description	Package Option
HMC8073LP3DE	−40°C to +85°C	MSL3	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-38
HMC8073LP3DETR	−40°C to +85°C	MSL3	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-38
EV1HMC8073LP3D			Evaluation Board	

[1] All models are RoHS compliant.
[2] See the Absolute Maximum Ratings section.