

## FEATURES

### Extreme high temperature operation

–40°C to +210°C, 8-lead FLATPACK

–40°C to +175°C, 8-lead SOIC

### Temperature coefficient

40 ppm/°C, 8-lead FLATPACK

10 ppm/°C, 8-lead SOIC

### High output current: 10 mA

### Low supply current: 50 µA maximum

### Initial accuracy: ±0.4% (±10 mV maximum), 8-lead SOIC

### Low dropout voltage

### Wide supply range: 3.3 V to 16 V

## APPLICATIONS

### Down-hole drilling and instrumentation

### Avionics

### Heavy industrial

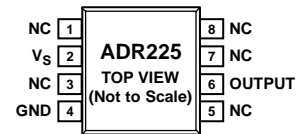
### High temperature environments

## GENERAL DESCRIPTION

The [ADR225](#) is a precision 2.5 V band gap voltage reference specified for a high temperature operation of 175°C and 210°C. It uses a micropower core topology and laser trimming of highly stable, thin film resistors to achieve a temperature coefficient of 30 ppm/°C (maximum) up to 175°C and an initial accuracy of 0.4% (±10 mV maximum). A maximum operating current of 50 µA and a low dropout voltage allow the [ADR225](#) to function very well in battery-powered equipment.

The [ADR225](#) voltage reference is offered in an 8-lead SOIC package with an operating temperature range of –40°C to +175°C.

## PIN CONFIGURATION



### NOTES

1. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.

11625-001

Figure 1. Pin Configuration for SOIC and FLATPACK Packages

It is also available in an 8-lead ceramic flat pack (FLATPACK) with an operating temperature range of –40°C to +210°C. Both devices are designed for robustness at extreme temperatures and are qualified for 1000 hours of operation at the maximum temperature rating.

The [ADR225](#) is a member of a growing series of high temperature qualified products offered by Analog Devices, Inc. For a complete selection table of the available high temperature products, see the high temperature product list and qualification data available at [www.analog.com/hightemp](http://www.analog.com/hightemp).

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**REVISION HISTORY**

**11/13—Rev. A to Rev. B**

Change to Features Section .....	1
Added Caption to Figure 1 .....	1
Changes to Table 1 .....	3
Added Figure 6, Figure 7, Figure 8, Figure 12, Figure 13, Figure 14, Figure 18, and Figure 19; Renumbered Sequentially .....	5

**9/13—Rev. 0 to Rev. A**

Changes to Data Sheet Title and Added Wide Supply Range: 3.3 V to 16 V to Features Section .....	1
Changed Supply Voltage from -0.3 V to +15 V to -0.3 V to +18 V; Table 2 .....	4

**7/13—Revision 0: Initial Version**

## SPECIFICATIONS

### ELECTRICAL CHARACTERISTICS

$V_S = 3.3\text{ V}$ ,  $V_{OUT} = 2.5\text{ V}$ ,  $T_{MIN} < T_A < T_{MAX}$ , unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	8-Lead SOIC -40°C ≤ T <sub>A</sub> ≤ +175°C			8-Lead FLATPACK -40°C ≤ T <sub>A</sub> ≤ +210°C			Unit
			Min	Typ	Max	Min	Typ	Max	
SUPPLY CURRENT	I <sub>SY</sub>	No load	30	50		40	60	μA	
INITIAL ACCURACY <sup>1</sup>	V <sub>O</sub>	I <sub>OUT</sub> = 0 mA	±2	±10		±5	±60	mV	
TEMPERATURE COEFFICIENT <sup>2</sup>	TCV <sub>OUT</sub>	I <sub>OUT</sub> = 0 mA	10	30		40	80	ppm/°C	
REGULATION									
Line Regulation	ΔV <sub>OUT</sub> /ΔV <sub>IN</sub>	3.0 V ≤ V <sub>S</sub> ≤ 15 V, I <sub>OUT</sub> = 0 mA	0.025	0.1		0.25	1.5	mV/V	
Load Regulation <sup>3</sup>	ΔV <sub>OUT</sub> /ΔV <sub>LOAD</sub>	V <sub>S</sub> = 5.0 V, 0 mA ≤ I <sub>OUT</sub> ≤ 10 mA	0.025	0.1		0.25	1.5	mV/mA	
VOLTAGE									
Dropout Voltage	V <sub>S</sub> - V <sub>OUT</sub>	I <sub>LOAD</sub> = 10 mA		1.00			1.00	V	
Noise Voltage	e <sub>N</sub>	0.1 Hz to 10 Hz	25			25		μV p-p	

<sup>1</sup> For proper operation, a 1 μF capacitor is required between the OUTPUT pin and the GND pin of the device.

<sup>2</sup> TCV<sub>OUT</sub> is defined as the ratio of output change with temperature variation to the specified temperature range expressed in ppm/°C.

$$TCV_{OUT} = (V_{MAX} - V_{MIN}) / V_{OUT}(T_{MAX} - T_{MIN})$$

<sup>3</sup> Load regulation specification includes the effect of self-heating.

## ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	-0.3 V to +18 V
OUTPUT to GND	-0.3 V to $V_s + 0.3$ V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
8-Lead SOIC	-40°C to +175°C
8-Lead FLATPACK	-40°C to +210°C
Junction Temperature Range	
8-Lead SOIC	-40°C to +200°C
8-Lead FLATPACK	-40°C to +245°C
Lead Temperature (Soldering 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### PREDICTED LIFETIME vs. OPERATING TEMPERATURE

Comprehensive reliability testing is performed on the [ADR225](#). Product lifetimes at extended operating temperature are obtained using high temperature operating life (HTOL). Lifetimes are predicted from the Arrhenius equation, taking into account potential design and manufacturing failure mechanism assumptions. HTOL is performed to JEDEC JESD22-A108. A minimum of three wafer fab and assembly lots are processed through HTOL at the maximum operating temperature. Comprehensive reliability testing is performed on all Analog Devices, Inc., high temperature (HT) products.

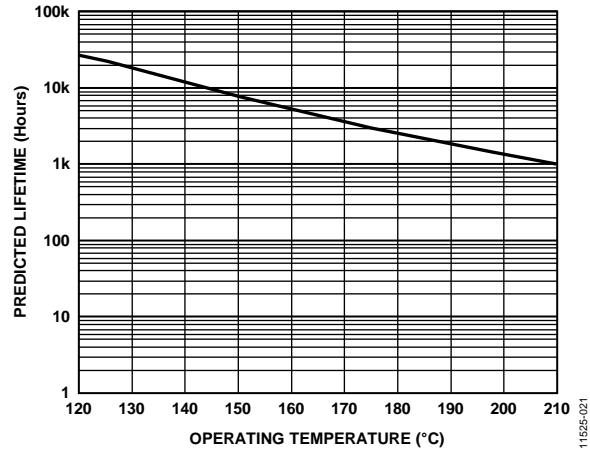


Figure 2. Predicted Lifetime vs. Operating Temperature

### THERMAL RESISTANCE

$\theta_{JA}$  is specified for worst-case conditions; that is,  $\theta_{JA}$  is specified for the device soldered in the circuit board.

Table 3.

Package Type	$\theta_{JA}$	$\theta_{JC}$	Unit
8-Lead SOIC	121	43	°C/W
8-Lead FLATPACK	100	15	°C/W

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# TYPICAL PERFORMANCE CHARACTERISTICS

$V_S = 3.3\text{ V}$ ,  $V_{OUT} = 2.5\text{ V}$ ,  $T_{MIN} \leq T_A \leq T_{MAX}$  for 8-lead SOIC package, unless otherwise noted.

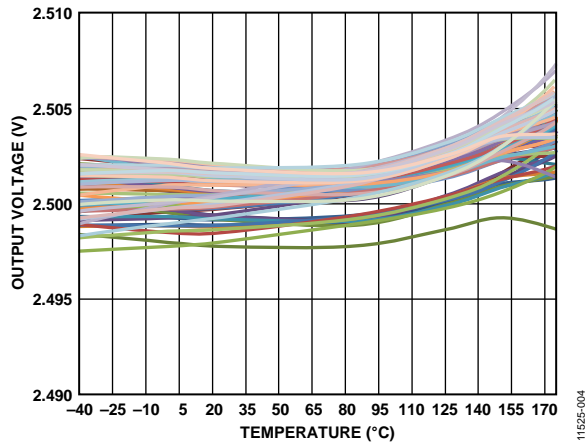


Figure 3. Output Voltage ( $V_{OUT}$ ) vs. Temperature

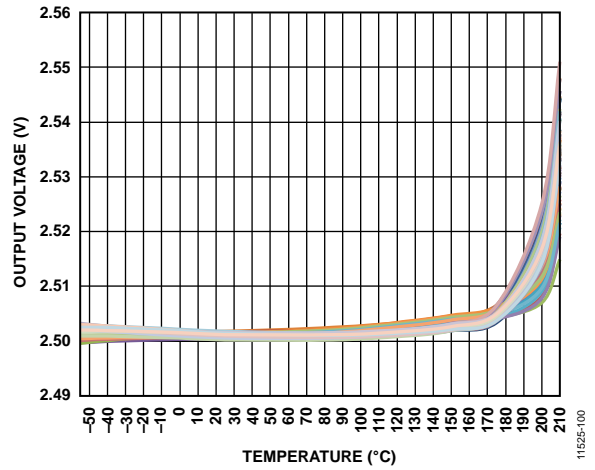


Figure 6. Output Voltage ( $V_{OUT}$ ) vs. Temperature, FLATPACK Package

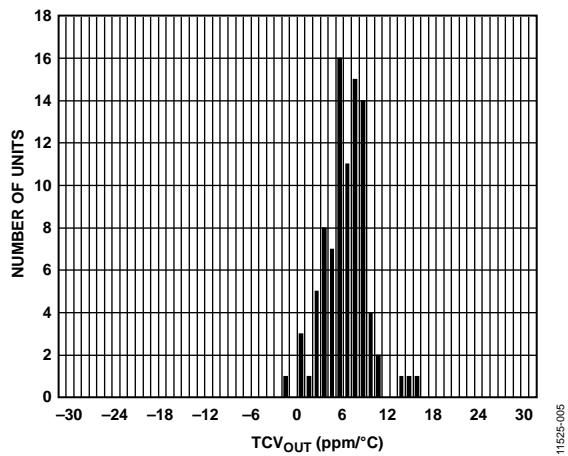


Figure 4.  $TCV_{OUT}$  Distribution,  $-40^{\circ}\text{C}$  to  $+175^{\circ}\text{C}$

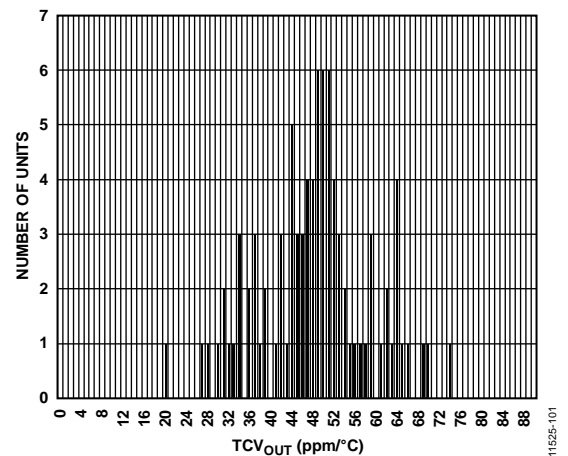


Figure 7.  $TCV_{OUT}$  Distribution,  $-40^{\circ}\text{C}$  to  $+210^{\circ}\text{C}$ , FLATPACK Package

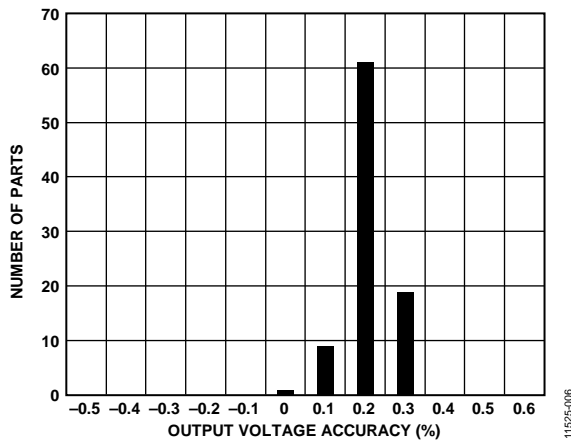


Figure 5. Output Voltage Accuracy at  $175^{\circ}\text{C}$

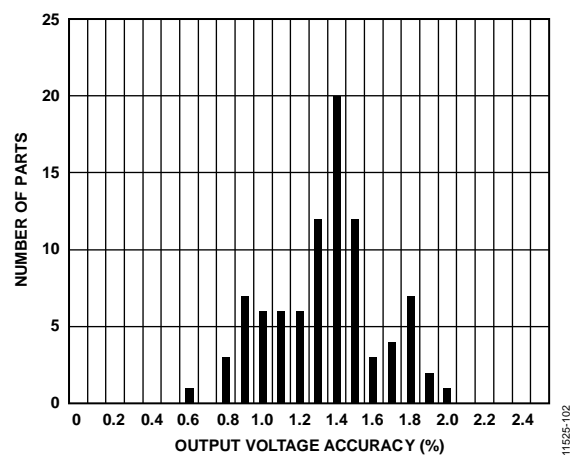


Figure 8. Output Voltage Accuracy at  $210^{\circ}\text{C}$ , FLATPACK Package

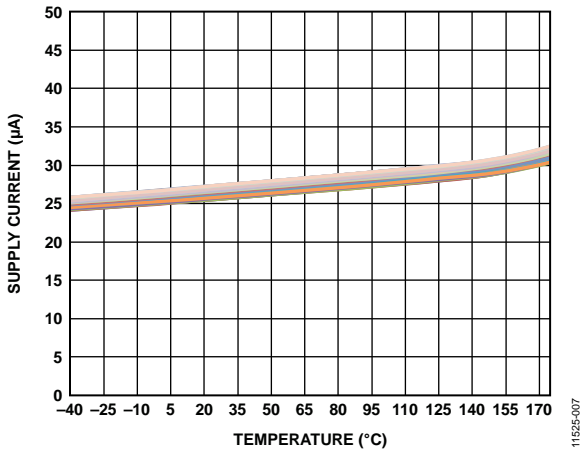


Figure 9. Supply Current ( $I_{SV}$ ) vs. Temperature

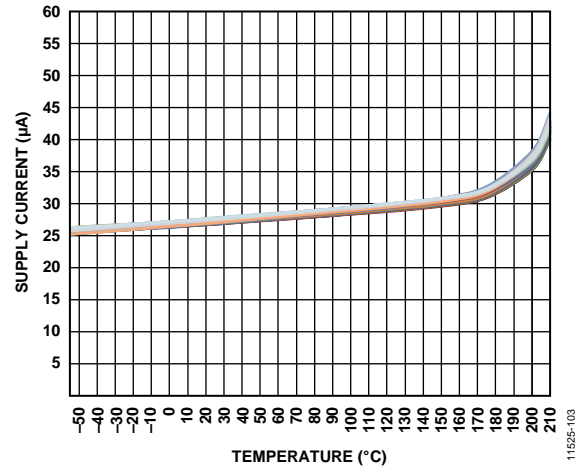


Figure 12. Supply Current ( $I_{SV}$ ) vs. Temperature, FLATPACK Package

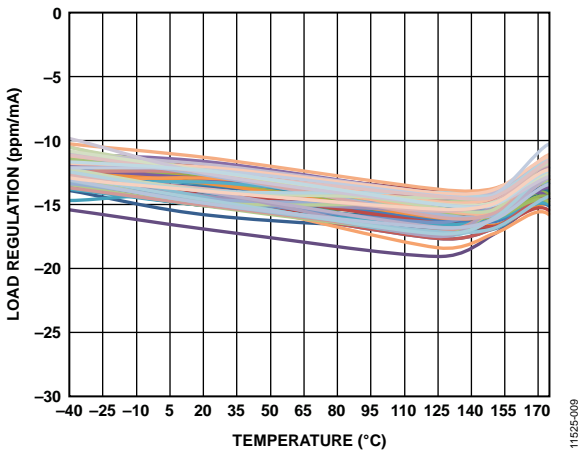


Figure 10. Load Regulation vs. Temperature ( $I_{LOAD} = 0 \text{ mA to } 10 \text{ mA}$ )

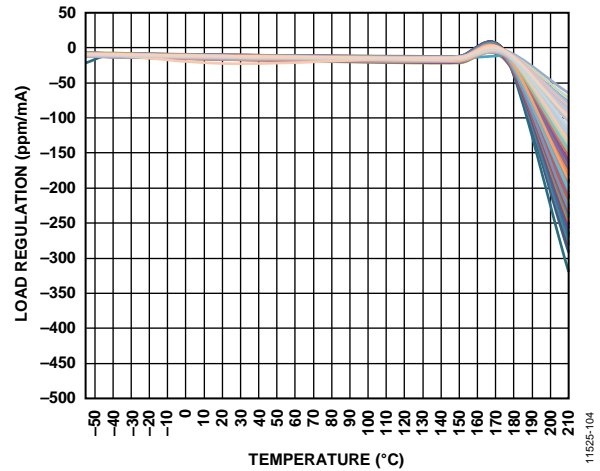


Figure 13. Load Regulation vs. Temperature ( $I_{LOAD} = 0 \text{ mA to } 10 \text{ mA}$ ), FLATPACK Package

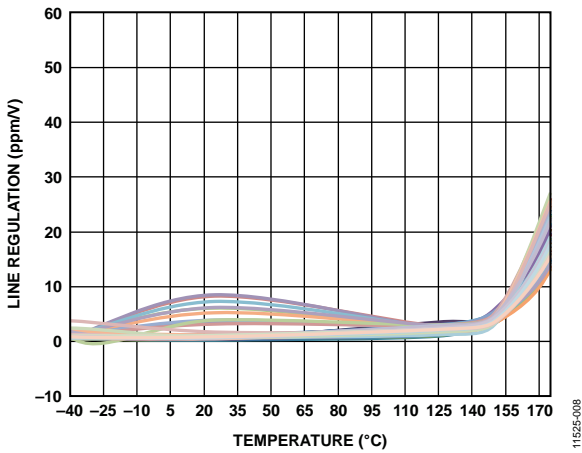


Figure 11. Line Regulation vs. Temperature

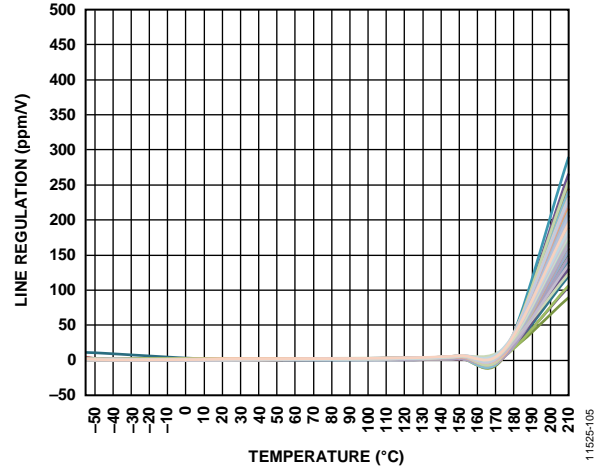


Figure 14. Line Regulation vs. Temperature, FLATPACK Package

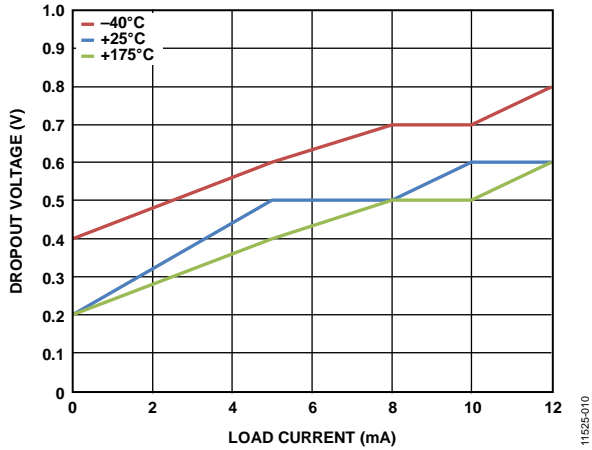


Figure 15. Dropout Voltage vs. Load Current ( $I_{LOAD}$ )

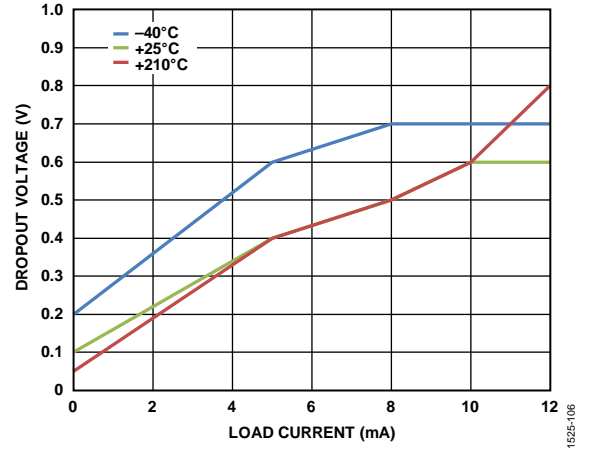


Figure 18. Dropout Voltage vs. Load Current ( $I_{LOAD}$ ), FLATPACK Package

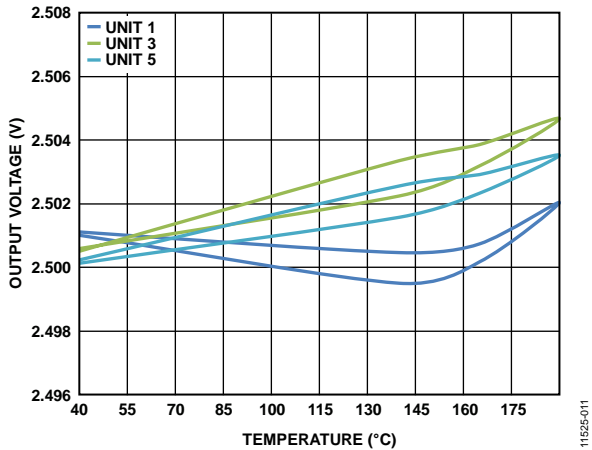


Figure 16. Thermal Hysteresis,  $I_{LOAD} = 0$  mA

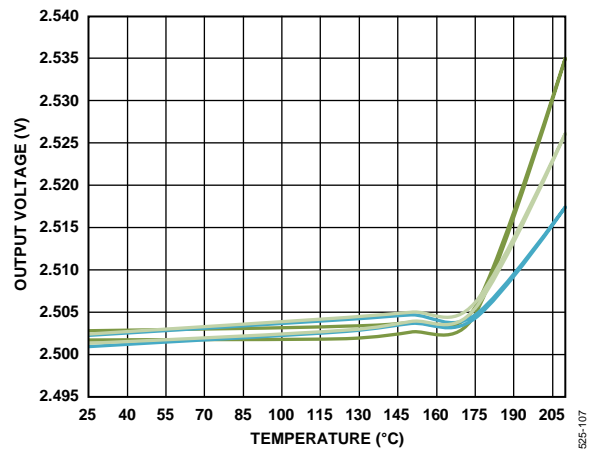


Figure 19. Thermal Hysteresis,  $I_{LOAD} = 0$  mA, FLATPACK Package

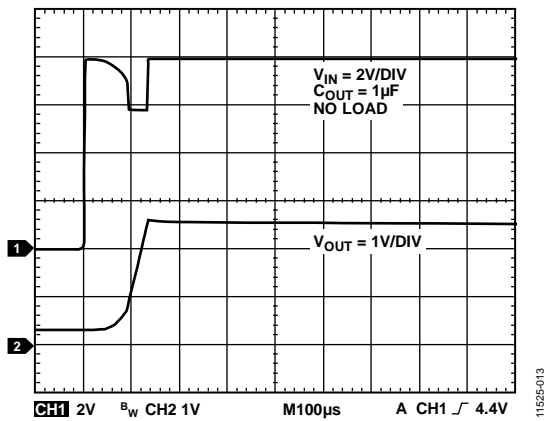


Figure 17. Power-On Response (see Figure 25)

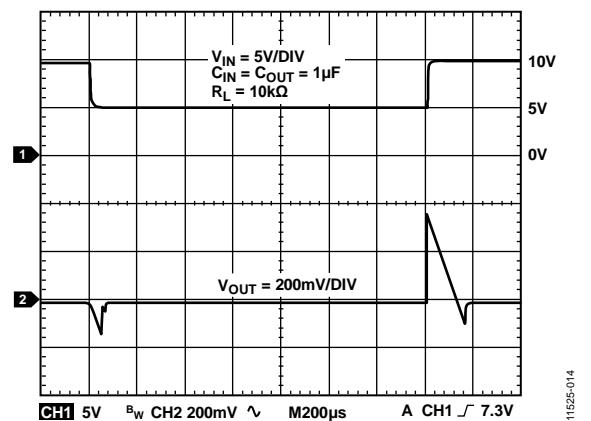


Figure 20. Line Transient Response (see Figure 25)

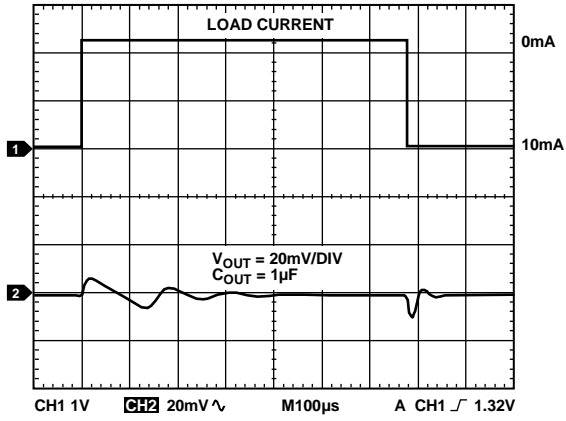


Figure 21. Load Transient Response

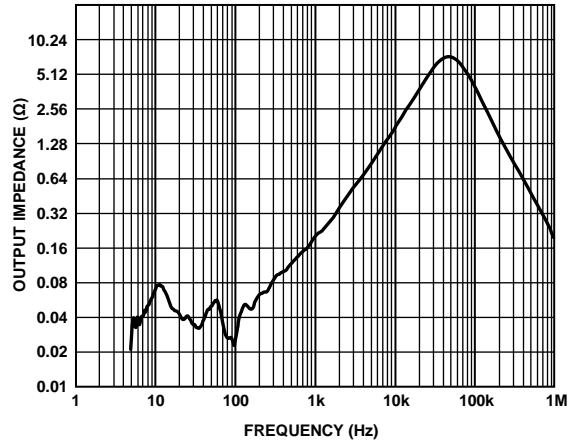


Figure 23. Output Impedance ( $Z_{out}$ ) vs. Frequency,  $C_{IN} = C_{OUT} = 1 \mu F$

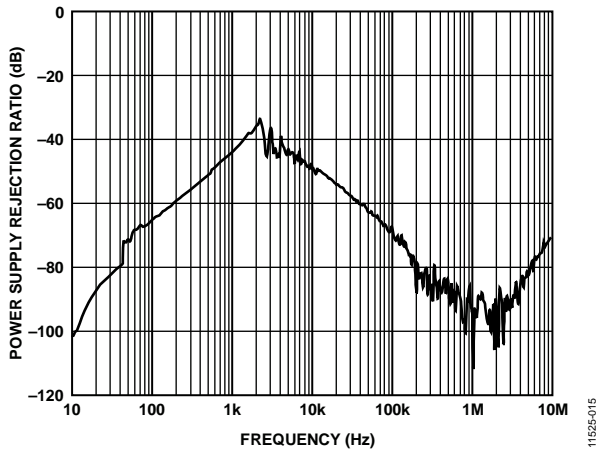


Figure 22. Power Supply Rejection Ratio (PSRR) vs. Frequency,  $C_{LOAD} = 1 \mu F$



# THEORY OF OPERATION

## BASIC VOLTAGE REFERENCE CONNECTIONS

The circuit shown in Figure 24 is the basic configuration for the ADR225. Note that a 10  $\mu$ F and 0.1  $\mu$ F bypass network on the input and at least a 1  $\mu$ F bypass capacitor on the output are required for proper device operation. It is recommended that no connections be made to Pin 1, Pin 3, Pin 5, Pin 7, and Pin 8.

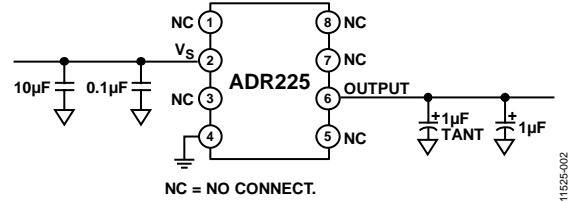


Figure 24. Basic Voltage Reference Connections

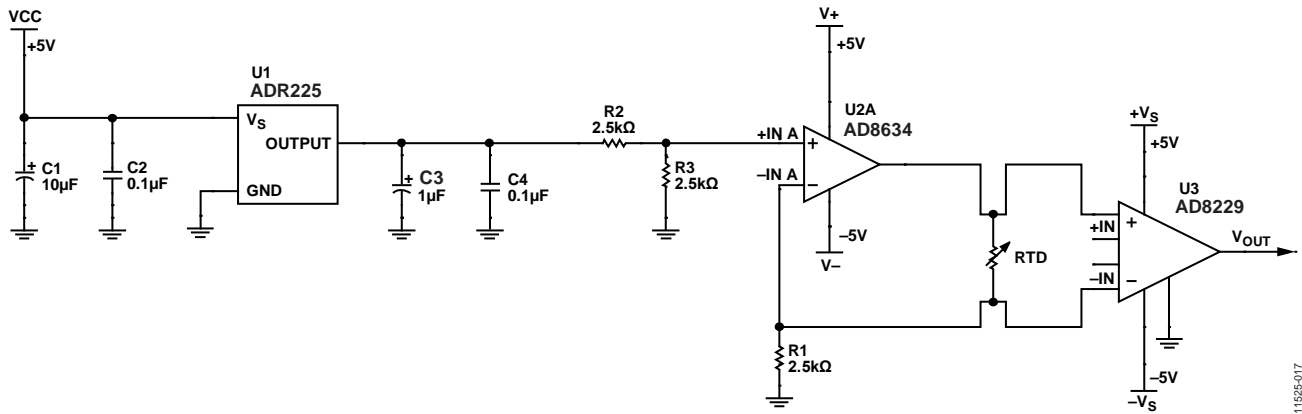
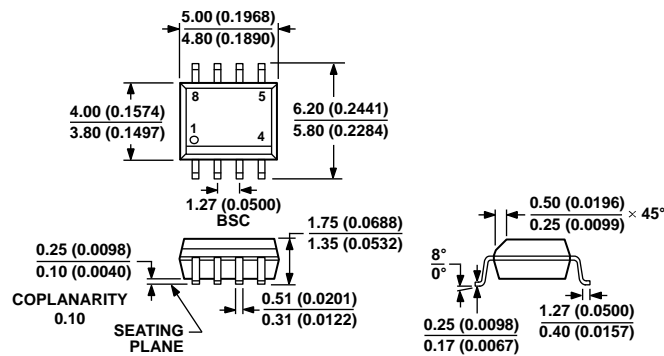


Figure 25. Typical High Temperature Resistance Temperature Detector (RTD) Signal Conditioning Circuit

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA  
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407A

Figure 26. 8-Lead Standard Small Outline Package [SOIC\_N]  
 Narrow Body  
 (R-8)

Dimensions shown in millimeters and (inches)

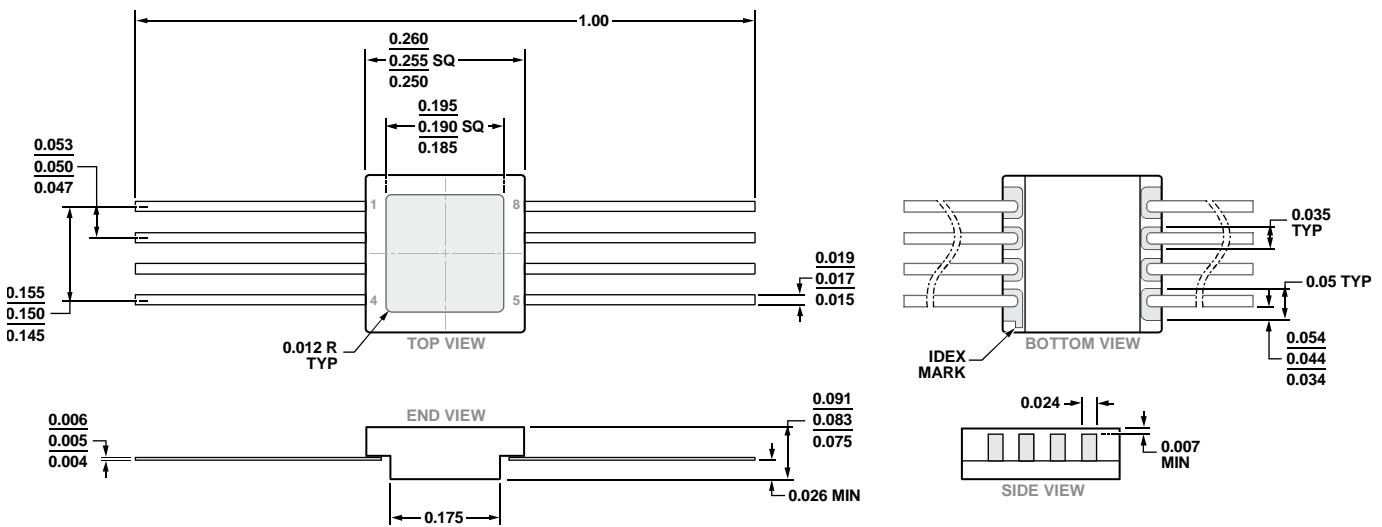


Figure 27. 8-Lead Ceramic Flat Package [FLATPACK]  
 (F-8-2)

Dimensions shown in inches

03-26-2013-A

ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Package Option
ADR225HRZN	-40°C to +175°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
ADR225HFZ	-40°C to +210°C	8-Lead Ceramic Flat Package [FLATPACK]	F-8-2

<sup>1</sup> Z = RoHS Compliant Part.

**NOTES**

**NOTES**