16-Channel DAS with 16-Bit, Bipolar Input, Dual Simultaneous Sampling ADC

Data Sheet

AD7616-P

FEATURES

- 16-channel, dual, simultaneously sampled inputs
- Independently selectable channel input ranges
  - True bipolar: ±10 V, ±5 V, ±2.5 V
- Single 5 V analog supply and 2.3 V to 3.6 V V_{DRIVE} supply
- Fully integrated data acquisition solution
  - Analog input clamp protection
  - Input buffer with 1 MΩ analog input impedance
  - 1st-order antialiasing analog filter
  - On-chip accurate reference and reference buffer
  - Dual 16-bit SAR ADC
  - Throughput rate: 2 × 1 MSPS
  - Oversampling capability with digital filter
  - Flexible sequencer with burst mode
  - Parallel digital interface
  - Optional CRC error checking
- Hardware/software configuration
- Performance
  - 92 dB SNR at 500 kSPS (2× OSR)
  - 90.5 dB SNR at 1 MSPS
  - −103 dB THD
  - ±1 LSB INL (typical), ±0.99 LSB DNL (maximum)
  - 8 kV ESD rating on analog input pins
- On-chip self detect function
- 80-lead LQFP package

APPLICATIONS

- Power line monitoring
- Protective relays
- Multiphase motor control
- Instrumentation and control systems
- Data acquisition systems (DASs)

GENERAL DESCRIPTION

The AD7616-P is a 16-bit, DAS that supports dual simultaneous sampling of 16 channels. The AD7616-P operates from a single 5 V supply and can accommodate ±10 V, ±5 V, and ±2.5 V true bipolar input signals while sampling at throughput rates up to 1 MSPS per channel pair with 90.5 dB SNR. Higher signal-to-noise ratio (SNR) performance can be achieved with the on-chip oversampling mode (92 dB for an oversampling ratio (OSR) of 2).

The input clamp protection circuitry tolerates voltages up to ±21 V. The AD7616-P has 1 MΩ analog input impedance, regardless of sampling frequency. The single-supply operation, on-chip filtering, and high input impedance eliminate the need for driver op amps and external bipolar supplies.

The device contains analog input clamp protection, a dual, 16-bit charge redistribution successive approximation register (SAR) analog-to-digital converter (ADC), a flexible digital filter, a 2.5 V reference and reference buffer, and a high speed parallel interface.

FUNCTIONAL BLOCK DIAGRAM

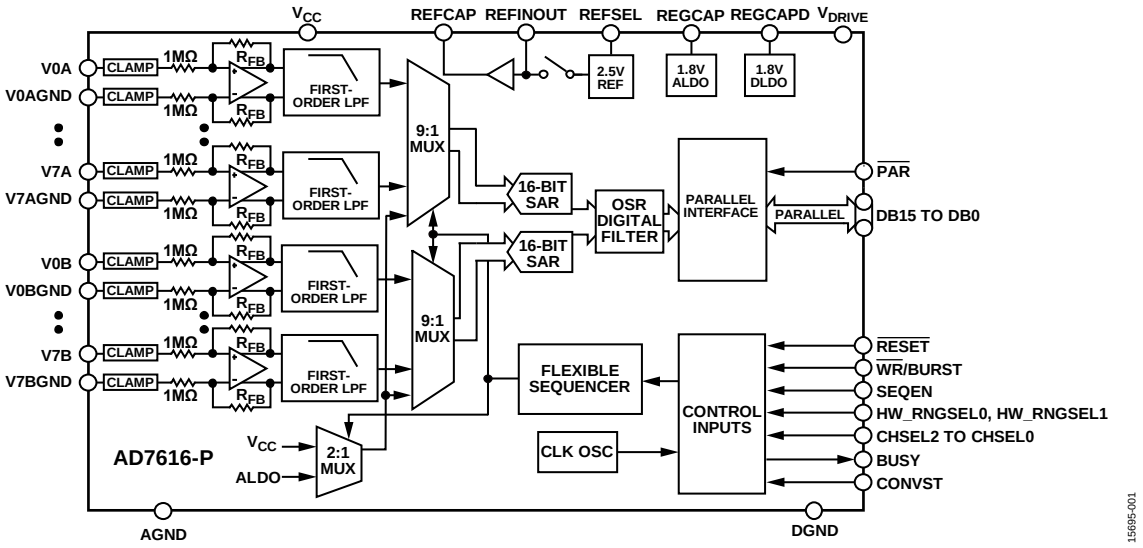

Figure 1.

Rev. 0 Document Feedback

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REVISION HISTORY

6/2017—Revision 0: Initial Version

SPECIFICATIONS

V_{REF} = 2.5 V external/internal, V_{CC} = 4.75 V to 5.25 V, V_{DRIVE} = 2.3 V to 3.6 V, f_{SAMPLE} = 1 MSPS, T_A = −40°C to +125°C, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE	f_{IN} = 1 kHz sine wave, unless otherwise noted				
SNR[1, 2]	No oversampling, ±10 V range	89	90.5		dB
	OSR = 2, ±10 V range,[3] f_{SAMPLE} = 500 kSPS		92		dB
	OSR = 4, ±10 V range[3]		93		dB
	No oversampling, ±5 V range	88	89.5		dB
	No oversampling, ±2.5 V range	85.5	87		dB
Signal-to-Noise-and-Distortion (SINAD)[1]	No oversampling, ±10 V range	88.5	90		dB
	No oversampling, ±5 V range	87.5	89		dB
	No oversampling, ±2.5 V range	85	87		dB
Dynamic Range	No oversampling, ±10 V range		92		dB
	No oversampling, ±5 V range		90.5		dB
	No oversampling, ±2.5 V range		88		dB
Total Harmonic Distortion (THD)[1]	No oversampling, ±10 V range		−103	−92.5	dB
	No oversampling, ±5 V range		−100		dB
	No oversampling, ±2.5 V range		−97		dB
Peak Harmonic or Spurious Noise[1]			−103		dB
Intermodulation Distortion (IMD)[1]	fa = 1 kHz, fb = 1.1 kHz				
Second-Order Terms			−105		dB
Third-Order Terms			−113		dB
Channel to Channel Isolation[1]	f_{IN} on unselected channels up to 5 kHz		−106		dB
ANALOG INPUT FILTER					
Full Power Bandwidth	−3 dB, ±10 V range		39		kHz
	−3 dB, ±5 V/2.5 V range		33		kHz
	−0.1 dB		5.5		kHz
Phase Delay[1, 3]	±10 V range		4.4	6	µs
	±5 V range		5		µs
	±2.5 V range		4.9		µs
Drift[1, 3]	±10 V range		±0.55	5	ns/°C
Matching (Dual Simultaneous Pair)[3]	±10 V range		4.4	100	ns
	±5 V range		4.7		ns
	±2.5 V range		4.1		ns
DC ACCURACY					
Resolution	No missing codes	16			Bits
Differential Nonlinearity (DNL)[1]			±0.5	±0.99	LSB[4]
Integral Nonlinearity (INL)[1]			±1	±2	LSB[4]
Total Unadjusted Error (TUE)	±10 V range		±6		LSB[4]
	±5 V range		±8		LSB[4]
	±2.5 V range		±10		LSB[4]
Positive Full-Scale (PFS) Error[1, 5]					
External Reference	±10 V range		±5	±38	LSB[4]
	±5 V range		±4		LSB[4]
	±2.5 V range		±2		LSB[4]
Internal Reference					
	±10 V range		±5		LSB[4]
Drift[3]	External reference		±2	±5	ppm/°C
	Internal reference		±3	±10	ppm/°C
Matching[1]	±10 V range		3	11	LSB[4]
	±5 V range		4		LSB[4]

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
	±2.5 V range		8		LSB[4]
Bipolar Zero Code Error[1]	±10 V range		±0.8	±8	LSB[4]
	±5 V range		±1	±10	LSB[4]
	±2.5 V range		±3	±15	LSB[4]
Drift[3]	±10 V range		±1.3	±20.4	µV/°C
	±5 V range		±0.9		µV/°C
	±2.5 V range		±0.5		µV/°C
Matching[1]	±10 V range		±2	±10	LSB[4]
	±5 V range		±3		LSB[4]
	±2.5 V range		±3		LSB[4]
Negative Full-Scale (NFS) Error[1, 6]	External reference				
	±10 V range		±4	±38	LSB[4]
	±5 V range		±3		LSB[4]
	±2.5 V range		±6		LSB[4]
	Internal reference				
	±10 V range		±3		LSB[4]
Drift[3]	External reference		±2	±5	ppm/°C
	Internal reference		±4	±10	ppm/°C
Matching[1]	±10 V range		3	11	LSB[4]
	±5 V range		4		LSB[4]
	±2.5 V range		8		LSB[4]
ANALOG INPUT					
Input Voltage Ranges	Software/hardware selectable			±10	V
	Software/hardware selectable			±5	V
	Software/hardware selectable			±2.5	V
Analog Input Current	±10 V range, see Figure 33		±10.5		µA
	±5 V range, see Figure 33		±6.5		µA
	±2.5 V range, see Figure 33		±4		µA
Input Capacitance[6]			10		pF
Input Impedance	See the Analog Input section	0.85	1		MΩ
Input Impedance Drift[3]				25	ppm/°C
REFERENCE INPUT/OUTPUT					
Reference Input Voltage Range	See the ADC Transfer Function section	2.495	2.5	2.505	V
DC Leakage Current				±1	µA
Input Capacitance[6]	REFSEL = 1		7.5		pF
Reference Output Voltage	REFINOUT	2.495		2.505	V
Reference Temperature Coefficient[3]			±2	±15	ppm/°C
LOGIC INPUTS					
Input Voltage					
High (V_{INH})	V_{DRIVE} = 2.7 V to 3.6 V	2			V
	V_{DRIVE} = 2.3 V to 2.7 V	1.7			V
Low (V_{INL})	V_{DRIVE} = 2.7 V to 3.6 V			0.8	V
	V_{DRIVE} = 2.3 V to 2.7 V			0.7	V
Input Current (I_{IN})				±1	µA
Input Capacitance (C_{IN})[6]			5		pF
LOGIC OUTPUTS					
Output Voltage					
High (V_{OH})	I_{SOURCE} = 100 µA	V_{DRIVE} − 0.2			V
Low (V_{OL})	I_{SINK} = 100 µA			0.4	V
Floating State Leakage Current			±0.005	±1	µA
Floating State Output Capacitance[6]			5		pF
Output Coding	Twos complement				

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CONVERSION RATE	Per channel pair				
Conversion Time			0.5		µs
Acquisition Time			0.5		µs
Throughput Rate				1	MSPS
POWER REQUIREMENTS					
V_{CC}		4.75		5.25	V
V_{DRIVE}		2.3		3.6	V
V_{CC} Pin Current, I_{VCC}					
Normal Mode					
Static			37	57	mA
Operational	f_{SAMPLE} = 1 MSPS		42	65	mA
Shutdown Mode			28		µA
I_{DRIVE}	Digital inputs = 0 V or V_{DRIVE}				
Normal Mode					
Static			0.3	0.95	mA
Operational	f_{SAMPLE} = 1 MSPS		2.4	3.2	mA
Shutdown Mode			20		µA
Power Dissipation					
Normal Mode					
Static			185	300	mW
Operational	f_{SAMPLE} = 1 MSPS		230	360	mW
Shutdown Mode			0.25		mW

[1] See the Terminology section.
[2] The user can achieve 93 dB SNR by enabling oversampling. The values are valid for manual mode. In burst mode, values degrade by ~1 dB.
[3] Not production tested. Sample tested during initial release to ensure compliance.
[4] LSB means least significant bit. With a ±2.5 V input range, 1 LSB = 76.293 µV. With a ±5 V input range, 1 LSB = 152.58 µV. With a ±10 V input range, 1 LSB = 305.175 µV.
[5] Positive and negative full-scale error for the internal reference excludes reference errors.
[6] Supported by simulation data.

TIMING SPECIFICATIONS

Note that throughout the timing specifications, multifunction pins, such as $\overline{WR}$/ BURST, are referred to either by the entire pin name or by a single function of the pin, for example, $\overline{WR}$, when only that function is relevant.

Universal Timing Specifications

V_{CC} = 4.75 V to 5.25 V, V_{DRIVE} = 2.3 V to 3.6 V, V_{REF} = 2.5 V external reference/internal reference, T_A = −40°C to +125°C, unless otherwise noted. Interface timing tested using a load capacitance of 30 pF.

Table 2.

Parameter[1]	Min	Typ	Max	Unit	Description
t_{CYCLE}	1			µs	Minimum time between consecutive CONVST rising edges (excluding burst and oversampling modes)
t_{CONV_LOW}	50			ns	CONVST low pulse width
t_{CONV_HIGH}	50			ns	CONVST high pulse width
t_{BUSY_DELAY}			34	ns	CONVST high to BUSY high (manual mode)
$t_{\overline{CS}_SETUP}$	20			ns	BUSY falling edge to $\overline{CS}$ falling edge setup time
t_{CH_SETUP}	50			ns	Channel select setup time in hardware mode for CHSELx
t_{CH_HOLD}	20			ns	Channel select hold time in hardware mode for CHSELx
t_{CONV}		475	530	ns	Conversion time for the selected channel pair
t_{ACQ}	470			ns	Acquisition time for the selected channel pair
t_{QUIET}	50			ns	$\overline{CS}$ rising edge to next CONVST rising edge
$t_{\overline{RESET}_LOW}$					See Figure 3
Partial Reset	40		500	ns	Partial $\overline{RESET}$ low pulse width
Full Reset	1.2			µs	Full $\overline{RESET}$ low pulse width
t_{DEVICE_SETUP}					See Figure 3
Partial Reset	120			ns	Time between partial $\overline{RESET}$ high and CONVST rising edge
Full Reset	15			ms	Time between full $\overline{RESET}$ high and CONVST rising edge
t_{WRITE}					See Figure 3
Partial Reset	50			ns	Time between partial $\overline{RESET}$ high and $\overline{CS}$ for write operation
Full Reset	240			µs	Time between full $\overline{RESET}$ high and $\overline{CS}$ for write operation
$t_{\overline{RESET}_WAIT}$	1			ms	Time between stable V_{CC}/V_{DRIVE} and release of $\overline{RESET}$ (see Figure 3)
$t_{\overline{RESET}_SETUP}$					Time prior to release of $\overline{RESET}$ that queried hardware inputs must be stable for (see Figure 3)
Partial Reset	10			ns	
Full Reset	0.05			ms	
$t_{\overline{RESET}_HOLD}$					Time after release of $\overline{RESET}$ that latched hardware inputs must be stable for (see Figure 3)
Partial Reset	10			ns	
Full Reset	0.24			ms	

[1] Not production tested. Sample tested during initial release to ensure compliance.

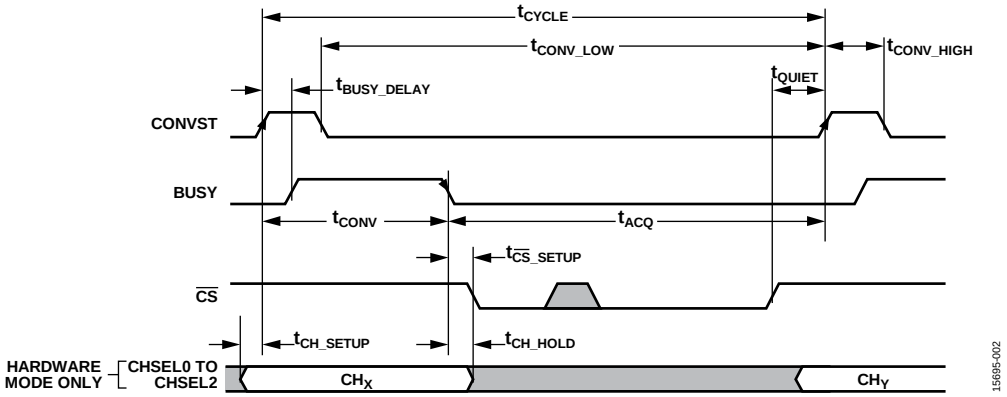


Figure 2. Universal Timing Diagram Across All Interfaces

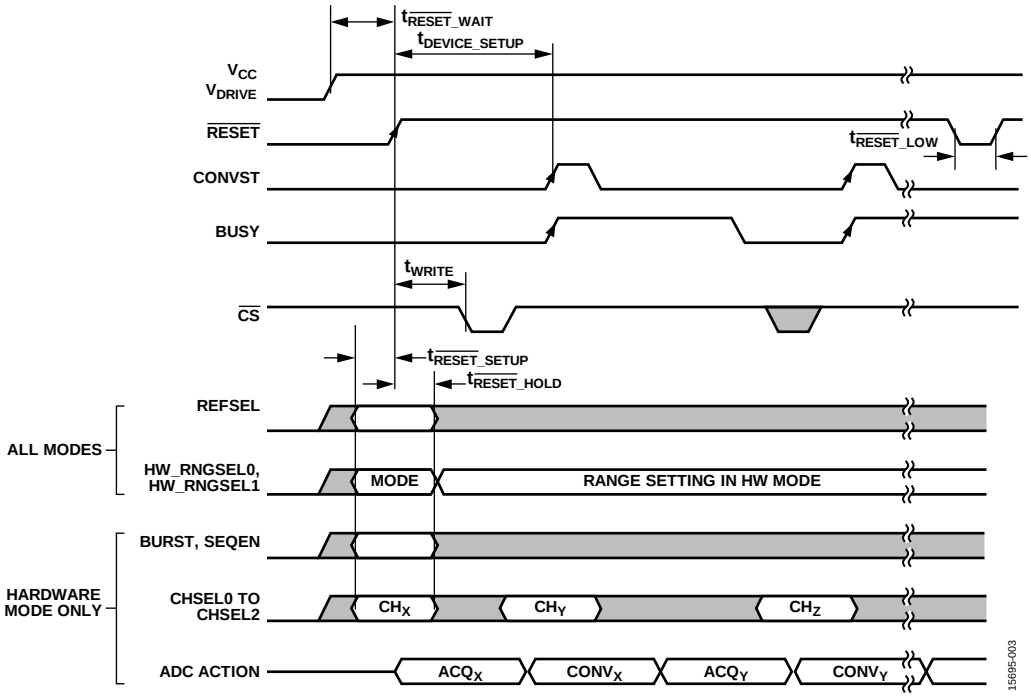


Figure 3. Reset Timing Diagram

Parallel Interface Timing Specifications

Table 3.

Parameter	Min	Typ	Max	Unit	Description
$t_{\overline{CS}_HIGH}$	20			ns	$\overline{CS}$ high pulse width
$t_{\overline{RD}_SETUP}$	0			ns	$\overline{CS}$ falling edge to $\overline{RD}$ falling edge setup time
$t_{\overline{RD}_HOLD}$	0			ns	$\overline{RD}$ rising edge to $\overline{CS}$ rising edge hold time
$t_{\overline{RD}_HIGH}$	20			ns	$\overline{RD}$ high pulse width
$t_{\overline{RD}_LOW}$	40			ns	$\overline{RD}$ low pulse width
t_{DOUT_SETUP}			40	ns	Data access time after falling edge of $\overline{RD}$
t_{DOUT_3STATE}			16	ns	$\overline{CS}$ rising edge to DBx high impedance
$t_{\overline{WR}_SETUP}$	0			ns	$\overline{CS}$ to $\overline{WR}$ setup time
$t_{\overline{WR}_HIGH}$	20			ns	$\overline{WR}$ high pulse width
$t_{\overline{WR}_LOW}$	40			ns	$\overline{WR}$ low pulse width
$t_{\overline{WR}_HOLD}$	0			ns	$\overline{WR}$ hold time
t_{DIN_SETUP}	12			ns	Configuration data to $\overline{WR}$ setup time
t_{DIN_HOLD}	5			ns	Configuration data to $\overline{WR}$ hold time
t_{CONF_SETTLE}	20			ns	Configuration data settle time, $\overline{WR}$ rising edge to CONVST rising edge

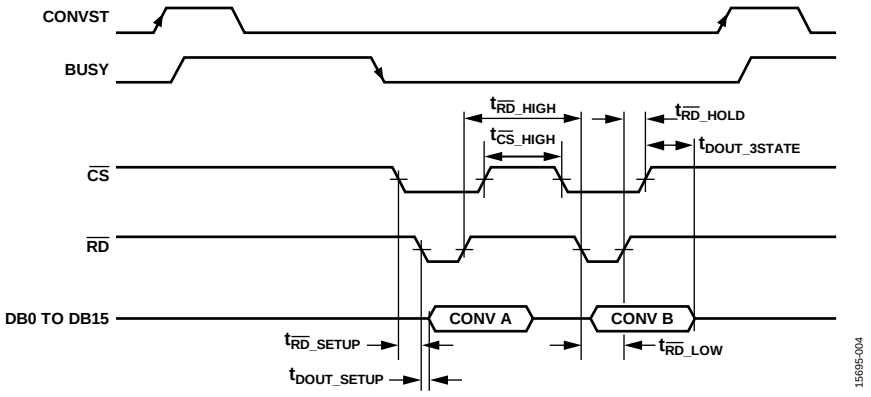


Figure 4. Parallel Read Timing Diagram

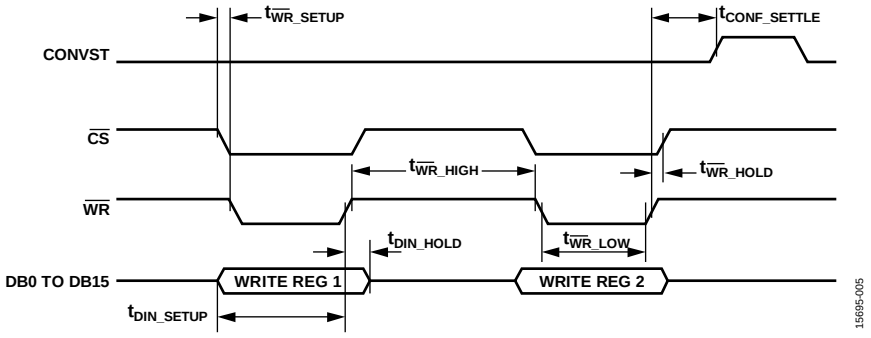


Figure 5. Parallel Write Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
V_{CC} to AGND	−0.3 V to +7 V
V_{DRIVE} to AGND	−0.3 V to V_{CC} + 0.3 V
Analog Input Voltage to AGND[1]	±21 V
Digital Input Voltage to AGND	−0.3 V to V_{DRIVE} + 0.3 V
Digital Output Voltage to AGND	−0.3 V to V_{DRIVE} + 0.3 V
REFINOUT to AGND	−0.3 V to V_{CC} + 0.3 V
Input Current to Any Pin Except Supplies[1]	±10 mA
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Soldering Reflow	
Pb/Sn Temperature (10 sec to 30 sec)	240 (+0)°C
Pb-Free Temperature	260 (+0)°C
ESD	
All Pins Except Analog Inputs	2 kV
Analog Input Pins Only	8 kV

[1] Transient currents of up to 100 mA do not cause silicon controlled rectifier (SCR) latch-up.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
ST-80-2[1]	41	7.5	°C/W

[1] Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board. See JEDEC JESD51.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

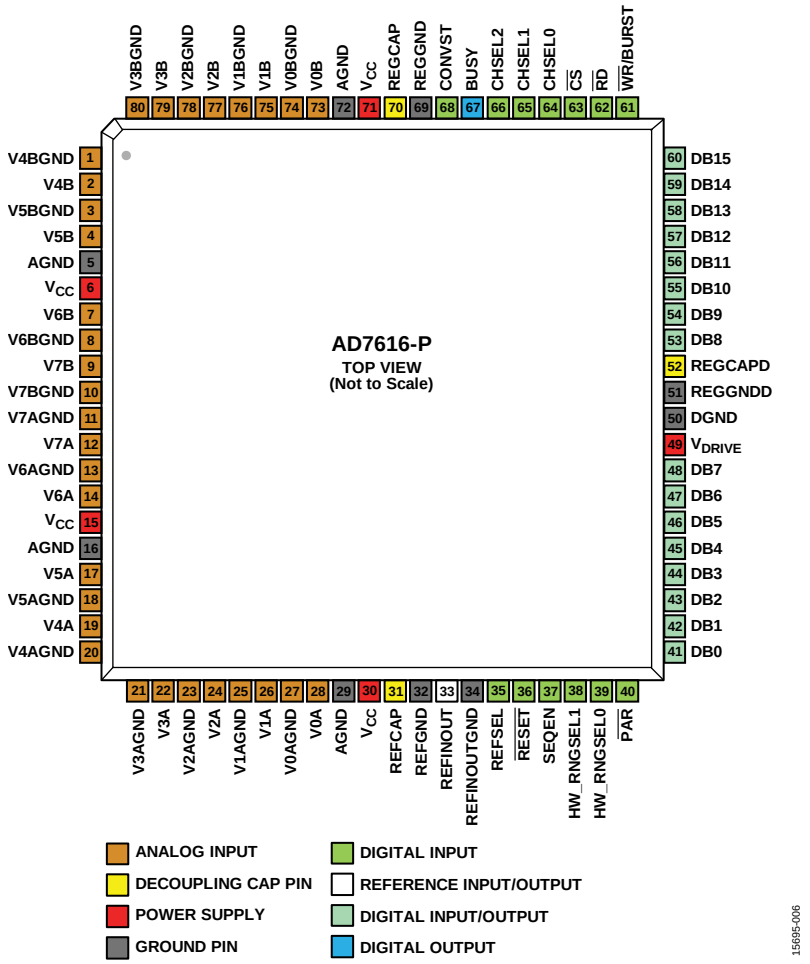


Figure 6. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Type[1]	Mnemonic[2]	Description
1	AI GND	V4BGND	Analog Input Ground for V4B.
2	AI	V4B	Analog Input Channel 4, ADC B.
3	AI GND	V5BGND	Analog Input Ground for V5B.
4	AI	V5B	Analog Input Channel 5, ADC B.
5, 16, 29, 72	P	AGND	Analog Supply Ground.
6, 15, 30, 71	P	V_{CC}	Analog Supply Voltage, 4.7 V to 5.25 V. This supply voltage is applied to the internal front-end amplifiers and to the ADC core. Decouple these pins to AGND using 0.1 µF and 10 µF capacitors in parallel.
7	AI	V6B	Analog Input Channel 6, ADC B.
8	AI GND	V6BGND	Analog Input Ground for V6B.
9	AI	V7B	Analog Input Channel 7, ADC B.
10	AI GND	V7BGND	Analog Input Ground for V7B.
11	AI GND	V7AGND	Analog Input Ground for V7A.
12	AI	V7A	Analog Input Channel 7, ADC A.
13	AI GND	V6AGND	Analog Input Ground for V6A.
14	AI	V6A	Analog Input Channel 6, ADC A.
17	AI	V5A	Analog Input Channel 5, ADC A.
18	AI GND	V5AGND	Analog Input Ground for V5A.
19	AI	V4A	Analog Input V4A.
20	AI GND	V4AGND	Analog Input Ground for V4A.

Pin No.	Type[1]	Mnemonic[2]	Description
21	AI GND	V3AGND	Analog Input Ground for V3A.
22	AI	V3A	Analog Input Channel 3, ADC A.
23	AI GND	V2AGND	Analog Input Ground for V2A.
24	AI	V2A	Analog Input Channel 2, ADC A.
25	AI GND	V1AGND	Analog Input Ground for V1A.
26	AI	V1A	Analog Input Channel 1, ADC A.
27	AI GND	V0AGND	Analog Input Ground for V0A.
28	AI	V0A	Analog Input Channel 0, ADC A.
31	CAP	REFCAP	Reference Buffer Output Force/Sense. Decouple this pin to REFGND using a low effective series resistance (ESR), 10 µF, X5R ceramic capacitor, as close to the REFCAP pin as possible. The voltage on this pin is typically 4.096 V.
32	GND	REFGND	Reference Ground. Connect this pin to AGND.
33	REF	REFINOUT	Reference Input/Reference Output. The on-chip voltage reference of 2.5 V is available on this pin for external use when the REFSEL pin is set to logic high. Alternatively, the internal reference can be disabled by setting the REFSEL pin to logic low, and an external reference of 2.5 V can be applied to this input. Decoupling is required on this pin for both the internal and external reference options. Connect a 100 nF, X7R capacitor between the REFINOUT and REFINOUTGND pins, as close to the REFINOUT pin as possible. If using an external reference, connect a 10 kΩ series resistor to this pin to band limit the reference signal.
34	GND	REFINOUTGND	Reference Input, Reference Output Ground.
35	DI	REFSEL	Internal/External Reference Selection Input. REFSEL is a logic input. If this pin is set to logic high, the internal reference is selected and enabled. If this pin is set to logic low, the internal reference is disabled and an external reference voltage must be applied to the REFINOUT pin. The signal state is latched on the release of a full reset, and requires an additional full reset to reconfigure.
36	DI	$\overline{\text{RESET}}$	Reset Input. Connect a 100 pF capacitor between $\overline{\text{RESET}}$ and ground. Full and partial reset options are available. The type of reset is determined by the length of the $\overline{\text{RESET}}$ pulse. Keeping $\overline{\text{RESET}}$ low places the device into shutdown mode. See the Reset Functionality section for further details.
37	DI	SEQEN	Channel Sequencer Enable Input (Hardware Mode Only). When SEQEN is tied low, the sequencer is disabled. When SEQEN is high, the sequencer is enabled (with restricted functionality in hardware mode). See the Sequencer section for further details. The signal state is latched on the release of a full reset, and requires an additional full reset to reconfigure. In software mode, this pin must be connected to DGND.
38, 39	DI	HW_RNGSEL1, HW_RNGSEL0	Hardware/Software Mode Selection, Hardware Mode Range Select Inputs. Hardware/software mode selection is latched at full reset. Range selection in hardware mode is not latched. HW_RNGSELx = 00: software mode; the AD7616-P is configured via the software registers. HW_RNGSELx = 01: hardware mode; analog input range is ±2.5 V. HW_RNGSELx = 10: hardware mode; analog input range is ±5 V. HW_RNGSELx = 11: hardware mode; analog input range is ±10 V.
40	DI	$\overline{\text{PAR}}$	Parallel Interface Selection Input. $\overline{\text{PAR}}$ is a logic input. This pin must be tied to a logic low state on power-up or before the release of a full reset. PAR = 0: parallel interface selected. PAR = 1: invalid.
41 to 48	DO/DI	DB0 to DB7	Parallel Output/Input Data Bit 0 to Data Bit 7. These pins are output/input parallel data bits, DB7 to DB0. Refer to the Parallel Interface section for further details.
49	P	V_{DRIVE}	Logic Power Supply Input. The voltage supplied at this pin (2.3 V to 3.6 V) determines the operating voltage of the interface. This pin is nominally at the same supply as the supply of the host interface. Decouple this pin with 0.1 µF and 10 µF capacitors in parallel.
50	GND	DGND	Digital Ground. This pin is the ground reference point for all digital circuitry on the AD7616-P. The DGND pin must connect to the DGND plane of a system.
51	GND	REGGNDD	Ground for the Digital Low Dropout (LDO) Regulator Connected to REGCAPD (Pin 52).
52	CAP	REGCAPD	Decoupling Capacitor Pin for Voltage Output from the Internal Digital Regulator. Decouple this output pin separately to REGGNDD using a 10 µF capacitor. The voltage at this pin is 1.89 V typical.

Pin No.	Type[1]	Mnemonic[2]	Description
53 to 60	DO/DI	DB8 to DB15	Parallel Output/Input Data Bit 8 to Data Bit 15. These pins act as three-state parallel digital input/outputs. Refer to the Parallel Interface section for further details.
61	DI	$\overline{WR}$/BURST	Write/Burst Mode Enable. In software mode, this pin acts as $\overline{WR}$ for register write commands. In hardware mode, this pin enables burst mode. The signal state is latched on the release of a full reset, and requires an additional full reset to reconfigure. Refer to the Burst Sequencer section for further information.
62	DI	$\overline{RD}$	Parallel Data Read Control Input. When both $\overline{CS}$ and $\overline{RD}$ are logic low in parallel mode, the output bus is enabled.
63	DI	$\overline{CS}$	Chip Select. This active low logic input frames the data transfer. When both $\overline{CS}$ and $\overline{RD}$ are logic low, the DBx output bus is enabled and the conversion result is output on the parallel data bus lines.
64 to 66	DI	CHSEL0 to CHSEL2	Channel Selection Input 0 to Input 2 (Hardware Mode Only). In hardware mode, these inputs select the input channels for the next conversion in ADC A and ADC B. For example, CHSELx = 0x000 selects V0A and V0B for the next conversion; CHSELx = 0x001 selects V1A and V1B for the next conversion.
67	DO	BUSY	Busy Output. This pin transitions to a logic high after a CONVST rising edge and indicates that the conversion process started. The BUSY output remains high until the conversion process for the current selected channels is complete. The falling edge of BUSY signals that the conversion data is being latched into the output data registers and is available to read. Data must be read after BUSY returns to low. Rising edges on CONVST have no effect while the BUSY signal is high.
68	DI	CONVST	Conversion Start Input for ADC A and ADC B. This logic input initiates conversions on the analog input channels. A conversion is initiated when CONVST transitions from low to high for the selected analog input pair. When burst mode and oversampling mode are disabled, every CONVST transition from low to high converts one channel pair. In sequencer mode, when burst mode or oversampling is enabled, a single CONVST transition from low to high is necessary to perform the required number of conversions.
69	GND	REGGND	Internal Analog Regulator Ground. This pin must connect to the AGND plane of a system.
70	CAP	REGCAP	Decoupling Capacitor Pin for Voltage Output from Internal Analog Regulator. Decouple this output pin separately to REGGND using a 10 µF capacitor. The voltage at this pin is 1.87 V typical.
73	AI	V0B	Analog Input Channel 0, ADC B.
74	AI GND	V0BGND	Analog Input Ground for V0B.
75	AI	V1B	Analog Input Channel 1, ADC B.
76	AI GND	V1BGND	Analog Input Ground for V1B.
77	AI	V2B	Analog Input Channel 2, ADC B.
78	AI GND	V2BGND	Analog Input Ground for V2B.
79	AI	V3B	Analog Input Channel 3, ADC B.
80	AI GND	V3BGND	Analog Input Ground for V3B.

[1] AI is analog input, GND is ground, P is power supply, CAP is decoupling capacitor pin, REF is reference input/output, DI is digital input, and DO is digital output.
[2] Note that throughout this data sheet, multifunction pins, such as $\overline{WR}$/BURST, are referred to either by the entire pin name or by a single function of the pin, for example, $\overline{WR}$, when only that function is relevant.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{REF} = 2.5 V internal, V_{CC} = 5 V, V_{DRIVE} = 3.3 V, f_{SAMPLE} = 1 MSPS, f_{IN} = 1 kHz T_A = 25°C, unless otherwise noted.

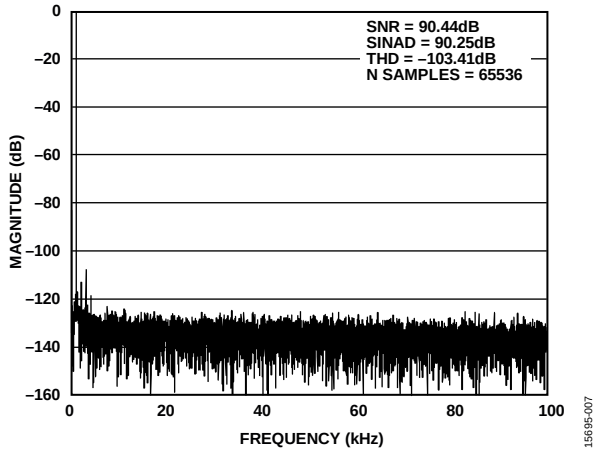


Figure 7. Fast Fourier Transform (FFT), ±10 V Range

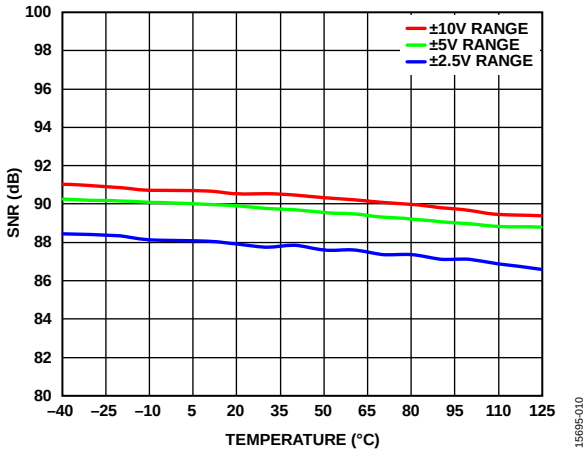


Figure 10. SNR vs. Temperature

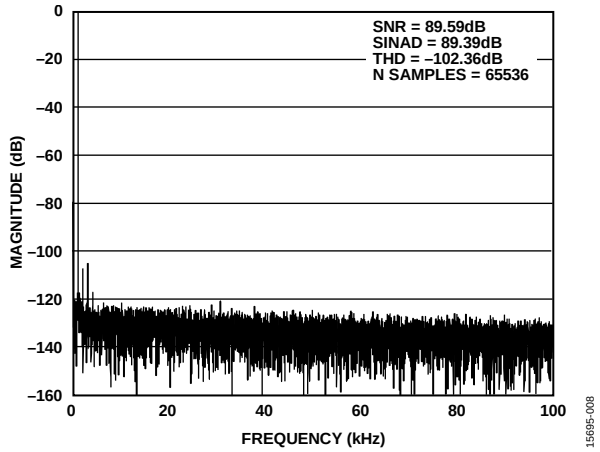


Figure 8. FFT, ±5 V Range

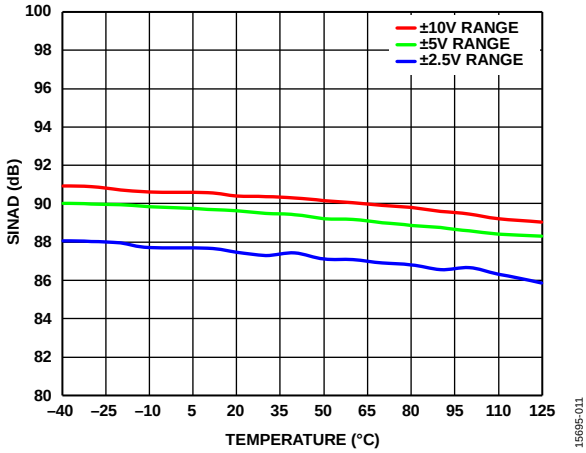


Figure 11. SINAD vs. Temperature

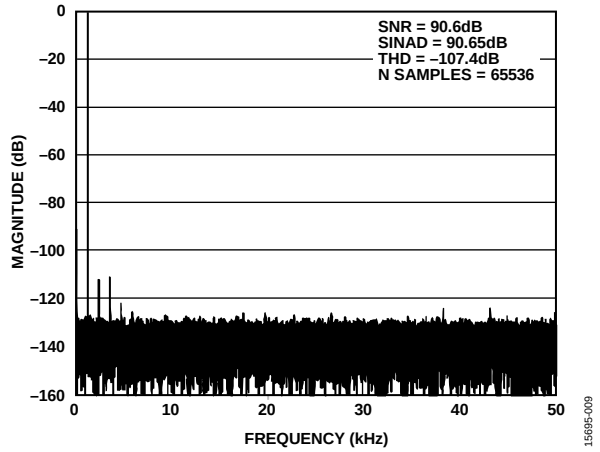


Figure 9. FFT Burst Mode, ±10 V Range

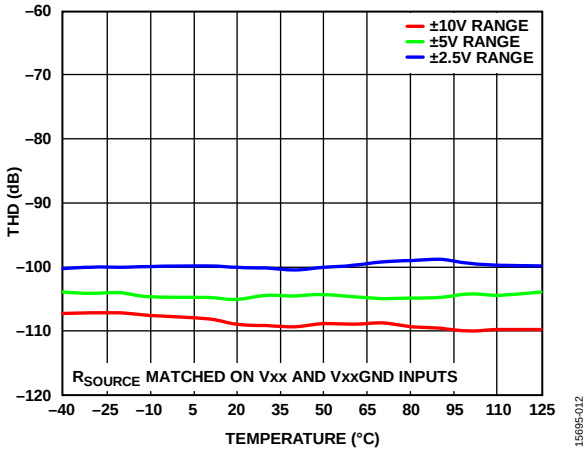


Figure 12. THD vs. Temperature

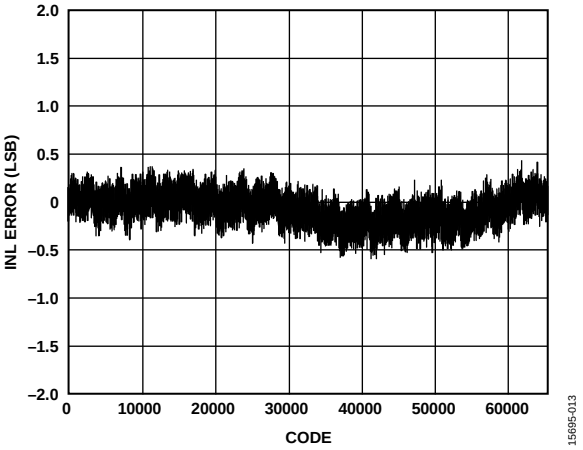


Figure 13. Typical INL Error, ±10 V Range

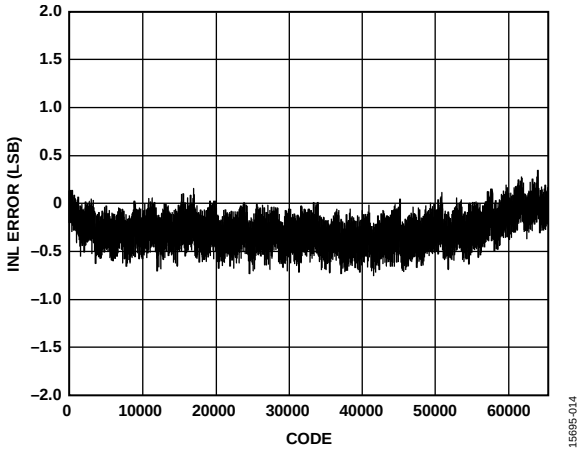


Figure 14. Typical INL Error, ±5 V Range

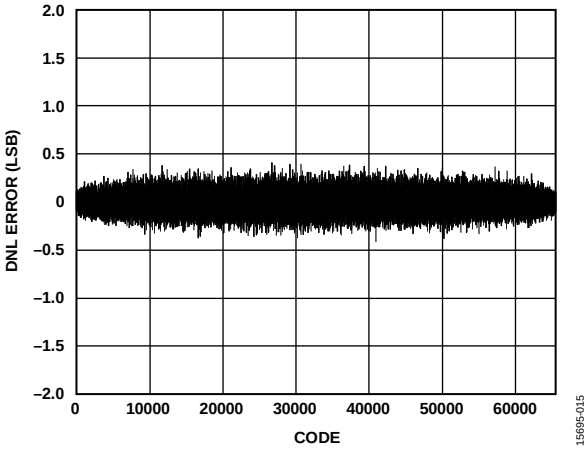


Figure 15. Typical DNL Error, ±10 V Range

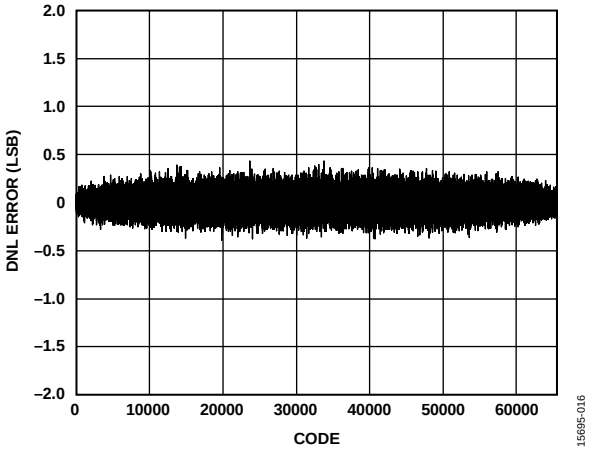


Figure 16. Typical DNL Error, ±5 V Range

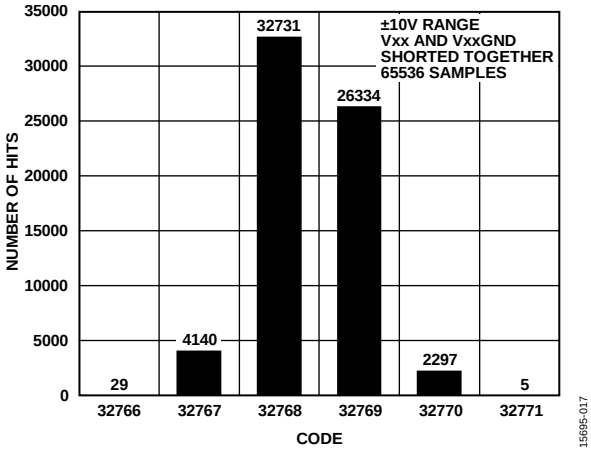


Figure 17. DC Histogram of Codes at Code Center, ±10 V Range

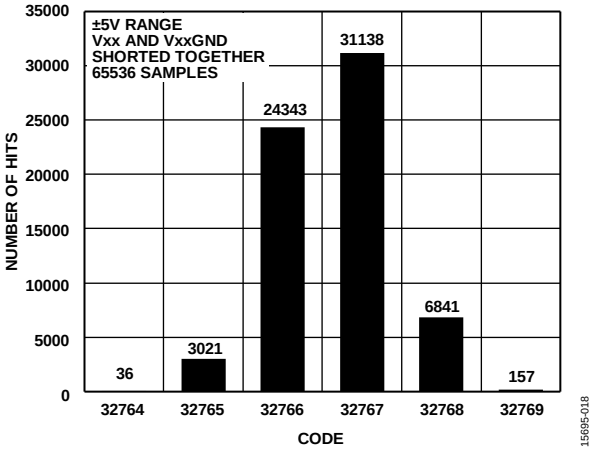


Figure 18. DC Histogram of Codes at Code Center, ±5 V Range

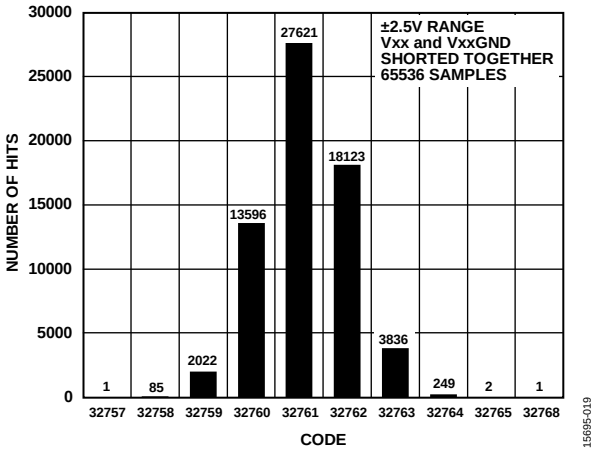


Figure 19. DC Histogram of Codes at Code Center, ±2.5 V Range

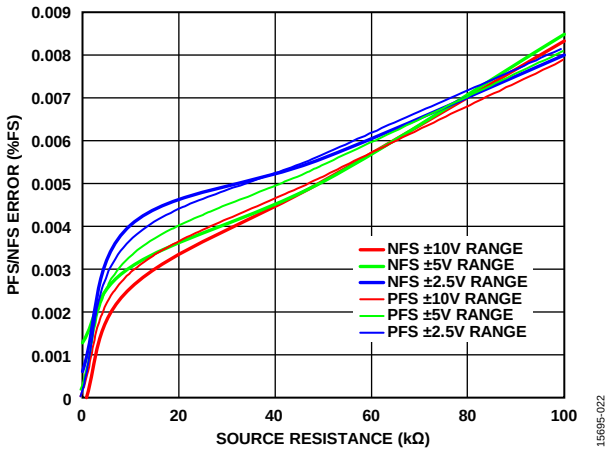


Figure 22. PFS/NFS Error vs. Source Resistance

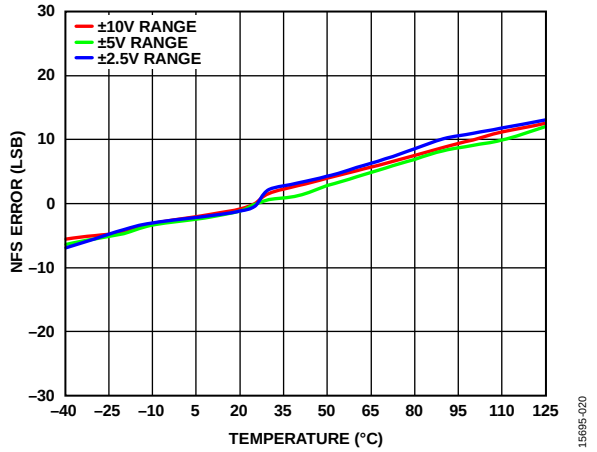


Figure 20. NFS Error vs. Temperature

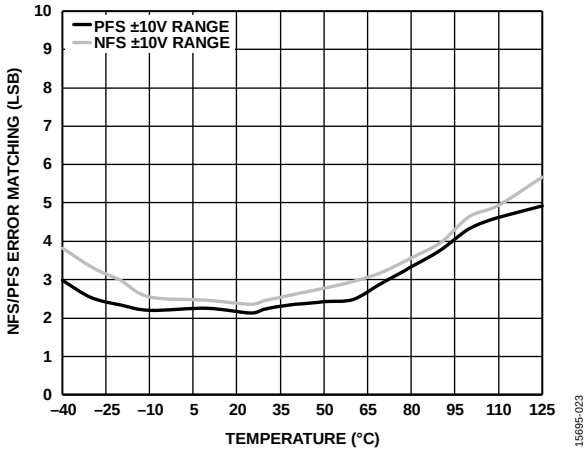


Figure 23. NFS/PFS Error Matching vs. Temperature

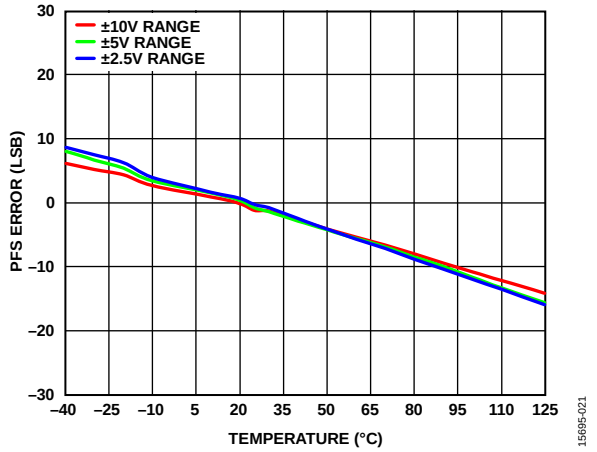


Figure 21. PFS Error vs. Temperature

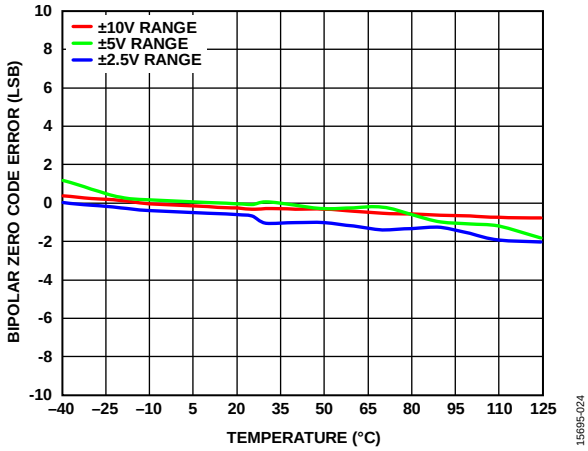


Figure 24. Bipolar Zero Code Error vs. Temperature

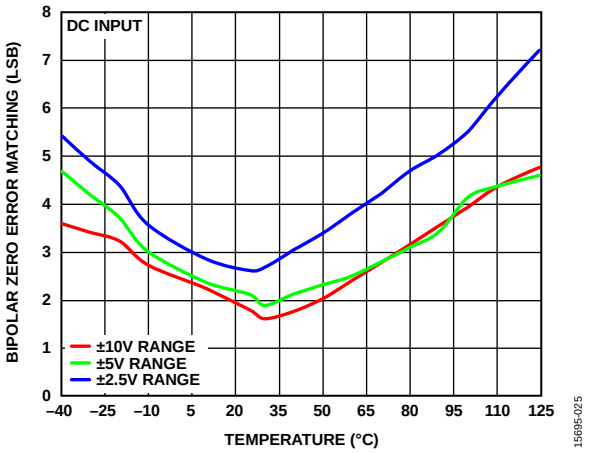


Figure 25. Bipolar Zero Error Matching vs. Temperature

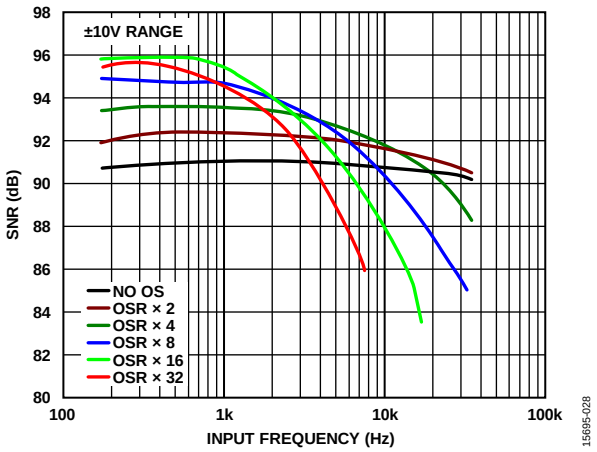


Figure 28. SNR vs. Input Frequency for Different Oversampling Rates, ±10 V Range

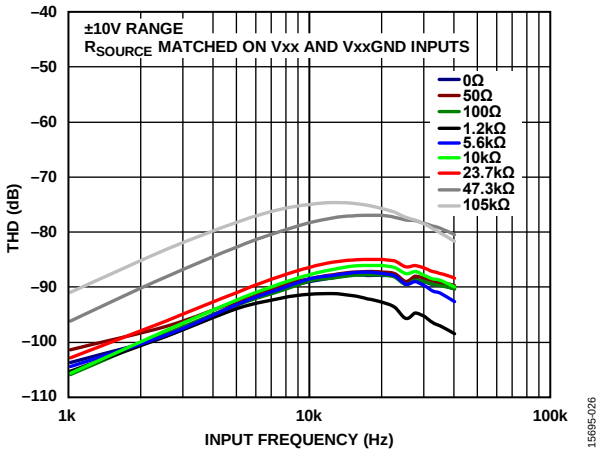


Figure 26. THD vs. Input Frequency for Various Source Impedances, ±10 V Range

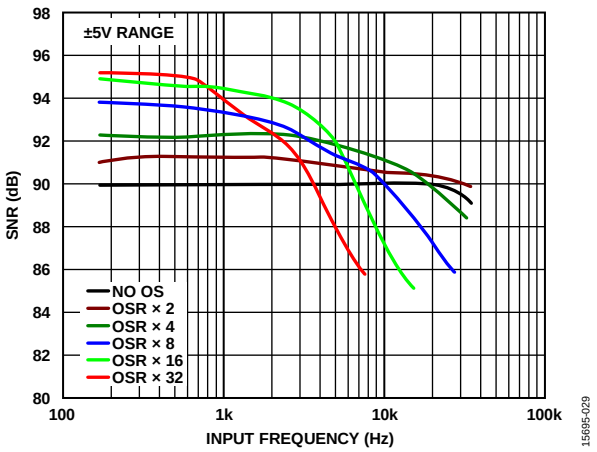


Figure 29. SNR vs. Input Frequency for Different Oversampling Rates, ±5 V Range

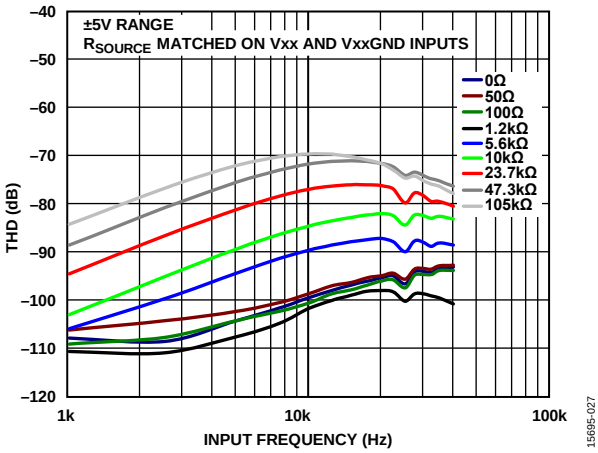


Figure 27. THD vs. Input Frequency for Various Source Impedances, ±5 V Range

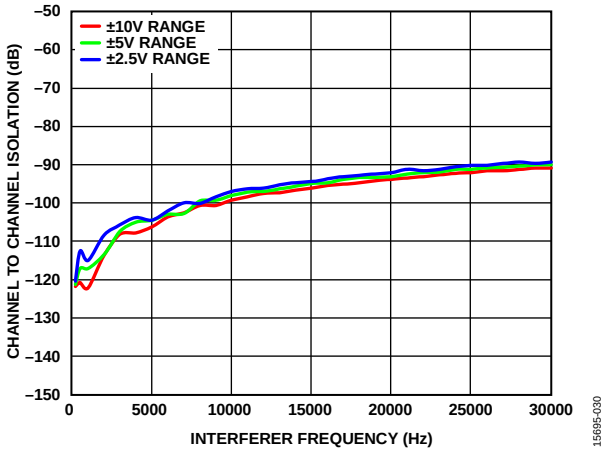


Figure 30. Channel to Channel Isolation vs. Interferer Frequency

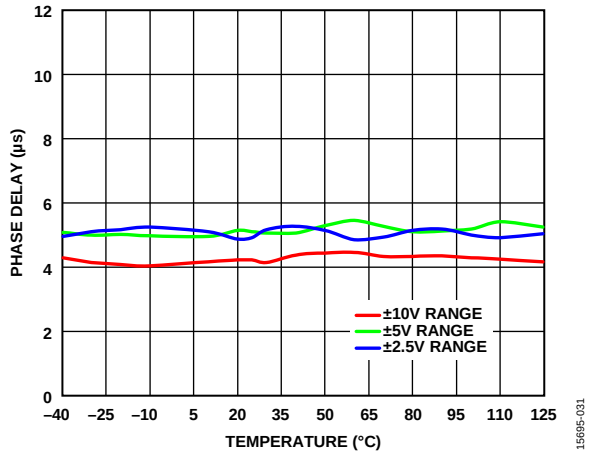


Figure 31. Phase Delay vs. Temperature

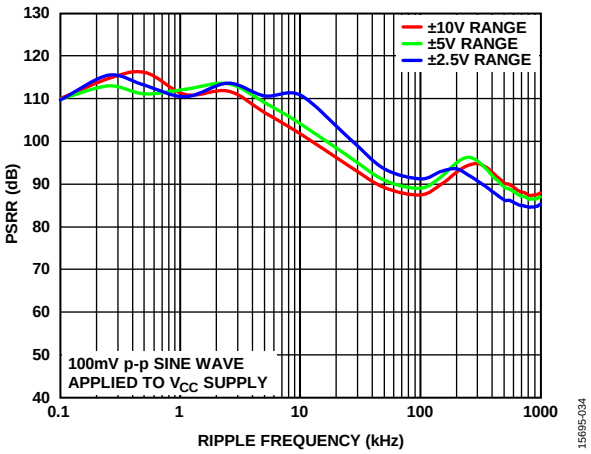


Figure 34. PSRR vs. Ripple Frequency

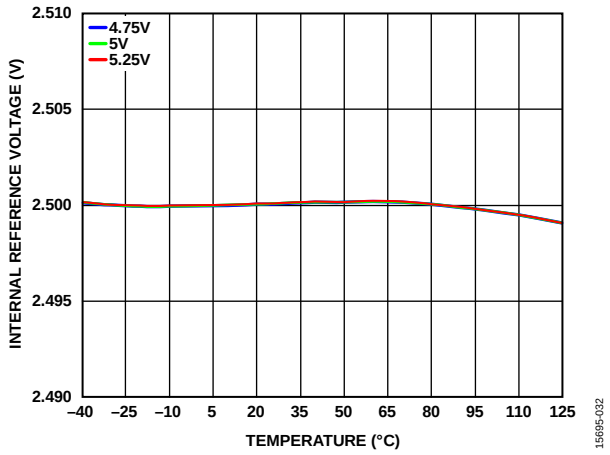


Figure 32. Internal Reference Voltage vs. Temperature for Various Supply Voltages

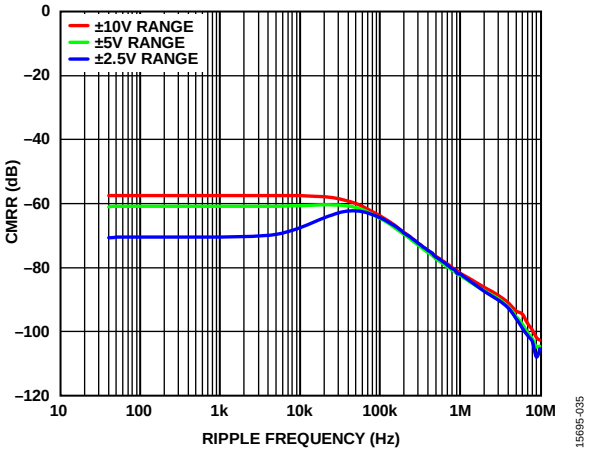


Figure 35. CMRR vs. Ripple Frequency

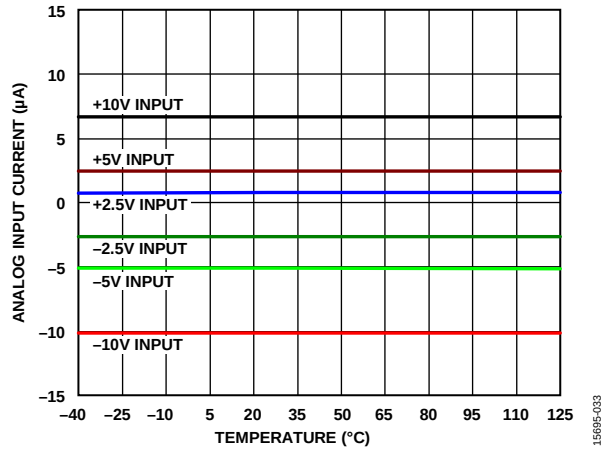


Figure 33. Analog Input Current vs. Temperature for Various Supply Voltages

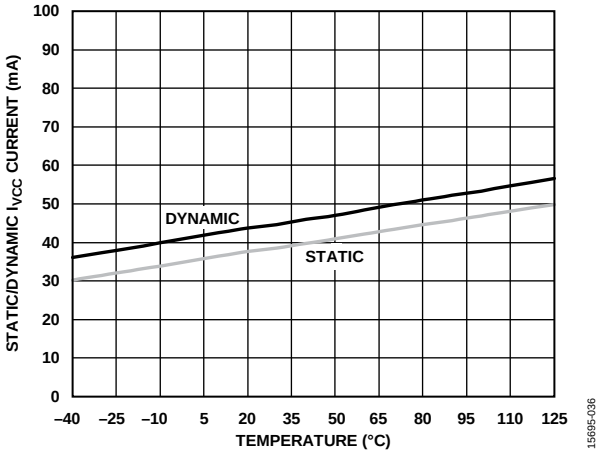


Figure 36. Static/Dynamic I_{VCC} Current vs. Temperature

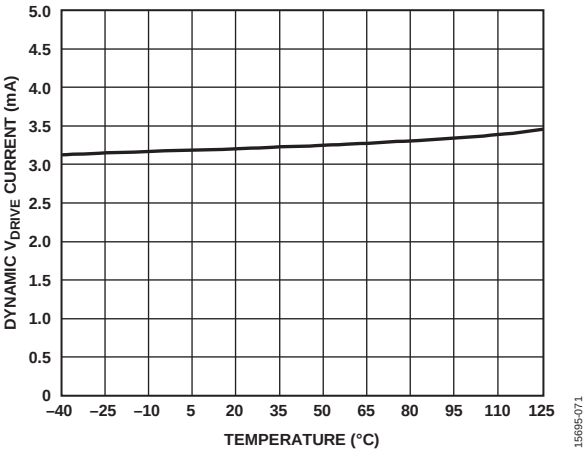


Figure 37. Dynamic V_{DRIVE} Current vs. Temperature

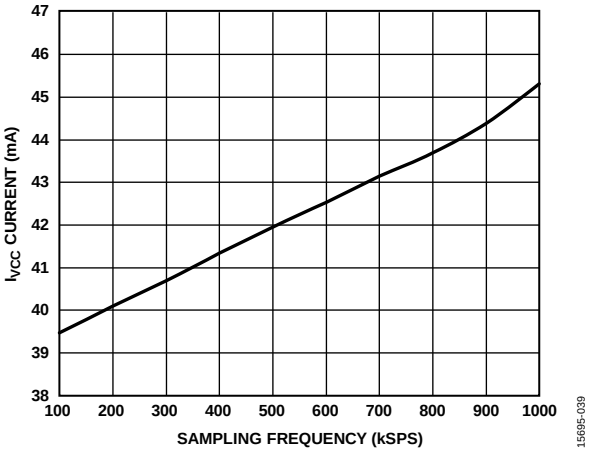


Figure 39. I_{VCC} Current vs. Sampling Frequency

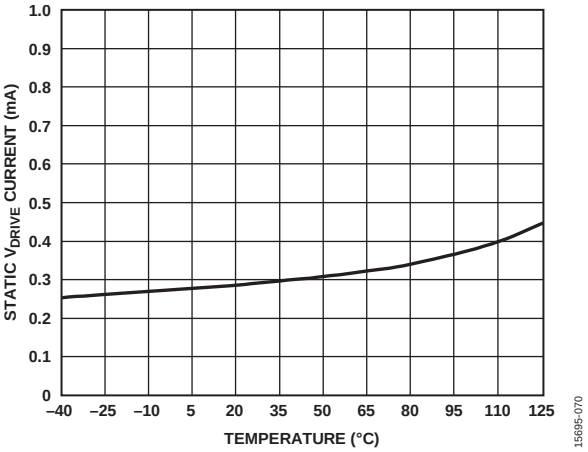


Figure 38. Static V_{DRIVE} Current vs. Temperature

TERMINOLOGY

Integral Nonlinearity (INL)
INL is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, at ½ LSB below the first code transition; and full scale, at ½ LSB above the last code transition.

Differential Nonlinearity (DNL)
DNL is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Bipolar Zero Code Error
Bipolar zero code error is the deviation of the midscale transition (all 1s to all 0s) from the ideal, which is 0 V − ½ LSB.

Bipolar Zero Code Error Matching
Bipolar zero code error matching is the absolute difference in bipolar zero code error between any two input channels.

Positive Full-Scale (PFS) Error
PFS error is the deviation of the actual last code transition from the ideal last code transition (10 V − 1½ LSB (9.99954), 5 V − 1½ LSB (4.99977), and 2.5 V − 1½ LSB (2.49989)) after bipolar zero code error is adjusted out. The PFS error includes the contribution from the internal reference buffer.

PFS Error Matching
PFS error matching is the absolute difference in positive full-scale error between any two input channels.

Negative Full-Scale (NFS) Error
NFS error is the deviation of the first code transition from the ideal first code transition (−10 V + ½ LSB (−9.99985), −5 V + ½ LSB (−4.99992) and −2.5 V + ½ LSB (−2.49996)) after the bipolar zero code error is adjusted out. The NFS error includes the contribution from the internal reference buffer.

NFS Error Matching
NFS error matching is the absolute difference in negative full-scale error between any two input channels.

Signal-to-Noise-and-Distortion Ratio (SINAD)
SINAD is the measured ratio of signal to noise and distortion at the output of the ADC. The signal is the rms value of the sine wave, and noise is the rms sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), including harmonics, but excluding dc.

Signal-to-Noise Ratio (SNR)
SNR is the measured ratio of signal to noise at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc.

The ratio is dependent on the number of quantization levels in the digitization process: the greater the number of levels, the smaller the quantization noise. The theoretical SNR for an ideal N-bit converter with a sine wave input is given by

$$SNR = (6.02N + 1.76)\ \text{dB}$$

where N is the number of bits.

Therefore, for a 16-bit converter, the SNR is 98 dB.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels (dB).

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$, excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it is determined by a noise peak.

Intermodulation Distortion (IMD)
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at the sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3. Intermodulation distortion terms are those for which neither m nor n is equal to 0. For example, the second-order terms include (fa + fb) and (fa − fb), and the third-order terms include (2fa + fb), (2fa − fb), (fa + 2fb), and (fa − 2fb).

The calculation of the intermodulation distortion is per the THD specification, where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in decibels (dB).

Power Supply Rejection Ratio (PSRR)
Variations in power supply affect the full-scale transition but not the linearity of the converter. Power supply rejection is the maximum change in full-scale transition point due to a change in power supply voltage from the nominal value. The PSRR is defined as the ratio of the power in the ADC output at full-scale frequency, f, to the power of a 100 mV p-p sine wave applied to the V_{CC} supply of the ADC of frequency, f_S.

$$PSRR\ (\text{dB}) = 10\log(Pf/Pf_S)$$

where:
Pf is equal to the power at frequency, f, in the ADC output.
Pf_S is equal to the power at frequency, f_S, coupled onto the V_{CC} supply.

AC Common-Mode Rejection Ratio (AC CMRR)
AC CMRR is defined as the ratio of the power in the ADC output at frequency, f, to the power of a sine wave applied to the common-mode voltage of Vxx and VxxGND at frequency, f_S.

$$AC\ CMRR\ (\text{dB}) = 10\log(Pf/Pf_S)$$

where:
Pf is the power at frequency, f, in the ADC output.
Pf_S is the power at frequency, f_S, in the ADC output.

Channel to Channel Isolation
Channel to channel isolation is a measure of the level of crosstalk between all input channels. It is measured by applying a full-scale sine wave signal, up to 160 kHz, to all unselected input channels and then determining the degree to which the signal attenuates in the selected channel with a 1 kHz sine wave signal applied.

Phase Delay
Phase delay is a measure of the absolute time delay between when an analog input is sampled by the converter and when the result associated with that sample is available to be read back from the ADC, including delay induced by the analog front end of the device.

Phase Delay Drift
Phase delay drift is the change in phase delay per unit temperature across the entire operating temperature of the device.

Phase Delay Matching
Phase delay matching is the maximum phase delay seen between any simultaneously sampled pair.

THEORY OF OPERATION

CONVERTER DETAILS

The AD7616-P is a DAS that employs a high speed, low power, charge redistribution, SAR ADC, and allows dual simultaneous sampling of 16 analog input channels. The analog inputs on the AD7616-P can accept true bipolar input signals. Analog input range options include ±10 V, ±5 V, and ±2.5 V. The AD7616-P operates from a single 5 V supply.

The AD7616-P contains input clamp protection, input signal scaling amplifiers, a first-order antialiasing filter, an on-chip reference, a reference buffer, a dual high speed ADC, a digital filter, a flexible sequencer, and a high speed parallel interface.

The AD7616-P can be operated in hardware or software mode by controlling the HW_RNGSELx pins. In hardware mode, the AD7616-P is configured by pin control. In software mode, the AD7616-P is configured by the control registers accessed via the parallel interface.

ANALOG INPUT

Analog Input Channel Selection

The AD7616-P contains dual, simultaneous sampling, 16-bit ADCs. Each ADC has eight analog input channels for a total of 16 analog input channels. Additionally, the AD7616-P has on-chip diagnostic channels to monitor the V_{CC} supply and an on-chip adjustable LDO regulator. Channels can be selected for conversion by using the CHSELx pins in hardware mode or via the channel register control in software mode. Software mode is required to sample the diagnostic channels. Channels can be selected dynamically or the AD7616-P has an on-chip sequencer to allow the channels for conversion to be preprogrammed. In hardware mode, simultaneous sampling is limited to the corresponding ADC A and ADC B analog input channels. For example, Channel V0A is always sampled with Channel V0B. In software mode, it is possible to select any ADC A channel with any ADC B channel for simultaneous sampling.

Analog Input Ranges

The AD7616-P can handle true bipolar, single-ended input voltages. The logic levels on the range select pins, HW_RNGSEL0 and HW_RNGSEL1, determine the analog input range of all analog input channels. If both range select pins are tied to a logic low, the analog input range is determined in software mode via the input range registers (see the Register Summary section for more details). In software mode, it is possible to configure an individual analog input range per channel.

Table 7. Analog Input Range Selection

Analog Input Range	HW_RNGSEL1	HW_RNGSEL0
Configured via the Input Range Registers	0	0
±2.5 V	0	1
±5 V	1	0
±10 V	1	1

In hardware mode, a logic change on these pins has an immediate effect on the analog input range; however, there is typically a settling time of approximately 120 µs in addition to the normal acquisition time requirement. The recommended practice is to hardwire the range select pins according to the desired input range for the system signals.

Analog Input Impedance

The analog input impedance of the AD7616-P is 1 MΩ, a fixed input impedance that does not vary with the AD7616-P sampling frequency. This high analog input impedance eliminates the need for a driver amplifier in front of the AD7616-P, allowing direct connection to the source or sensor.

Analog Input Clamp Protection

Figure 40 shows the analog input circuitry of the AD7616-P. Each analog input of the AD7616-P contains clamp protection circuitry. Despite single 5 V supply operation, this analog input clamp protection allows an input overvoltage of between −20 V and +20 V.

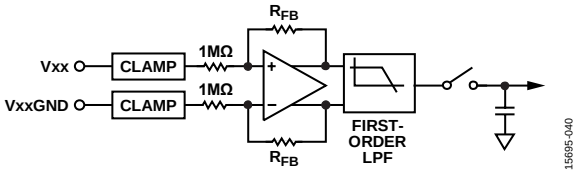


Figure 40. Analog Input Circuitry

Figure 41 shows the input clamp current vs. source voltage characteristic of the clamp circuit. For source voltages between −20 V and +20 V, no current flows in the clamp circuit. For input voltages that are greater than +20 V and less than −20 V, the AD7616-P clamp circuitry turns on.

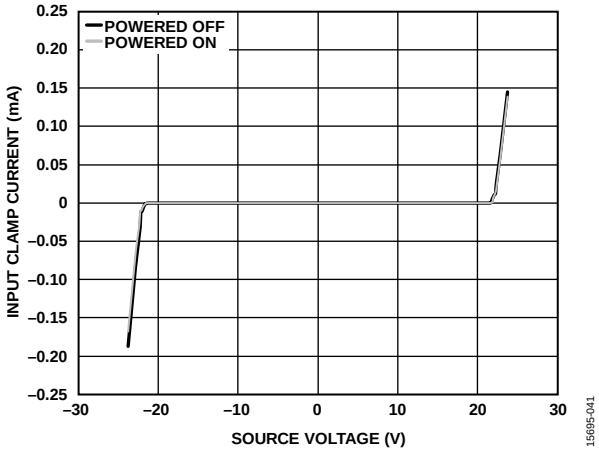


Figure 41. Input Protection Clamp Profile, Input Clamp Current vs. Source Voltage

Place a series resistor on the analog input channels to limit the current to ±10 mA for input voltages greater than +20 V and less than −20 V. In an application where there is a series resistance on an analog input, VxA or VxB, a corresponding resistance is required on the analog input ground channel, VxAGND or VxBGND (see Figure 42). If there is no corresponding resistor on

the VxAGND or VxBGND channel, an offset error occurs on that channel. Use the input overvoltage clamp protection circuitry to protect the AD7616-P against transient overvoltage events. It is not recommended to leave the AD7616-P in a condition where the clamp protection circuitry is active in normal or power-down conditions for extended periods.

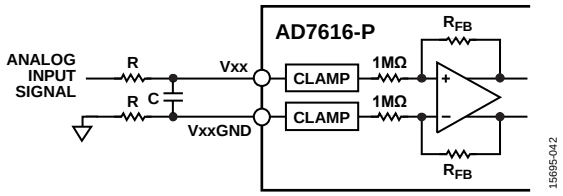


Figure 42. Input Resistance Matching on the Analog Input

Analog Input Antialiasing Filter

An analog antialiasing filter (first-order Butterworth) is also provided on the AD7616-P. Figure 43 and Figure 44 show the frequency and phase response, respectively, of the analog antialiasing filter. The typical corner frequency in the ±10 V range is 39 kHz, and 33 kHz in the ±5 V range.

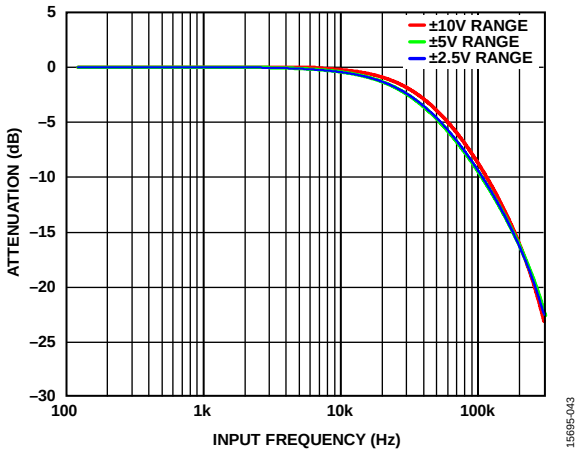


Figure 43. Analog Antialiasing Filter Frequency Response

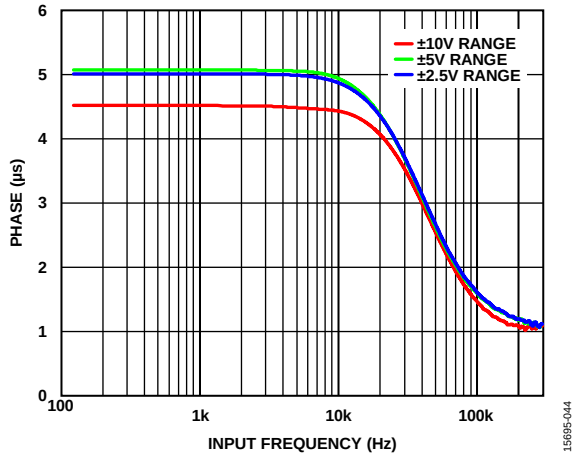
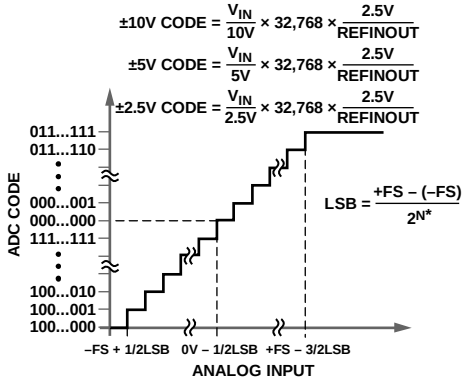


Figure 44. Analog Antialiasing Filter Phase Response

ADC TRANSFER FUNCTION

The output coding of the AD7616-P is twos complement. The designed code transitions occur midway between successive integer LSB values, that is, 1/2 LSB and 3/2 LSB. The LSB size is full-scale range ÷ 65,536 for the AD7616-P. The ideal transfer characteristics for the AD7616-P are shown in Figure 45. The LSB size is dependent on the analog input range selected.



	+FS	MIDSCALE	–FS	LSB
±10V RANGE	+10V	0V	–10V	305µV
±5V RANGE	+5V	0V	–5V	152µV
±2.5V RANGE	+2.5V	0V	–2.5V	76µV

*WHERE N IS THE NUMBER OF BITS OF THE CONVERTER

15695-045

Figure 45. Transfer Characteristics

INTERNAL/EXTERNAL REFERENCE

The AD7616-P can operate with either an internal or external reference. The device contains an on-chip, 2.5 V band gap reference. The REFINOUT pin allows access to the 2.5 V reference that generates the on-chip 4.096 V reference internally, or it allows an external reference of 2.5 V to be applied to the AD7616-P. An externally applied reference of 2.5 V is also amplified to 4.096 V using the internal buffer. This 4.096 V buffered reference is the reference used by the SAR ADC.

The REFSEL pin is a logic input pin that allows the user to select between the internal reference and an external reference. If this pin is set to logic high, the internal reference is selected and enabled. If this pin is set to logic low, the internal reference is disabled and an external reference voltage must be applied to the REFINOUT pin.

The internal reference buffer is always enabled. After a full reset, the AD7616-P operates in the reference mode selected by the REFSEL pin. Decoupling is required on the REFINOUT pin for both the internal and external reference options. A 100 nF, X8R ceramic capacitor is required on the REFINOUT pin to REFINOUTGND.

The AD7616-P contains a reference buffer configured to amplify the reference voltage to ~4.096 V. A 10 µF, X5R ceramic capacitor is required between REFCAP and REFGND. The reference voltage available at the REFINOUT pin is 2.5 V. When the AD7616-P is configured in external reference mode, the REFINOUT pin is a high input impedance pin.

If the internal reference is to be applied elsewhere within the system, it must first be buffered externally.

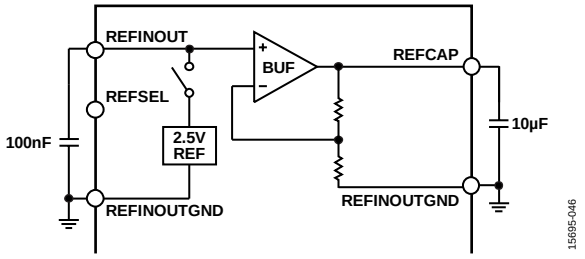


Figure 46. Reference Circuitry

SHUTDOWN MODE

The AD7616-P enters shutdown mode by keeping the RESET pin low for greater than 1.2 µs. When the RESET pin is set from low to high, the device exits shutdown mode and enters normal mode.

When the AD7616-P is placed in shutdown mode, the current consumption is typically 78 µA and the power-up time to perform a write to the device is approximately 240 µs. The power-up time to perform a conversion is 15 ms. In shutdown mode, all circuitry is powered down and all registers are cleared and reset to their default values.

DIGITAL FILTER

The AD7616-P contains an optional digital, first-order sinc filter for use in applications where slower throughput rates are in use or where higher SNR or dynamic range is desirable.

The OSR of the digital filter is controlled in software via the OS bits in the configuration register. In software mode, oversampling is enabled for all channels after the OS bits are set in the configuration register.

Table 8 provides the oversampling bit decoding to select the different oversample rates. In addition to the oversampling function, the output result is decimated to 16-bit resolution.

If the OS bits are set to select an OSR of eight, the next CONVST rising edge takes the first sample for the selected channel, and the remaining seven samples for that channel are taken with an internally generated sampling signal. These samples are then averaged to yield an improvement in SNR performance. As the OS ratio increases, the −3 dB frequency is reduced, and the allowed sampling frequency is also reduced. The conversion time extends as the oversampling rate is increased, and the BUSY signal scales with oversampling rates. Acquisition and conversion time increase linearly with the OSR.

If oversampling is enabled with the sequencer or in burst mode, the extra samples are gathered for a given channel before the sequencer moves on to the next channel.

Table 8 shows the typical SNR performance of the device for each permissible OSR. The input tone used is a 100 Hz sine wave for the three input ranges of the device. A plot of SNR vs. OSR is shown in Figure 47.

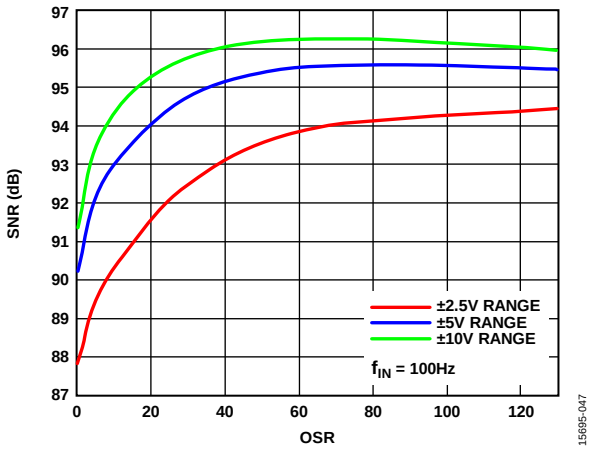


Figure 47. Typical SNR vs. OSR for All Analog Input Ranges

Table 8. Oversampling Bit Decoding

OS Bits	OSR	Typical SNR (dB)			−3 dB Bandwidth (kHz), All Ranges
		±2.5 V Range	±5 V Range	±10 V Range	
000	No oversampling	87.5	89.7	90.8	37
001	2	88.1	90.6	91.8	36.5
010	4	89	91.6	92.9	35
011	8	89.9	92.6	93.9	30.5
100	16	91	93.6	94.9	22
101	32	92.6	94.8	95.8	13.2
110	64	93.9	95.5	96.2	7.2
111	128	94.4	95.4	95.9	3.6

APPLICATIONS INFORMATION

FUNCTIONALITY OVERVIEW

The AD7616-P has two main modes of operation: hardware mode and software mode. Depending on the mode of operation, certain functionality may not be available. Full functionality is available in software mode; restricted functionality is available in hardware mode. Table 9 shows the functionality available in the different modes of operation.

Table 9. Available Functionality

	Operation Mode[1]	
Functionality	**Software Mode (HW_RNGSELx = 00)**	**Hardware Mode (HW_RNGSELx ≠ 00)**
Internal/External Reference	Yes	Yes
Selectable Analog Input Ranges		
Individual Channel Configuration	Yes	No
Common Channel Configuration	No	Yes
Sequential Sequencer	Yes	Yes
Fully Configurable Sequencer	Yes	No
Burst Mode	Yes	Yes
On-Chip Oversampling	Yes	No
Cyclic redundancy check (CRC)	Yes	No
Diagnostic Channel Conversion	Yes	No
Hardware Reset	Yes	Yes
Register Access	Yes	No

[1] Yes means available; no means not available.

POWER SUPPLIES

The AD7616-P has two independent power supplies, V_{CC} and V_{DRIVE}, that supply the analog circuitry and digital interface, respectively. Decouple both the V_{CC} supply and the V_{DRIVE} supply with a 10 µF capacitor in parallel with a 100 nF capacitor.

Additionally, these supplies are regulated by two internal LDO regulators. The analog LDO (ALDO) typically supplies 1.87 V. Decouple the ALDO with a 10 µF capacitor between the REGCAP and REGGND pins. The digital LDO (DLDO) typically supplies 1.89 V. Decouple the DLDO with a 10 µF capacitor between the REGCAPD and REGGNDD pins.

The AD7616-P is robust to power supply sequencing. The recommended sequence is to power up V_{DRIVE} first, followed by V_{CC}. Hold $\overline{RESET}$ low until both supplies are stabilized.

TYPICAL CONNECTIONS

Figure 48 shows the typical connections required for correct operation of the AD7616-P. Decouple the V_{CC} and V_{DRIVE} supplies as shown in Figure 48. Place the smaller, 0.1 µF capacitor as close to the supply pin as possible, with the larger, 10 µF bulk capacitor in parallel. Decouple the reference and LDO regulators as shown in Figure 48 and as described in Table 6.

The analog input pins require a matched resistance, R, on both the VxA and VxAGND (similarly, VxB and VxBGND) inputs to avoid a gain error on the analog input channels caused by an impedance mismatch.

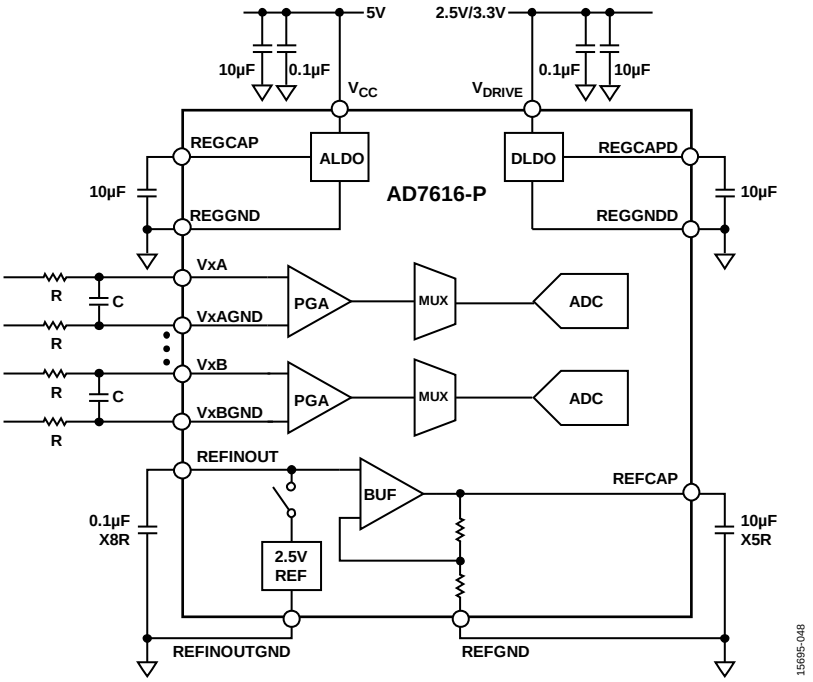


Figure 48. Typical External Connections

DEVICE CONFIGURATION

OPERATIONAL MODE

The mode of operation, hardware mode or software mode, is configured when the AD7616-P is released from full reset. The logic level of the HW_RNGSELx pins when the $\overline{\text{RESET}}$ pin transitions from low to high determines the operational mode. The HW_RNGSELx pins are dual function. If HW_RNGSELx = 0b00, the AD7616-P enters software mode. Any other combination of the HW_RNGSELx configures the AD7616-P to hardware mode and the analog input range is configured as per Table 7. After software mode is configured, the logic level of the HW_RNGSELx signals is ignored. After an operational mode is configured, a full reset via the $\overline{\text{RESET}}$ pin is required to exit the operational mode and to set up an alternative mode. If hardware mode is selected, all further device configuration is via pin control. Access to the on-chip registers is prohibited in hardware mode. In software mode, the interface and reference configuration must be configured via pin control, but all further device configuration is via register access only.

INTERNAL/EXTERNAL REFERENCE

The internal reference is enabled or disabled when the AD7616-P is released from a full reset. The logic level of the REFSEL signal when the $\overline{\text{RESET}}$ pin transitions from low to high configures the reference. After the reference is configured, changes to the logic level of the REFSEL signal are ignored. If the REFSEL signal is set to 1, the internal reference is enabled. If REFSEL is set to Logic 0, the internal reference is disabled and an external reference must be supplied to the REFINOUT pin for correct operation of the AD7616-P. A full reset via the $\overline{\text{RESET}}$ pin is required to exit the operational mode and set up an alternative mode.

Connect a 100 nF capacitor between the REFINOUT and REFINOUTGND pins. If using an external reference, place a 10 kΩ band limiting resistor in series between the reference and the REFINOUT pin of the AD7616-P.

HARDWARE MODE

If hardware mode is selected, the available functionality is restricted and all functionality is configured via pin control. The logic level of the following signals is checked after a full reset to configure the functionality of the AD7616-P: CRC, BURST, and SEQEN. Table 10 provides a summary of the signals that are latched by the device on the release of a full reset, depending on the mode of operation chosen. After the device is configured, a full reset via the $\overline{\text{RESET}}$ pin is required to exit the configuration and set up an alternative configuration.

The CHSELx pins are read at reset to determine the initial analog input channel pair to acquire for conversion or to configure the initial settings for the sequencer. The channel pair selected for conversion or the hardware sequencer can be reconfigured during normal operation by setting and maintaining the CHSELx signal level before the CONVST rising edge until the BUSY falling edge.

The HW_RNGSELx signals control the analog input range for all 16 analog input channels. A logic change on these pins has an immediate effect on the analog input range; however, the typical settling time is approximately 120 µs, in addition to the normal acquisition time requirement, t_{ACQ}. The recommended practice is to hardwire the range select pins according to the desired input range for the system signals.

Access to the on-chip registers is prohibited in hardware mode.

Table 10. Summary of Latched Hardware Signals[1]

	Latched at Full Reset		Read at Reset		Read During Busy		Edge Driven	
Signal	**HW Mode**	**SW Mode**	**HW Mode**	**SW Mode**	**HW Mode**	**SW Mode**	**HW Mode**	**SW Mode**
REFSEL	Yes	Yes	N/A	N/A	N/A	N/A	N/A	N/A
SEQEN	Yes	No	N/A	N/A	N/A	N/A	N/A	N/A
HW_RNGSELx (Range Change)	N/A	N/A	Yes	Yes	N/A	N/A	Yes	No
HW_RNGSELx (Hardware (HW) or Software (SW) Mode)	Yes	Yes	N/A	N/A	N/A	N/A	N/A	N/A
$\overline{\text{PAR}}$	Yes	Yes	N/A	N/A	N/A	N/A	N/A	N/A
BURST	Yes	No	N/A	N/A	N/A	N/A	N/A	N/A
CHSELx	N/A	N/A	Yes	No	Yes	No	N/A	N/A

[1] Blank cells in Table 10 mean not applicable.

SOFTWARE MODE

If software mode is selected and the reference is configured, all other configuration settings in the AD7616-P are controlled via the on-chip registers. All functionality of the AD7616-P is available when software mode is selected. Table 10 provides a summary of the signals that are latched by the device on the release of a full reset, depending on the mode of operation chosen.

RESET FUNCTIONALITY

The AD7616-P has two reset modes: full or partial. The reset mode selected is dependent on the length of the reset low pulse. A partial reset requires the $\overline{\text{RESET}}$ pin to be held low between 40 ns and 500 ns. After 120 ns from the release of $\overline{\text{RESET}}$, the device is fully functional and a conversion can be initiated. A full reset requires the $\overline{\text{RESET}}$ pin to be held low for a minimum of 1.2 µs. After 15 ms from the release of $\overline{\text{RESET}}$, the device is completely reconfigured and a conversion can be initiated.

A partial reset reinitializes the following modules:

- Sequencer
- Digital filter
- Both SAR ADCs

The current conversion result is discarded on completion of a partial reset. The partial reset does not affect the register values programmed in software mode or the latches that store the user configuration in both hardware and software modes. A dummy conversion is required in software mode after a partial reset.

A full reset returns the device to its default power-on state. The following features are configured when the AD7616-P is released from full reset:

- Hardware mode or software mode
- Internal/external reference
- Interface type

On power-up, the $\overline{\text{RESET}}$ signal can be released as soon as both the V_{CC} and V_{DRIVE} supplies are stable. The logic level of the HW_RNGSELx, REFSEL, and $\overline{\text{PAR}}$ pins when the $\overline{\text{RESET}}$ pin is released after a full reset determines the configuration.

If hardware mode is selected, the functionality determined by the BURST and SEQEN signals is also latched when the $\overline{\text{RESET}}$ pin transitions from low to high in full reset mode, as shown in Figure 3. After the functionality is configured, changes to these signals are ignored. In hardware mode, the analog input range (HW_RNGSELx signals) can be configured during a full reset, a partial reset, or during normal operation, but hardware/software mode selection requires a full reset to reconfigure when latched.

In hardware mode, the CHSELx and HW_RNGSELx pins are read upon release of a full or partial reset to perform the following actions:

- Determine the initial analog input channel pair to acquire for conversion.
- Configure the initial settings for the sequencer.
- Select the analog input voltage range.

The CHSELx and HW_RNGSELx signals are not latched. The channel pair selected for conversion, or the hardware sequencer, can be reconfigured during normal operation by setting and maintaining the CHSELx signal level before the CONVST rising edge, and ensuring the signal level remains constant until after BUSY transitions low again. See the Channel Selection section for further details.

In software mode, all additional functionality is configured by controlling the on-chip registers.

PIN FUNCTION OVERVIEW

There are several dual-function pins on the AD7616-P. Their functionality is dependent on the mode of operation selected by the HW_RNGSELx pins. Table 11 outlines the pin functionality in the different modes of operation and interface modes.

Table 11. Pin Functionality Overview

	Operation Mode	
Pins	**Software (HW_RNGSELx = 00)**	**Hardware (HW_RNGSELx ≠ 00)**
CHSELx	No function, connect to DGND	CHSELx
$\overline{\text{RD}}$	$\overline{\text{RD}}$	$\overline{\text{RD}}$
$\overline{\text{WR}}$/BURST	$\overline{\text{WR}}$	BURST
DB15 to DB0	DB15 to DB0	DB15 to DB0
HW_RNGSELx	HW_RNGSELx, connect to DGND	HW_RNGSELx, configure analog input range
SEQEN	No function, connect to DGND	SEQEN
REFSEL	REFSEL	REFSEL

DIGITAL INTERFACE

CHANNEL SELECTION

Hardware Mode

The logic level of the CHSELx signals determines the channel pair for conversion; see Table 12 for signal decoding information. The CHSELx signals at the time that either full or partial reset is released determine the initial channel pair to sample. After a reset, the logic levels of the CHSELx signals are examined during the BUSY high period to set the channel pair for the next conversion. The CHSELx signal level must be set before CONVST goes from low to high and must be maintained until BUSY goes from high to low to indicate a conversion is complete. See Figure 49 for further details.

Software Mode

In software mode, the channels for conversion are selected using the channel register. On power-up or after a reset, the default channels selected for conversion are Analog Input V0A and Analog Input V0B.

Table 12. CHSELx Pin Decoding

Channel Selection Input Pin			
CHSEL0	CHSEL1	CHSEL2	Analog Inputs for Conversion
0	0	0	V0A, V0B
0	0	1	V1A, V1B
0	1	0	V2A, V2B
0	1	1	V3A, V3B
1	0	0	V4A, V4B
1	0	1	V5A, V5B
1	1	0	V6A, V6B
1	1	1	V7A, V7B

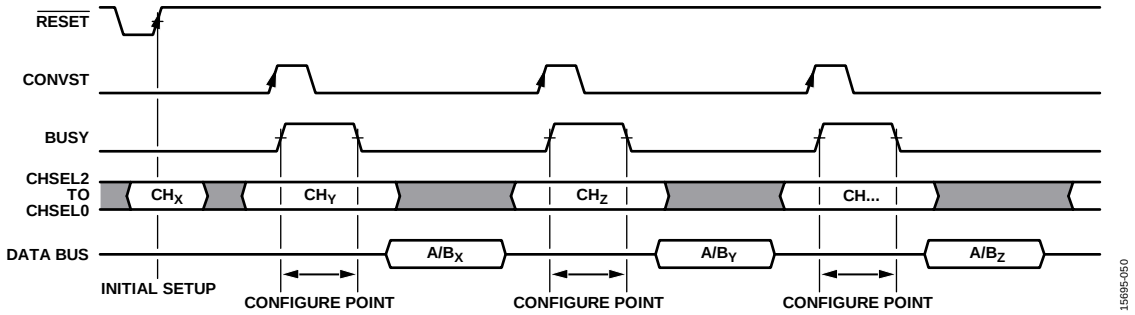


Figure 49. Hardware Mode Channel Conversion Setting

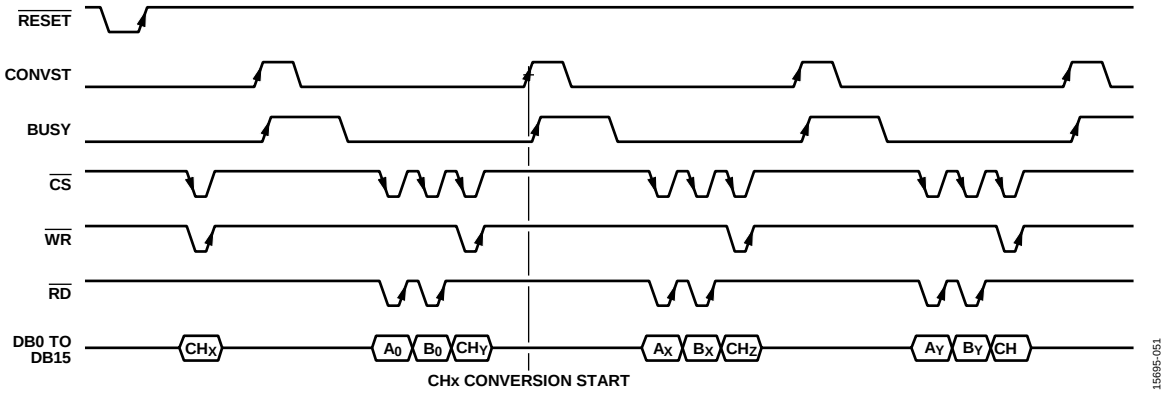


Figure 50. Software Mode Channel Conversion Setting

PARALLEL INTERFACE

The parallel interface reads the conversion results and, in software mode, configures/reads back the on-chip registers. Data can be read from the AD7616-P via the parallel data bus with standard $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$ signals.

Reading Conversion Results

The CONVST signal initiates the conversion process. A low to high transition on the CONVST signal initiates a conversion of the selected inputs. The BUSY signal goes high to indicate a conversion is in progress. When the BUSY signal transitions from high to low to indicate that a conversion is complete, it is possible to read back conversion results on the parallel interface.

Data can be read from the AD7616-P via the parallel data bus with standard $\overline{CS}$ and $\overline{RD}$ signals. The $\overline{CS}$ and $\overline{RD}$ input signals are internally gated to enable the conversion result onto the data bus. The data lines, DB15 to DB0, leave their high impedance state when both $\overline{CS}$ and $\overline{RD}$ are logic low.

The rising edge of the $\overline{CS}$ input signal three-states the bus, and the falling edge of the $\overline{CS}$ input signal takes the bus out of the high impedance state. $\overline{CS}$ is the control signal that enables the data lines; it is the function that allows multiple AD7616-P devices to share the same parallel data bus.

The number of required read operations depends on the device configuration. A minimum of two reads are required to read the conversion result for the simultaneously sampled ADC A and ADC B channels. If additional functions such as CRC, status, and burst mode are enabled, the number of required readbacks increases accordingly.

The $\overline{RD}$ pin reads data from the output conversion results register. Applying a sequence of $\overline{RD}$ pulses to the $\overline{RD}$ pin of the AD7616-P clocks the conversion results out from each channel onto the parallel bus, DB15 to DB0. The first $\overline{RD}$ falling edge after BUSY goes low clocks out the conversion result from ADC A. The next $\overline{RD}$ falling edge updates the bus with the ADC B conversion result.

Writing Register Data

In software mode, all the read/write registers in the AD7616-P can be written to over the parallel interface. A register write command is performed by a single 16-bit parallel access via the parallel bus (DB15 to DB0), $\overline{CS}$, and $\overline{WR}$ signals. Provide data written to the AD7616-P on the DB15 to DB0 inputs, with DB0 as the LSB of the data-word. The format for a write command is shown in Figure 51. Bit D15 must be set to 1 to select a write command. Bits[D14:D9] contain the register address, REGADDR[5:0]. The subsequent nine bits (Bits[D8:D0]) contain the data to be written to the selected register. See the Register Summary section for the complete list of register addresses. Data is latched into the device on the rising edge of $\overline{WR}$.

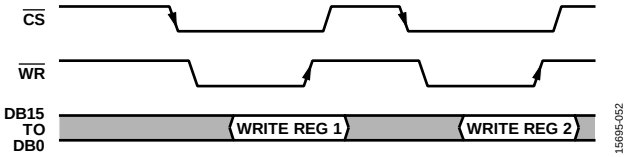


Figure 51. Parallel Interface Register Write

Reading Register Data

All the registers in the device can be read over the parallel interface. A register read is performed by first writing the address of the register to be read to the AD7616-P. The format for a register read command is shown in Figure 53. Bit D15 must be set to 0 to select a read command. Bits[D14:D9] contain the register address. The subsequent nine bits (Bits[D8:D0]) are ignored. The read command is latched into the AD7616-P on the rising edge of $\overline{WR}$. This latch transfers the relevant register data to the output register. The register data can then be read on the DB15 to DB0 pins by using a standard read command. See Figure 53 for additional information.

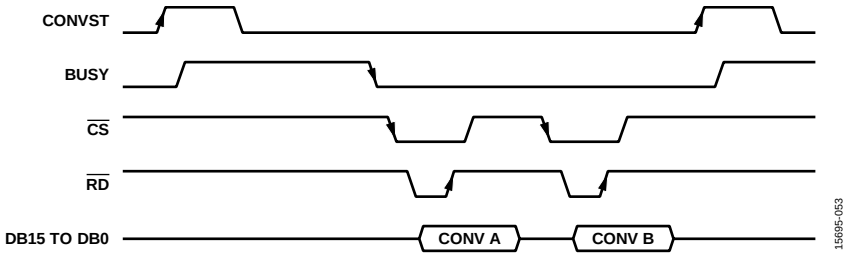


Figure 52. Parallel Interface Conversion Readback

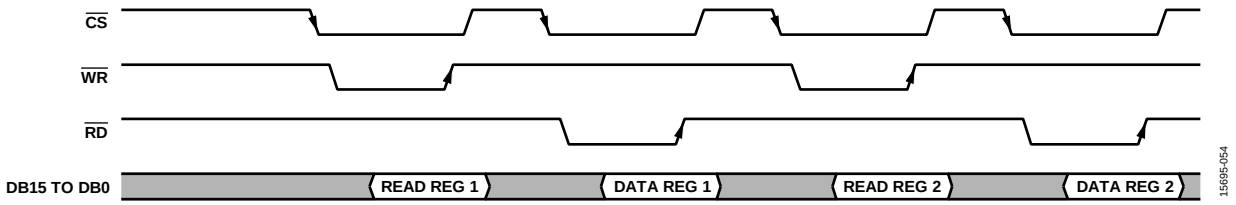


Figure 53. Parallel Interface Register Read

Table 13. Write Command Message Configuration

MSB															LSB
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
W/R	REGADDR[5:0]						Data[8:0]								
1	Register address						Data to write								

Table 14. Read Command Message Configuration

MSB															LSB
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
W/R	REGADDR[5:0]						Data[8:0]								
0	Register address						Do not care								

SEQUENCER

The AD7616-P features a highly configurable on-chip sequencer. The functionality and configuration of the sequencer is dependent on the mode of operation of the AD7616-P.

In hardware mode, the sequencer is sequential only. The sequencer always starts converting at Analog Input V0A and Analog Input V0B and converts each subsequent channel up to the configured end channel.

In software mode, the sequencer has additional functionality and configurability. The sequencer stack has 32 uniquely configurable sequence steps, allowing any channel order to be programmed. Additionally, any VxA analog input can be paired with any VxB analog input or diagnostic channel.

The sequencer can be operated with or without the burst function enabled. With the burst function enabled, only one CONVST pulse is required to convert every channel in a sequence. With burst mode disabled, one CONVST pulse is required for every conversion step in the sequence. See the Burst Sequencer section for additional details on operating in burst mode.

HARDWARE MODE SEQUENCER

In hardware mode, the sequencer is controlled by the SEQEN pin and the CHSELx pins. The sequencer is enabled or disabled when the AD7616-P is released from full reset. The logic level of the SEQEN pin when the $\overline{\text{RESET}}$ pin is released determines whether the sequencer is enabled or disabled (see Table 15 for settings). After the $\overline{\text{RESET}}$ pin is released, the function is fixed and a full reset via the $\overline{\text{RESET}}$ pin is required to exit the function and set up an alternative configuration.

Table 15. Hardware Mode Sequencer Configuration

SEQEN	Interface Mode
0	Sequencer disabled
1	Sequencer enabled

When the sequencer is enabled, the logic levels of the CHSELx pins determine the final channel pair of the sequence. The CHSELx pins at the time $\overline{\text{RESET}}$ is released determine the initial settings for the channels to convert in the sequence. To reconfigure the channels selected for conversion thereafter, set the CHSELx pins to the required setting for the duration of the final BUSY pulse before the current conversion sequence is complete. See Figure 54 for further details.

Table 16. CHSELx Pin Decoding Sequencer

Channel Selection Input Pin			Analog Inputs for Sequential Conversion
CHSEL0	CHSEL1	CHSEL2	
0	0	0	V0x only
0	0	1	V0x to V1x
0	1	0	V0x to V2x
0	1	1	V0x to V3x
1	0	0	V0x to V4x
1	0	1	V0x to V5x
1	1	0	V0x to V6x
1	1	1	V0x to V7x

SOFTWARE MODE SEQUENCER

In software mode, the AD7616-P contains a 32-layer fully configurable sequencer stack. Control of the sequencer is achieved by programming the configuration register and sequencer stack registers via the parallel interface.

Each stack layer can be individually programmed to pair any input from Analog Input VxA to any input from Analog Input VxB, or any diagnostic channel can be selected for conversion. The sequencer depth can be set to any length from 1 to 32 layers. The sequencer depth is controlled via the SSRENx bit. Set the SSRENx bit in the sequencer stack register corresponding to the last step required. The channels to convert are selected by programming the ASELx and BSELx bits in each sequence stack register for the depth required.

The sequencer is activated by setting the SEQEN bit in the configuration register to 1.

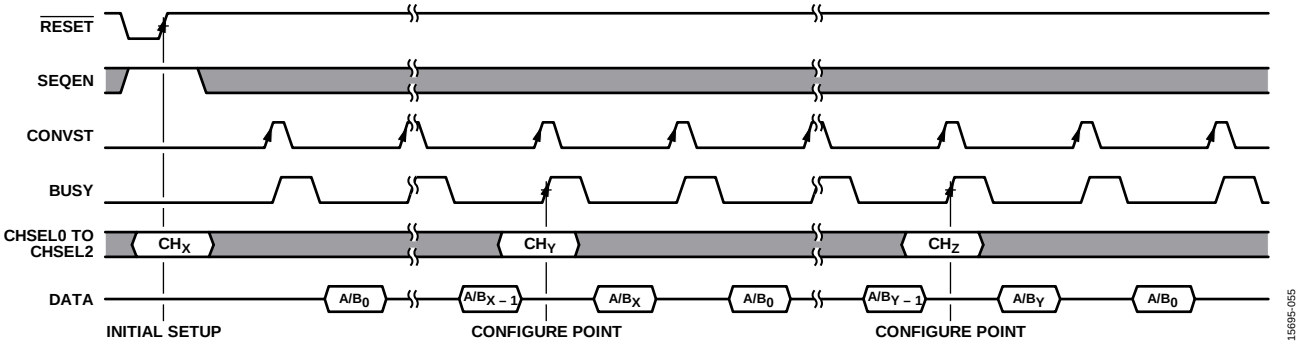


Figure 54. Hardware Mode Sequencer Configuration

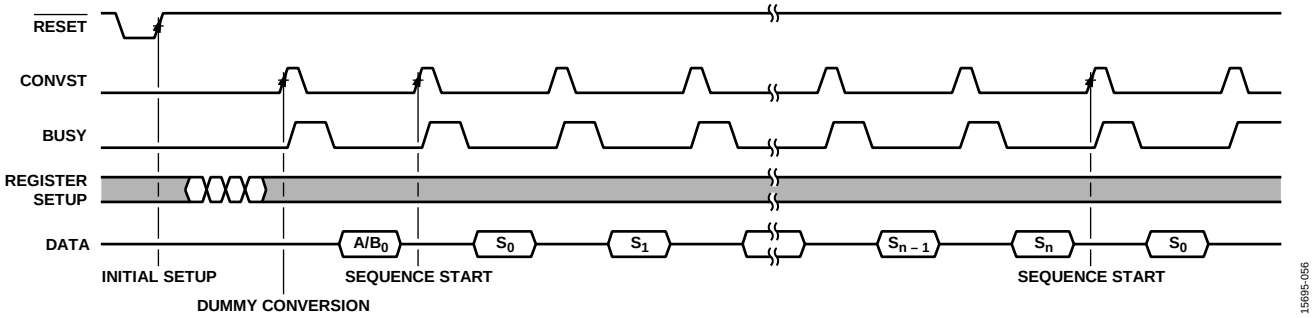


Figure 55. Software Mode Sequencer Configuration

To configure and enable the sequencer, it is recommended to complete the following procedure (see Figure 55):

1. Configure the analog input range for the required analog input channels.
2. Program the sequencer stack registers to select the channels for the sequence.
3. Set the SSRENx bit in the last required sequence step.
4. Set the SEQEN bit in the configuration register.
5. Provide a dummy CONVST pulse.
6. Cycle through CONVST pulses and conversion reads to step through each element of the sequencer stack.

The sequence automatically restarts from the first element in the sequencer stack with the next CONVST pulse.

Following a partial reset, the sequencer pointer is repositioned to the first layer of the stack, but the register programmed values remain unchanged.

BURST SEQUENCER

Burst mode avoids generating a CONVST pulse for each step in a sequence of conversions. One CONVST pulse converts every step in the sequence.

The burst sequencer is an additional feature that works in conjunction with the sequencer. If the burst function is enabled, one CONVST pulse initiates a conversion of all the channels configured in the sequencer. The burst function avoids generating a CONVST pulse for each step in a sequence of conversions, as is the case when the burst function is disabled.

Configuration of the burst function varies depending on the mode of operation: hardware or software mode. See the Hardware Mode Burst section and the Software Mode Burst section for specific details on configuring the burst function in each mode.

When configured, the burst sequence is initiated at the rising edge of CONVST. The BUSY pin goes high to indicate that a conversion is in progress. The BUSY pin remain highs until all conversions in the sequence are complete. The conversion results are available for readback after the BUSY pin goes low.

The number of data reads required to read all the data in the burst sequence is dependent on the length of the sequence configured. The conversion results are presented on the parallel data bus in the same order as the programmed sequence.

The throughput rate of the AD7616-P is limited in burst mode and dependent on the length of the sequence. Each channel pair requires an acquisition, conversion, and readback time. The time taken to complete a sequence with number of channel pairs, N, is estimated by

$$t_{BURST} = (t_{CONV} + 25\text{ ns}) + (N - 1)(t_{ACQ} + t_{CONV}) + N(t_{RB})$$

where:
t_{CONV} is the typical conversion time.
t_{ACQ} is typical acquisition time.
t_{RB} is the time required to read back the conversion results.

Hardware Mode Burst

Burst mode is enabled in hardware mode by setting the $\overline{\text{WR}}$/BURST pin to 1. The SEQEN pin must also be set to 1 to enable the sequencer.

In hardware mode, the burst sequencer is controlled by the BURST, SEQEN, and CHSELx pins. The burst sequencer is enabled or disabled when the AD7616-P is released from full reset. The logic level of the SEQEN pin and the BURST pin when the $\overline{\text{RESET}}$ pin is released determines whether the burst sequencer is enabled or disabled. After the $\overline{\text{RESET}}$ pin is released, the burst sequencer function is fixed and a full reset via the $\overline{\text{RESET}}$ pin is required to exit the function and set up an alternative configuration.

When the burst sequencer is enabled, the logic levels of the CHSELx pins determine the channels selected for conversion in the burst sequence. The CHSELx pins at the time $\overline{\text{RESET}}$ is released determine the initial settings for the channels to convert in the burst sequence. To reconfigure the channels selected for conversion after a reset, set the CHSELx pins to the required setting for the duration of the next BUSY pulse (see Figure 56 for further details).

Software Mode Burst

In software mode, the burst function is enabled by setting the BURSTEN bit in the configuration register to 1. This action must be performed when setting the SEQEN bit in the configuration register as outlined in the steps described in the Software Mode Sequencer section to configure the sequencer (see Figure 57 for additional information).

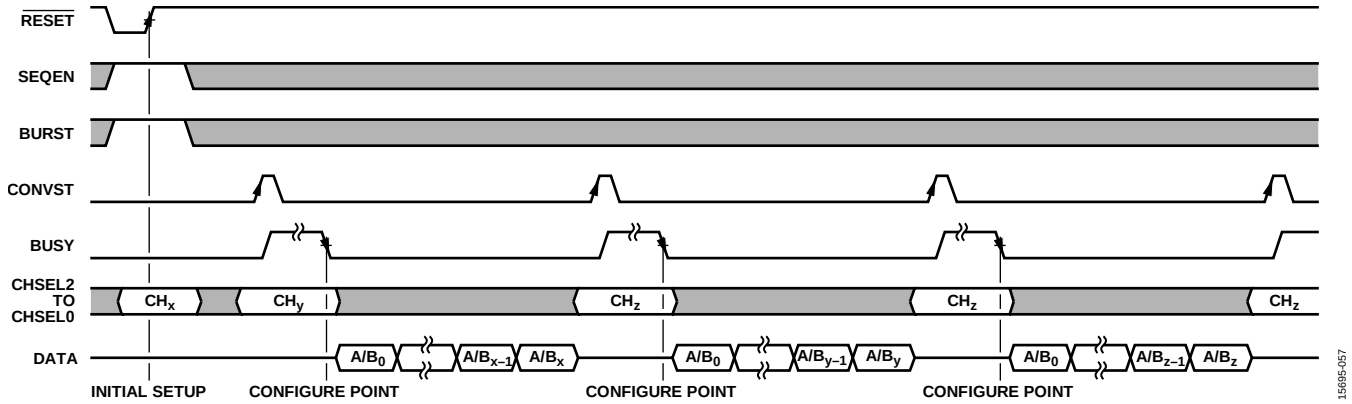


Figure 56. Burst Sequencer, Hardware Mode

Figure 57. Burst Sequencer, Software Mode

DIAGNOSTICS

DIAGNOSTIC CHANNELS

In addition to the 16 analog inputs, VxA and VxB, the AD7616-P can also convert the following diagnostic channels: V_{CC} and the analog ALDO voltage. The diagnostic channels are selected for conversion by programming the channel register (see the Channel Register section) to the corresponding channel identifier. Diagnostic channels can also be added to the sequencer stack in software mode, but only provide an accurate reading at throughput rates <250 kSPS. See Figure 58 for a plot of the deviation from the expected value vs. sampling frequency that can be expected when using the diagnostic channels.

The expected output for each channel is governed by the following transfer functions:

$$V_{CC}\ Code = \frac{\left(\left(4 \times V_{CC}\right) - V_{REF}\right) \times 32{,}768}{5 \times V_{REF}}$$

$$LDO\ Code = \frac{\left(\left(10 \times V_{ALDO}\right) - \left(7 \times V_{REF}\right)\right) \times 32{,}768}{10 \times V_{REF}}$$

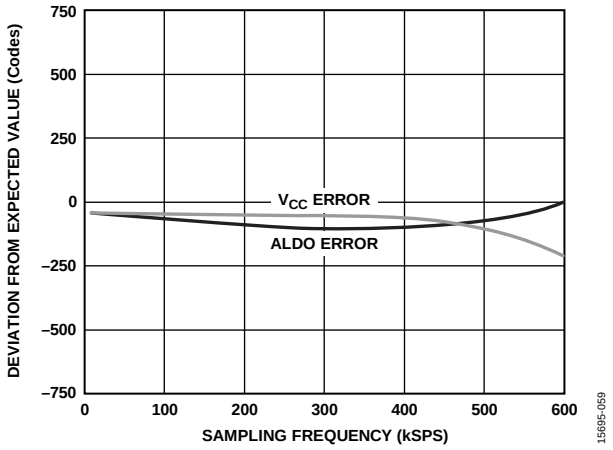


Figure 58. Deviation from Expected Value vs. Sampling Frequency

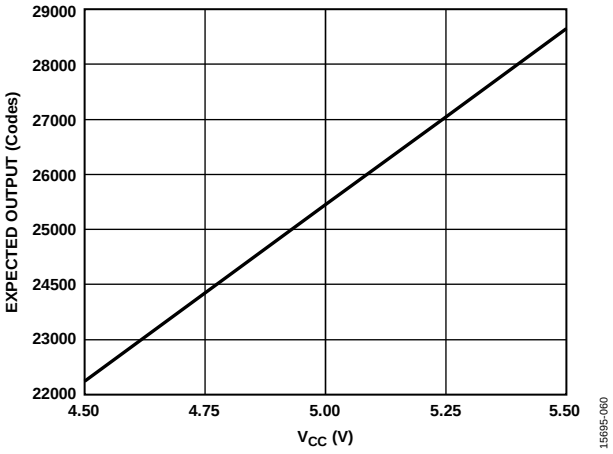


Figure 59. V_{CC} Diagnostic Transfer Function

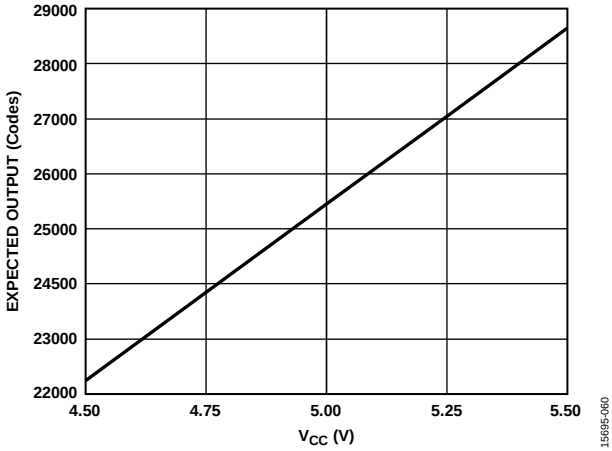


Figure 60. ALDO Diagnostic Transfer Function

INTERFACE SELF TEST

It is possible to test the integrity of the digital interface by selecting the communication self test channel in the channel register (see the Channel Register section).

Selecting the communication self test for conversion forces the conversion result register to a known fixed output. When the conversion code is read, Code 0xAAAA is output as the conversion code of ADC A, and Code 0x5555 is output as the conversion code of ADC B.

CRC

The AD7616-P has a CRC checksum mode to improve interface robustness by detecting errors in data. The CRC feature is available only in software mode. The CRC feature is not available in hardware mode. The CRC result is contained within the status register. Enabling the CRC feature enables the status register and vice versa.

The CRC function is enabled by setting either the CRCEN bit or the STATUSEN bit in the configuration register to 1 (see the Configuration Register section).

After being enabled, the CRC result is appended to the conversion result and consists of a 16-bit word, where the first eight bits contain the channel ID of the last channel pair converted and the last eight bits are the CRC result. The result is accessed via an extra read command, as shown in Figure 61.

If the CRC function is enabled, a CRC is calculated on the conversion results for Channel VxA and Channel VxB. The CRC is calculated and transferred on the parallel interface after the conversion results are transmitted, depending on the configuration of the device. The Hamming distance varies relative to the number of bits in the conversion result. For conversions with ≤119 bits, the Hamming distance is 4. For >119 bits, the Hamming distance is 1, that is, 1-bit errors are always detected.

The following is a pseudocode description of how the CRC is implemented in the AD7616-P:

```
crc = 8'b0;
i = 0;
x = number of conversion channel pairs;
for (i=0, i<x, i++) begin
crc1 = crc_out(An,Crc);
crc = crc_out(Bn,Crc1);
i = i +1;
end
```

where the function crc_out(data, crc) is

```
crc_out[0] = data[14] ^ data[12] ^ data[8] ^
data[7] ^ data[6] ^ data[0] ^ crc[0] ^
crc[4] ^ crc[6];
crc_out[1] = data[15] ^ data[14] ^ data[13]
^ data[12] ^ data[9] ^ data[6] ^ data[1] ^
data[0] ^ crc[1] ^ crc[4] ^ crc[5] ^ crc[6]
^ crc[7];
crc_out[2] = data[15] ^ data[13] ^ data[12]
^ data[10] ^ data[8] ^ data[6] ^ data[2] ^
data[1] ^ data[0] ^ crc[0] ^ crc[2] ^ crc[4]
^ crc[5] ^ crc[7];
crc_out[3] = data[14] ^ data[13] ^ data[11]
^ data[9] ^ data[7] ^ data[3] ^ data[2] ^
data[1] ^ crc[1] ^ crc[3] ^ crc[5] ^ crc[6];
crc_out[4] = data[15] ^ data[14] ^ data[12]
^ data[10] ^ data[8] ^ data[4] ^ data[3] ^
data[2] ^ crc[0] ^ crc[2] ^ crc[4] ^ crc[6]
^ crc[7];
crc_out[5] = data[15] ^ data[13] ^ data[11]
^ data[9] ^ data[5] ^ data[4] ^ data[3] ^
crc[1] ^ crc[3] ^ crc[5] ^ crc[7];
crc_out[6] = data[14] ^ data[12] ^ data[10]
^ data[6] ^ data[5] ^ data[4] ^ crc[2] ^
crc[4] ^ crc[6];
crc_out[7] = data[15] ^ data[13] ^ data[11]
^ data[7] ^ data[6] ^ data[5] ^ crc[3] ^
crc[5] ^ crc[7];
```

The initial CRC word used by the AD7616-P is an 8-bit word equal to zero. The XOR operation described in the preceding code is executed to calculate each bit of the CRC word for the conversion result, A_N. This CRC word (crc1) is then used as the starting point for calculating the CRC word (crc) for the conversion result, B_N. The process repeats cyclically for each channel pair converted.

Depending on the mode of operation of the AD7616-P, the status register value is appended to the conversion data and read via an extra read command over the parallel interface. The user can then repeat the XOR calculation described in the preceding code for the received conversion results to check whether both CRC words match. See Figure 61 for a description of how the CRC word is appended to the data for each mode of operation.

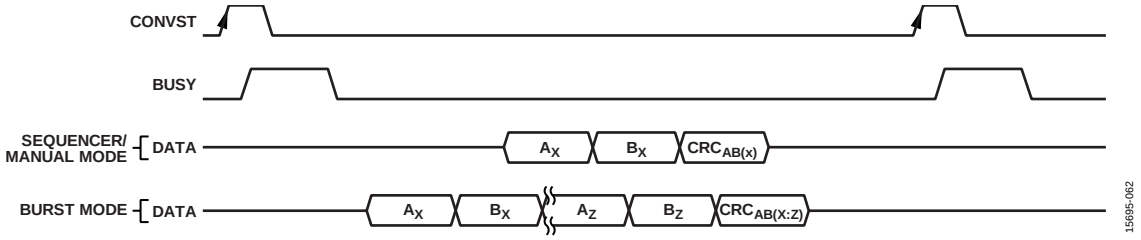


Figure 61. CRC Readback for All Modes

REGISTER SUMMARY

The AD7616-P has six read/write registers for configuring the device in software mode, an additional 32 sequencer stack registers for programming the flexible on-chip sequencer, and a read only status register. Table 17 shows an overview of the read/write registers available on the AD7616-P. The status register is an additional read only register that contains information on the channel pair previously converted and the CRC result.

Table 17. Register Summary[1]

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x02	Configuration register	[15:8]	Addressing							Reserved	0x0000	R/W
		[7:0]	SDEF	BURSTEN	SEQEN	OS			STATUSEN	CRCEN		
0x03	Channel register	[15:8]	Addressing							Reserved	0x0000	R/W
		[7:0]	CHB				CHA					
0x04	Input Range Register A1	[15:8]	Addressing							Reserved	0x00FF	R/W
		[7:0]	V3A		V2A		V1A		V0A			
0x05	Input Range Register A2	[15:8]	Addressing							Reserved	0x00FF	R/W
		[7:0]	V7A		V6A		V5A		V4A			
0x06	Input Range Register B1	[15:8]	Addressing							Reserved	0x00FF	R/W
		[7:0]	V3B		V2B		VB1		V0B			
0x07	Input Range Register B2	[15:8]	Addressing							Reserved	0x00FF	R/W
		[7:0]	V7B		V6B		VB5		V4B			
0x20 to 0x3F	Sequencer Stack Registers[0:31]	[15:8]	Addressing							SSRENx	0x0000[2]	R/W
		[7:0]	BSELx				ASELx					
N/A	Status register	[15:8]	A[3:0]				B[3:0]				N/A	R
		[7:0]	CRC[7:0]									

[1] N/A means not applicable.
[2] After a full or partial rest is issued, the sequencer stack register is reinitialized to cycle through Channel V0A and Channel V0B to Channel V7A and Channel V7B. The remaining 24 layers of the stack are reinitialized to 0x0.

ADDRESSING REGISTERS

The seven MSBs written to the device are decoded to determine the register that is addressed. The seven MSBs consist of the register address (REGADDR), Bits[5:0], and the read/write bit. The register address bits determine the on-chip register that is selected. The read/write bit determines whether the remaining nine bits of data on the DBx lines are loaded into the addressed register. If the read/write bit is 1, the bits load into the register addressed by the register select bits. If the read/write bit is 0, the command is seen as a read request. The addressed register data is available to be read during the next read operation.

MSB **LSB**

D15	D14	D13	D12	D11	D10	D9	D8 to D0
W/$\overline{R}$	REGADDR[5]	REGADDR[4]	REGADDR[3]	REGADDR[2]	REGADDR[1]	REGADDR[0]	Data[8:0]

Table 18.

Bit	Mnemonic	Description
D15	W/$\overline{R}$	If a 1 is written to this bit, Bits[D8:D0] of this register are written to the register specified by REGADDR[5:0]. Alternatively, if a 0 is written, the next operation is a read from the designated register.
D14	REGADDR[5]	If a 1 is written to this bit, the contents of REGADDR[4:0] specifies the 32 sequencer stack registers. Alternatively, if a 0 is written to this bit, a register is selected as defined by REGADDR[4:0].
[D13:D9]	REGADDR[4:0]	When W/$\overline{R}$ =1, the contents of REGADDR[4:0] determine the register for selection, as follows: 00001: reserved. 00010: selects the configuration register. 00011: selects the channel register. 00100: selects Input Range Register A1. 00101: selects Input Range Register A2. 00110: selects Input Range Register B1. 00111: selects Input Range Register B2. 01000: selects the status register When W/$\overline{R}$ = 0 and REGADDR[4:0] contains 00000, the conversion codes are read.
[D8:D0]	Data[8:0]	These bits are written into the corresponding register specified by REGADDR[5:0]. See the following sections for detailed descriptions of each register.

CONFIGURATION REGISTER

The configuration register is used in software mode to configure many of the main functions of the ADC, including the sequencer, burst mode, oversampling, and CRC options.

Address: 0x02, Reset: 0x0000, Name: Configuration Register

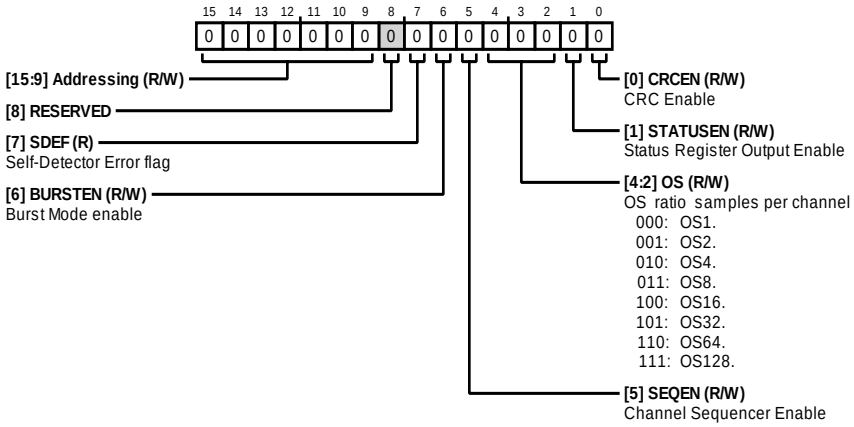


Table 19. Bit Descriptions for the Configuration Register

Bits	Bit Name	Settings	Description	Reset[1]	Access
[15:9]	Addressing	0	Bits[15:9] define the address of the relevant register. See the Addressing Registers section for further details.	0x0	RW
8	RESERVED		Reserved.	0x0	R/W
7	SDEF		Self detector error flag.	N/A	R
		0	Test passed. The AD7616-P configured itself after power-up.		
		1	Test failed. An issue was detected during device configuration. A reset is required.		
6	BURSTEN		Burst mode enable.	0x0	RW
		0	Burst mode is disabled. Each channel pair to be converted requires a CONVST pulse.		
		1	A single CONVST pulse converts every channel pair programmed in the 32-layer sequencer stack registers up to and including the layer defined by the SSRENx bit. See the Software Mode Sequencer section and the Software Mode Burst section for further details.		
5	SEQEN		Channel sequencer enable.	0x0	RW
		0	The channel sequencer is disabled.		
		1	The channel sequencer is enabled.		
[4:2]	OS		Oversampling (OS) ratio, samples per channel.	0x0	RW
		000	Oversampling disabled.		
		001	Oversampling enabled, OSR = 2.		
		010	Oversampling enabled, OSR = 4.		
		011	Oversampling enabled, OSR = 8.		
		100	Oversampling enabled, OSR = 16.		
		101	Oversampling enabled, OSR = 32.		
		110	Oversampling enabled, OSR = 64.		
		111	Oversampling enabled, OSR = 128.		
1	STATUSEN		Status register output enable.	0x0	RW
		0	The status register is not read out when reading the conversion result.		
		1	The status register is read out at the end of all the conversion words (including the self test channel if enabled in sequencer mode) if all the selected channels are read out. The CRC result is included in the last eight bits.		
0	CRCEN		CRC enable. The STATUSEN and CRCEN bits have identical functionality.	0x0	RW

[1] N/A means not applicable.

CHANNEL REGISTER

Address: 0x03, Reset: 0x0000, Name: Channel Register

In software manual mode, the channel register selects the input channel or self test channel for the next conversion.

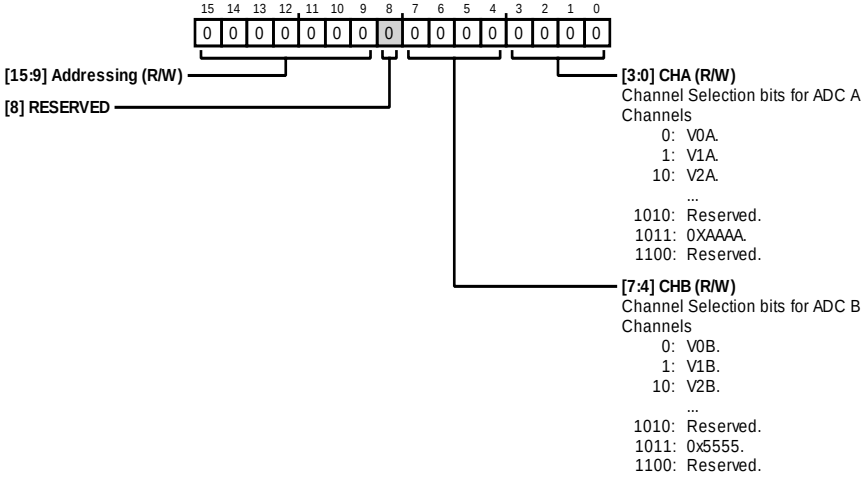


Table 20. Bit Descriptions for the Channel Register

Bits	Bit Name	Settings	Description	Reset	Access
[15:9]	Addressing		Bits[15:9] define the address of the relevant register. See the Addressing Registers section for further details.	0x0	R/W
8	RESERVED		Reserved.	0x0	R/W
[7:4]	CHB		Channel selection bits for ADC B channels.		
		0000	V0B.		
		0001	V1B.		
		0010	V2B.		
		0011	V3B.		
		0100	V4B.		
		0101	V5B.		
		0110	V6B.		
		0111	V7B.		
		1000	V_{CC}.		
		1001	ALDO.		
		1010	Reserved.		
		1011	0x5555. Set the dedicated bits for digital interface communication self test function. When conversion codes are read, Code 0x5555 is output as the conversion code of Channel B.		
		1100	Reserved.		
[3:0]	CHA		Channel selection bits for ADC A Channels. Settings are the same as for ADC B.	0x0	R/W
		0000	V0A.		
		0001	V1A.		
		0010	V2A.		
		0011	V3A.		
		0100	V4A.		
		0101	V5A.		
		0110	V6A.		
		0111	V7A.		
		1000	V_{CC}.		
		1001	ALDO.		
		1010	Reserved.		
		1011	0xAAAA. Set the dedicated bits for digital interface communication self test function. When conversion codes are read, Code 0xAAAA is read out as the conversion code of Channel A.		
		1100	Reserved.		

INPUT RANGE REGISTERS

Input Range Register A1 and Input Range Register A2 select from one of the three possible input ranges (±10 V, ±5 V, or ±2.5 V) for Analog Input V0A to Analog Input V7A. Input Range Register B1 and Input Range Register B2 select from one of the three possible input ranges (±10 V, ±5 V, or ±2.5 V) for Analog Input V0B to Analog Input V7B.

Input Range Register A1

Address: 0x04, Reset: 0x00FF, Name: Input Range Register A1

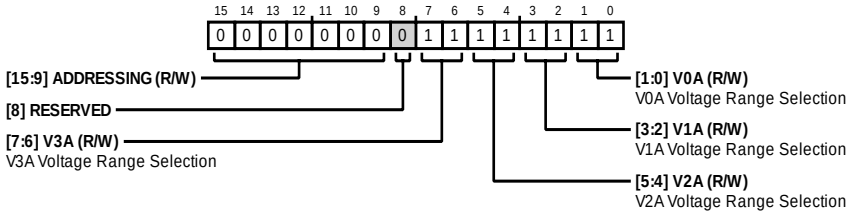


Table 21. Bit Descriptions for Input Range Register A1

Bits	Bit Name	Settings	Description	Reset	Access
[15:9]	Addressing		Bits[15:9] define the address of the relevant register. See the Addressing Registers section for further details.	0x0	R/W
8	RESERVED		Reserved.	0x0	R/W
[7:6]	V3A		V3A voltage range selection.	0x3	R/W
		00	V3A ± 10 V.		
		01	V3A ± 2.5 V.		
		10	V3A ± 5 V.		
		11	V3A ± 10 V.		
[5:4]	V2A		V2A voltage range selection.	0x3	R/W
		00	V2A ± 10 V.		
		01	V2A ± 2.5 V.		
		10	V2A ± 5 V.		
		11	V2A ± 10 V.		
[3:2]	V1A		V1A voltage range selection.	0x3	R/W
		00	V1A ± 10 V.		
		01	V1A ± 2.5 V.		
		10	V1A ± 5 V.		
		11	V1A ± 10 V.		
[1:0]	V0A		V0A voltage range selection.	0x3	R/W
		00	V0A ± 10 V.		
		01	V0A ± 2.5 V.		
		10	V0A ± 5 V.		
		11	V0A ± 10 V.		

Input Range Register A2

Address: 0x05, Reset: 0x00FF, Name: Input Range Register A2

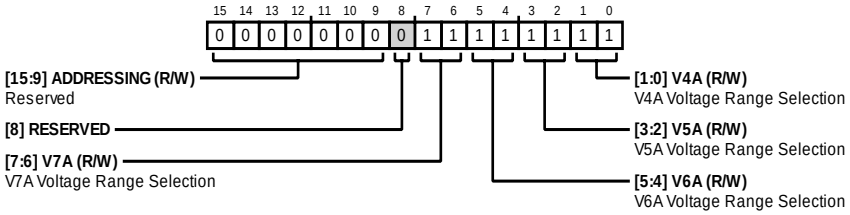


Table 22. Bit Descriptions for Input Range Register A2

Bits	Bit Name	Settings	Description	Reset	Access
[15:9]	Addressing		Bits[15:9] define the address of the relevant register. See the Addressing Registers section for further details.	0x0	R/W
8	RESERVED		Reserved.	0x0	R/W
[7:6]	V7A		V7A voltage range selection.	0x3	R/W
		00	V7A ± 10 V.		
		01	V7A ± 2.5 V.		
		10	V7A ± 5 V.		
		11	V7A ± 10 V.		
[5:4]	V6A		V6A voltage range selection.	0x3	R/W
		00	V6A ± 10 V.		
		01	V6A ± 2.5 V.		
		10	V6A ± 5 V.		
		11	V6A ± 10 V.		
[3:2]	V5A		V5A voltage range selection.	0x3	R/W
		00	V5A ± 10 V.		
		01	V5A ± 2.5 V.		
		10	V5A ± 5 V.		
		11	V5A ± 10 V.		
[1:0]	V4A		V4A voltage range selection.	0x3	R/W
		00	V4A ± 10 V.		
		01	V4A ± 2.5 V.		
		10	V4A ± 5 V.		
		11	V4A ± 10 V.		

Input Range Register B1

Address: 0x06, Reset: 0x00FF, Name: Input Range Register B1

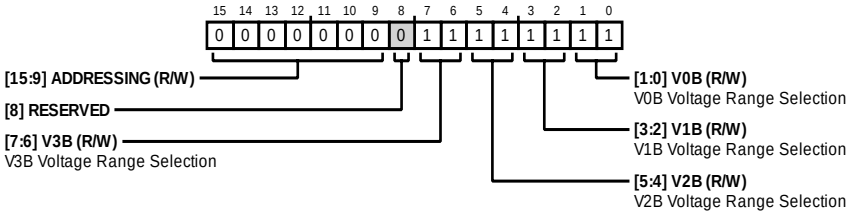


Table 23. Bit Descriptions for Input Range Register B1

Bits	Bit Name	Settings	Description	Reset	Access
[15:9]	Addressing		Bits[15:9] define the address of the relevant register. See the Addressing Registers section for further details.	0x0	R/W
8	RESERVED		Reserved.	0x0	R/W
[7:6]	V3B		V3B voltage range selection.	0x3	R/W
		00	V3B ± 10 V.		
		01	V3B ± 2.5 V.		
		10	V3B ± 5 V.		
		11	V3B ± 10 V.		
[5:4]	V2B		V2B voltage range selection.	0x3	R/W
		00	V2B ± 10 V.		
		01	V2B ± 2.5 V.		
		10	V2B ± 5 V.		
		11	V2B ± 10 V.		
[3:2]	V1B		V1B voltage range selection.	0x3	R/W
		00	V1B ± 10 V.		
		01	V1B ± 2.5 V.		
		10	V1B ± 5 V.		
		11	V1B ± 10 V.		
[1:0]	V0B		V0B voltage range selection.	0x3	R/W
		00	V0B ± 10 V.		
		01	V0B ± 2.5 V.		
		10	V0B ± 5 V.		
		11	V0B ± 10 V.		

Input Range Register B2

Address: 0x07, Reset: 0x00FF, Name: Input Range Register B2

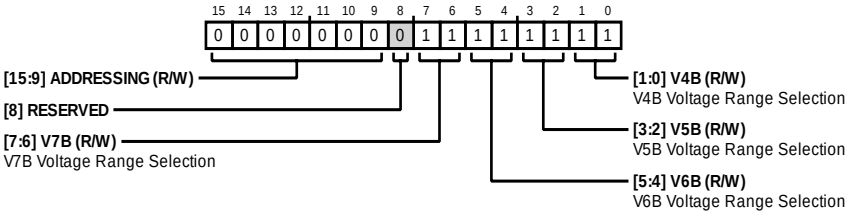


Table 24. Bit Descriptions for Input Range Register B2

Bits	Bit Name	Settings	Description	Reset	Access
[15:9]	Addressing		Bits[15:9] define the address of the relevant register. See the Addressing Registers section for further details.	0x0	R/W
8	RESERVED		Reserved.	0x0	R/W
[7:6]	V7B		V7B voltage range selection.	0x3	R/W
		00	V7B ± 10 V.		
		01	V7B ± 2.5 V.		
		10	V7B ± 5 V.		
		11	V7B ± 10 V.		
[5:4]	V6B		V6B voltage range selection.	0x3	R/W
		00	V6B ± 10 V.		
		01	V6B ± 2.5 V.		
		10	V6B ± 5 V.		
		11	V6B ± 10 V.		
[3:2]	V5B		V5B voltage range selection.	0x3	R/W
		00	V5B ± 10 V.		
		01	V5B ± 2.5 V.		
		10	V5B ± 5 V.		
		11	V5B ± 10 V.		
[1:0]	V4B		V4B voltage range selection.	0x3	R/W
		00	V4B ± 10 V.		
		01	V4B ± 2.5 V.		
		10	V4B ± 5 V.		
		11	V4B ± 10 V.		

SEQUENCER STACK REGISTERS

Although the channel register defines the next channel for conversion (be it a diagnostic channel or pair of analog input channels), to sample numerous analog input channels, the 32 sequencer stack registers offer a convenient solution. Within the communication register, when the REGADDR5 bit is set to Logic 1, the contents of REGADDR[4:0] specify 1 of the 32 sequencer stack registers. Within each sequencer stack register, the user can define a pair of analog inputs to sample simultaneously.

The structure of the sequence forms a stack, in which each row represents two channels to convert simultaneously. The sequence begins with Sequencer Stack Register 1 and cycles through to Sequencer Stack Register 32. If Bit D8 (the enable bit, SSRENx) within a sequencer stack register is set to 1, the sequence ends with the pair of analog inputs defined by that register, then returns to the first sequencer stack register, and resumes the cycle again.

By default, the first eight layers of the sequencer stack registers are programmed to cycle through Analog Input V0A and Analog Input V0B to Analog Input V7A and Analog Input V7B. After a full or partial reset is issued, the sequencer stack register reinitializes to cycle through Analog Input V0A and Analog Input V0B to Analog Input V7A and Analog Input V7B. The remaining sequencer stack registers are reinitialized to 0x0000.

Sequencer Stack Register 0 to Sequencer Stack Register 7

Address: 0x20 to 0x27, Reset: 0x0000, 0x0011, 0x0022, 0x0033, 0x0044, 0x0055, 0x0066, 0x0077, Name: Sequencer Stack Register 0 to Sequencer Stack Register 7

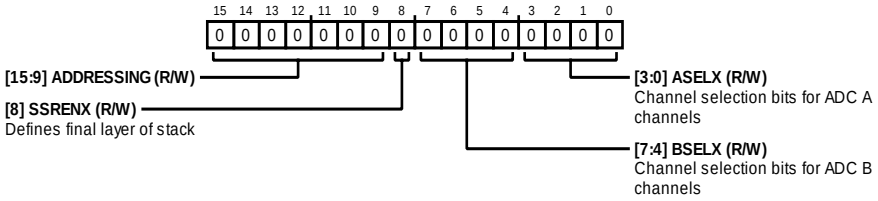


Table 25. Bit Descriptions for Sequencer Stack Register 0 to Sequencer Stack Register 7

Bits	Bit Name	Settings	Description	Reset	Access
[15:9]	Addressing		Bits[15:9] define the address of the relevant register. See the Addressing Registers section for further details.	0x0	R/W
8	SSRENx		Setting this bit to 0 instructs the ADC to move to the next layer of the sequencer stack after converting the present channel pair. Setting this bit to 1 defines that layer of the sequencer stack as the final layer in the sequence. Thereafter, the sequencer loops back to the first layer of the stack.	0x0	R/W
[7:4]	BSELx		Channel selection bits for ADC B channels.	0x0[1]	R/W
		0000	V0B.		
		0001	V1B.		
		0010	V2B.		
		0011	V3B.		
		0100	V4B.		
		0101	V5B.		
		0110	V6B.		
		0111	V7B.		
		1000	V_{CC}.		
		1001	ALDO.		
		1010	Reserved.		
		1011	Set the dedicated bits for digital interface communication self test function. When the conversion codes is read, Code 0xAAAA is read out as the conversion code of Channel A, and Code 0x5555 is output as the conversion code of Channel B.		
		1100	Reserved.		
[3:0]	ASELx		Channel selection bits for ADC A channels. Settings are the same as for ADC B.	0x0[1]	R/W

[1] By default, the first eight layers of the sequencer stack registers are programmed to cycle through Analog Input V0A and Analog Input V0B to Analog Input V7A and Analog Input V7B. After a full or partial reset is issued, the sequencer stack register reinitializes to cycle through Analog Input V0A and Analog Input V0B to Analog Input V7A and Analog Input V7B. The remaining sequencer stack registers are reinitialized to 0x0000.

Sequencer Stack Register 8 to Sequencer Stack Register 31

Address: 0x28 to 0x3F, Reset: 0x00, Name: Sequencer Stack Register 8 to Sequencer Stack Register 31

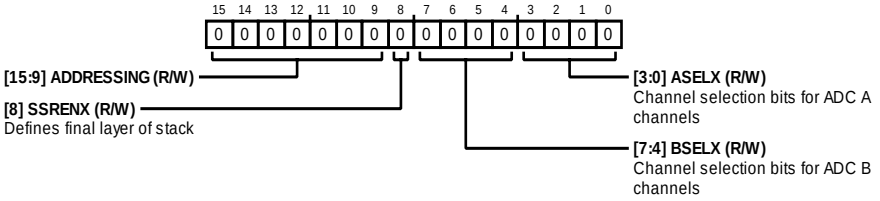


Table 26. Bit Descriptions for Sequencer Stack Register 8 to Sequencer Stack Register 31

Bits	Bit Name	Settings	Description	Reset	Access
[15:9]	Addressing		Bits[15:9] define the address of the relevant register. See the Addressing Registers section for further details.	0x0	R/W
8	SSRENx		Setting this bit to 0 instructs the ADC to move to the next layer of the sequencer stack after converting the present channel pair. Setting this bit to 1 defines that layer of the sequencer stack as the final layer in the sequence. Thereafter, the sequencer loops back to the first layer of the stack.	0x0	R/W
[7:4]	BSELx		Channel selection bits for ADC B channels.	0x0	R/W
		0000	V0B.		
		0001	V1B.		
		0010	V2B.		
		0011	V3B.		
		0100	V4B.		
		0101	V5B.		
		0110	V6B.		
		0111	V7B.		
		1000	V_{CC}.		
		1001	ALDO.		
		1010	Reserved.		
		1011	Set the dedicated bits for digital interface communication self test function. When the conversion codes is read, Code 0xAAAA is read out as the conversion code of Channel A, and Code 0x5555 is output as the conversion code of Channel B.		
		1100	Reserved.		
[3:0]	ASELx		Channel selection bits for ADC A channels. Settings are the same as for ADC B.	0x0[1]	R/W

STATUS REGISTER

The status register is a 16-bit read only register. If the STATUSEN bit or the CRCEN bit is set to Logic 1 in the configuration register, the status register is read out at the end of all conversion words for the selected channels, including the self test channel if enabled in sequencer mode. See the CRC section and Figure 61 for more information.

MSB **LSB**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
A[3:0]				B[3:0]				CRC[7:0]							

Table 27. Bit Descriptions for Status Register

Bits	Bit Name	Settings	Description	Reset[1]	Access
[D15:D12]	A[3:0]		Channel index for previous conversion result on Channel A.	N/A	R
[D11:D8]	B[3:0]		Channel index for previous conversion result on Channel B.	N/A	R
[D7:D0]	CRC[7:0]		CRC calculation for the previous conversion result(s). Refer to the CRC section for further details.	N/A	R

[1] N/A means not applicable.

OUTLINE DIMENSIONS

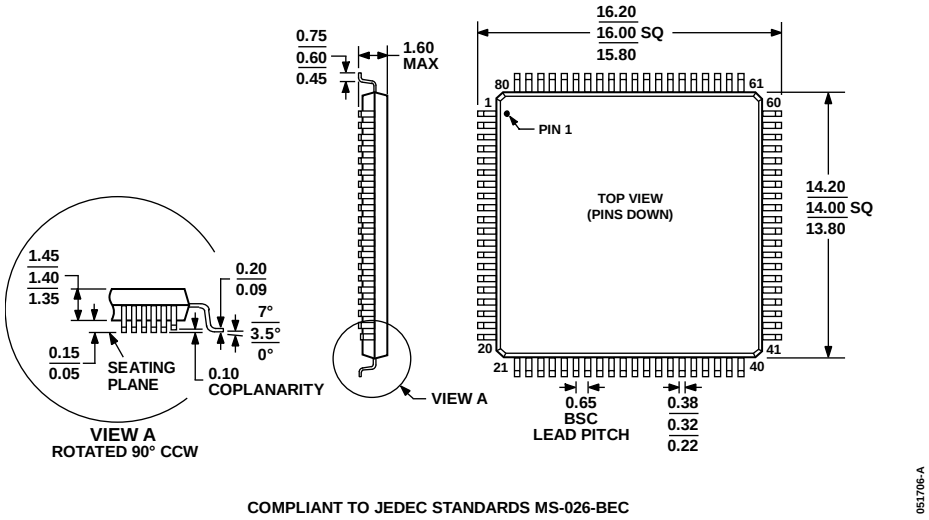


Figure 62. 80-Lead Low Profile Quad Flat Package [LQFP]
(ST-80-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Junction Temperature Range	Package Description	Package Option
AD7616-PBSTZ	−40°C to +125°C	80-Lead Low Profile Quad Flat Package [LQFP]	ST-80-2
AD7616-PBSTZ-RL	−40°C to +125°C	80-Lead Low Profile Quad Flat Package [LQFP]	ST-80-2
EVAL-AD7616-PSDZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

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