



2N7002NXAK

60 V, single N-channel Trench MOSFET

1 July 2019

Product data sheet

1. General description

N-channel enhancement mode Field-Effect Transistor (FET) in a small SOT23 (TO-236AB) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Very fast switching
- Trench MOSFET technology
- ESD protected

3. Applications

- Relay driver
- High-speed line driver
- Low-side load switch
- Switching circuits

4. Quick reference data

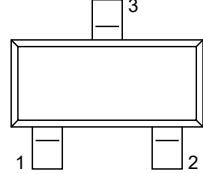
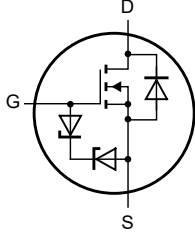
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$	-	-	60	V
V_{GS}	gate-source voltage		-20	-	20	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{sp} = 25\text{ °C}$	-	-	300	mA
		$V_{GS} = 10\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	190	mA
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 100\text{ mA}; T_j = 25\text{ °C}$	-	3	4.5	Ω

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm².

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>TO-236AB (SOT23)</p>	 <p>017aaa255</p>
2	S	source		
3	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
2N7002NXAK	TO-236AB	plastic surface-mounted package; 3 leads	SOT23

7. Marking

Table 4. Marking codes

Type number	Marking code ^[1]
2N7002NXAK	%CM

[1] % = placeholder for manufacturing site code

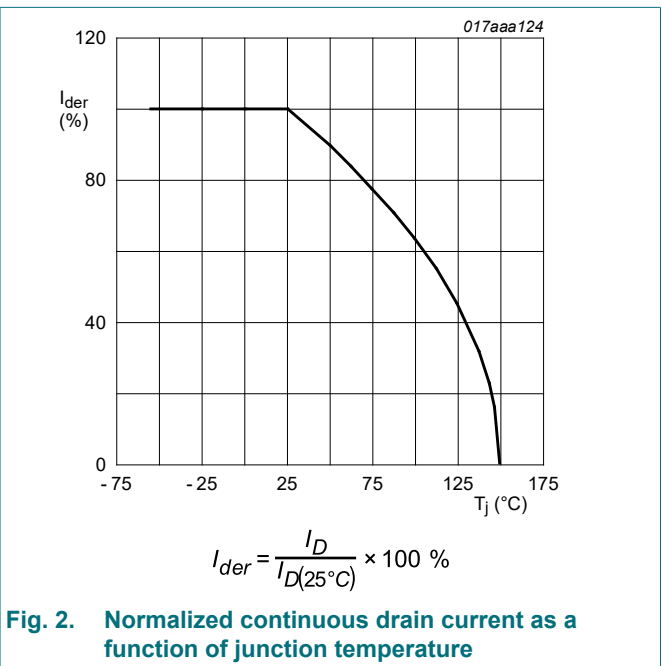
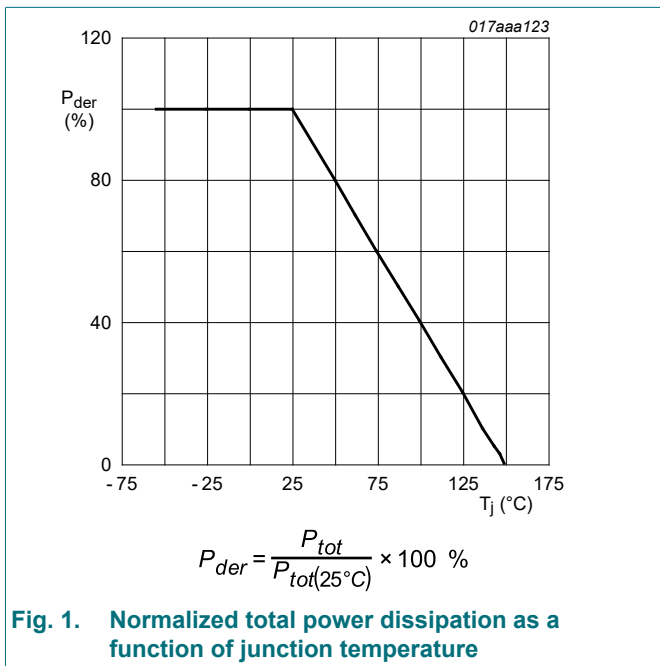
8. Limiting values

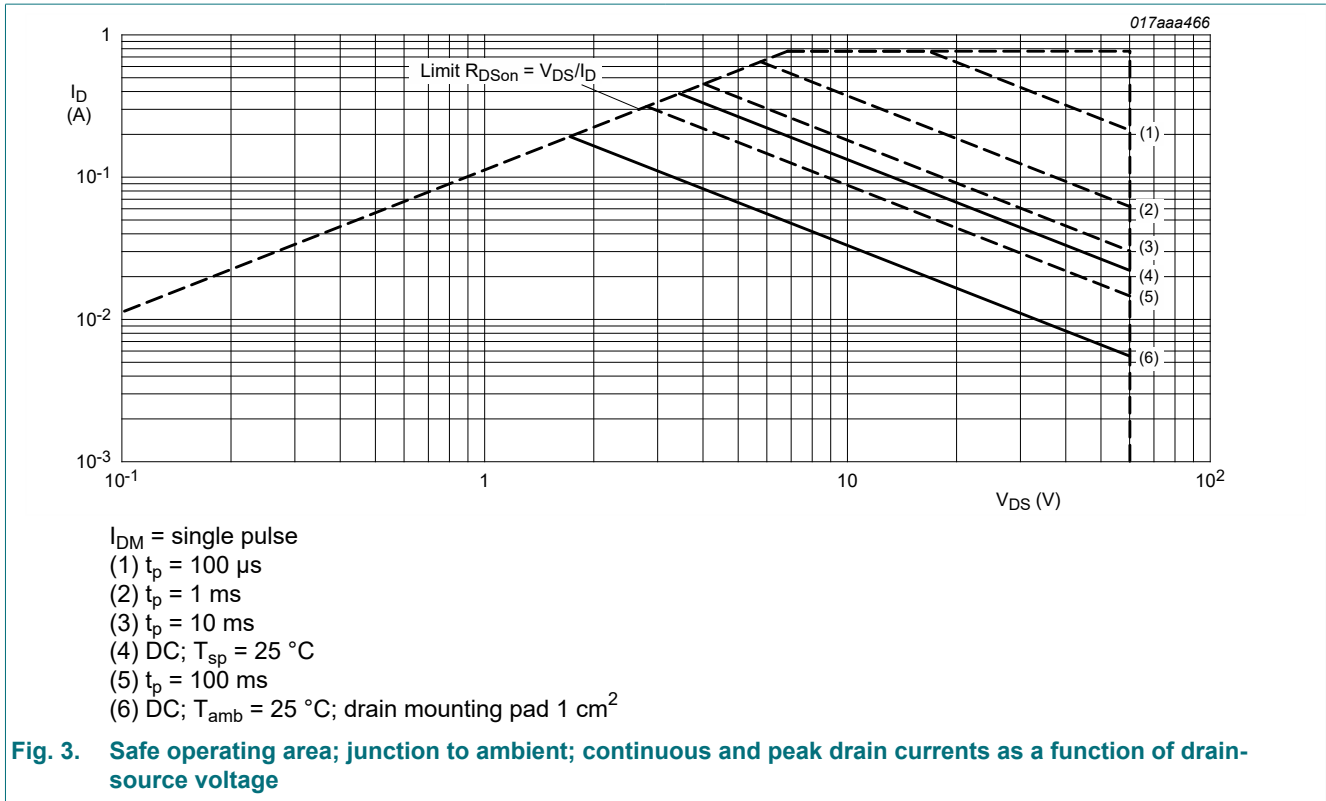
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C	-	60	V
V _{GS}	gate-source voltage		-20	20	V
I _D	drain current	V _{GS} = 10 V; T _{sp} = 25 °C	-	300	mA
		V _{GS} = 10 V; T _{amb} = 25 °C	[1]	190	mA
		V _{GS} = 10 V; T _{amb} = 100 °C	[1]	120	mA
I _{DM}	peak drain current	T _{amb} = 25 °C; single pulse; t _p ≤ 10 μs	-	760	mA
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	265	mW
			[1]	325	mW
		T _{sp} = 25 °C	-	1330	mW
T _j	junction temperature		-55	150	°C
T _{amb}	ambient temperature		-55	150	°C
T _{stg}	storage temperature		-65	150	°C
Source-drain diode					
I _S	source current	T _{amb} = 25 °C	[1]	-	190 mA

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm².
- [2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.





9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	410	470	K/W
			[2]	-	330	380	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	-	95	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm^2 .

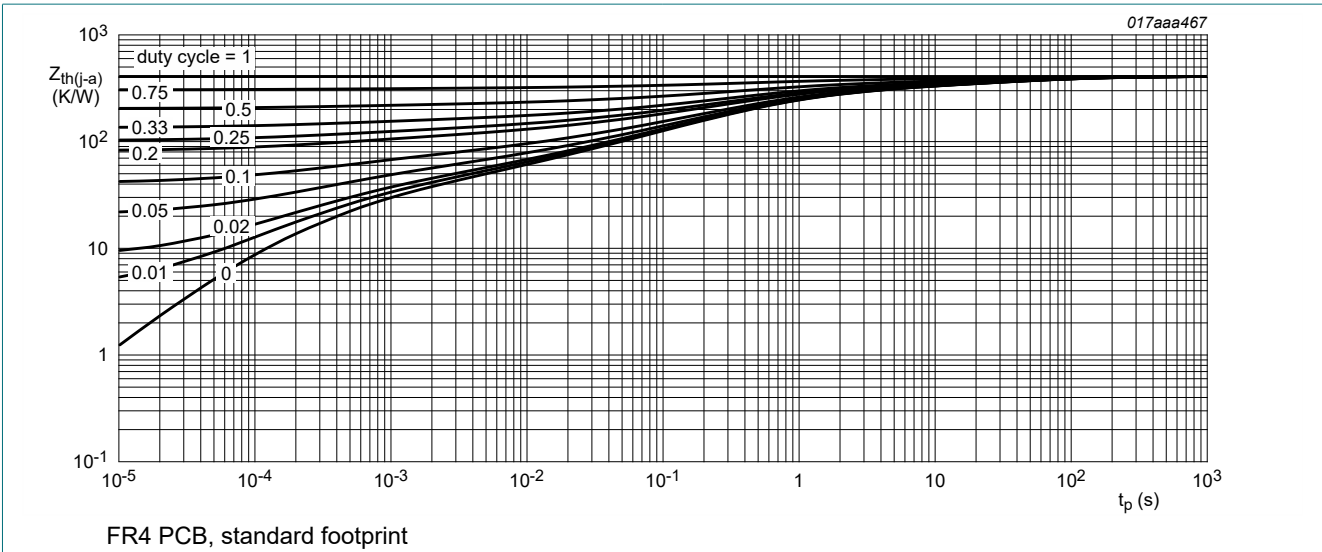


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

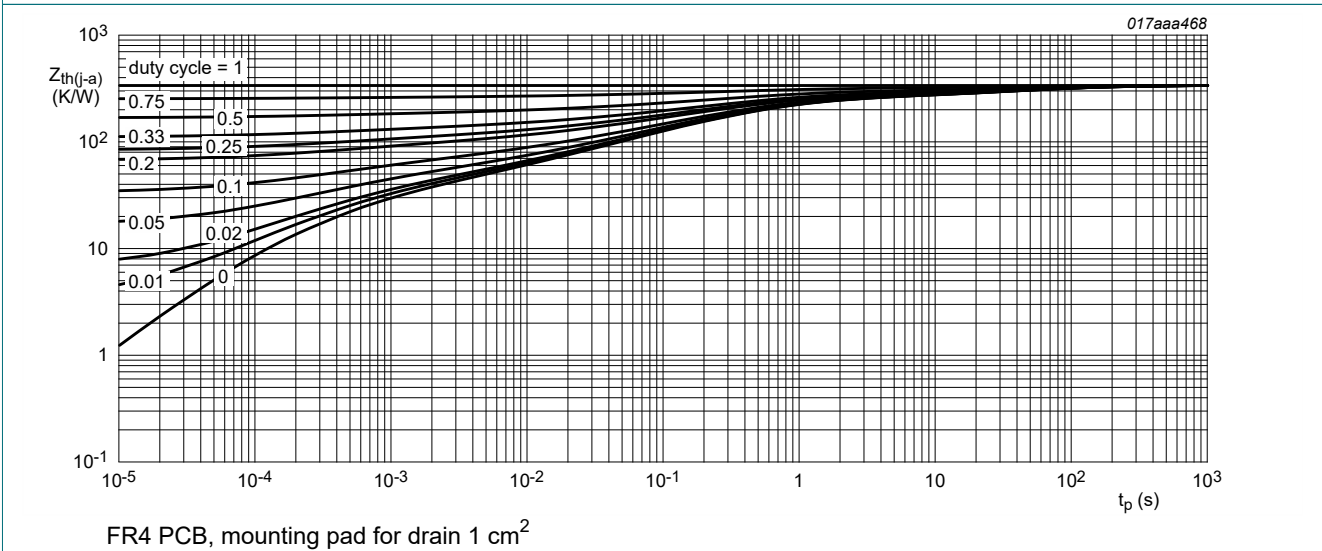


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	60	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = 250 \mu A; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$	1.1	1.6	2.1	V
I_{DSS}	drain leakage current	$V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	1	μA
		$V_{DS} = 60 V; V_{GS} = 0 V; T_j = 150 \text{ }^\circ C$	-	-	10	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	2	μA
		$V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	-2	μA
		$V_{GS} = 10 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	0.5	μA
		$V_{GS} = -10 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	-0.5	μA
		$V_{GS} = 5 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	100	nA
		$V_{GS} = -5 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	-100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 V; I_D = 100 \text{ mA}; T_j = 25 \text{ }^\circ C$	-	3	4.5	Ω
		$V_{GS} = 10 V; I_D = 100 \text{ mA}; T_j = 150 \text{ }^\circ C$	-	6.2	9.2	Ω
		$V_{GS} = 5 V; I_D = 100 \text{ mA}; T_j = 25 \text{ }^\circ C$	-	3.7	5.2	Ω
g_{fs}	forward transconductance	$V_{DS} = 10 V; I_D = 200 \text{ mA}; T_j = 25 \text{ }^\circ C$	-	500	-	mS
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$V_{DS} = 30 V; I_D = 200 \text{ mA}; V_{GS} = 4.5 V; T_j = 25 \text{ }^\circ C$	-	0.33	0.43	nC
Q_{GS}	gate-source charge		-	0.12	-	nC
Q_{GD}	gate-drain charge		-	0.09	-	nC
C_{iss}	input capacitance	$V_{DS} = 10 V; f = 1 \text{ MHz}; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	15	20	pF
C_{oss}	output capacitance		-	3.4	-	pF
C_{rss}	reverse transfer capacitance		-	2	-	pF
$t_{d(on)}$	turn-on delay time		$V_{DS} = 40 V; R_L = 250 \Omega; V_{GS} = 10 V; R_{G(ext)} = 6 \Omega; T_j = 25 \text{ }^\circ C$	-	6	12
t_r	rise time	-		7	-	ns
$t_{d(off)}$	turn-off delay time	-		11	20	ns
t_f	fall time	-		5	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 115 \text{ mA}; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	0.47	0.8	1.2	V

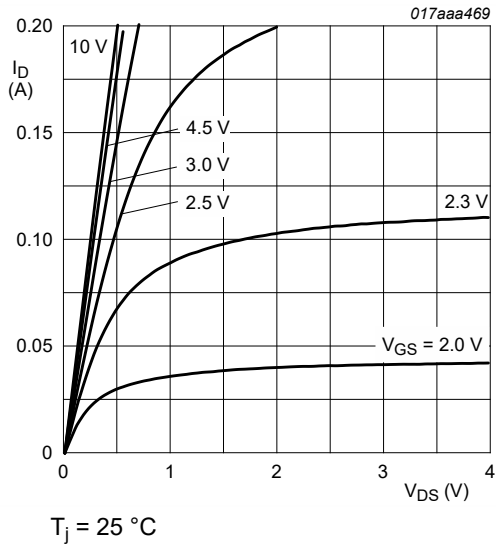


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

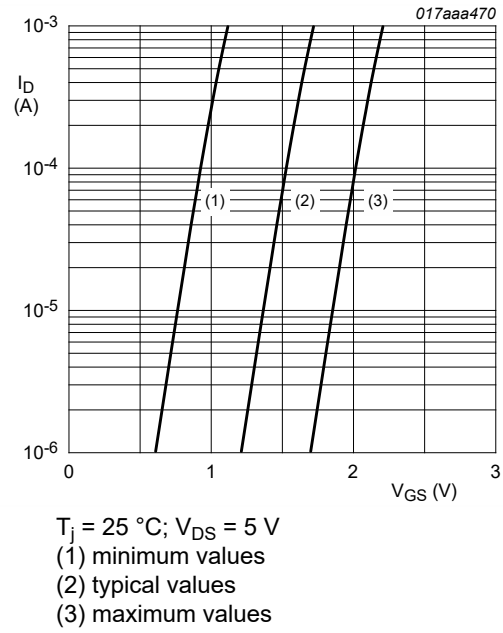


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

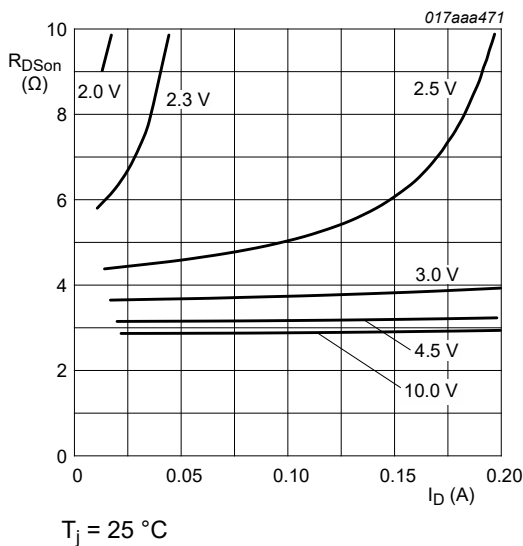


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

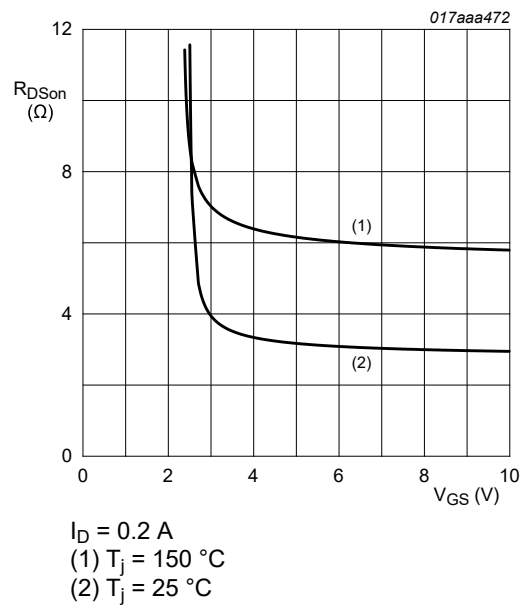


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

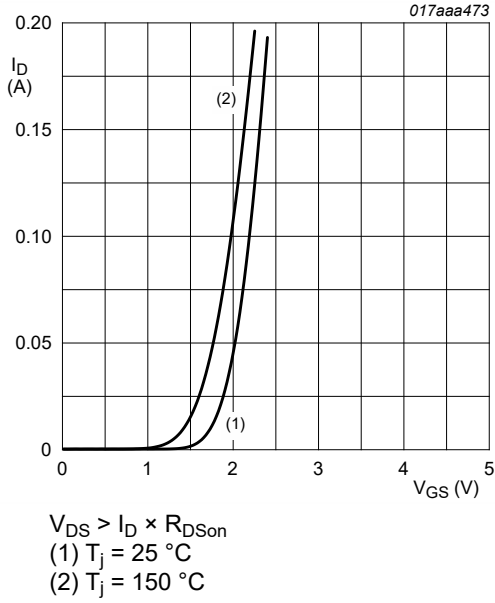


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

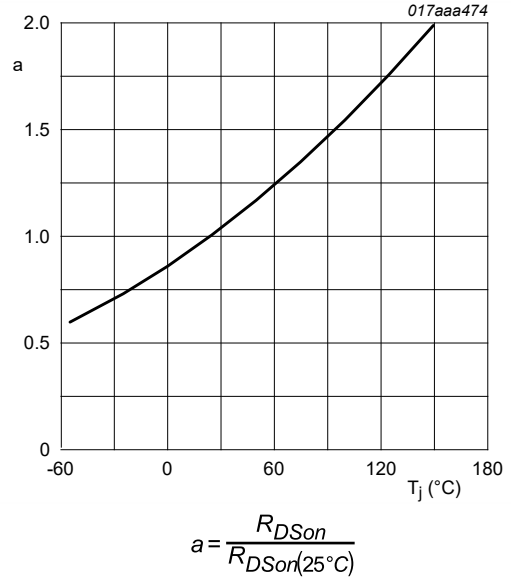


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

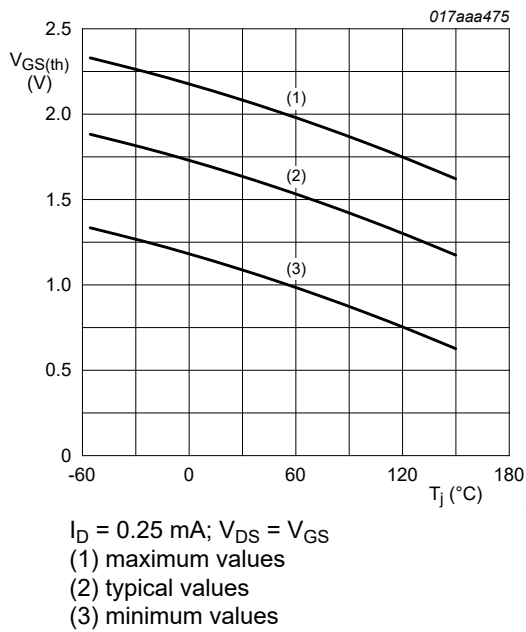


Fig. 12. Gate-source threshold voltage as a function of junction temperature

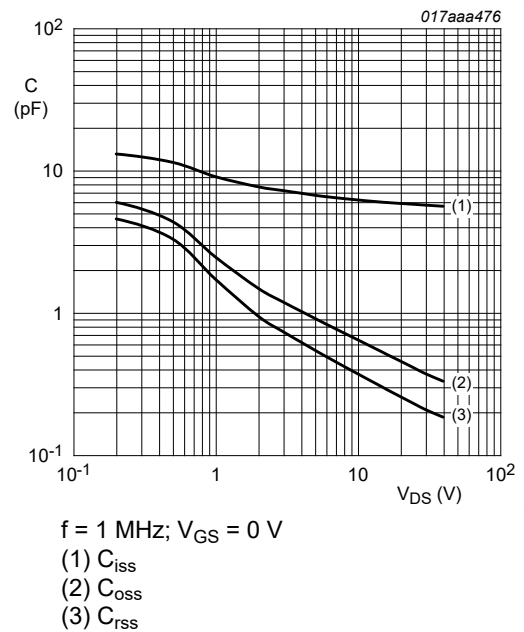
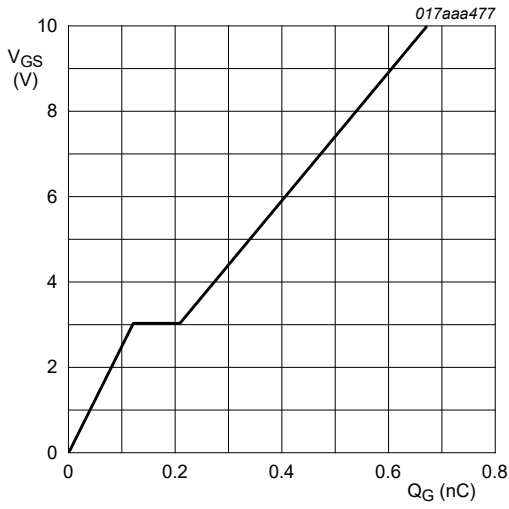


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$I_D = 0.2$ A; $V_{DS} = 30$ V; $T_{amb} = 25$ °C

Fig. 14. Gate-source voltage as a function of gate charge; typical values

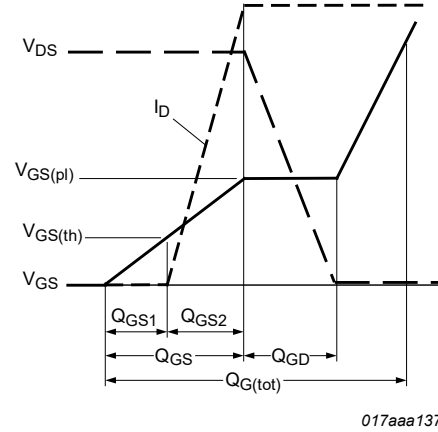
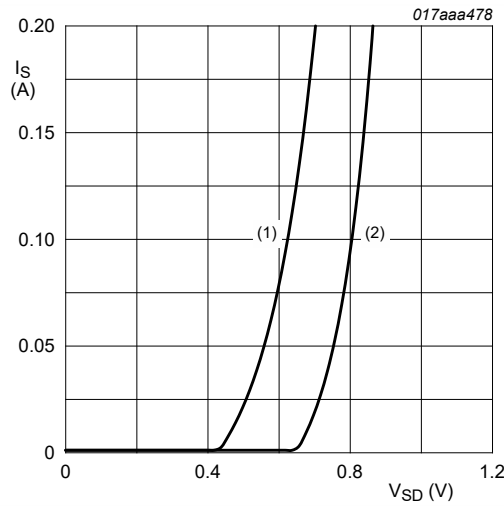


Fig. 15. MOSFET transistor: Gate charge waveform definitions



$V_{GS} = 0$ V
(1) $T_j = 150$ °C
(2) $T_j = 25$ °C

Fig. 16. Source current as a function of source-drain voltage; typical values

11. Test information

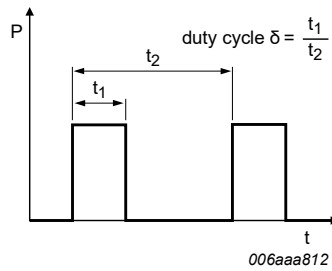


Fig. 17. Duty cycle definition

12. Package outline

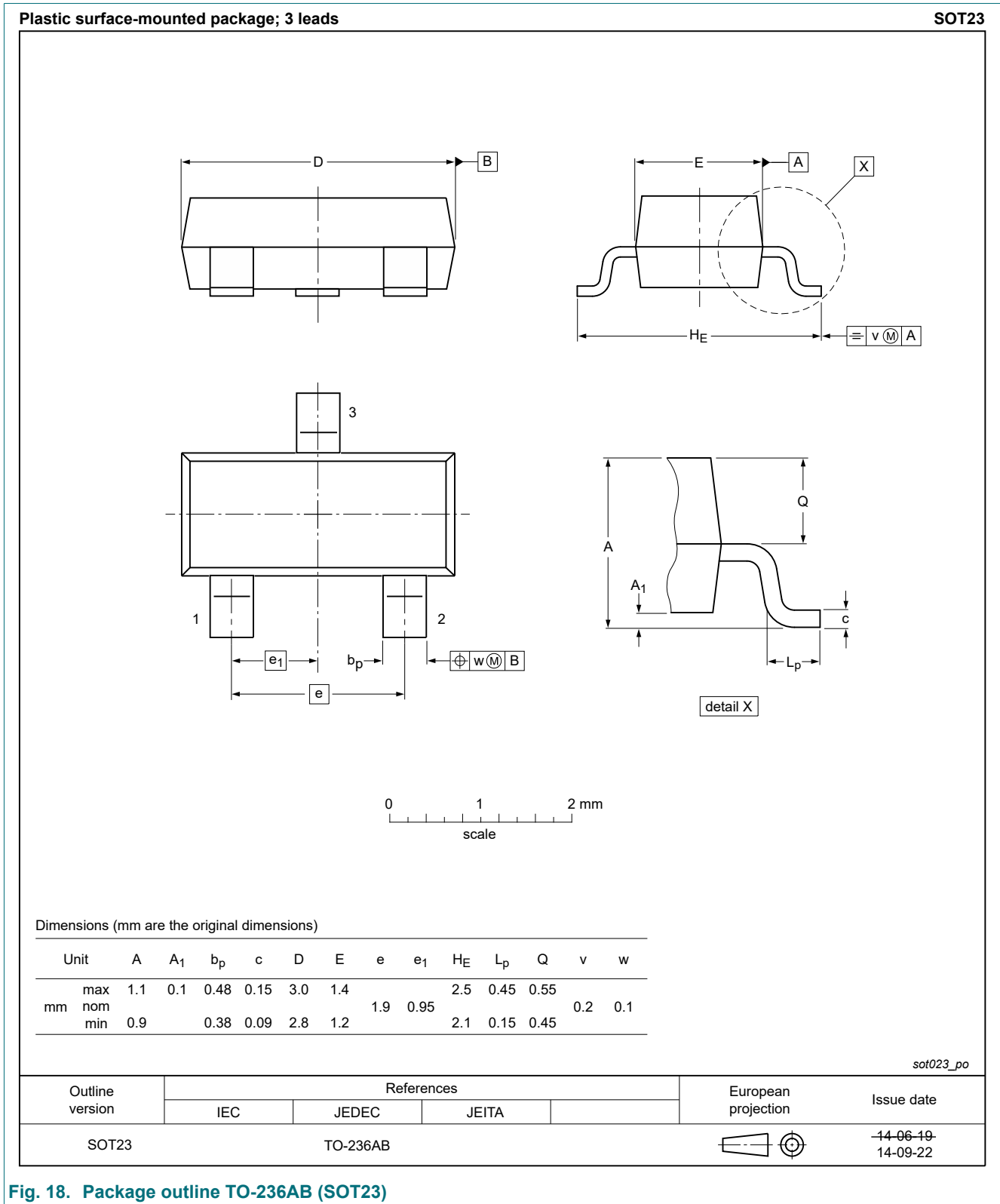


Fig. 18. Package outline TO-236AB (SOT23)

13. Soldering

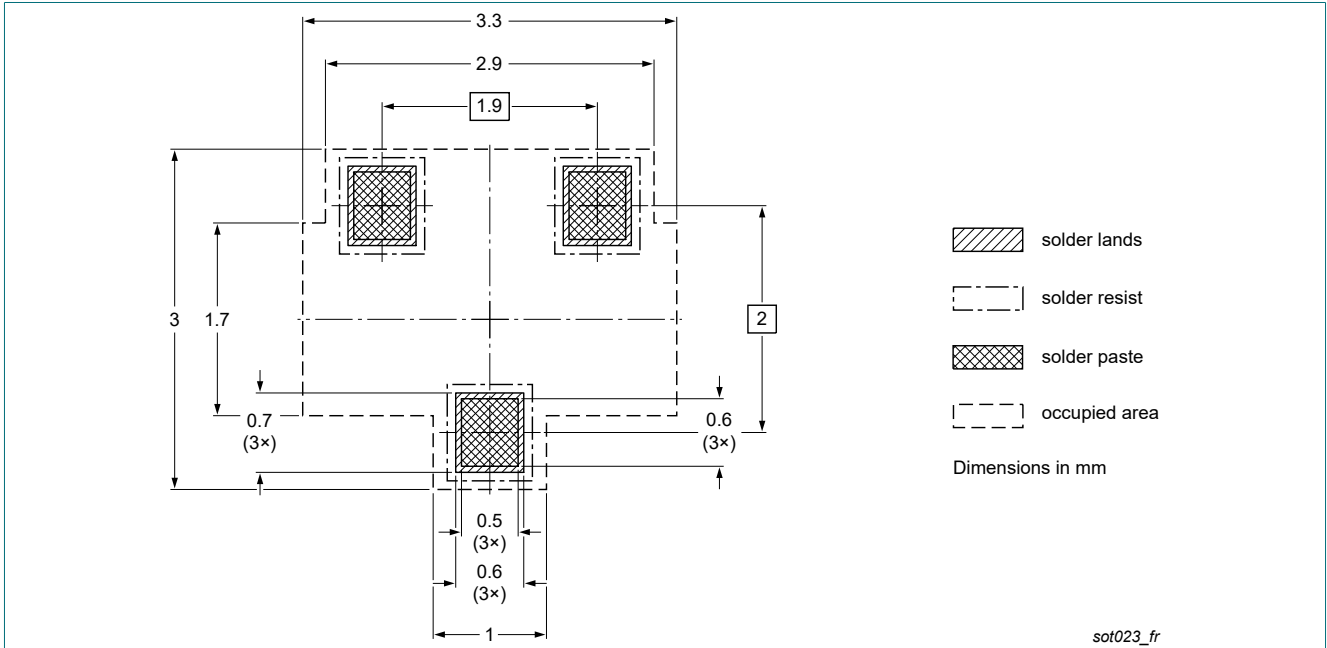


Fig. 19. Reflow soldering footprint for TO-236AB (SOT23)

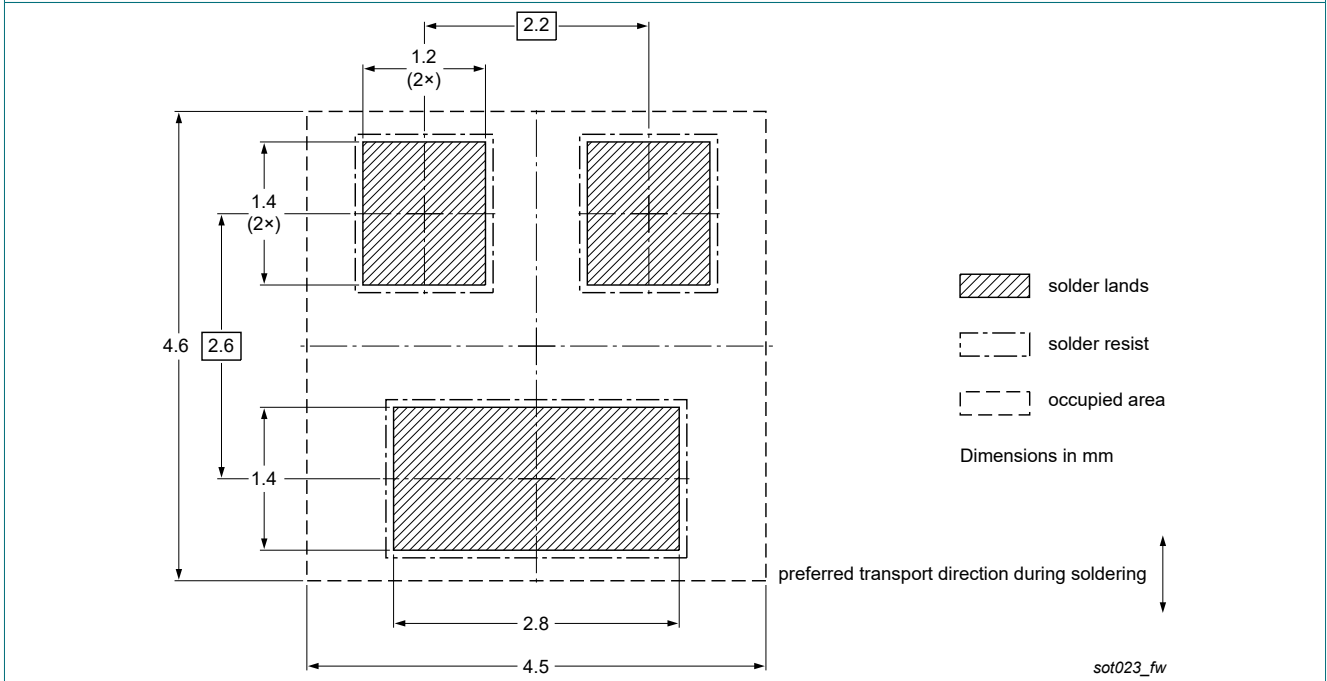


Fig. 20. Wave soldering footprint for TO-236AB (SOT23)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
2N7002NXAK v.1	20190701	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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